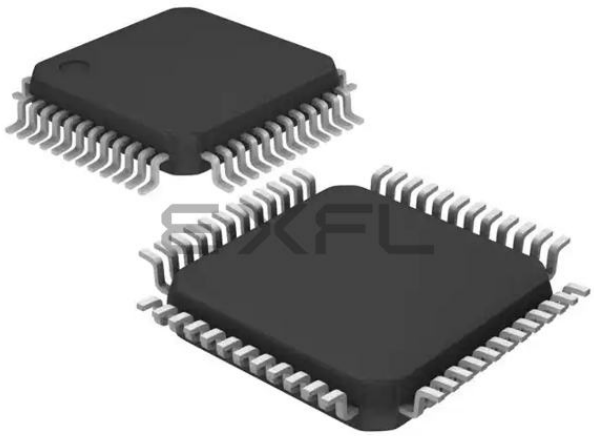

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Details	
Product Status	Active
Applications	Automotive
Core Processor	S12
Program Memory Type	FLASH (48kB)
Controller Series	HCS12
RAM Size	2K x 8
Interface	LIN, SCI
Number of I/O	9
Voltage - Supply	2.25V ~ 5.5V
Operating Temperature	-40°C ~ 105°C
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mm912g634dc2ap

Table 4. MM912_634 Pin Description

Pin #	Pin Name	Formal Name	Description
37	LS1	Low Side Output 1	Low Side output 1 used to drive small inductive loads like relays. The output is short-circuit protected, includes active clamp circuitry and can be also controlled by the PWM module. See Section 5.13, “Low Side Drivers - LSx"
38	PGND	Power Ground Pin	This pin is the device Low Side Ground connection. DGND, LGND and AGND are internally connected to PGND via a back to back diode.
39	LS2	Low Side Output 2	Low Side output 2 used to drive small inductive loads like relays. The output is short-circuit protected, includes active clamp circuitry and can be also controlled by the PWM module. See Section 5.13, “Low Side Drivers - LSx"
40	ISENSEL	Current Sense Pin L	Current Sense differential input “Low”. This pin is used in combination with ISENSEH to measure the voltage drop across a shunt resistor. See Section 5.21, “Current Sense Module - ISENSE". Note: This pin function is not available on all device configurations.
41	ISENSEH	Current Sense Pin H	Current Sense differential input “High”. This pin is used in combination with ISENSEL to measure the voltage drop across a shunt resistor. Section 5.21, “Current Sense Module - ISENSE". Note: This pin function is not available on all device configurations.
42	NC	Not connected	This pin is reserved for alternative function and should be left floating.
43	TEST_A	Test Mode	Analog die Test Mode pin for Test Mode only. This pin must be grounded in user mode.
44	TCLK	Test Clock Input	Test Mode Clock Input pin for Test Mode only. The pin can be used to disable the internal watchdog for development purpose in user mode. See Section 5.10, “Window Watchdog". The pin is recommended to be grounded in user mode.
45	$\overline{\text{RESET\_A}}$	Reset I/O	Bidirectional Reset I/O pin of the analog die. Active low signal. Internal pull-up. V_{DDX} based. See Section 5.8, “Resets". To be externally connected to the $\overline{\text{RESET}}$ pin.
46	$\overline{\text{RESET}}$	MCU Reset	The RESET pin is an active low bidirectional control signal. It acts as an input to initialize the MCU to a known start-up state, and an output when an internal MCU function causes a reset. The $\overline{\text{RESET}}$ pin has an internal pull-up device to VDDRX.
47	BKGD	MCU Background Debug and Mode	The BKGD/MODC pin is used as a pseudo-open-drain pin for the background debug communication. It is used as MCU operating mode select pin during reset. The state of this pin is latched to the MODC bit at the rising edge of $\overline{\text{RESET}}$. The BKGD pin has a pull-up device.
48	PA7	MCU PA7	General purpose port A input or output pin 7. See Section 5.28, “Port Integration Module (S12IPIMV1)"

3.2 MCU Die Signal Properties

This section describes the external MCU signals. It includes a table of signal properties.

Table 5. Signal Properties Summary

Pin Name Function 1	Pin Name Function 2	Power Supply	Internal Pull Resistor		Description
			CTRL	Reset State	
PE0	EXTAL	VD_{DRX}	PUPEE/ OSCPINS_EN	DOWN	Port E I/O, Oscillator pin
PE1	XTAL	V_{DDRX}	PUPBE/ OSCPINS_EN	DOWN	Port E I/O, Oscillator pin
$\overline{\text{RESET}}$	—	VDDRX	PULLUP		External reset
TEST	—	N.A.	$\overline{\text{RESET}}$ pin	DOWN	Test input
BKGD	MODC	VDDRX	BKPUE	UP	Background debug
PA7	—	VDDRX	NA	NA	Port A I/O

Table 23. Static Electrical Characteristics - Current Sense Module - ISENSE

Ratings	Symbol	Min	Typ	Max	Unit
Gain					
CSGS (Current Sense Gain Select) = 000	G	-	7	-	
CSGS (Current Sense Gain Select) = 001		-	9	-	
CSGS (Current Sense Gain Select) = 010		-	10	-	
CSGS (Current Sense Gain Select) = 011		-	12	-	
CSGS (Current Sense Gain Select) = 100		-	14	-	
CSGS (Current Sense Gain Select) = 101		-	18	-	
CSGS (Current Sense Gain Select) = 110		-	24	-	
CSGS (Current Sense Gain Select) = 111		-	36	-	
Gain Accuracy		-3.0	-	3.0	%
Offset		-1.5	-	1.5	%
Resolution(29)	RES	-	51	-	mA/LSB
ISENSEH, ISENSEL Input Common Mode Voltage Range	V_{IN}	-0.2	-	3.0	V
Current Sense Module - Normal Mode Current Consumption Adder (CSE = 1)	I_{ISENSE}	-	600	-	µA

Note:
29. RES = 2.44 mV/(GAIN*R_{SHUNT})

Table 24. Static Electrical Characteristics - Temperature Sensor - TSENSE

Ratings	Symbol	Min	Typ	Max	Unit
Internal Chip Temperature Sense Gain(30)	TS_G	-	9.17	-	mV/k
Internal Chip Temperature Sense Error at the end of conversion(30)	TS_{Err}	–5.0	-	5.0	°C
Temperature represented by a ADC_{IN} Voltage of 0.150 V(30)	$T_{0.15V}$	-55	-50	-45	°C
Temperature represented by a ADC_{IN} Voltage of 1.984 V(30)	$T_{1.984V}$	145	150	155	°C

Note:
30. Guaranteed by design and characterization.

Table 25. Static Electrical Characteristics - Supply Voltage Sense - VSENSE and VS1SENSE

Ratings	Symbol	Min	Typ	Max	Unit
VSENSE Input Divider Ratio ($RATIO_{VSENSE}$ = V_{VSENSE} / ADCIN) 5.5 V < V_{SUP} < 27 V	$RATIO_{VSENSE}$	-	10.8	5.0%	
VSENSE error - whole path (VSENSE pad to Digital value)	Er_{VSENSE}	-	-	5.0	%
VS1SENSE Input Divider Ratio ($RATIO_{VS1SENSE}$ = $V_{VS1SENSE}$ / ADCIN) 5.5 V < V_{SUP} < 27 V	$RATIO_{VS1SENSE}$	-	10.8	5.0%	
VS1SENSE error - whole path (VS1 pad to Digital value)	$Er_{VS1SENSE}$	-	-	5.0	%
VSENSE Series Resistor	R_{VSENSE}	9.5	10	10.5	kOhm
VSENSE Capacitor (optional)(31)	C_{VSENSE}	-	100	-	nF

Note:
31. The ESD behavior specified in Section 4.8, “ESD Protection and Latch-up Immunity" is guaranteed without the optional capacitor.

The maximum D-Flash programming time is given by:

$$t_{dpgm} \approx \left((14 + (54 \cdot N_W) + (14 \cdot BC)) \cdot \frac{1}{f_{NVMOP}} \right) + \left((500 + (750 \cdot N_W) + (100 \cdot BC)) \cdot \frac{1}{f_{NVMBUS}} \right)$$

4.6.2.1.1.16 Erase D-Flash Sector (FCMD=0x12)

Typical D-Flash sector erase times, expected on a new device where no margin verify fails occur, is given by:

$$t_{dera} \approx 5025 \cdot \frac{1}{f_{NVMOP}} + 700 \cdot \frac{1}{f_{NVMBUS}}$$

Maximum D-Flash sector erase times is given by:

$$t_{dera} \approx 20100 \cdot \frac{1}{f_{NVMOP}} + 3400 \cdot \frac{1}{f_{NVMBUS}}$$

The D-Flash sector erase time is ~5.0 ms on a new device and can extend to ~20 ms as the flash is cycled.

Table 39. NVM Timing Characteristics (FTMRC)

C	Rating	Symbol	Min	Typ(43)	Max(44)	Unit(45)
	Bus frequency(46)	f_{NVMBUS}	1	—	32	MHz
	Operating frequency	f_{NVMOP}	0.8	1.0	1.05	MHz
D	Erase all blocks (mass erase) time	t_{mass}	—	100	130	ms
D	Erase verify all blocks (blank check) time	t_{CHECK}	—	—	19200	t_{CYC}
D	Unsecure Flash time	t_{UNS}	—	100	130	ms
D	P-Flash block erase time	t_{PMASS}	—	100	130	ms
D	P-Flash erase verify (blank check) time	t_{PCHECK}	—	—	17200	t_{CYC}
D	P-Flash sector erase time	t_{PERA}	—	20	26	ms
D	P-Flash phrase programming time	t_{PPGM}	—	226	285	µs
D	D-Flash sector erase time	t_{DERA}	—	5(47)	26	ms
D	D-Flash erase verify (blank check) time	t_{DCHECK}	—	—	2800	t_{CYC}
D	D-Flash one word programming time	t_{DPGM1}	—	100	107	µs
D	D-Flash two word programming time	t_{DPGM2}	—	170	185	µs
D	D-Flash three word programming time	t_{DPGM3}	—	241	262	µs
D	D-Flash four word programming time	t_{DPGM4}	—	311	339	µs
D	D-Flash four word programming time crossing row boundary	t_{DPGM4C}	—	328	357	µs

Note:
43. Typical program and erase times are based on typical f_{NVMOP} and maximum f_{NVMBUS}.
44. Maximum program and erase times are based on minimum f_{NVMOP} and maximum f_{NVMBUS}.
45. $t_{CYC} = 1 / f_{NVMBUS}$
46. The maximum device bus clock is specified as fBUS.
47. Typical value for a new device.

4.6.2.1.2 NVM Reliability Parameters

The reliability of the NVM blocks is guaranteed by stress test during qualification, constant process monitors, and burn-in to screen early life failures.

The data retention and program/erase cycling failure rates are specified at the operating conditions noted. The program/erase cycle count on the sector is incremented every time a sector or mass erase event is executed.

NOTE

All values shown in Table 40 are preliminary and subject to further characterization.

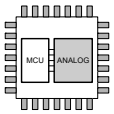
Table 60. 0x0020–0x002F Debug Module (DBG)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0022	DBGTCR	R	0	TSOURCE	0	0	TRCMOD		0	TALIGN
		W								
0x0023	DBGC2	R	0	0	0	0	0	0	ABCM	
		W								
0x0024	DBGTBH	R	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		W								
0x0025	DBGTBL	R	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		W								
0x0026	DBGCNT	R	TBF	0	CNT					
		W								
0x0027	DBGSCRX	R	0	0	0	0	SC3	SC2	SC1	SC0
		W								
	DBGMFR	R	0	0	0	0	0	MC2	MC1	MC0
		W								
	DBGACTL	R	SZE	SZ	TAG	BRK	RW	RWE	NDB	COMPE
		W								
0x0028	DBGBCTL	R	SZE	SZ	TAG	BRK	RW	RWE	0	COMPE
		W								
	DBGCCTL	R	0	0	TAG	BRK	RW	RWE	0	COMPE
		W								
0x0029	DBGXAH	R	0	0	0	0	0	0	Bit 17	Bit 16
		W								
0x002A	DBGXAM	R	Bit 15	14	13	12	11	10	9	Bit 8
		W								
0x002B	DBGXAL	R	Bit 7	6	5	4	3	2	1	Bit 0
		W								
0x002C	DBGADH	R	Bit 15	14	13	12	11	10	9	Bit 8
		W								
0x002D	DBGADL	R	Bit 7	6	5	4	3	2	1	Bit 0
		W								
0x002E	DBGADHM	R	Bit 15	14	13	12	11	10	9	Bit 8
		W								
0x002F	DBGADLM	R	Bit 7	6	5	4	3	2	1	Bit 0
		W								

Table 61. 0x0030–0x033 Reserved

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0030-0x0033	Reserved	R	0	0	0	0	0	0	0	0
		W								

5.11 Hall Sensor Supply Output - HSUP



To supply Hall Effect Sensors or similar external loads, the HSUP output is implemented. To reduce power dissipation inside the device, the output is implemented as a switchable Voltage Regulator, internally connected to the VS1 supply input. For protection, an Over-temperature Shutdown and a Current Limitation is implemented. A write to the Hall Supply Register (HSR), when the over-temperature condition is gone, will re-enable the Hall Supply Output.

The HSUP output is active only during Normal mode. A capacitor CHSUP is recommended for operation.

5.11.1 Register Definition

5.11.1.1 Hall Supply Register (HSR)

Table 104. Hall Supply Register (HSR)

Offset[81] 0x38 — Access: User read/write

	7	6	5	4	3	2	1	0
R	HOTIE	HOTC	0	0	0	0	0	HSUPON
W								
Reset	0	0	0	0	0	0	0	0

Note:
81. Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

Table 105. HSR - Register Field Descriptions

Field	Description
7 - HOTIE	Hall Supply Over-temperature Interrupt Enable
6 - HOTC	Hall Supply Over-temperature Condition present. During the event, the Hall Supply is shut down. Reading the register will clear the HOT flag if present. See Section 5.7, “Interrupts" for details.
0 - HSUPON	Hall Supply On: 0 - Hall Supply Regulator disabled 1 - Hall Supply Regulator enabled

5.14 PWM Control Module (PWM8B2C)

5.14.1 Introduction

To control the High Side (HS1, HS2) and the Low Side (LS1, LS2) duty cycle as well as the PTB2 output, the PWM module is implemented. Refer to the individual driver section for details on the use of the internal PWM1 and PWM0 signal (Section 5.12, “High Side Drivers - HS", Section 5.13, “Low Side Drivers - LSx" and Section 5.18, “General Purpose I/O - PTB[0…2]")

The PWM definition is based on the HC12 PWM definitions with some of the simplifications incorporated. The PWM module has two channels with independent controls of left and center aligned outputs on each channel.

Each of the two channels has a programmable period and duty cycle as well as a dedicated counter. A flexible clock select scheme allows a total of four different clock sources to be used with the counters. Each of the modulators can create independent continuous waveforms with software-selectable duty rates from 0% to 100%.

5.14.1.1 Features

The PWM block includes these distinctive features:

- Two independent PWM channels with programmable periods and duty cycles
- Dedicated counter for each PWM channel
- Programmable PWM enable/disable for each channel
- Software selection of PWM duty pulse polarity for each channel
- Period and duty cycle are double buffered. Change takes effect when the end of the effective period is reached (PWM counter reaches zero), or when the channel is disabled
- Programmable center or left aligned outputs on individual channels
- Four clock sources (A, B, SA, and SB) provide for a wide range of frequencies
- Programmable clock select logic

5.14.1.2 Modes of Operation

The PWM8B2C module does operate in Normal mode only.

5.14.1.3 Block Diagram

Figure 22 shows the block diagram for the 8-bit 2-channel PWM block.

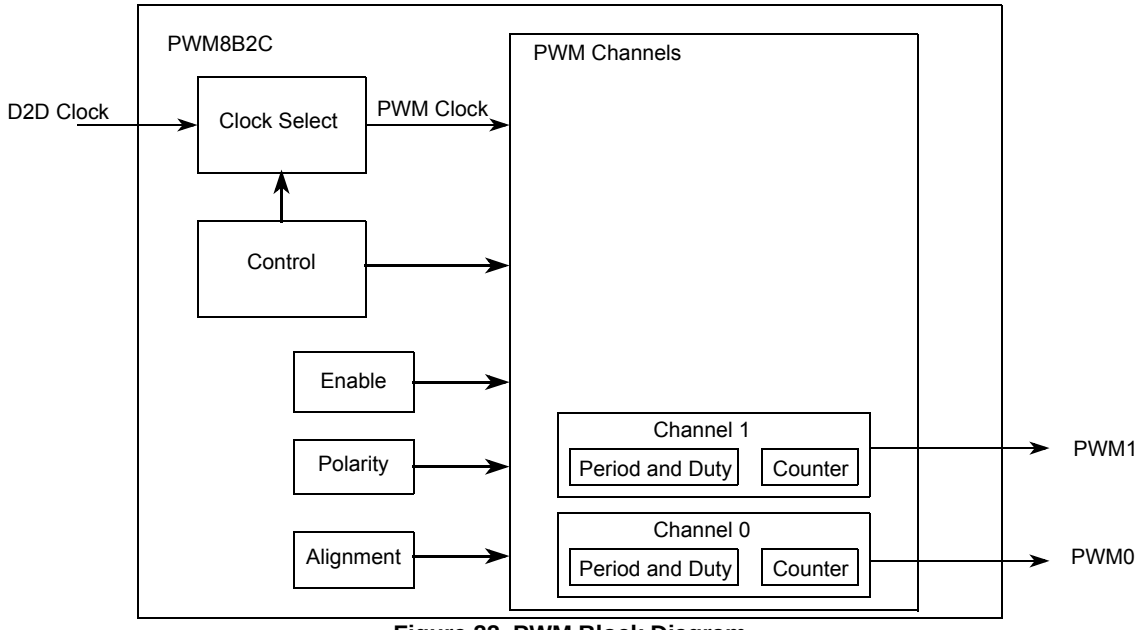


Figure 22. PWM Block Diagram

5.14.4.2.7 PWM Boundary Cases

Table 131 summarizes the boundary conditions for the PWM, regardless of the output mode (left aligned or center aligned).

Table 131. PWM Boundary Cases

PWMDTYx	PWMPERx	PPOLx	PWMx Output
$00 (indicates no duty)	>$00	1	Always low
$00 (indicates no duty)	>$00	0	Always high
XX	$00[97] (indicates no period)	1	Always high
XX	$00[97] (indicates no period)	0	Always low
>= PWMPERx	XX	1	Always high

Note:
97. Counter = $00 and does not count.

5.14.5 Resets

The reset state of each individual bit is listed within the Section 5.14.3, “Register Descriptions", which details the registers and their bit-fields. All special functions or modes which are initialized during or just following reset are described within this section.

- The 8-bit up/down counter is configured as an up counter out of reset.
- All the channels are disabled and all the counters do not count.

5.14.6 Interrupts

The PWM module has no Interrupts.

(synchronized to the baud rate clock), an additional break character is queued. If the receiving device is another Freescale Semiconductor SCI, the break characters will be received as 0s in all eight data bits and a framing error (FE = 1) occurs.

When idle-line wake-up is used, a full character time of idle (logic 1) is needed between messages to wake up any sleeping receivers. Normally, a program would wait for TDRE to become set to indicate the last character of a message has moved to the transmit shifter, then write 0 and then write 1 to the TE bit. This action queues an idle character to be sent as soon as the shifter is available. As long as the character in the shifter does not finish while TE = 0, the SCI transmitter never actually releases control of the TxD pin. If there is a possibility of the shifter finishing while TE = 0, set the general-purpose I/O controls so the pin that is shared with TxD is an output driving a logic 1. This ensures that the TxD line will look like a normal idle line even if the SCI loses control of the port pin between writing 0 and then 1 to TE.

The length of the break character is affected by the BRK13 and M bits as shown below.

Table 149. Break Character Length

BRK13	M	Break Character Length
0	0	10 bit times
0	1	11 bit times
1	0	13 bit times
1	1	14 bit times

5.16.3.3 Receiver Functional Description

In this section, the receiver block diagram (Figure 30) is used as a guide for the overall receiver functional description. Next, the data sampling technique used to reconstruct receiver data is described in more detail. Finally, two variations of the receiver wake-up function are explained.

The receiver input is inverted by setting RXINV = 1. The receiver is enabled by setting the RE bit in SCIC2. Character frames consist of a start bit of logic 0, eight (or nine) data bits (LSB first), and a stop bit of logic 1. For information about 9-bit data mode, refer to Section •, “8 and 9-bit data modes". For the remainder of this discussion, we assume the SCI is configured for normal 8-bit data mode.

After receiving the stop bit into the receive shifter, and provided the receive data register is not already full, the data character is transferred to the receive data register and the receive data register full (RDRF) status flag is set. If RDRF was already set indicating the receive data register (buffer) was already full, the overrun (OR) status flag is set and the new data is lost. Because the SCI receiver is double-buffered, the program has one full character time after RDRF is set before the data in the receive data buffer must be read to avoid a receiver overrun.

When a program detects that the receive data register is full (RDRF = 1), it gets the data from the receive data register by reading SCID. The RDRF flag is cleared automatically by a 2-step sequence which is normally satisfied in the course of the user’s program that handles receive data. Refer to Section 5.16.3.4, “Interrupts and Status Flags" for more details about flag clearing.

5.16.3.3.1 Data Sampling Technique

The SCI receiver uses a 16× baud rate clock for sampling. The receiver starts by taking logic level samples at 16 times the baud rate to search for a falling edge on the RxD serial data input pin. A falling edge is defined as a logic 0 sample after three consecutive logic 1 samples. The 16× baud rate clock is used to divide the bit time into 16 segments labeled RT1 through RT16. When a falling edge is located, three more samples are taken at RT3, RT5, and RT7 to make sure this was a real start bit and not merely noise. If at least two of these three samples are 0, the receiver assumes it is synchronized to a receive character.

The receiver then samples each bit time, including the start and stop bits, at RT8, RT9, and RT10 to determine the logic level for that bit. The logic level is interpreted to be that of the majority of the samples taken during the bit time. In the case of the start bit, the bit is assumed to be 0 if at least two of the samples at RT3, RT5, and RT7 are 0 even if one or all of the samples taken at RT8, RT9, and RT10 are 1s. If any sample in any bit time (including the start and stop bits) in a character frame fails to agree with the logic level for that bit, the noise flag (NF) will be set when the received character is transferred to the receive data buffer.

The falling edge detection logic continuously looks for falling edges, and if an edge is detected, the sample clock is resynchronized to bit times. This improves the reliability of the receiver in the presence of noise or mismatched baud rates. It does not improve worst case analysis because some characters do not have any extra falling edges anywhere in the character frame.

In the case of a framing error, provided the received character was not a break character, the sampling logic that searches for a falling edge is filled with three logic 1 samples so that a new start bit can be detected almost immediately.

If the associated error was detected in the received character that caused RDRF to be set, the error flags — noise flag (NF), framing error (FE), and parity error flag (PF) — get set at the same time as RDRF. These flags are not set in overrun cases.

If RDRF was already set when a new character is ready to be transferred from the receive shifter to the receive data buffer, the overrun (OR) flag gets set instead the data along with any associated NF, FE, or PF condition is lost.

At any time, an active edge on the RxD serial data input pin causes the RXEDGIF flag to set. The RXEDGIF flag is cleared by writing a “1” to it. This function does depend on the receiver being enabled (RE = 1).

5.16.3.5 Additional SCI Functions

The following sections describe additional SCI functions.

5.16.3.5.1 8- and 9-Bit Data Modes

The SCI system (transmitter and receiver) can be configured to operate in 9-bit data mode by setting the M control bit in SCIC1. In 9-bit mode, there is a ninth data bit to the left of the MSB of the SCI data register. For the transmit data buffer, this bit is stored in T8 in SCIC3. For the receiver, the ninth bit is held in R8 in SCIC3.

For coherent writes to the transmit data buffer, write to the T8 bit before writing to SCID.

If the bit value to be transmitted as the ninth bit of a new character is the same as for the previous character, it is not necessary to write to T8 again. When data is transferred from the transmit data buffer to the transmit shifter, the value in T8 is copied at the same time data is transferred from SCID to the shifter.

9-bit data mode typically is used in conjunction with parity to allow eight bits of data plus the parity in the ninth bit. Or it is used with address-mark wake-up so the ninth data bit can serve as the wake-up bit. In custom protocols, the ninth bit can also serve as a software-controlled marker.

5.16.3.5.2 Stop Mode Operation

During all stop modes, clocks to the SCI module are halted.

In stop1 and stop2 modes, all SCI register data is lost and must be re-initialized upon recovery from these two stop modes. No SCI module registers are affected in stop3 mode.

The receive input active edge detect circuit is still active in stop3 mode, but not in stop2. An active edge on the receive input brings the CPU out of stop3 mode if the interrupt is not masked (RXEDGIE = 1).

Note that because the clocks are halted, the SCI module will resume operation upon exit from stop (only in stop3 mode). Software should ensure stop mode is not entered while there is a character being transmitted out of or received into the SCI module.

5.16.3.5.3 Loop Mode

When LOOPS = 1, the RSRC bit in the same register chooses between loop mode (RSRC = 0) or single-wire mode (RSRC = 1). Loop mode is sometimes used to check software, independent of connections in the external system, to help isolate system problems. In this mode, the transmitter output is internally connected to the receiver input and the RxD pin is not used by the SCI, so it reverts to a general purpose port I/O pin.

5.16.3.5.4 Single-wire Operation

When LOOPS = 1, the RSRC bit in the same register chooses between loop mode (RSRC = 0) or single-wire mode (RSRC = 1). Single-wire mode is used to implement a half-duplex serial connection. The receiver is internally connected to the transmitter output and to the TxD pin. The RxD pin is not used and reverts to a general purpose port I/O pin.

In single-wire mode, the TXDIR bit in SCIC3 controls the direction of serial data on the TxD pin. When TXDIR = 0, the TxD pin is an input to the SCI receiver and the transmitter is temporarily disconnected from the TxD pin so an external device can send serial data to the receiver. When TXDIR = 1, the TxD pin is an output driven by the transmitter. In single-wire mode, the internal loop back connection from the transmitter to the receiver causes the receiver to receive characters that are sent out by the transmitter.

5.18 General Purpose I/O - PTB[0…2]

The three multipurpose I/O pins can be configured to operate as documented in the table below.

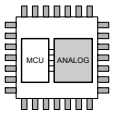


Table 154. General purpose I/O - Operating modes

Priority	Function	PTB2	PTB1	PTB0	Chp/Pg
1 (H)	2.5 V Analog Input	AD2	AD1	AD0	5.20/135
2	Timer Input Capture / Output Compare	TIMCH2	TIMCH1	TIMCH0	5.19/122
3	LIN / SCI - Rx / Tx (PTB0…1) or PWM (PTB2)	PWM	Tx	Rx	5.15/102
4 (L)	5.0 V Input Output	PTB2	PTB1	PTB0	current

The alternate function of PTB2, PTB1 and PTB0 can be configured by selecting the function in the corresponding module (e.g. TIMER). The selection with the highest priority will take effect when more than one function is selected.

5.18.1 Digital I/O Functionality

All three pins act as standard digital Inputs / Outputs with selectable pull-up resistor.

5.18.2 Alternative SCI / LIN Functionality

For alternative serial configuration and for debug and certification purpose, PTB0 and PTB1 can be configured to connect to the internal LIN and / or SCI signals (RxD and TxD). Figure 32 shows the 4 available configurations.

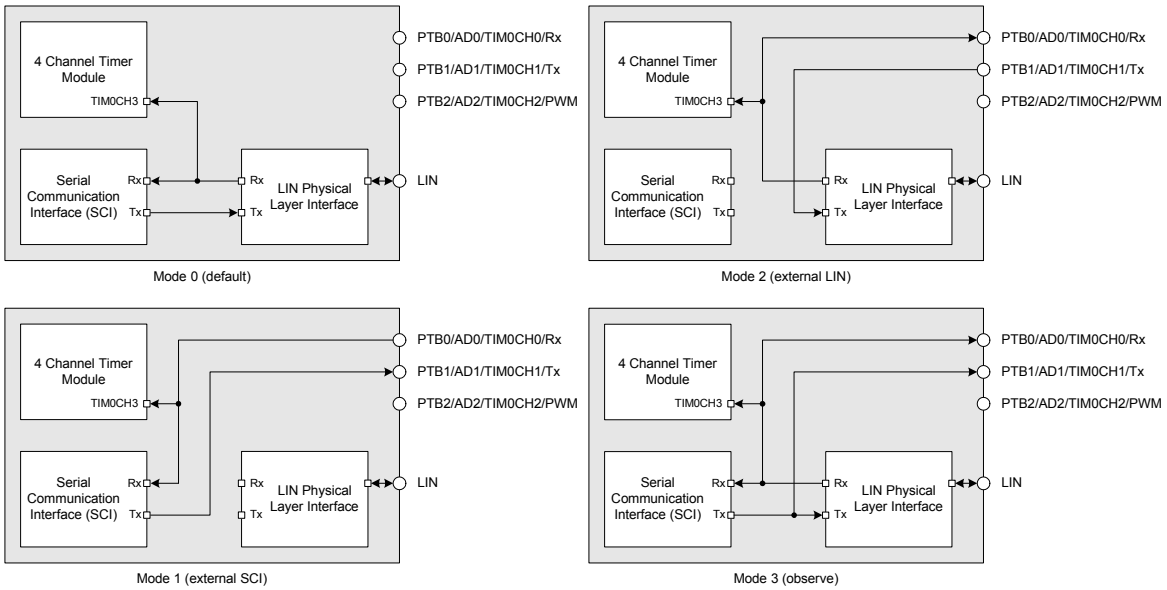


Figure 32. Alternative SCI / LIN Functionality

5.18.3 Alternative PWM Functionality

As an alternative routing for the PWM channel (0 or 1) output, the PortB 2 (PTB2) can be configured to output one of the two PWM channels defined in the Section 5.14, “PWM Control Module (PWM8B2C)". The selection and output enable can be configured in the Port B Configuration Register 2 (PTBC2).

5.18.4 Register definition

5.18.4.1 Port B Configuration Register 1 (PTBC1)

Table 155. Port B Configuration Register 1 (PTBC1)

Offset(111) 0x20 — Access: User read/write

	7	6	5	4	3	2	1	0
R	0	PUEB2	PUEB1	PUEB0	0	DDRB2	DDRB1	DDRB0
W								
Reset	0	0	0	0	0	0	0	0

Note:
111. Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

Table 156. PTBC1 - Register Field Descriptions

Field	Description
6-4 PUEB[2-0]	Pull-up Enable Port B[2…0] 0 - Pull-up disabled on PTBx pin. 1- Pull-up enabled on PTBx pin.
2-0 DDRB[2-0]	Data Direction Port B[2…0] 0 - PTBx configured as input. 1 - PTBx configured as output.

NOTE

The pull-up resistor is not active once the port is configured as an output.

5.18.4.2 Port B Configuration Register 2 (PTBC2)

Table 157. Port B Configuration Register 2 (PTBC2)

Offset(112) 0x21 — Access: User read/write

	7	6	5	4	3	2	1	0
R	0	0	0	0	PWMCS	PWMEN	SERMOD	
W								
Reset	0	0	0	0	0	0	0	0

Note:
112. Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

Table 169. OC3D - Register Field Descriptions

Field	Description
3-0 OC3D[3-0]	Output Compare 3 Data for Channel "n"

NOTE

A channel 3 output compare will cause bits in the output compare 3 data register to transfer to the timer port data register if the corresponding output compare 3 mask register bits are set.

5.19.3.3.5 Timer Count Register (TCNT)

Table 170. Timer Count Register (TCNT)

Offset(121) 0xC4, 0xC5 — Access: User read(anytime)/write (special mode)

	15	14	13	12	11	10	9	8
R W	tcnt15	tcnt14	tcnt13	tcnt12	tcnt11	tcnt10	tcnt9	tcnt8
Reset	0	0	0	0	0	0	0	0
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
R W	tcnt7	tcnt6	tcnt5	tcnt4	tcnt3	tcnt2	tcnt1	tcnt0
Reset	0	0	0	0	0	0	0	0

Note:
121. Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

Table 171. TCNT - Register Field Descriptions

Field	Description
15-0 tcnt[15-0]	16 Bit Timer Count Register

NOTE

The 16-bit main timer is an up counter. A full access for the counter register should take place in one clock cycle. A separate read/write for high byte and low byte will give a different result than accessing them as a word. The period of the first count after a write to the TCNT registers may be a different length because the write is not synchronized with the prescaler clock.

5.19.3.3.6 Timer System Control Register 1 (TSCR1)

Table 172. Timer System Control Register 1 (TSCR1)

Offset(122) 0xC6 — Access: User read/write

	7	6	5	4	3	2	1	0
R	TEN	0	0	TFFCA	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

Note:
122. Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

pin low, in order to allow the negative edge to be detected by the target.In this case, the target will not execute the SYNC protocol but the pending command will be aborted along with the ACK pulse. The potential problem with this abort procedure is when there is a conflict between the ACK pulse and the short abort pulse. In this case, the target may not perceive the abort pulse. The worst case is when the pending command is a read command (i.e., READ_BYTE). If the abort pulse is not perceived by the target the host will attempt to send a new command after the abort pulse was issued, while the target expects the host to retrieve the accessed memory byte. In this case, host and target will run out of synchronism. However, if the command to be aborted is not a read command the short abort pulse could be used. After a command is aborted the target assumes the next negative edge, after the abort pulse, is the first bit of a new BDM command.

NOTE

The details about the short abort pulse are being provided only as a reference for the reader to better understand the BDM internal behavior. It is not recommended that this procedure be used in a real application.

Since the host knows the target serial clock frequency, the SYNC command (used to abort a command) does not need to consider the lower possible target frequency. In this case, the host could issue a SYNC very close to the 128 serial clock cycles length. Providing a small overhead on the pulse length in order to assure the SYNC pulse will not be misinterpreted by the target. See Section 5.31.4.9, “SYNC — Request Timed Reference Pulse".

Figure 60 shows a SYNC command being issued after a READ_BYTE, which aborts the READ_BYTE command. Note that, after the command is aborted a new command could be issued by the host computer.

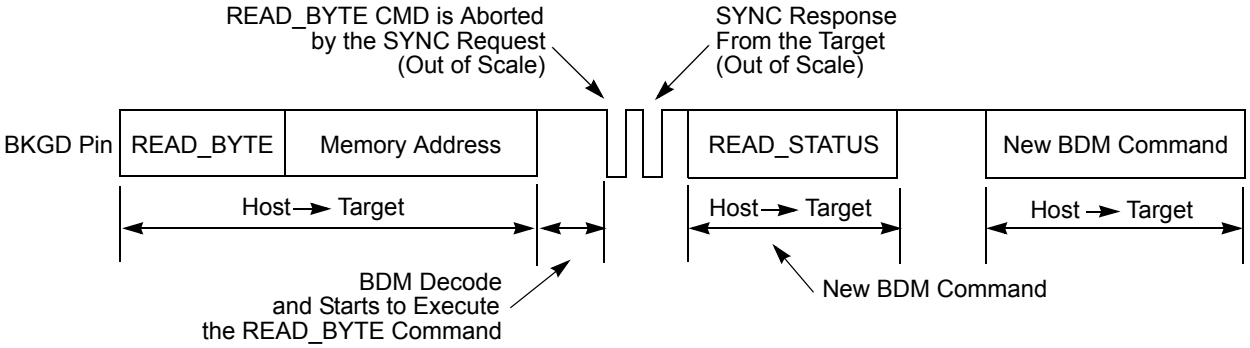


Figure 60. ACK Abort Procedure at the Command Level

NOTE

Figure 60 does not represent the signals in a true timing scale

Figure 61 shows a conflict between the ACK pulse and the SYNC request pulse. This conflict could occur if a POD device is connected to the target BKGD pin and the target is already in debug active mode. Consider that the target CPU is executing a pending BDM command at the exact moment the POD is being connected to the BKGD pin. In this case, an ACK pulse is issued along with the SYNC command. In this case, there is an electrical conflict between the ACK speedup pulse and the SYNC pulse. Since this is not a probable situation, the protocol does not prevent this conflict from happening.

5.32.2 External Signal Description

There are no external signals associated with this module.

5.32.3 Memory Map and Registers

5.32.3.1 Module Memory Map

A summary of the registers associated with the DBG sub-block is shown in Figure 270. Detailed descriptions of the registers and bits are given in the subsections that follow.

Table 270. Quick Reference to DBG Registers

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0020	DBGC1	R	ARM	0	0	BDM	DBGBRK	0	COMRV	
		W		TRIG						
0x0021	DBGSR	R	TBF[184]	0	0	0	0	SSF2	SSF1	SSF0
		W								
0x0022	DBGTCR	R	0	TSOURCE	0	0	TRCMOD		0	TALIGN
		W								
0x0023	DBGC2	R	0	0	0	0	0	0	ABCM	
		W								
0x0024	DBGTBH	R	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		W								
0x0025	DBGTBL	R	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		W								
0x0026	DBGCNT	R	TBF	0	CNT					
		W								
0x0027	DBGSCRX	R	0	0	0	0	SC3	SC2	SC1	SC0
		W								
0x0027	DBGMFR	R	0	0	0	0	0	MC2	MC1	MC0
		W								
0x0028	DBGACTL	R	SZE	SZ	TAG	BRK	RW	RWE	NDB	COMPE
		W								
0x0028	DBGBCTL	R	SZE	SZ	TAG	BRK	RW	RWE	0	COMPE
		W								
0x0028	DBGCCTL	R	0	0	TAG	BRK	RW	RWE	0	COMPE
		W								
0x0029	DBGXAH	R	0	0	0	0	0	0	Bit 17	Bit 16
		W								
0x002A	DBGXAM	R	Bit 15	14	13	12	11	10	9	Bit 8
		W								
0x002B	DBGXAL	R	Bit 7	6	5	4	3	2	1	Bit 0
		W								
0x002C	DBGADH	R	Bit 15	14	13	12	11	10	9	Bit 8
		W								
0x002D	DBGADL	R	Bit 7	6	5	4	3	2	1	Bit 0
		W								

Table 279. TRCMOD Trace Mode Bit Encoding

TRCMOD	Description
00	Normal
01	Loop1
10	Detail
11	Compressed Pure PC

5.32.3.2.4 Debug Control Register2 (DBGC2)

Table 280. Debug Control Register2 (DBGC2)

Address: 0x0023

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	ABCM	
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Read: Anytime

Write: Anytime the module is disarmed.

This register configures the comparators for range matching.

Table 281. DBGC2 Field Descriptions

Field	Description
1–0 ABCM[1:0]	A and B Comparator Match Control — These bits determine the A and B comparator match mapping as described in Table 282.

Table 282. ABCM Encoding

ABCM	Description
00	Match0 mapped to comparator A match: Match1 mapped to comparator B match.
01	Match 0 mapped to comparator A/B inside range: Match1 disabled.
10	Match 0 mapped to comparator A/B outside range: Match1 disabled.
11	Reserved(188)

Note:

188. Currently defaults to Comparator A, Comparator B disabled

5.32.3.2.5 Debug Trace Buffer Register (DBGTBH:DBGTBL)

Table 283. Debug Trace Buffer Register (DBGTB)

Address: 0x0024, 0x0025

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
POR	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Other Resets	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—

Read: Only when unlocked AND unsecured AND not armed AND TSOURCE set.

Write: Aligned word writes when disarmed unlock the trace buffer for reading but do not affect trace buffer contents.

5.32.3.2.8.2 Debug Comparator Address High Register (DBGXAH)

Table 305. Debug Comparator Address High Register (DBGXAH)

Address: 0x0029

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	Bit 17	Bit 16
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

The DBGC1_COMRV bits determine which comparator address registers are visible in the 8-byte window from 0x0028 to 0x002F as shown in Table 306.

Table 306. Comparator Address Register Visibility

COMRV	Visible Comparator
00	DBGAAH, DBGAAM, DBGAAL
01	DBGBAH, DBGBAM, DBGBAL
10	DBGCAH, DBGCAM, DBGCAL
11	None

Read: Anytime. See Table 306 for visible register encoding.

Write: If DBG not armed. See Table 306 for visible register encoding.

Table 307. DBGXAH Field Descriptions

Field	Description
1–0 Bit[17:16]	**Comparator Address High Compare Bits** — The Comparator address high compare bits control whether the selected comparator compares the address bus bits [17:16] to a logic one or logic zero. 0 Compare corresponding address bit to a logic zero 1 Compare corresponding address bit to a logic one

5.32.3.2.8.3 Debug Comparator Address Mid Register (DBGXAM)

Table 308. Debug Comparator Address Mid Register (DBGXAM)

Address: 0x002A

	7	6	5	4	3	2	1	0
R	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
W								
Reset	0	0	0	0	0	0	0	0

Read: Anytime. See Table 306 for visible register encoding.

Write: If DBG not armed. See Table 306 for visible register encoding.

Table 309. DBGXAM Field Descriptions

Field	Description
7–0 Bit[15:8]	**Comparator Address Mid Compare Bits** — The Comparator address mid compare bits control whether the selected comparator compares the address bus bits [15:8] to a logic one or logic zero. 0 Compare corresponding address bit to a logic zero 1 Compare corresponding address bit to a logic one

One cycle after bdm_unsecure is asserted the secure firmware is disabled from the map.

In secure mode aBDM access to a non register address will be translated to a peripheral register address, and BDM registers are not accessible.

No BDM global access is possible if the chip is secured.

In secured expanded mode or emulation mode, FLASH and EEPROM are disabled by the MMC.

5.34.2 BDM

When security is active and the blank check is performed and failed, only BDM hardware commands are available. If the blank check is succeeds, all BDM commands are available.

The BDM status register contains a bit called UNSEC. This bit is only writable by the secure firmware in special single chip mode. Based on the state of this bit, the BDM generates a signal called “unsecure”. The bit and signal are always reset to 0 (= de-asserted = secure).

If the user resets into special single chip mode with the part secured, an alternate BDM firmware (“SECURE firmware”), is placed in the map along with the standard BDM firmware. The secure firmware has higher priority than the standard firmware, but it is smaller (less bytes). The secure firmware covers the vector space, but does not reach the beginning of the BDM firmware space.

When blank check is successfully performed, UNSEC is asserted. The BDM program jumps to the start of the standard BDM firmware program and the secure firmware is turned off. If the blank check fails, then the ENBDM bit in the BDMSTS register is set without asserting UNSEC, and the BDM firmware code enters a loop. This enables the BDM hardware commands. In secure mode the MMC restricts BDM accesses to the register space.

With UNSEC asserted, security is off and the user can change the state of the secure bits in the FLASH. Note that if the user does not change the state of these bits to “unsecured”, the part will be secured again when it is next taken out of reset.

5.34.3 DBG

S12X_DBG will disable the trace buffer, but breakpoints are still valid.

5.34.4 XGATE

XGATE internal registers XGCCR, XGPC, and XGR1 - XGR7 can not be written and will read zero from IPBI.

Single stepping in XGATE is not possible.

XGATE code residing in the internal RAM cannot be protected:

1. start MCU in NSC, let it run for a while
2. reset into SSC, MASERS the NVM
3. reset into SSC, blank check of BDM secure firmware succeeds
4. MCU is temporarily unsecured
5. BDM can be used to read internal RAM (contents not affected by reset)

5.35 Secure firmware Code Overview

The BDM contains a secure firmware code. This firmware code is invoked when the user comes out of reset in special single chip mode with security enabled. The function of the firmware code is straight forward:

- Verify the FLASH is erased
- Verify the EEPROM is erased
- If both are erased, release security

If either the FLASH or the EEPROM is not erased, then security is not released. The ENBDM bit is set and the code enters a loop. This allows BDM hardware commands, which may be used to erase the EEPROM and FLASH.

Note that erasing the memories and erasing / reprogramming the security bits is NOT part of the firmware code. The user must perform these operations.

The blank check of FLASH and EEPROM is done in the BDM firmware. As such it could be changed on future parts. The current scheme uses the NVM command state-machines (FTX, EETX) to perform the blank check.

Table 370. CPMUAPICTL Field Descriptions

Field	Description
7 APICLK	**Autonomous Periodical Interrupt Clock Select Bit** — Selects the clock source for the API. Writable only if APIFE = 0. APICLK cannot be changed if APIFE is set by the same write operation. 0 Autonomous periodical interrupt clock used as source. 1 Bus Clock used as source.
4 APIES	**Autonomous Periodical Interrupt External Select Bit** — Selects the waveform at the external pin API_EXTCLK as shown in Figure . See device level specification for connectivity of API_EXTCLK pin. 0 If APIEA and APIFE are set, at the external pin API_EXTCLK periodic high pulses are visible at the end of every selected period with the size of half of the minimum period (APIR=0x0000 in Table 377). 1 If APIEA and APIFE are set, at the external pin API_EXTCLK a clock is visible with 2 times the selected API Period.
3 APIEA	**Autonomous Periodical Interrupt External Access Enable Bit** — If set, the waveform selected by bit APIES can be accessed externally. See device level specification for connectivity. 0 Waveform selected by APIES can not be accessed externally. 1 Waveform selected by APIES can be accessed externally, if APIFE is set.
2 APIFE	**Autonomous Periodical Interrupt Feature Enable Bit** — Enables the API feature and starts the API timer when set. 0 Autonomous periodical interrupt is disabled. 1 Autonomous periodical interrupt is enabled and timer starts running.
1 APIE	Autonomous Periodical Interrupt Enable Bit 0 API interrupt request is disabled. 1 API interrupt will be requested whenever APIF is set.
0 APIF	**Autonomous Periodical Interrupt Flag** — APIF is set to 1 when the in the API configured time has elapsed. This flag can only be cleared by writing a 1. Writing a 0 has no effect. If enabled (APIE = 1), APIF causes an interrupt request. 0 API time-out has not yet occurred. 1 API time-out has occurred.

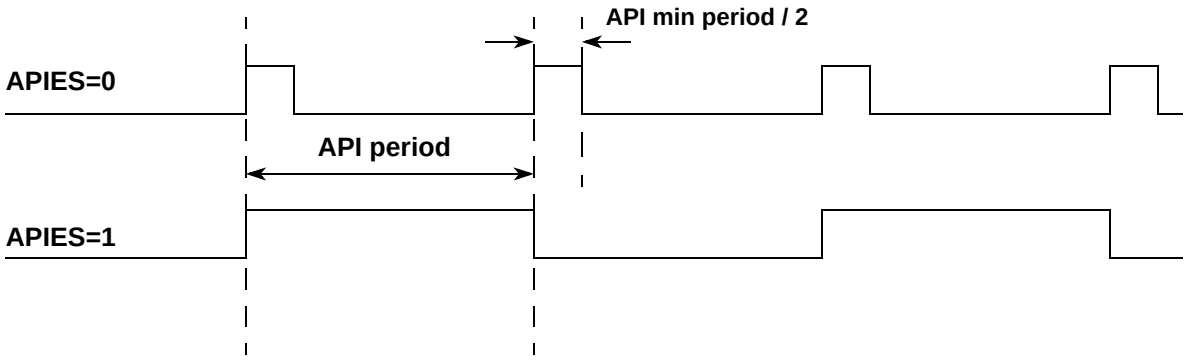


Figure 84. Waveform selected on API_EXTCLK pin (APIEA=1, APIFE=1)

5.38.3.2.20 S12CPMU Oscillator Register (CPMUOSC)

This register configures the external oscillator (OSCLCP).

Table 383. S12CPMU Oscillator Register (CPMUOSC)

0x02FA

	7	6	5	4	3	2	1	0
R	OSCE	OSCBW	OSCPINS_EN	OSCFILT[4:0]				
W								
Reset	0	0	0	0	0	0	0	0

Read: Anytime

Write: Anytime if PROT=0 (CPMUPROT register) and PLLSEL=1 (CPMUCLKS register). Else write has no effect.

NOTE

Write to this register clears the LOCK and UPOSC status bits.

NOTE

If the chosen VCOCLK-to-OSCCLK ratio divided by two ((f_{VCO} / f_{OSC})/2) is not an integer number, the filter can not be used and the OSCFILT[4:0] bits must be set to 0.

NOTE

The frequency modulation (FM1 and FM0) can not be used if the Adaptive Oscillator Filter is enabled.

Table 384. CPMUOSC Field Descriptions

Field	Description
7 OSCE	**Oscillator Enable Bit** — This bit enables the external oscillator (OSCLCP). The UPOSC status bit in the CPMUFLG register indicates when the oscillation is stable and OSCCLK can be selected as Bus Clock or source of the COP or RTI. A loss of oscillation will lead to a clock monitor reset. 0 External oscillator is disabled. REFCLK for PLL is IRCCLK. 1 External oscillator is enabled.Clock monitor is enabled. REFCLK for PLL is external oscillator clock divided by REFDIV. Note: When starting up the external oscillator (either by programming OSCE bit to 1 or on exit from Full Stop Mode with OSCE bit already 1) the software must wait for a minimum time equivalent to the startup-time of the external oscillator t_{UPOSC} before entering Pseudo Stop Mode.
6 OSCBW	**Oscillator Filter Bandwidth Bit** — If the VCOCLK frequency exceeds 25 MHz wide bandwidth must be selected. The Oscillator Filter is described in more detail at Section 5.38.4.5.2, “The Adaptive Oscillator Filter" 0 Oscillator filter bandwidth is narrow (window for expected OSCCLK edge is one VCOCLK cycle). 1 Oscillator filter bandwidth is wide (window for expected OSCCLK edge is three VCOCLK cycles).
5 OSCPINS_EN	**Oscillator Pins EXTAL and XTAL Enable Bit** If OSCE=1 this read-only bit is set. It can only be cleared with the next reset. Enabling the external oscillator reserves the EXTAL and XTAL pins exclusively for oscillator application. 0 EXTAL and XTAL pins are not reserved for oscillator. 1 EXTAL and XTAL pins exclusively reserved for oscillator.
4-0 OSCFILT	**Oscillator Filter Bits** — When using the oscillator a noise filter can be enabled, which filters noise from the incoming external oscillator clock and detects if the external oscillator clock is qualified or not (quality status shown by bit UPOSC). The VCOCLK-to-OSCCLK ratio divided by two ((f_{VCO} / f_{OSC})/2) must be an integer value. This value must be written to the OSCFILT[4:0] bits to enable the Adaptive Oscillator Filter. 0x0000 Adaptive Oscillator Filter disabled. else Adaptive Oscillator Filter enabled]

5.38.3.2.21 S12CPMU Protection Register (CPMUPROT)

This register protects the following clock configuration registers from accidental overwrite:

CPMUSYNR, CPMUREFDIV, CPMUCLKS, CPMUPLL, CPMUIRCTRIMH/L and CPMUOSC

Table 403. Example SPI Baud Rate Selection (25 MHz us Clock) (continued)

SPPR2	SPPR1	SPPR0	SPR2	SPR1	SPR0	Baud Rate Divisor	Baud Rate
1	0	1	1	1	0	768	32.55 kbit/s
1	0	1	1	1	1	1536	16.28 kbit/s
1	1	0	0	0	0	14	1.78571 Mbit/s
1	1	0	0	0	1	28	892.86 kbit/s
1	1	0	0	1	0	56	446.43 kbit/s
1	1	0	0	1	1	112	223.21 kbit/s
1	1	0	1	0	0	224	111.61 kbit/s
1	1	0	1	0	1	448	55.80 kbit/s
1	1	0	1	1	0	896	27.90 kbit/s
1	1	0	1	1	1	1792	13.95 kbit/s
1	1	1	0	0	0	16	1.5625 Mbit/s
1	1	1	0	0	1	32	781.25 kbit/s
1	1	1	0	1	0	64	390.63 kbit/s
1	1	1	0	1	1	128	195.31 kbit/s
1	1	1	1	0	0	256	97.66 kbit/s
1	1	1	1	0	1	512	48.83 kbit/s
1	1	1	1	1	0	1024	24.41 kbit/s
1	1	1	1	1	1	2048	12.21 kbit/s

5.39.3.2.4 SPI Status Register (SPISR)

Table 404. SPI Status Register (SPISR)

	7	6	5	4	3	2	1	0
R	SPIF	0	SPTEF	MODF	0	0	0	0
W								
Reset	0	0	1	0	0	0	0	0

= Unimplemented or Reserved

Read: Anytime

Write: Has no effect