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Details	
Product Status	Active
Applications	Automotive
Core Processor	S12
Program Memory Type	FLASH (48kB)
Controller Series	HCS12
RAM Size	2K x 8
Interface	LIN, SCI
Number of I/O	9
Voltage - Supply	2.25V ~ 5.5V
Operating Temperature	-40°C ~ 105°C
Mounting Type	Surface Mount
Package / Case	48-LQFP Exposed Pad
Supplier Device Package	48-HLQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mm912g634dv1ae

Table 23. Static Electrical Characteristics - Current Sense Module - ISENSE

Ratings	Symbol	Min	Typ	Max	Unit
Gain					
CSGS (Current Sense Gain Select) = 000	G	-	7	-	
CSGS (Current Sense Gain Select) = 001		-	9	-	
CSGS (Current Sense Gain Select) = 010		-	10	-	
CSGS (Current Sense Gain Select) = 011		-	12	-	
CSGS (Current Sense Gain Select) = 100		-	14	-	
CSGS (Current Sense Gain Select) = 101		-	18	-	
CSGS (Current Sense Gain Select) = 110		-	24	-	
CSGS (Current Sense Gain Select) = 111		-	36	-	
Gain Accuracy		-3.0	-	3.0	%
Offset		-1.5	-	1.5	%
Resolution(29)	RES	-	51	-	mA/LSB
ISENSEH, ISENSEL Input Common Mode Voltage Range	V_{IN}	-0.2	-	3.0	V
Current Sense Module - Normal Mode Current Consumption Adder (CSE = 1)	I_{ISENSE}	-	600	-	µA

Note:
29. RES = 2.44 mV/(GAIN*R_{SHUNT})

Table 24. Static Electrical Characteristics - Temperature Sensor - TSENSE

Ratings	Symbol	Min	Typ	Max	Unit
Internal Chip Temperature Sense Gain(30)	TS_G	-	9.17	-	mV/k
Internal Chip Temperature Sense Error at the end of conversion(30)	TS_{Err}	–5.0	-	5.0	°C
Temperature represented by a ADC_{IN} Voltage of 0.150 V(30)	$T_{0.15V}$	-55	-50	-45	°C
Temperature represented by a ADC_{IN} Voltage of 1.984 V(30)	$T_{1.984V}$	145	150	155	°C

Note:
30. Guaranteed by design and characterization.

Table 25. Static Electrical Characteristics - Supply Voltage Sense - VSENSE and VS1SENSE

Ratings	Symbol	Min	Typ	Max	Unit
VSENSE Input Divider Ratio ($RATIO_{VSENSE}$ = V_{VSENSE} / ADCIN) 5.5 V < V_{SUP} < 27 V	$RATIO_{VSENSE}$	-	10.8	5.0%	
VSENSE error - whole path (VSENSE pad to Digital value)	Er_{VSENSE}	-	-	5.0	%
VS1SENSE Input Divider Ratio ($RATIO_{VS1SENSE}$ = $V_{VS1SENSE}$ / ADCIN) 5.5 V < V_{SUP} < 27 V	$RATIO_{VS1SENSE}$	-	10.8	5.0%	
VS1SENSE error - whole path (VS1 pad to Digital value)	$Er_{VS1SENSE}$	-	-	5.0	%
VSENSE Series Resistor	R_{VSENSE}	9.5	10	10.5	kOhm
VSENSE Capacitor (optional)(31)	C_{VSENSE}	-	100	-	nF

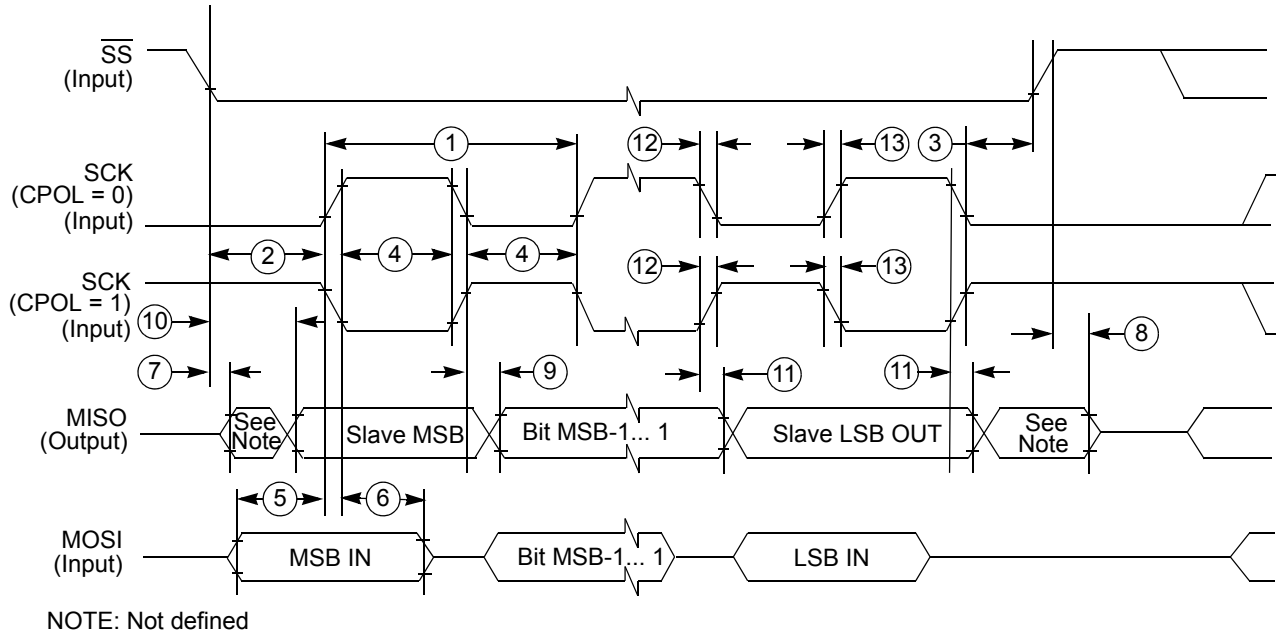
Note:
31. The ESD behavior specified in Section 4.8, “ESD Protection and Latch-up Immunity" is guaranteed without the optional capacitor.

Table 46. SPI Master Mode Timing Characteristics

Characteristic	Symbol	Min	Typ	Max	Unit
SCK Frequency	f_{SCK}	1/2048	—	1/2	f_{BUS}
SCK Period	t_{SCK}	2.0	—	2048	t_{BUS}
Enable Lead Time	t_{LEAD}	—	1/2	—	t_{SCK}
Enable Lag Time	t_{LAG}	—	1/2	—	t_{SCK}
Clock (SCK) High or Low Time	t_{WSCK}	—	1/2	—	t_{SCK}
Data Setup Time (inputs)	t_{SU}	8.0	—	—	ns
Data Hold Time (inputs)	t_{HI}	8.0	—	—	ns
Data Valid After SCK Edge	t_{VSCK}	—	—	29	ns
Data Valid After $\overline{SS}$ Fall (CPHA = 0)	t_{VSS}	—	—	15	ns
Data Hold Time (outputs)	t_{HO}	20	—	—	ns
Rise and Fall Time Inputs	t_{RFI}	—	—	8.0	ns
Rise and Fall Time Outputs	t_{RFO}	—	—	8.0	ns

4.6.2.6.2 Slave Mode

In Figure 14 the timing diagram for slave mode with transmission format CPHA = 0 is depicted.



NOTE: Not defined

Figure 14. SPI Slave Timing (CPHA = 0)

In Figure 15 the timing diagram for slave mode with transmission format CPHA = 1 is depicted.

4.7 Thermal Protection Characteristics

Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 18 V, -40 °C ≤ T_A ≤ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Table 48. Thermal Characteristics - Voltage Regulators VDD (2.5 V) & VDDX (5.0 V)[58]

Ratings	Symbol	Min	Typ	Max	Unit
VDD/VDDX High-temperature Warning (HTI) Threshold Hysteresis	 T_{HTI} T_{HTI_H}	 110 -	 125 10	 140 -	 °C
VDD/VDDX Over-temperature Shutdown Threshold Hysteresis	 T_{SD} T_{SD_H}	 155 -	 170 10	 185 -	 °C
HSUP Over-temperature Shutdown	T_{HSUPSD}	150	165	180	°C
HSUP Over-temperature Shutdown Hysteresis	T_{HSUPSD_HYS}	-	10	-	°C
HS Over-temperature Shutdown	T_{HSSD}	150	165	180	°C
HS Over-temperature Shutdown Hysteresis	T_{HSSD_HYS}	-	10	-	°C
LS Over-temperature Shutdown	T_{LSSD}	150	165	180	°C
LS Over-temperature Shutdown Hysteresis	T_{LSSD_HYS}	-	10	-	°C
LIN Over-temperature Shutdown	T_{LINSD}	150	165	200	°C
LIN Over-temperature Shutdown Hysteresis	T_{LINSD_HYS}	-	20	-	°C

Note:
58. Guaranteed by characterization. Functionality tested.

4.8 ESD Protection and Latch-up Immunity

All ESD testing is in conformity with CDF-AEC-Q100 stress test qualification for automotive grade integrated circuits. During the device qualification, ESD stresses were performed for the Human Body Model (HBM), Machine Model (MM), Charge Device Model (CDM), as well as LIN transceiver specific specifications.

A device will be defined as a failure if after exposure to ESD pulses, the device no longer meets the device specification. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature, followed by hot temperature, unless specified otherwise in the device specification.

Table 49. ESD and Latch-up Protection Characteristics

Ratings	Symbol	Value	Unit
ESD - Human Body Model (HBM) following AEC-Q100 / JESD22-A114 (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω) - LIN (DGND, PGND, AGND, and LGND shorted) - VS1, VS2, VSENSE, Lx - HSx - All other Pins	V_{HBM}	 ±8000 ±4000 ±3000 ±2000	V
ESD - Charged Device Model (CDM) following AEC-Q100, Corner Pins (1, 12, 13, 24, 25, 36, 37, and 48) All other Pins	V_{CDM}	 ±750 ±500	V
ESD - Machine Model (MM) following AEC-Q100 (C_{ZAP} = 200 pF, R_{ZAP} = 0 Ω), All Pins	V_{MM}	±200	V
Latch-up current at T_A = 125 °C[59]	I_{LAT}	±100	mA

Table 74. Analog die Registers[63] - 0x0200–0x02FF D2D Blocking Access (D2DI) 2 of 3/ 0x0300–0x03FF D2D Non Blocking Access (D2DI) 3 of 3

Offset	Name		7	6	5	4	3	2	1	0
0x63	PWMSCLB	R	Bit 7	6	5	4	3	2	1	Bit 0
	PWM Scale B Register	W								
0x64	PWMCNT0	R	Bit 7	6	5	4	3	2	1	Bit 0
	PWM Ch Counter Reg 0	W	0	0	0	0	0	0	0	0
0x65	PWMCNT1	R	Bit 7	6	5	4	3	2	1	Bit 0
	PWM Ch Counter Reg 1	W	0	0	0	0	0	0	0	0
0x66	PWMPER0	R	Bit 7	6	5	4	3	2	1	Bit 0
	PWM Ch Period Register 0	W								
0x67	PWMPER1	R	Bit 7	6	5	4	3	2	1	Bit 0
	PWM Ch Period Register 1	W								
0x68	PWMDTY0	R	Bit 7	6	5	4	3	2	1	Bit 0
	PWM Ch Duty Register 0	W								
0x69	PWMDTY1	R	Bit 7	6	5	4	3	2	1	Bit 0
	PWM Ch Duty Register 1	W								
0x80	ACR	R	SCIE	CCE	OCE	ADCRST	0	PS2	PS1	PS0
	ADC Config Register	W								
0x81	ASR	R	SCF	2p5CLF	0	0	CCNT3	CCNT2	CCNT1	CCNT0
	ADC Status Register	W								
0x82	ACCR (hi)	R	CH15	CH14	0	CH12	CH11	CH10	CH9	CH8
	ADC Conversion Ctrl Reg	W								
0x83	ACCR (lo)	R	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
	ADC Conversion Ctrl Reg	W								
0x84	ACCSR (hi)	R	CC15	CC14	0	CC12	CC11	CC10	CC9	CC8
	ADC Conv Complete Reg	W								
0x85	ACCSR (lo)	R	CC7	CC6	CC5	CC4	CC3	CC2	CC1	CC0
	ADC Conv Complete Reg	W								
0x86	ADR0 (hi)	R	adr0 9	adr0 8	adr0 7	adr0 6	adr0 5	adr0 4	adr0 3	adr0 2
	ADC Data Result Register 0	W								
0x87	ADR0 (lo)	R	adr0 1	adr0 0	0	0	0	0	0	0
	ADC Data Result Register 0	W								
0x88	ADR1 (hi)	R	adr1 9	adr1 8	adr1 7	adr1 6	adr1 5	adr1 4	adr1 3	adr1 2
	ADC Data Result Register 1	W								
0x89	ADR1 (lo)	R	adr1 1	adr1 0	0	0	0	0	0	0
	ADC Data Result Register 1	W								
0x8A	ADR2 (hi)	R	adr2 9	adr2 8	adr2 7	adr2 6	adr2 5	adr2 4	adr2 3	adr2 2
	ADC Data Result Register 2	W								
0x8B	ADR2 (lo)	R	adr2 1	adr2 0	0	0	0	0	0	0
	ADC Data Result Register 2	W								
0x8C	ADR3 (hi)	R	adr3 9	adr3 8	adr3 7	adr3 6	adr3 5	adr3 4	adr3 3	adr3 2
	ADC Data Result Register 3	W								
0x8D	ADR3 (lo)	R	adr3 1	adr3 0	0	0	0	0	0	0
	ADC Data Result Register 3	W								

Table 74. Analog die Registers[63] - 0x0200–0x02FF D2D Blocking Access (D2DI) 2 of 3/ 0x0300–0x03FF D2D Non Blocking Access (D2DI) 3 of 3

Offset	Name		7	6	5	4	3	2	1	0
0xD4	TC3 (hi) TIM InCap/OutComp Reg 3	R W	tc3 15	tc3 14	tc3 13	tc3 12	tc3 11	tc3 10	tc3 9	tc3 8
0xD5	TC3 (lo) TIM InCap/OutComp Reg 3	R W	tc3 7	tc3 6	tc3 5	tc3 4	tc3 3	tc3 2	tc3 1	tc3 0
0xF0	CTR0 Trimming Reg 0	R W	LINTRE	LINTR	WDCTRE	CTR0_4	CTR0_3	WDCTR2	WDCTR1	WDCTR0
0xF1	CTR1 Trimming Reg 1	R W	BGTRE	CTR1_6	BGTRIM UP	BGTRIM DN	IREFTRE	IREFTR2	IREFTR1	IREFTR0
0xF2	CTR2 Trimming Reg 2	R W	CTR2_E	CTR2_1	CTR2_0	SLPBGT RE	SLPBG_L OCK	SLPBGT R2	SLPBGT R1	SLPBGT R0
0xF3	CTR3 Trimming Reg 3	R W	OFFCTR E	OFFCTR 2	OFFCTR 1	OFFCTR 0	CTR3_E	CTR3_2	CTR3_1	CTR3_0
0xF4	SRR Silicon Revision Register	R W	0	0	0	0	FMREV		MMREV	

Note:
63. Registers not shown are reserved and must not be accessed.

5.13 Low Side Drivers - LSx

5.13.1 Introduction / Features

These outputs are two low side drivers intended to drive relays (inductive loads) incorporating the following features:

- PWM capability
- Open load detection
- Current limitation
- Over-temperature shutdown (with maskable interrupt)
- Active clamp
- Independent VREG - High Voltage Shutdown

5.13.1.1 Block Diagram

The following Figure shows the basic structure of the LS drivers.

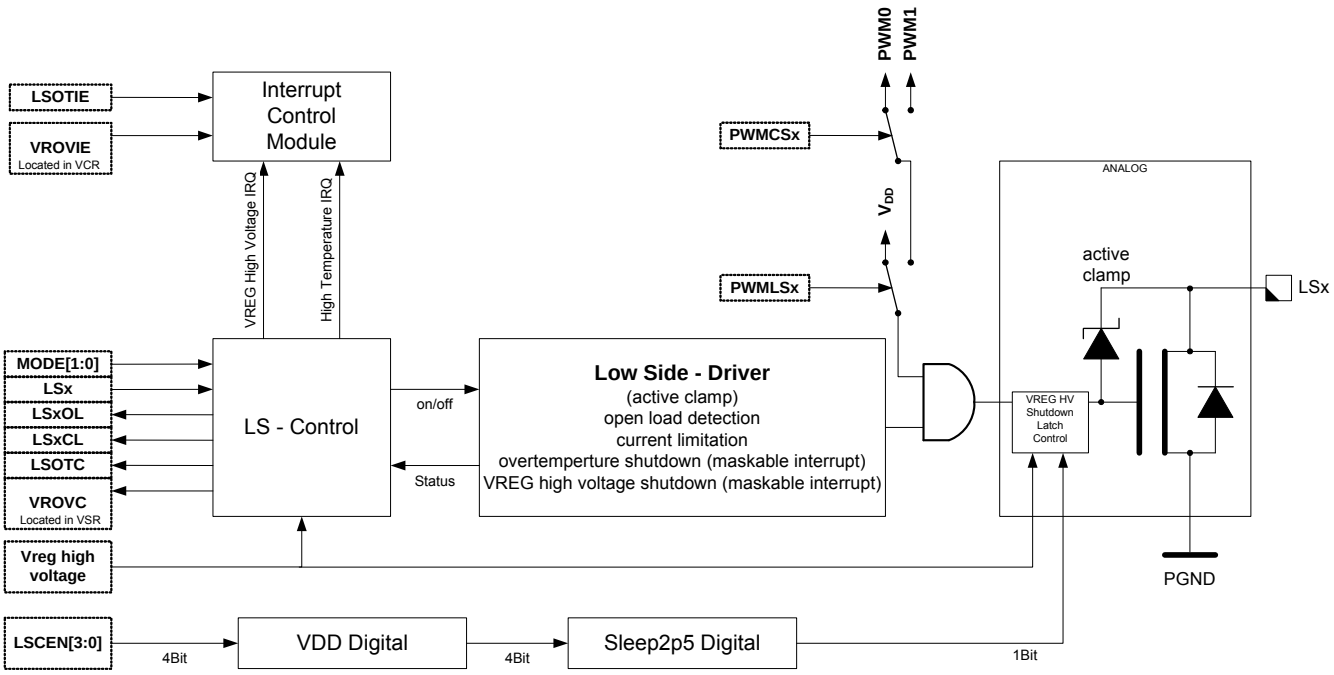


Figure 21. Low Side Drivers - Block Diagram

5.13.1.2 Modes of Operation

The Low Side module is active only in Normal mode; the Low Side drivers are disabled in Sleep and Stop mode.

5.13.2 External Signal Description

This section lists and describes the signals that do connect off-chip.

Table 110 shows all the pins and their functions that are controlled by the Low Side module.

Table 110. Pin Functions and Priorities

Pin Name	Pin Function & Priority	I/O	Description	Pin Function after Reset
LS1	High Voltage Output	O	Low Side Power Output Driver, Active Clamping	LS1
LS2		O		LS2

5.14.2 Signal Description

The PWM module has a total of two internal outputs to control the Low Side Outputs, the High Side Outputs and / or the PTB2 output with pulse width modulation. See Section 5.12, “High Side Drivers - HS", Section 5.13, “Low Side Drivers - LSx" and Section 5.18, “General Purpose I/O - PTB[0…2]" for configuration details.

NOTE

Based on the D2D clock speed, the PWM8B2C module is capable of generating PWM signal frequencies higher than the maximum output frequency of the connected driver (HS, LS). Please refer to Section 4.6, “Dynamic Electrical Characteristics" for details.

Do not exceed the driver maximum output frequency.

5.14.2.1 D2DCLK

Die 2 Die Interface Clock.

5.14.2.2 PWM1 — Pulse Width Modulator Channel 1

This signal serves as waveform output of PWM channel 1.

5.14.2.3 PWM0 — Pulse Width Modulator Channel 0

This signal serves as waveform output of PWM channel 0.

5.14.3 Register Descriptions

This section describes in detail all the registers and register bits in the PWM module. Reserved bits within a register will always read as 0 and the write will be unimplemented. Unimplemented functions are indicated by shading the bit.

Table 118. PWM Register Summary

Name / Offset[89]		7	6	5	4	3	2	1	0
0x60 PWMCTL	R	CAE1	CAE0	PCLK1	PCLK0	PPOL1	PPOL0	PWME1	PWME0
	W								
0x61 PWMPRCLK	R	0	PCKB2	PCKB1	PCKB0	0	PCKA2	PCKA1	PCKA0
	W								
0x62 PWMSCLA	R	Bit 7	6	5	4	3	2	1	Bit 0
	W								
0x63 PWMSCLB	R	Bit 7	6	5	4	3	2	1	Bit 0
	W								
0x64 PWMCNT0	R	Bit 7	6	5	4	3	2	1	Bit 0
	W	0	0	0	0	0	0	0	0
0x65 PWMCNT1	R	Bit 7	6	5	4	3	2	1	Bit 0
	W	0	0	0	0	0	0	0	0
0x66 PWMPER0	R	Bit 7	6	5	4	3	2	1	Bit 0
	W								
0x67 PWMPER1	R	Bit 7	6	5	4	3	2	1	Bit 0
	W								
0x68 PWMDTY0	R	Bit 7	6	5	4	3	2	1	Bit 0
	W								
0x69 PWMDTY1	R	Bit 7	6	5	4	3	2	1	Bit 0
	W								

Note:
89. Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

Table 124. Clock A Prescaler Selects

PCKA2	PCKA1	PCKA0	Value of Clock A
0	0	0	D2D clock
0	0	1	D2D clock / 2
0	1	0	D2D clock / 4
0	1	1	D2D clock / 8
1	0	0	D2D clock / 16
1	0	1	D2D clock / 32
1	1	0	D2D clock / 64
1	1	1	D2D clock / 128

NOTE

PCKB2–0 and PCKA2–0 register bits can be written anytime. If the clock pre-scale is changed while a PWM signal is being generated, a truncated or stretched pulse can occur during the transition.

5.14.3.3 PWM Scale A Register (PWMSCLA)

PWMSCLA is the programmable scale value used in scaling clock A to generate clock SA. Clock SA is generated by taking clock A, dividing it by the value in the PWMSCLA register and dividing that by two.

Clock SA = Clock A / (2 * PWMSCLA)

NOTE

When PWMSCLA = $00, PWMSCLA value is considered a full scale value of 256. Clock A is thus divided by 512.

Any value written to this register will cause the scale counter to load the new scale value (PWMSCLA)

.

Table 125. PWM Scale A Register (PWMSCLA)

Offset[92] 0x62 Access: User read/write

	7	6	5	4	3	2	1	0
R W	Bit 7	6	5	4	3	2	1	Bit 0
Reset	0	0	0	0	0	0	0	0

Note:

92. Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

5.14.3.4 PWM Scale B Register (PWMSCLB)

PWMSCLB is the programmable scale value used in scaling clock B to generate clock SB. Clock SB is generated by taking clock B, dividing it by the value in the PWMSCLB register and dividing that by two.

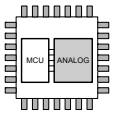
Clock SB = Clock B / (2 * PWMSCLB)

NOTE

When PWMSCLB = $00, PWMSCLB value is considered a full scale value of 256. Clock B is thus divided by 512.

Any value written to this register will cause the scale counter to load the new scale value (PWMSCLB).

5.17 High Voltage Inputs - Lx



Six High Voltage capable inputs are implemented with the following features:

- Digital Input Capable
- Analog Input Capable with selectable voltage divider.
- Wake-up Capable during Low Power mode. See Section 5.9, “Wake-up / Cyclic Sense".

When used as analog inputs to sense voltages outside the module a series resistor must be used on the used input. When a Lx input is not selected in the analog multiplexer, the voltage divider is disconnected from that input. When a Lx input is selected in the analog multiplexer, it will be disconnected in low power mode if configured as Wake-up input. Unused Lx pins are recommended to be connected to GND to improve EMC behavior.

5.17.1 Register Definition

5.17.1.1 Lx Status Register (LXR)

Table 150. Lx Status Register (LXR)

Offset[109] 0x08 — Access: User read

	7	6	5	4	3	2	1	0
R	0	0	L5	L4	L3	L2	L1	L0
W								

Note:
109. Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

Table 151. LXR - Register Field Descriptions

Field	Description
L[5-0]	Lx Status Register - Current Digital State of the Lx Input

5.17.1.2 Lx Control Register (LXCR)

Table 152. Lx Control Register (LXCR)

Offset[110] 0x09 — Access: User read/write

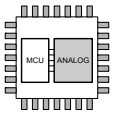
	7	6	5	4	3	2	1	0
R	0	0	L5DS	L4DS	L3DS	L2DS	L1DS	L0DS
W								
Reset	0	0	0	0	0	0	0	0

Note:
110. Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

Table 153. LXCR - Register Field Descriptions

Field	Description
5-0 L[5-0]DS	Analog Input Divider Ratio Selection - Lx 0 - 2 (typ.) 1 - 7.2 (typ)

5.20 Analog Digital Converter - ADC



5.20.1 Introduction

5.20.1.1 Overview

In order to sample the MM912_634 analog die analog sources, a 10-bit resolution successive approximation Analog to Digital Converter has been implemented. Controlled by the A/D Control Logic (ADC Wrapper), the Analog Digital Converter allows fast and high precision conversions.

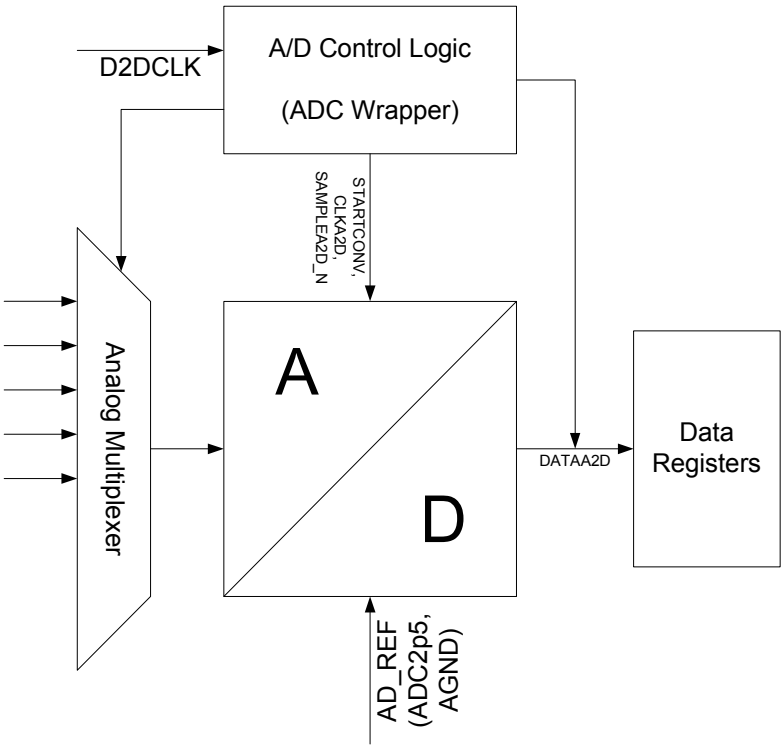


Figure 35. Analog Digital Converter Block Diagram

5.20.1.2 Features

- 10-bit resolution
- 13 µs (typ.), 10-bit Single Sample + Conversion Time
- External ADC2p5 pin with over-current protection to filter the analog reference voltage
- Total Error (TE) of ± 5 LSB without offset calibration active
- Integrated selectable offset compensation
- 14 + 1 analog channels (AD0…8; ISENSE, TSENSE and VSENSE, VS1SENSE, BANDGAP, plus calibration channel)
- Sequence- and Continuous Conversion Mode with IRQ for Sequence Complete indication
- Dedicated Result register for each channel

5.20.2 Modes of Operation

The Analog Digital Converter Module is active only in normal mode; it is disabled in Sleep and Stop mode.

5.20.3 External Signal Description

This section lists and describes the signals that do connect off-chip. Table 197 shows all the pins and their functions that are controlled by the Analog Digital Converter Module.

5.28.2.8 Reduced Drive Register (RDRIV)

Table 239. Reduced Drive Register (RDRIV)

Address 0x000D — Access: User read/write[162]

	7	6	5	4	3	2	1	0
R	0	0	0	0	RDPD	RDPC	0	0
W								
Reset	0	0	0	0	0	0	0	0

Note:
162. Read: Anytime.
Write: Anytime.

Table 240. RDRIV Register Field Descriptions

Field	Description
3 RDPD	**Port D reduced drive—Select reduced drive for output pins.** This bit configures the drive strength of output pins as either full or reduced. If a pin is used as input this bit has no effect. 1 Reduced drive selected (1/5 of the full drive strength) 0 Full drive strength enabled
2 RDPC	**Port C reduced drive—Select reduced drive for D2DCLK output pin.** This bit configures the drive strength of D2DCLK output pin as either full or reduced. 1 Reduced drive selected (1/5 of the full drive strength) 0 Full drive strength enabled

5.28.2.9 Port A Input Register (PTIA)

Table 241. Port A Input Register (PTIA)

Address 0x0120 — Access: User read[163]

	7	6	5	4	3	2	1	0
R	PTIA7	PTIA6	PTIA5	PTIA4	PTIA3	PTIA2	PTIA1	PTIA0
W								
Reset[164]	u	u	u	u	u	u	u	u

Note:
163. Read: Anytime.
Write: Unimplemented. Writing to this register has no effect.
164. u = Unaffected by reset

Table 242. PTIA Register Field Descriptions

Field	Description
7–0 PTIA	**Port A input data**— A read always returns the buffered input state of the associated pin.It can be used to detect overload or short circuit conditions on output pins.

A match can initiate a transition to another state sequencer state (see Section 5.32.4.4, “State Sequence Control"). The comparator control register also allows the type of access to be included in the comparison through the use of the RWE, RW, SZE, and SZ bits. The RWE bit controls whether read or write comparison is enabled for the associated comparator and the RW bit selects either a read or write access for a valid match. Similarly the SZE and SZ bits allow the size of access (word or byte) to be considered in the compare. Only comparators A and B feature SZE and SZ.

The TAG bit in each comparator control register is used to determine the match condition. By setting TAG, the comparator qualifies a match with the output of opcode tracking logic and a state sequencer transition occurs when the tagged instruction reaches the CPU execution stage. Whilst tagging the RW, RWE, SZE, and SZ bits and the comparator data registers are ignored; the comparator address register must be loaded with the exact opcode address.

If the TAG bit is clear (forced type match) a comparator match is generated when the selected address appears on the system address bus. If the selected address is an opcode address, the match is generated when the opcode is fetched from the memory, which precedes the instruction execution by an indefinite number of cycles due to instruction pipelining. For a comparator match of an opcode at an odd address when TAG = 0, the corresponding even address must be contained in the comparator register. Thus for an opcode at odd address (n), the comparator register must contain address (n–1).

Once a successful comparator match has occurred, the condition that caused the original match is not verified again on subsequent matches. Thus if a particular data value is verified at a given address, this address may not still contain that data value when a subsequent match occurs.

Match[0, 1, 2] map directly to Comparators [A, B, C] respectively, except in range modes (see Section 5.32.3.2.4, “Debug Control Register2 (DBGC2)"). Comparator channel priority rules are described in the priority section (Section 5.32.4.3.4, “Channel Priorities").

5.32.4.2.1 Single Address Comparator Match

With range comparisons disabled, the match condition is an exact equivalence of address bus with the value stored in the comparator address registers. Further qualification of the type of access (R/W, word/byte) and data bus contents is possible, depending on comparator channel.

5.32.4.2.1.1 Comparator C

Comparator C offers only address and direction (R/W) comparison. The exact address is compared, thus with the comparator address register loaded with address (n) a word access of address (n–1) also accesses (n) but does not cause a match.

Table 320. Comparator C Access Considerations

Condition For Valid Match	Comp C Address	RWE	RW	Examples
Read and write accesses of ADDR[n]	ADDR[n](189)	0	X	LDAA ADDR[n] STAA #$BYTE ADDR[n]
Write accesses of ADDR[n]	ADDR[n]	1	0	STAA #$BYTE ADDR[n]
Read accesses of ADDR[n]	ADDR[n]	1	1	LDAA #$BYTE ADDR[n]

Note:
189. A word access of ADDR[n-1] also accesses ADDR[n] but does not generate a match. The comparator address register must contain the exact address from the code.

5.32.4.2.1.2 Comparator B

Comparator B offers address, direction (R/W) and access size (word/byte) comparison. If the SZE bit is set the access size (word or byte) is compared with the SZ bit value such that only the specified size of access causes a match. Thus if configured for a byte access of a particular address, a word access covering the same address does not lead to match.

Assuming the access direction is not qualified (RWE=0), for simplicity, the size access considerations are shown in Table 321.

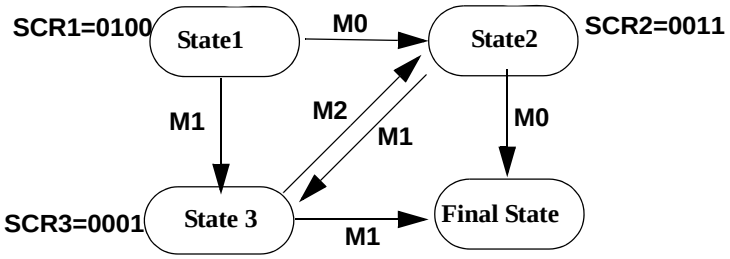


Figure 71. Scenario 4a

This scenario is currently not possible using 2 comparators only. S12SDBGV2 makes it possible with 2 comparators, State 3 allowing a M0 to return to state 2, whilst a M2 leads to final state as shown.

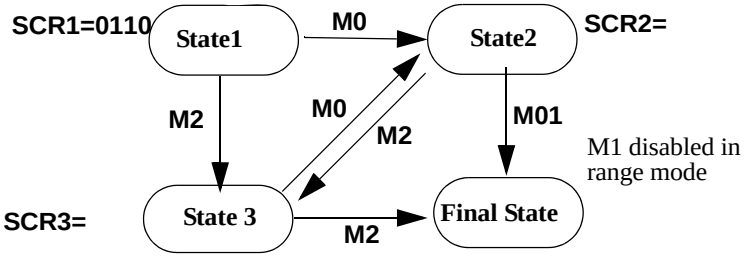


Figure 72. Scenario 4b (with 2 comparators)

The advantage of using only 2 channels is that now range comparisons can be included (channel0)

This however violates the S12SDBGV1 specification, which states that a match leading to final state always has priority in case of a simultaneous match, whilst priority is also given to the lowest channel number. For S12SDBG the corresponding CPU priority decoder is removed to support this, such that on simultaneous taghits, taghits pointing to final state have highest priority. If no taghit points to final state then the lowest channel number has priority. Thus with the above encoding from State3, the CPU and DBG would break on a simultaneous M0/M2.

5.32.5.6 Scenario 5

Trigger if following event A, event C precedes event B. i.e. the expected execution flow is A->B->C.

Figure 73. Scenario 5

Scenario 5 is possible with the S12SDBGV1 SCR encoding

5.32.5.7 Scenario 6

Trigger if event A occurs twice in succession before any of 2 other events (BC) occurs. This scenario is not possible using the S12SDBGV1 SCR encoding. S12SDBGV2 includes additions shown in red. The change in SCR1 encoding also has the advantage that a State1->State3 transition using M0 is now possible. This is advantageous because range and data bus comparisons use channel0 only.

Figure 74. Scenario 6

Table 340. VCO Clock Frequency Selection

VCOCLK Frequency Ranges	VCOFRQ[1:0]
32 MHz <= f_{VCO}<= 48 MHz	00
48 MHz < f_{VCO}<= 6 4MHz	01
Reserved	10
Reserved	11

5.38.3.2.2 S12CPMU Reference Divider Register (CPMUREFDIV)

The CPMUREFDIV register provides a finer granularity for the PLL multiplier steps when using the external oscillator as reference.

Table 341. S12CPMU Reference Divider Register (CPMUREFDIV)

0x0035

	7	6	5	4	3	2	1	0
R	REFFRQ[1:0]		0	0	REFDIV[3:0]			
W								
Reset	0	0	0	0	1	1	1	1

Read: Anytime

Write: Anytime if PROT=0 (CPMUPROT register) and PLLSEL=1 (CPMUCLKS register). Else write has no effect.

NOTE

Write to this register clears the LOCK and UPOSC status bits.

If OSCLCP is enabled (OSCE=1) $$f_{REF} = \frac{f_{OSC}}{(REFDIV + 1)}$$

If OSCLCP is disabled (OSCE=0) $$f_{REF} = f_{IRC1M}$$

The REFFRQ[1:0] bits are used to configure the internal PLL filter for optimal stability and lock time. For correct PLL operation the REFFRQ[1:0] bits have to be selected according to the actual REFCLK frequency as shown in Table 342.

If IRC1M is selected as REFCLK (OSCE=0) the PLL filter is fixed configured for the 1.0 MHz <= f_{REF} <= 2.0 MHz range. The bits can still be written but will have no effect on the PLL filter configuration.

For OSCE=1, setting the REFFRQ[1:0] bits incorrectly can result in a non functional PLL (no locking and/or insufficient stability).

5.38.3.2.5 S12CPMU Interrupt Enable Register (CPMUINT)

This register enables S12CPMU interrupt requests.

Table 346. S12CPMU Interrupt Enable Register (CPMUINT)

0x0038

	7	6	5	4	3	2	1	0
R	RTIE	0	0	LOCKIE	0	0	OSCIE	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Read: Anytime

Write: Anytime

Table 347. CRGINT Field Descriptions

Field	Description
7 RTIE	**Real Time Interrupt Enable Bit** 0 Interrupt requests from RTI are disabled. 1 Interrupt will be requested whenever RTIF is set.
4 LOCKIE	**PLL Lock Interrupt Enable Bit** 0 PLL LOCK interrupt requests are disabled. 1 Interrupt will be requested whenever LOCKIF is set.
1 OSCIE	**Oscillator Corrupt Interrupt Enable Bit** 0 Oscillator Corrupt interrupt requests are disabled. 1 Interrupt will be requested whenever OSCIF is set.

5.38.3.2.6 S12CPMU Clock Select Register (CPMUCLKS)

This register controls S12CPMU clock selection.

Table 348. S12CPMU Clock Select Register (CPMUCLKS)

0x0039

	7	6	5	4	3	2	1	0
R	PLLSEL	PSTP	0	0	PRE	PCE	RTI OSCSEL	COP OSCSEL
W								
Reset	1	0	0	0	0	0	0	0

= Unimplemented or Reserved

Read: Anytime

Write:

1. Only possible if PROT=0 (CPMUPROT register) in all MCU Modes (Normal and Special mode).
2. All bits in Special mode (if PROT=0).
3. PLLSEL, PSTP, PRE, PCE, RTIOSCSEL: In Normal mode (if PROT=0).
4. COPOSCSEL: In Normal mode (if PROT=0) until CPMUCOP write once is taken. If COPOSCSEL was cleared by UPOSC=0 (entering full stop mode with COPOSCSEL=1 or insufficient OSCCLK quality), then COPOSCSEL can be set again once.

NOTE

After writing CPMUCLKS register, it is strongly recommended to read back CPMUCLKS register to make sure that write of PLLSEL, RTIOSCSEL and COPOSCSEL was successful.

5.38.4.3 Stop Mode using PLLCLK as Bus Clock

An example of what happens going into Stop mode and exiting Stop mode after an interrupt is shown in Figure 88. Disable PLL Lock interrupt (LOCKIE=0) before going into Stop mode.

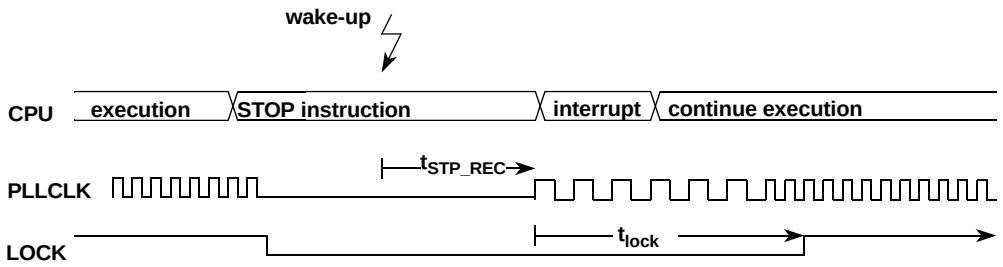


Figure 88. Stop Mode Using PLLCLK as Bus Clock

5.38.4.4 Full Stop Mode using Oscillator Clock as Bus Clock

An example of what happens going into Full Stop mode and exiting Full Stop mode after an interrupt is shown in Figure 89. Disable PLL Lock interrupt (LOCKIE=0) and oscillator status change interrupt (OSCIE=0) before going into Full Stop mode.

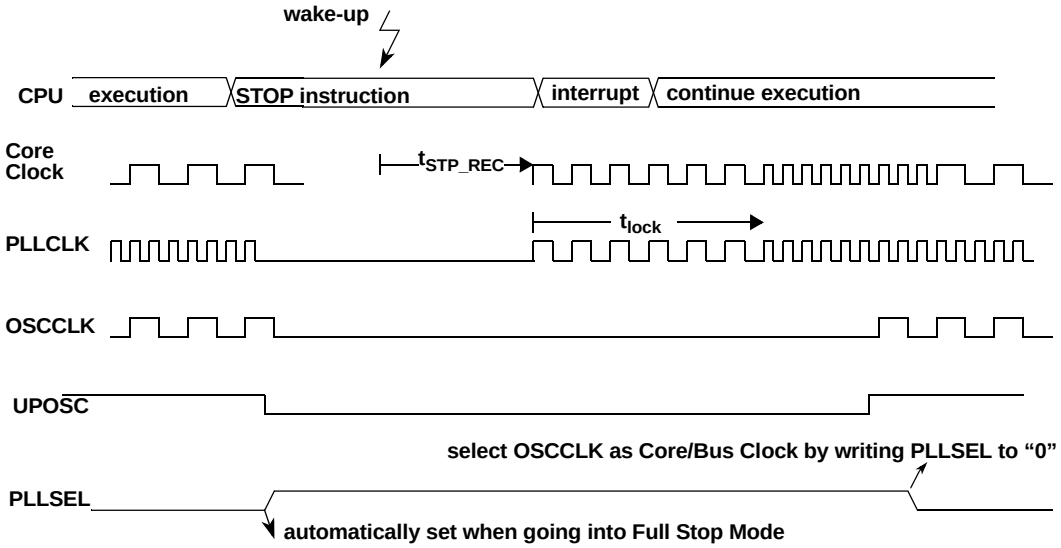


Figure 89. Full Stop Mode Using Oscillator Clock as Bus Clock

5.38.4.5 External Oscillator

5.38.4.5.1 Enabling the External Oscillator

An example of how to use the oscillator as Bus Clock is shown in Figure 90.

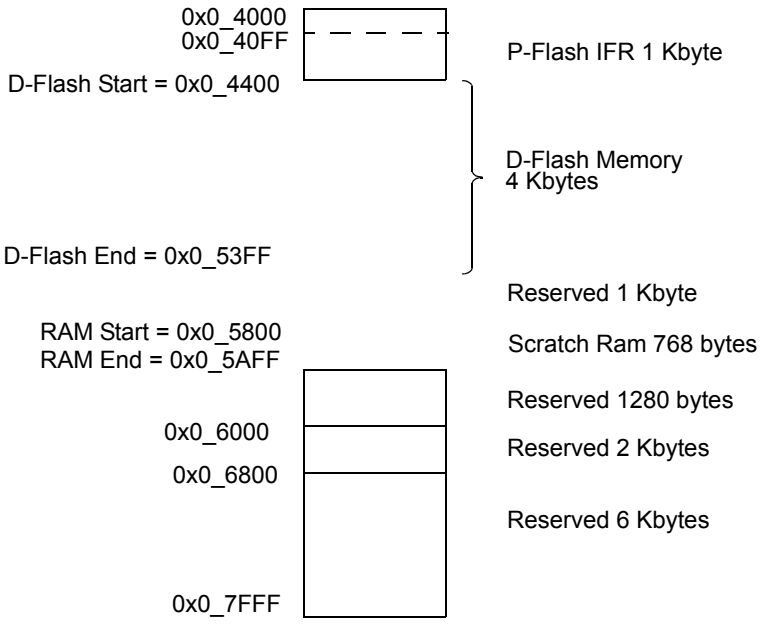


Figure 105. D-Flash and Memory Controller Resource Memory Map

5.40.3.2 Register Descriptions

The Flash module contains a set of 20 control and status registers located between Flash module base + 0x0000 and 0x0013. A summary of the Flash module registers is given in Figure 414 with detailed descriptions in the following subsections.

Writes to any Flash register must be avoided while a Flash command is active (CCIF=0) to prevent corruption of Flash register contents and adversely affect Memory Controller behavior.

The (unreserved) bits of the FPROT register are writable with the restriction that the size of the protected region can only be increased.

During the reset sequence, the FPROT register is loaded with the contents of the P-Flash protection byte in the Flash configuration field at global address 0x3_FF0C located in P-Flash memory (see Table 411) as indicated by reset condition ‘F’ in Table 433. To change the P-Flash protection that will be loaded during the reset sequence, the upper sector of the P-Flash memory must be unprotected, then the P-Flash protection byte must be reprogrammed. If a double bit fault is detected while reading the P-Flash phrase containing the P-Flash protection byte during the reset sequence, the FPOPEN bit will be cleared and remaining bits in the FPROT register will be set to leave the P-Flash memory fully protected.

Trying to alter data in any protected area in the P-Flash memory will result in a protection violation error and the FPVIOL bit will be set in the FSTAT register. The block erase of a P-Flash block is not possible if any of the P-Flash sectors contained in the same P-Flash block are protected.

Table 434. FPROT Field Descriptions

Field	Description
7 FPOPEN	**Flash Protection Operation Enable** — The FPOPEN bit determines the protection function for program or erase operations as shown in Table 10-17 for the P-Flash block. 0 When FPOPEN is clear, the FPHDIS and FPLDIS bits define unprotected address ranges as specified by the corresponding FPHS and FPLS bid 1 When FPOPEN is set, the FPHDIS and FPLDIS bits enable protection for the address range specified by the corresponding FPHS and FPLS bits
6 RNV[6]	**Reserved Nonvolatile Bit** — The RNV bit should remain in the erased state for future enhancements.
5 FPHDIS	**Flash Protection Higher Address Range Disable** — The FPHDIS bit determines whether there is a protected/unprotected area in a specific region of the P-Flash memory ending with global address 0x3_FFFF. 0 Protection/Unprotection enabled 1 Protection/Unprotection disabled
4–3 FPHS[1:0]	**Flash Protection Higher Address Size** — The FPHS bits determine the size of the protected/unprotected area in P-Flash memory as shown inTable 436. The FPHS bits can only be written to while the FPHDIS bit is set.
2 FPLDIS	**Flash Protection Lower Address Range Disable** — The FPLDIS bit determines whether there is a protected/unprotected area in a specific region of the P-Flash memory beginning with global address 0x3_8000. 0 Protection/Unprotection enabled 1 Protection/Unprotection disabled
1-0 FPLS	**Flash Protection Lower Address Size** — The FPLS bits determine the size of the protected/unprotected area in P-Flash memory as shown in Table 437. The FPLS bits can only be written to while the FPLDIS bit is set.

Table 435. P-Flash Protection Function

FPOPEN	FPHDIS	FPLDIS	Function
1	1	1	No P-Flash Protection
1	1	0	Protected Low Range
1	0	1	Protected High Range
1	0	0	Protected High and Low Ranges
0	1	1	Full P-Flash Memory Protected
0	1	0	Unprotected Low Range
0	0	1	Unprotected High Range
0	0	0	Unprotected High and Low Ranges

Note:

221. For range sizes, refer to Table 436 and Table 437.

Table 436. P-Flash Protection Higher Address Range

FPHS[1:0]	Global Address Range	Protected Size
00	0x3_F800–0x3_FFFF	2.0 kByte
01	0x3_F000–0x3_FFFF	4.0 kByte
10	0x3_E000–0x3_FFFF	8.0 kByte
11	0x3_C000–0x3_FFFF	16 kByte

Table 437. P-Flash Protection Lower Address Range

FPLS[1:0]	Global Address Range	Protected Size
00	0x3_8000–0x3_83FF	1.0 kByte
01	0x3_8000–0x3_87FF	2.0 kByte
10	0x3_8000–0x3_8FFF	4.0 kByte
11	0x3_8000–0x3_9FFF	8.0 kByte

All possible P-Flash protection scenarios are shown in Table 106. Although the protection scheme is loaded from the Flash memory at global address 0x3_FF0C during the reset sequence, it can be changed by the user. The P-Flash protection scheme can be used by applications requiring reprogramming in single chip mode while providing as much protection as possible if reprogramming is not required.

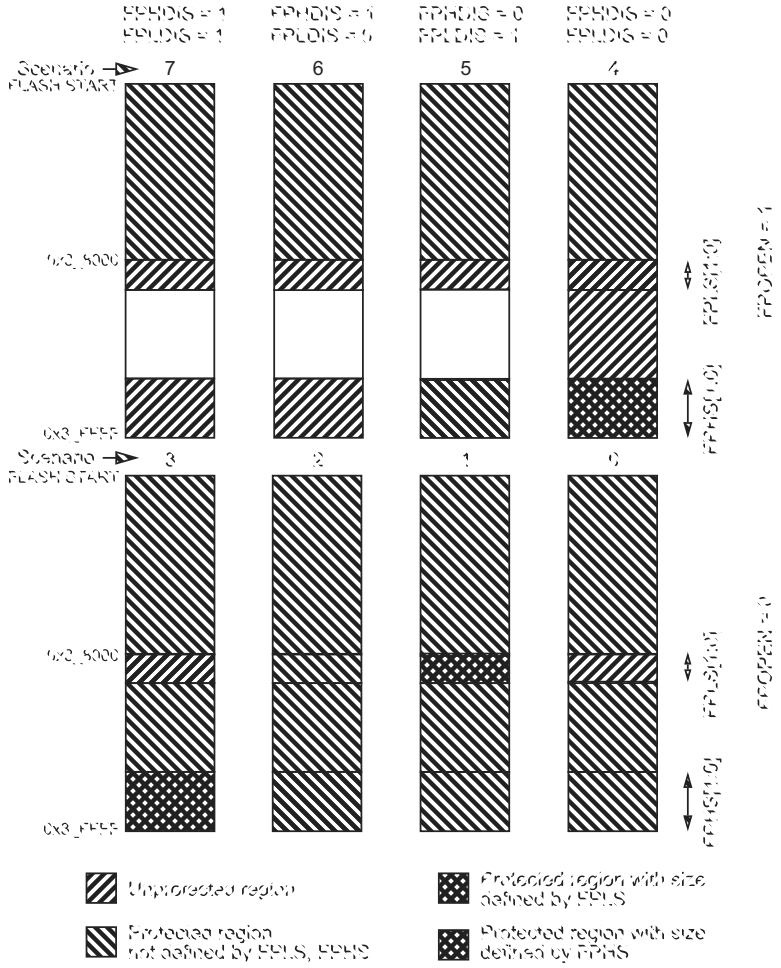


Figure 106. P-Flash Protection Scenarios

5.40.4.5.7 Erase All Blocks Command

The Erase All Blocks operation will erase the entire P-Flash and D-Flash memory space.

Table 472. Erase All Blocks Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x08	Not required

Upon clearing CCIF to launch the Erase All Blocks command, the Memory Controller will erase the entire Flash memory space and verify that it is erased. If the Memory Controller verifies that the entire Flash memory space was properly erased, security will be released. During the execution of this command (CCIF=0) the user must not write to any Flash module register. The CCIF flag will set after the Erase All Blocks operation has completed.

Table 473. Erase All Blocks Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 000 at command launch
		Set if command not available in current mode (see Table 456)
	FPVIOL	Set if any area of the P-Flash or D-Flash memory is protected
	MGSTAT1	Set if any errors have been encountered during the verify operation
	MGSTAT0	Set if any non-correctable errors have been encountered during the verify operation

5.40.4.5.8 Erase Flash Block Command

The Erase Flash Block operation will erase all addresses in a P-Flash or D-Flash block.

Table 474. Erase Flash Block Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x09	Global address [17:16] to identify Flash block
001	Global address [15:0] in Flash block to be erased	

Upon clearing CCIF to launch the Erase Flash Block command, the Memory Controller will erase the selected Flash block and verify that it is erased. The CCIF flag will set after the Erase Flash Block operation has completed.

Table 475. Erase Flash Block Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 001 at command launch
		Set if command not available in current mode (see Table 456)
		Set if an invalid global address [17:16] is supplied
		Set if the supplied P-Flash address is not phrase-aligned or if the D-Flash address is not word-aligned
	FPVIOL	Set if an area of the selected Flash block is protected
	MGSTAT1	Set if any errors have been encountered during the verify operation
	MGSTAT0	Set if any non-correctable errors have been encountered during the verify operation