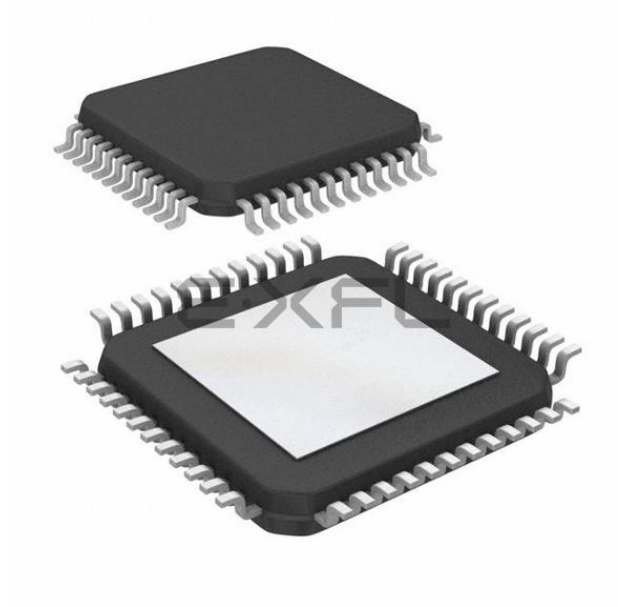

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Application-specific microcontrollers are engineered to

Details	
Product Status	Active
Applications	Automotive
Core Processor	S12
Program Memory Type	FLASH (48kB)
Controller Series	HCS12
RAM Size	2K x 8
Interface	LIN, SCI
Number of I/O	9
Voltage - Supply	2.25V ~ 5.5V
Operating Temperature	-40°C ~ 105°C
Mounting Type	Surface Mount
Package / Case	48-LQFP Exposed Pad
Supplier Device Package	48-HLQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mm912g634dv1aer2

Table 16. Static Electrical Characteristics - Hall Sensor Supply Output - HSUP

Ratings	Symbol	Min	Typ	Max	Unit
Current Limitation	I_{HSUP}	40	70	90	mA
Output Drain-to-Source On resistance T_J = 150 °C, ILOAD = 30 mA; 5.5 V ≤ VSUP ≤ 16 V T_J = 150 °C, ILOAD = 30 mA; 3.7 V ≤ VSUP < 5.5 V	$R_{DS(ON)}$	- -	- -	10 12	Ohm
Output Voltage: (18 V ≤ V_{SUP} ≤ 27 V)	$VHSUP_{MAX}$	16	17.5	18	V
Load Regulation (1.0 mA < I_{HSUP} < 30 mA; V_{SUP} > 18 V)	LD_{HSUP}	-	-	500	mV
Hall Supply Capacitor Range	C_{HSUP}	0.22	-	10	µF
External Capacitor ESR	C_{HSUP_R}	-	-	10	Ohm

Table 17. Static Electrical Characteristics - High Side Drivers - HS

Ratings	Symbol	Min	Typ	Max	Unit
Output Drain-to-Source On resistance T_J = 25 °C, I_{LOAD} = 50 mA; V_{SUP} > 9.0 V T_J = 150 °C, I_{LOAD} = 50 mA; V_{SUP} > 9.0 V T_J = 150 °C, I_{LOAD} = 30 mA; 5.5 V < V_{SUP} < 9.0 V	$R_{DS(ON)}$	- - -	- - -	7.0 10 14	Ohm
Output Current Limitation (0 V < V_{OUT} < V_{SUP} - 2.0 V)	I_{LIMHSX}	60	110	250	mA
Open Load Current Detection	I_{OLHSX}	-	5.0	7.5	mA
Leakage Current (-0.2 V < V_{HSx} < V_{S2} + 0.2 V)	I_{LEAK}	-	-	10	µA
Current Limitation Flag Threshold (5.5 V < V_{SUP} < 27 V)	V_{THSC}	V_{SUP} -2	-	-	V

Table 18. Static Electrical Characteristics - Low Side Drivers - LS

Ratings	Symbol	Min	Typ	Max	Unit
Output Drain-to-Source On resistance T_J = 25 °C, I_{LOAD} = 150 mA, V_{SUP} > 9.0 V T_J = 150 °C, I_{LOAD} = 150 mA, V_{SUP} > 9.0 V T_J = 150 °C, I_{LOAD} = 120 mA, 5.5 V < V_{SUP} < 9.0 V	$R_{DS(ON)}$	– – –	– – –	2.5 4.5 10	Ohm
Output Current Limitation (2.0 V < V_{OUT} < V_{SUP})	I_{LIMLSX}	180	275	380	mA
Open Load Current Detection	I_{OLLSX}	-	8.0	12	mA
Leakage Current (-0.2 V < V_{OUT} < VS1)	I_{LEAK}	-	-	10	µA
Active Output Energy Clamp (I_{OUT} = 150 mA)	V_{CLAMP}	40	-	45	V
Coil Series Resistance (I_{OUT} = 150 mA)	R_{COIL}	120	-		Ohm
Coil Inductance (I_{OUT} = 150 mA)	R_{COIL}	-	-	400	mH
Current Limitation Flag Threshold (5.5 V < V_{SUP} < 27 V)	V_{THSC}	2.0	-	-	V

Table 19. Static Electrical Characteristics - LIN Physical Layer Interface - LIN

Ratings	Symbol	Min	Typ	Max	Unit
Current Limitation for Driver dominant state. V_{BUS} = 18 V	I_{BUSLIM}	40	120	200	mA
Input Leakage Current at the Receiver incl. Pull-up Resistor RSLAVE; Driver OFF; V_{BUS} = 0 V; V_{BAT} = 12 V	$I_{BUS\_PAS\_DOM}$	-1.0	-	-	mA
Input Leakage Current at the Receiver incl. Pull-up Resistor RSLAVE; Driver OFF; 8.0 V < V_{BAT} < 18 V; 8.0 V < V_{BUS} < 18 V; V_{BUS} ≥ V_{BAT}	$I_{BUS\_PAS\_REC}$	-	-	20	µA

Table 74. Analog die Registers[63] - 0x0200–0x02FF D2D Blocking Access (D2DI) 2 of 3/ 0x0300–0x03FF D2D Non Blocking Access (D2DI) 3 of 3

Offset	Name		7	6	5	4	3	2	1	0
0x8E	ADR4 (hi)	R	adr4 9	adr4 8	adr4 7	adr4 6	adr4 5	adr4 4	adr4 3	adr4 2
	ADC Data Result Register 4	W								
0x8F	ADR4 (lo)	R	adr4 1	adr4 0	0	0	0	0	0	0
	ADC Data Result Register 4	W								
0x90	ADR5 (hi)	R	adr5 9	adr5 8	adr5 7	adr5 6	adr5 5	adr5 4	adr5 3	adr5 2
	ADC Data Result Register 5	W								
0x91	ADR5 (lo)	R	adr5 1	adr5 0	0	0	0	0	0	0
	ADC Data Result Register 5	W								
0x92	ADR6 (hi)	R	adr6 9	adr6 8	adr6 7	adr6 6	adr6 5	adr6 4	adr6 3	adr6 2
	ADC Data Result Register 6	W								
0x93	ADR6 (lo)	R	adr6 1	adr6 0	0	0	0	0	0	0
	ADC Data Result Register 6	W								
0x94	ADR7 (hi)	R	adr7 9	adr7 8	adr7 7	adr7 6	adr7 5	adr7 4	adr7 3	adr7 2
	ADC Data Result Register 7	W								
0x95	ADR7 (lo)	R	adr7 1	adr7 0	0	0	0	0	0	0
	ADC Data Result Register 7	W								
0x96	ADR8 (hi)	R	adr8 9	adr8 8	adr8 7	adr8 6	adr8 5	adr8 4	adr8 3	adr8 2
	ADC Data Result Register 8	W								
0x97	ADR8 (lo)	R	adr8 1	adr8 0	0	0	0	0	0	0
	ADC Data Result Register 8	W								
0x98	ADR9 (hi)	R	adr9 9	adr9 8	adr9 7	adr9 6	adr9 5	adr9 4	adr9 3	adr9 2
	ADC Data Result Register 9	W								
0x99	ADR9 (lo)	R	adr9 1	adr9 0	0	0	0	0	0	0
	ADC Data Result Register 9	W								
0x9A	ADR10 (hi)	R	adr10 9	adr10 8	adr10 7	adr10 6	adr10 5	adr10 4	adr10 3	adr10 2
	ADC Data Result Reg 10	W								
0x9B	ADR10 (lo)	R	adr10 1	adr10 0	0	0	0	0	0	0
	ADC Data Result Reg 10	W								
0x9C	ADR11 (hi)	R	adr11 9	adr11 8	adr11 7	adr11 6	adr11 5	adr11 4	adr11 3	adr11 2
	ADC Data Result Reg 11	W								
0x9D	ADR11 (lo)	R	adr11 1	adr11 0	0	0	0	0	0	0
	ADC Data Result Reg 11	W								
0x9E	ADR12 (hi)	R	adr12 9	adr12 8	adr12 7	adr12 6	adr12 5	adr12 4	adr12 3	adr12 2
	ADC Data Result Reg 12	W								
0x9F	ADR12 (lo)	R	adr12 1	adr12 0	0	0	0	0	0	0
	ADC Data Result Reg 12	W								
0xA2	ADR14 (hi)	R	adr14 9	adr14 8	adr14 7	adr14 6	adr14 5	adr14 4	adr14 3	adr14 2
	ADC Data Result Reg 14	W								
0xA3	ADR14 (lo)	R	adr14 1	adr14 0	0	0	0	0	0	0
	ADC Data Result Reg 14	W								
0xA4	ADR15 (hi)	R	adr15 9	adr15 8	adr15 7	adr15 6	adr15 5	adr15 4	adr15 3	adr15 2
	ADC Data Result Reg 15	W								

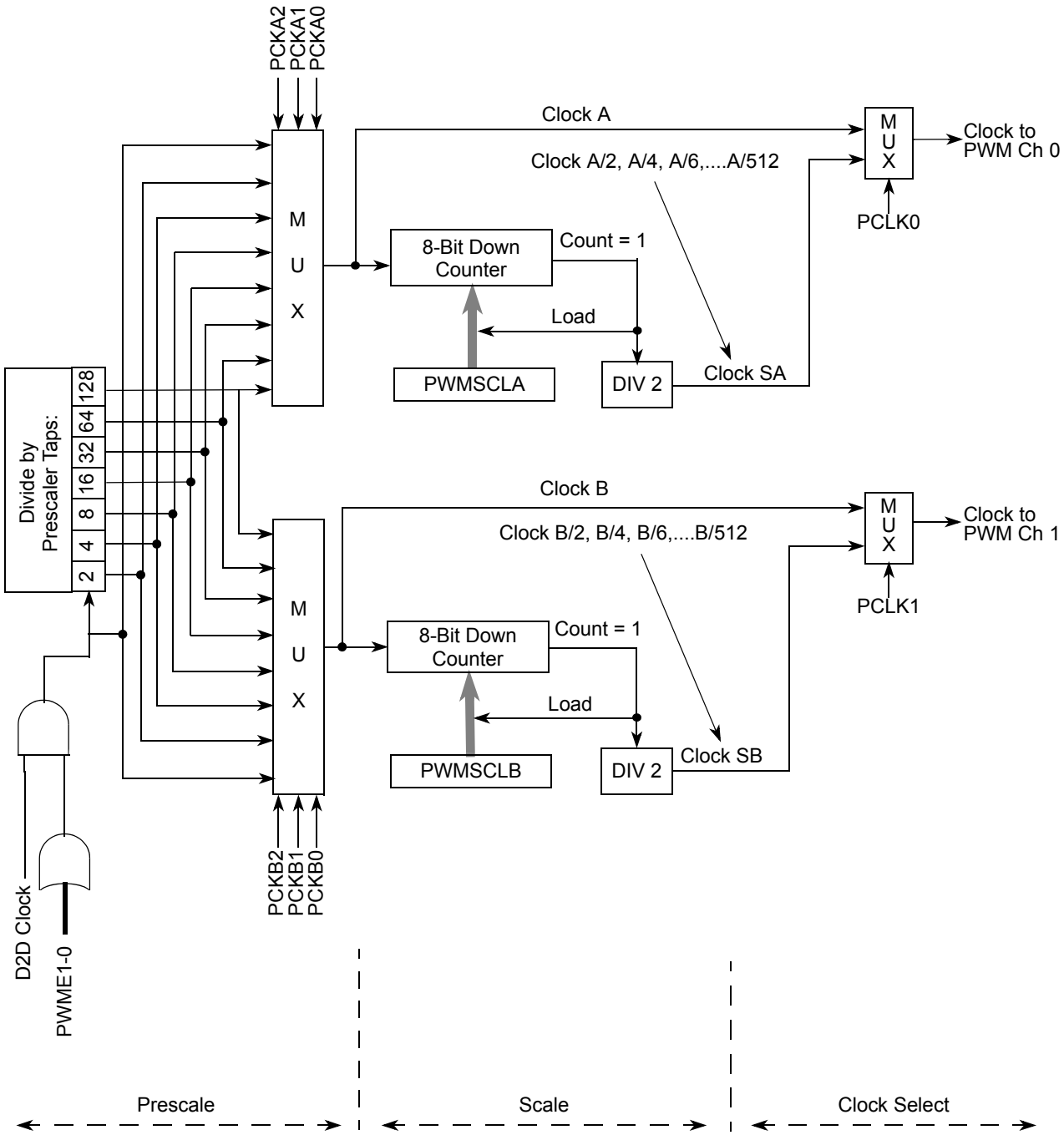


Figure 23. PWM Clock Select Block Diagram

Clock A is used as an input to an 8-bit down counter. This down counter loads a user programmable scale value from the scale register (PWMSCLA). When the down counter reaches one, a pulse is output and the 8-bit counter is re-loaded. The output signal from this circuit is further divided by two. This gives a greater range with only a slight reduction in granularity. Clock SA equals clock A divided by two times the value in the PWMSCLA register.

NOTE

Changing the PWM output mode from left aligned to center aligned output (or vice versa) while channels are operating can cause irregularities in the PWM output. It is recommended to program the output mode before enabling the PWM channel.

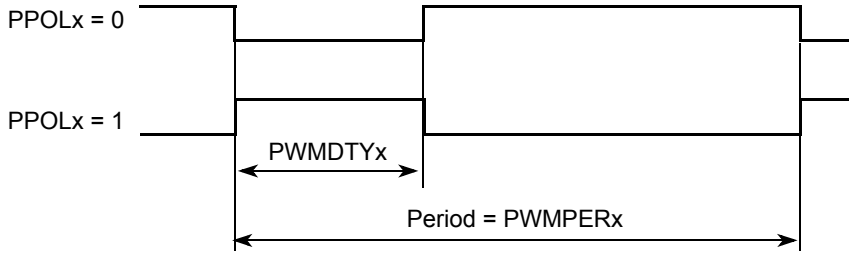


Figure 25. PWM Left Aligned Output Waveform

To calculate the output frequency in left aligned output mode for a particular channel, take the selected clock source frequency for the channel (A, B, SA, or SB), and divide it by the value in the period register for that channel.

- PWMx Frequency = Clock (A, B, SA, or SB) / PWMPERx
- PWMx Duty Cycle (high time as a % of period):
  - Polarity = 0 (PPOLx = 0)
- Duty Cycle = [(PWMPERx-PWMDTYx)/PWMPERx] * 100%
  - Polarity = 1 (PPOLx = 1)

  Duty Cycle = [PWMDTYx / PWMPERx] * 100%

As an example of a left aligned output, consider the following case:

Clock Source = E, where E = 10 kHz (100 µs period)

PPOLx = 0

PWMPERx = 4

PWMDTYx = 1

PWMx Frequency = 10 kHz/4 = 2.5 kHz

PWMx Period = 400 µs

PWMx Duty Cycle = 3/4 *100% = 75%

The output waveform generated is shown in Figure 26.

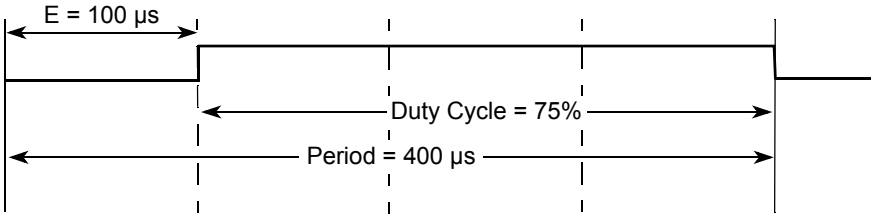


Figure 26. PWM Left Aligned Output Example Waveform

5.14.4.2.6 Center Aligned Outputs

For a center aligned output mode selection, set the CAEx bit (CAEx = 1) in the PWMCTL register, and the corresponding PWM output will be center aligned.

The 8-bit counter operates as an up/down counter in this mode, and is set to up whenever the counter is equal to $00. The counter compares to two registers, a duty register and a period register, as shown in the block diagram in Figure 24. When the PWM counter matches the duty register, the output flip-flop changes state, causing the PWM waveform to also change state. A match between the PWM counter and the period register changes the counter direction from an up-count to a down-count. When the PWM counter decrements and matches the duty register again, the output flip-flop changes state, causing the PWM output to also change state. When the PWM counter decrements and reaches zero, the counter direction changes from a down-count back to an up-count, and a load from the double buffer period and duty registers to the associated registers is performed, as described

5.18 General Purpose I/O - PTB[0…2]

The three multipurpose I/O pins can be configured to operate as documented in the table below.

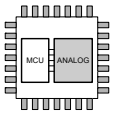


Table 154. General purpose I/O - Operating modes

Priority	Function	PTB2	PTB1	PTB0	Chp/Pg
1 (H)	2.5 V Analog Input	AD2	AD1	AD0	5.20/135
2	Timer Input Capture / Output Compare	TIMCH2	TIMCH1	TIMCH0	5.19/122
3	LIN / SCI - Rx / Tx (PTB0…1) or PWM (PTB2)	PWM	Tx	Rx	5.15/102
4 (L)	5.0 V Input Output	PTB2	PTB1	PTB0	current

The alternate function of PTB2, PTB1 and PTB0 can be configured by selecting the function in the corresponding module (e.g. TIMER). The selection with the highest priority will take effect when more than one function is selected.

5.18.1 Digital I/O Functionality

All three pins act as standard digital Inputs / Outputs with selectable pull-up resistor.

5.18.2 Alternative SCI / LIN Functionality

For alternative serial configuration and for debug and certification purpose, PTB0 and PTB1 can be configured to connect to the internal LIN and / or SCI signals (RxD and TxD). Figure 32 shows the 4 available configurations.

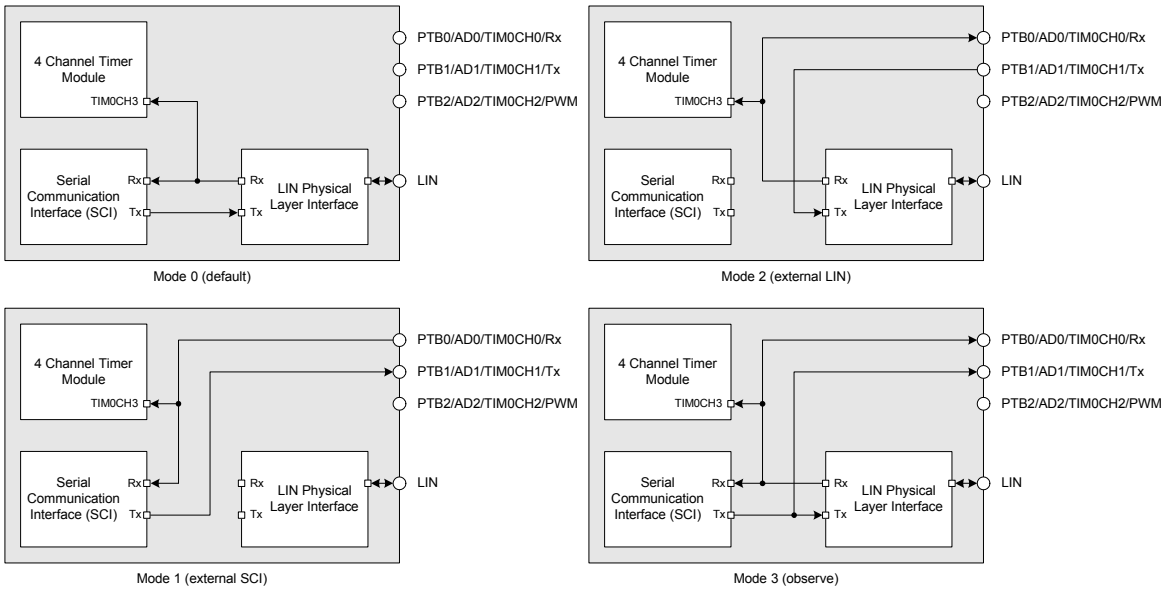


Figure 32. Alternative SCI / LIN Functionality

5.18.3 Alternative PWM Functionality

As an alternative routing for the PWM channel (0 or 1) output, the PortB 2 (PTB2) can be configured to output one of the two PWM channels defined in the Section 5.14, “PWM Control Module (PWM8B2C)". The selection and output enable can be configured in the Port B Configuration Register 2 (PTBC2).

5.18.4 Register definition

5.18.4.1 Port B Configuration Register 1 (PTBC1)

Table 155. Port B Configuration Register 1 (PTBC1)

Offset(111) 0x20 — Access: User read/write

	7	6	5	4	3	2	1	0
R	0	PUEB2	PUEB1	PUEB0	0	DDRB2	DDRB1	DDRB0
W								
Reset	0	0	0	0	0	0	0	0

Note:
111. Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

Table 156. PTBC1 - Register Field Descriptions

Field	Description
6-4 PUEB[2-0]	Pull-up Enable Port B[2…0] 0 - Pull-up disabled on PTBx pin. 1- Pull-up enabled on PTBx pin.
2-0 DDRB[2-0]	Data Direction Port B[2…0] 0 - PTBx configured as input. 1 - PTBx configured as output.

NOTE

The pull-up resistor is not active once the port is configured as an output.

5.18.4.2 Port B Configuration Register 2 (PTBC2)

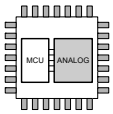
Table 157. Port B Configuration Register 2 (PTBC2)

Offset(112) 0x21 — Access: User read/write

	7	6	5	4	3	2	1	0
R	0	0	0	0	PWMCS	PWMEN	SERMOD	
W								
Reset	0	0	0	0	0	0	0	0

Note:
112. Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

5.20 Analog Digital Converter - ADC



5.20.1 Introduction

5.20.1.1 Overview

In order to sample the MM912_634 analog die analog sources, a 10-bit resolution successive approximation Analog to Digital Converter has been implemented. Controlled by the A/D Control Logic (ADC Wrapper), the Analog Digital Converter allows fast and high precision conversions.

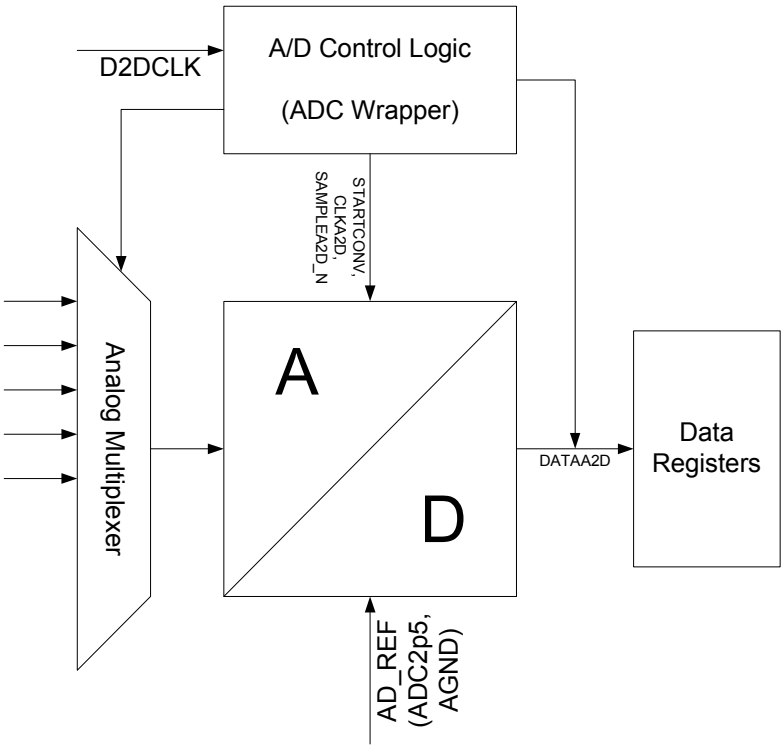


Figure 35. Analog Digital Converter Block Diagram

5.20.1.2 Features

- 10-bit resolution
- 13 µs (typ.), 10-bit Single Sample + Conversion Time
- External ADC2p5 pin with over-current protection to filter the analog reference voltage
- Total Error (TE) of ± 5 LSB without offset calibration active
- Integrated selectable offset compensation
- 14 + 1 analog channels (AD0…8; ISENSE, TSENSE and VSENSE, VS1SENSE, BANDGAP, plus calibration channel)
- Sequence- and Continuous Conversion Mode with IRQ for Sequence Complete indication
- Dedicated Result register for each channel

5.20.2 Modes of Operation

The Analog Digital Converter Module is active only in normal mode; it is disabled in Sleep and Stop mode.

5.20.3 External Signal Description

This section lists and describes the signals that do connect off-chip. Table 197 shows all the pins and their functions that are controlled by the Analog Digital Converter Module.

5.27.4 Part ID Assignments

The part ID is located in two 8-bit registers PARTIDH and PARTIDL (addresses 0x001A and 0x001B). The read-only value is a unique part ID for each revision of the chip. Table 222 shows the assigned part ID number and Mask Set number.

The Version ID in Table 222 is a word located in a flash information row. The version ID number indicates a specific version of internal NVM controller.

Table 222. Assigned Part ID Numbers

Device	Mask Set Number	Part ID[154]	Version ID
MC9S12I64	0N53A	0x38C0	0x0000

Note:

154. The coding is as follows:
Bit 15-12: Major family identifier
Bit 11-6: Minor family identifier
Bit 5-4: Major mask set revision number including FAB transfers
Bit 3-0: Minor — non full — mask set revision

5.27.5 System Clock Description

For the system clock description please refer to 5.38, “S12 Clock, Reset and Power Management Unit (S12CPMU)”.

5.27.6 Modes of Operation

The MCU can operate in different modes. These are described in Section 5.27.6.1, “Chip Configuration Summary". The MCU can operate in different power modes to facilitate power saving when full system performance is not required. These are described in Section 5.27.6.2, “Low Power Operation". Some modules feature a software programmable option to freeze the module status whilst the background debug module is active to facilitate debugging.

5.27.6.1 Chip Configuration Summary

The different modes and the security state of the MCU affect the debug features (enabled or disabled).

The operating mode out of reset is determined by the state of the MODC signal during reset (see Table 223). The MODC bit in the MODE register shows the current operating mode and provides limited mode switching during operation. The state of the MODC signal is latched into this bit on the rising edge of $\overline{\text{RESET}}$.

Table 223. Chip Modes

Chip Modes	MODC
Normal single chip	1
Special single chip	0

5.27.6.1.1 Normal Single-Chip Mode

This mode is intended for normal device operation. The opcode from the on-chip memory is being executed after reset (requires the reset vector to be programmed correctly). The processor program is executed from internal memory.

5.27.6.1.2 Special Single-Chip Mode

This mode is used for debugging single-chip operation, boot-strapping, or security related operations. The background debug module BDM is active in this mode. The CPU executes a monitor program located in an on-chip ROM. BDM firmware waits for additional serial commands through the BKGD pin.

5.27.6.2 Low Power Operation

The MM912_634 has two static low-power modes Pseudo Stop and Stop Mode. For a detailed description refer to S12CPMU section.

5.27.7 Security

The MCU security mechanism prevents unauthorized access to the Flash memory. Refer to 5.33, “Security (S12X9SECV2)”, Section 5.31.4.1, “Security"", and Section 5.40.5, “Security".

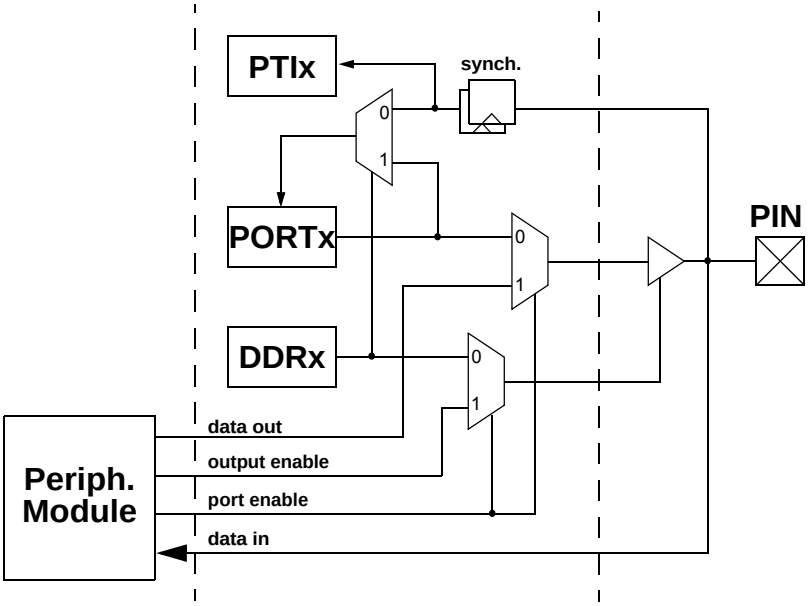


Figure 43. Illustration of I/O Pin Functionality

5.28.3.1.4 Reduced Drive Register (RDRIV)

If the pin is used as an output this register allows the configuration of the drive strength.

5.28.3.1.5 Pull Device Enable Register (PUCR)

This register turns on a pull-up or pull-down device. It becomes active only if the pin is used as an input.

5.28.3.2 Ports

5.28.3.2.1 Port A

This port is associated with the SPI. Port A pins PA7-0 can be used for general-purpose I/O and PA3-0 also with the SPI subsystem.

5.28.3.2.2 Port C

This port is associated with the D2DI interface. Port C pins PC1-0 can be used as the D2DI interrupt input and D2DI clock output, respectively. A pull-down device is enabled on pin PC1 if used as D2DI input.A reduced drive strength can be selected on PC0 if used as D2DI output. The D2DI interrupt input is synchronized and has an asynchronous bypass in STOP mode to allow the generation of a wake-up interrupt.

5.28.3.2.3 Port D

This port is associated with the D2DI interface. Port D pins PD7-0 can be used with the D2DI data I/O. Pull-down devices are enabled on all pins if used as D2DI inputs.A reduced drive strength can be selected on all pins if used as D2DI outputs.

5.28.3.2.4 Port E

This port is associated with the CPMU OSC. Port E pins PE1-0 can be used for general-purpose or with the CPMU OSC module.

5.28.4 Initialization Information

5.28.4.1 Port Data and Data Direction Register writes

It is not recommended to write PTx and DDRx in a word access. When changing the register pins from inputs to outputs, the data may have extra transitions during the write access. Initialize the port data register before enabling the outputs.

5.29 Memory Map Control (S12PMMCV1)

5.29.1 Introduction

The S12PMMC module controls the access to all internal memories and peripherals for the CPU12 and S12SBDM module. It regulates access priorities and determines the address mapping of the on-chip resources. Figure 44 shows a block diagram of the S12PMMC module.

5.29.1.1 Glossary

Table 246. Glossary Of Terms

Term	Definition
Local Addresses	Address within the CPU12's Local Address Map (Figure 49)
Global Address	Address within the Global Address Map (Figure 49)
Aligned Bus Access	Bus access to an even address.
Misaligned Bus Access	Bus access to an odd address.
NS	Normal Single-chip Mode
SS	Special Single-chip Mode
Unimplemented Address Ranges	Address ranges which are not mapped to any on-chip resource.
P-Flash	Program Flash
D-Plash	Data Flash
NVM	Non-volatile Memory; P-Flash or D-Flash
IFR	NVM Information Row. Refer to FTMRC Block Guide

5.29.1.2 Overview

The S12PMMC connects the CPU12's and the S12SBDM's bus interfaces to the MCU's on-chip resources (memories and peripherals). It arbitrates the bus accesses and determines all of the MCU's memory maps. Furthermore, the S12PMMC is responsible for constraining memory accesses on secured devices and for selecting the MCU's functional mode.

5.29.1.3 Features

The main features of this block are:

- Paging capability to support a global 256 kByte memory address space
- Bus arbitration between the masters CPU12, S12SBDM to different resources.
- MCU operation mode control
- MCU security control
- Separate memory map schemes for each master CPU12, S12SBDM
- Generation of system reset when CPU12 accesses an unimplemented address (i.e., an address which does not belong to any of the on-chip modules) in single-chip modes

5.29.1.4 Modes of Operation

The S12PMMC selects the MCU's functional mode. It also determines the devices behavior in secured and unsecured state.

5.29.1.4.1 Functional Modes

Two functional modes are implements on devices of the S12I product family:

- Normal Single Chip (NS)
  The mode used for running applications.
- Special Single Chip Mode (SS)
  A debug mode which causes the device to enter BDM Active Mode after each reset. Peripherals may also provide special debug features in this mode.

Example 1. This example demonstrates usage of the Direct Addressing Mode

```
MOVB    #$80,DIRECT     ;Set DIRECT register to 0x80. Write once only.
                        ;Global data accesses to the range 0xXX_80XX can be direct.
                        ;Logical data accesses to the range 0x80XX are direct.

LDY     <$00            ;Load the Y index register from 0x8000 (direct access).
                        ;< operator forces direct access on some assemblers but in
                        ;many cases assemblers are “direct page aware” and can
                        ;automatically select direct mode.
```

5.29.3.2.3 Program Page Index Register (PPAGE)

Table 253. Program Page Index Register (PPAGE)

Address: 0x0015

	7	6	5	4	3	2	1	0
R	0	0	0	0	PIX3	PIX2	PIX1	PIX0
W								
Reset	0	0	0	0	1	1	1	0

Read: Anytime

Write: Anytime

These four index bits are used to map 16 kB blocks into the Flash page window located in the local (CPU or BDM) memory map from address 0x8000 to address 0xBFFF (see Figure 47). This supports accessing up to 256 kB of Flash (in the Global map) within the 6 kB Local map. The PPAGE index register is effectively used to construct paged Flash addresses in the Local map format. The CPU has special access to read and write this register directly during execution of CALL and RTC instructions.

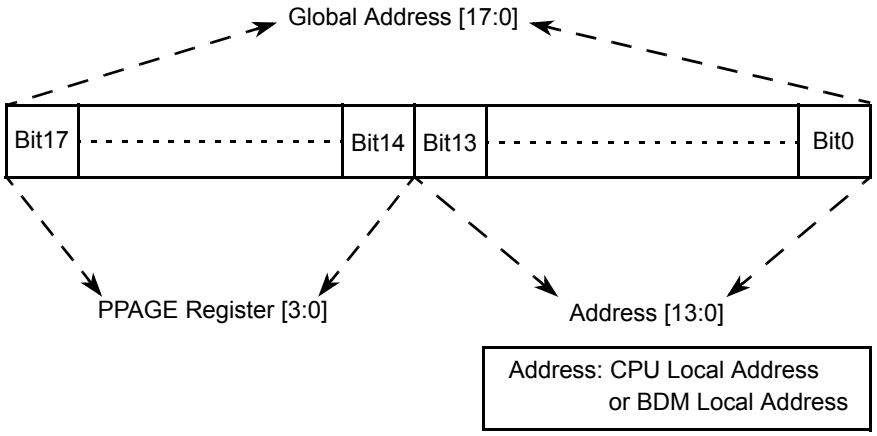


Figure 47. PAGE Address Mapping

NOTE

Writes to this register using the special access of the CALL and RTC instructions will be complete before the end of the instruction execution.

5.30.1.4 Block Diagram

Figure 52 shows a block diagram of the INT module.

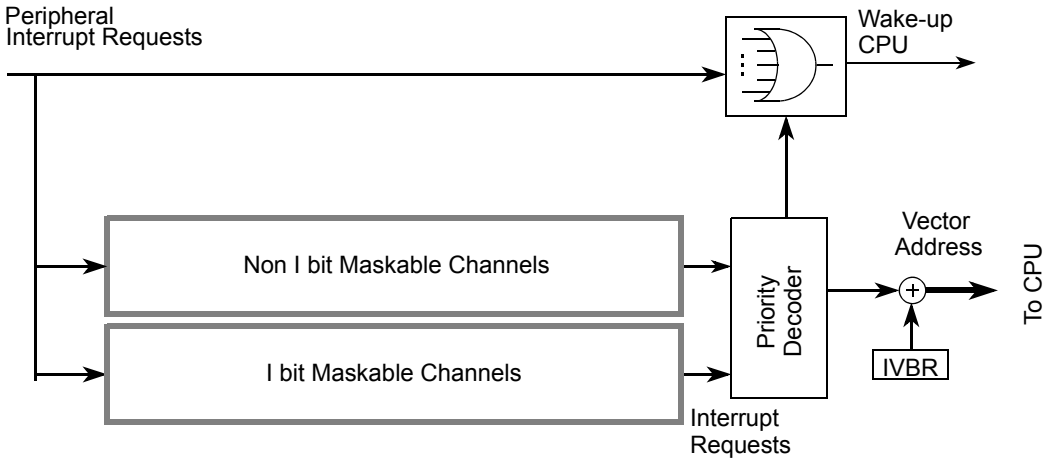


Figure 52. INT Block Diagram

5.30.2 External Signal Description

The INT module has no external signals.

5.30.3 Memory Map and Register Definition

This section provides a detailed description of all registers accessible in the INT module.

5.30.3.1 Register Descriptions

This section describes in address order all the INT registers and their individual bits.

5.30.3.1.1 Interrupt Vector Base Register (IVBR)

Table 257. Interrupt Vector Base Register (IVBR)

Address: 0x001F

	7	6	5	4	3	2	1	0
R W	IVB_ADDR[7:0]							
Reset	1	1	1	1	1	1	1	1

Read: Anytime

Write: Anytime

Table 258. IVBR Field Descriptions

Field	Description
7–0 IVB_ADDR[7:0]	Interrupt Vector Base Address Bits — These bits represent the upper byte of all vector addresses. Out of reset these bits are set to 0xFF (i.e., vectors are located at 0xFF80–0xFFFE) to ensure compatibility to HCS12. Note: A system reset will initialize the interrupt vector base register with “0xFF” before it is used to determine the reset vector address. Therefore, changing the IVBR has no effect on the location of the three reset vectors (0xFFFA–0xFFFE). Note: If the BDM is active (i.e., the CPU is in the process of executing BDM firmware code), the contents of IVBR are ignored and the upper byte of the vector address is fixed as “0xFF”. This is done to enable handling of all non-maskable interrupts in the BDM firmware.

5.31.1.2.3 Low-power Modes

The BDM can be used until stop mode is entered. The CPU cannot enter stop mode during BDM active mode.

In stop mode the BDM clocks are stopped. When BDM clocks are disabled and stop mode is exited, the BDM clocks will restart and BDM will have a soft reset (clearing the instruction register, any command in progress and disable the ACK function). The BDM is now ready to receive a new command.

5.31.1.3 Block Diagram

A block diagram of the BDM is shown in Figure 53.

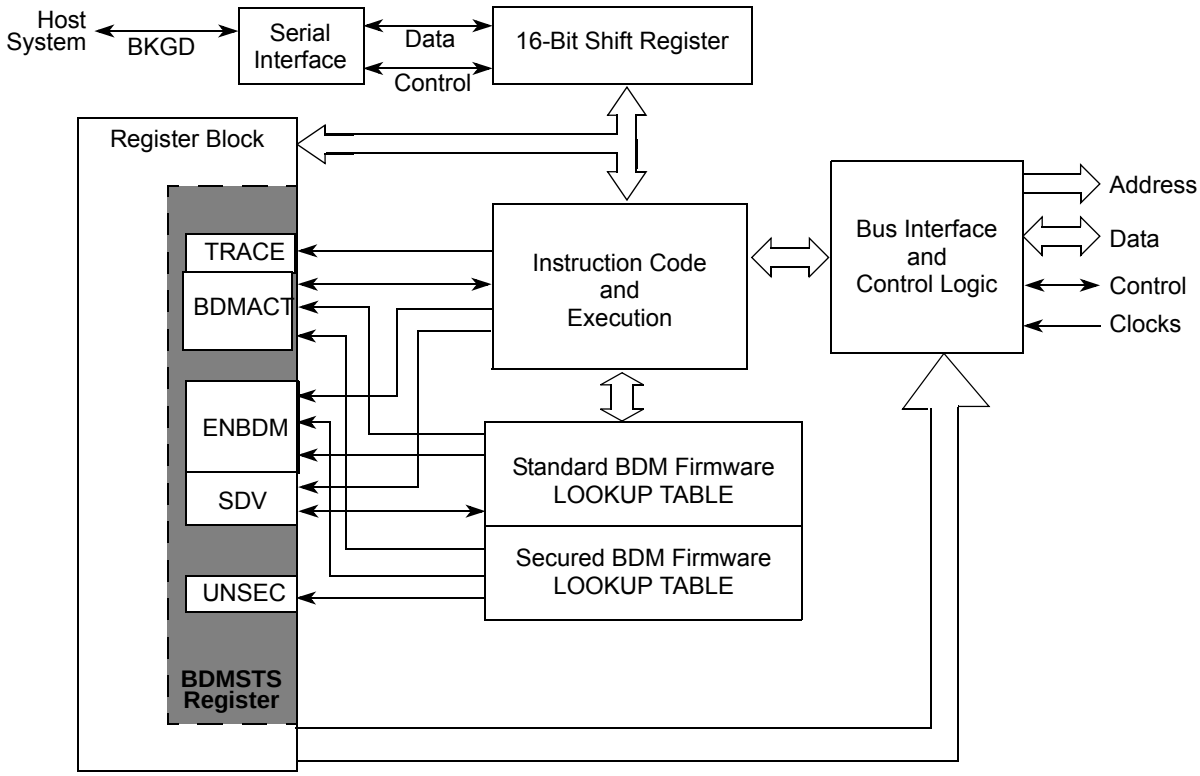


Figure 53. BDM Block Diagram

5.31.2 External Signal Description

A single-wire interface pin called the background debug interface (BKGD) pin is used to communicate with the BDM system. During reset, this pin is a mode select input which selects between normal and special modes of operation. After reset, this pin becomes the dedicated serial interface pin for the background debug mode.

Table 263. BDMSTS Field Descriptions (continued)

Field	Description
3 TRACE	**TRACE1 BDM Firmware Command is Being Executed** — This bit gets set when a BDM TRACE1 firmware command is first recognized. It will stay set until BDM firmware is exited by one of the following BDM commands: GO or GO_UNTIL(182). 0 TRACE1 command is not being executed 1 TRACE1 command is being executed
1 UNSEC	**Unsecure** — If the device is secured this bit is only writable in special single chip mode from the BDM secure firmware. It is in a zero state as secure mode is entered so that the secure BDM firmware lookup table is enabled and put into the memory map overlapping the standard BDM firmware lookup table. The secure BDM firmware lookup table verifies that the on-chip Flash is erased. This being the case, the UNSEC bit is set and the BDM program jumps to the start of the standard BDM firmware lookup table and the secure BDM firmware lookup table is turned off. If the erase test fails, the UNSEC bit will not be asserted. 0 System is in a secured mode. 1 System is in a unsecured mode. Note: When UNSEC is set, security is off and the user can change the state of the secure bits in the on-chip Flash EEPROM. Note that if the user does not change the state of the bits to “unsecured” mode, the system will be secured again when it is next taken out of reset.After reset this bit has no meaning or effect when the security byte in the Flash EEPROM is configured for unsecure mode.

Register Global Address 0x3_FF06

Table 264. BDM CCR Holding Register (BDMCCR)

	7	6	5	4	3	2	1	0
R W	CCR7	CCR6	CCR5	CCR4	CCR3	CCR2	CCR1	CCR0
Reset								
Special Single-Chip Mode	1	1	0	1	1	0	0	0
All Other Modes	0	0	0	0	0	0	0	0

Read: All modes through BDM operation when not secured

Write: All modes through BDM operation when not secured

NOTE

When BDM is made active, the CPU stores the content of its CCR register in the BDMCCR register. However, out of special single-chip reset, the BDMCCR is set to 0xD8 and not 0xD0 which is the reset value of the CCR register in this CPU mode. Out of reset in all other modes the BDMCCR register is read zero.

When entering background debug mode, the BDM CCR holding register is used to save the condition code register of the user’s program. It is also used for temporary storage in the standard BDM firmware mode. The BDM CCR holding register can be written to modify the CCR value.

5.31.3.2.2 BDM Program Page Index Register (BDMPPR)

Register Global Address 0x3_FF08

Table 265. BDM Program Page Register (BDMPPR)

	7	6	5	4	3	2	1	0
R	BPAE	0	0	0	BPP3	BPP2	BPP1	BPP0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented, Reserved

Read: All modes through BDM operation when not secured

Write: All modes through BDM operation when not secured

For hardware data read commands, the external host must wait at least 150 bus clock cycles after sending the address before attempting to obtain the read data. This is to be certain that valid data is available in the BDM shift register, ready to be shifted out. For hardware write commands, the external host must wait 150 bus clock cycles after sending the data to be written before attempting to send a new command. This is to avoid disturbing the BDM shift register before the write has been completed. The 150 bus clock cycle delay in both cases includes the maximum 128 cycle delay that can be incurred as the BDM waits for a free cycle before stealing a cycle.

For BDM firmware read commands, the external host should wait at least 48 bus clock cycles after sending the command opcode and before attempting to obtain the read data. The 48 cycle wait allows enough time for the requested data to be made available in the BDM shift register, ready to be shifted out.

For BDM firmware write commands, the external host must wait 36 bus clock cycles after sending the data to be written before attempting to send a new command. This is to avoid disturbing the BDM shift register before the write has been completed.

The external host should wait for at least for 76 bus clock cycles after a TRACE1 or GO command before starting any new serial command. This is to allow the CPU to exit gracefully from the standard BDM firmware lookup table and resume execution of the user code. Disturbing the BDM shift register prematurely may adversely affect the exit from the standard BDM firmware lookup table.

NOTE

If the bus rate of the target processor is unknown or could be changing, it is recommended that the ACK (acknowledge function) is used to indicate when an operation is complete. When using ACK, the delay times are automated.

Figure 54 represents the BDM command structure. The command blocks illustrate a series of eight bit times starting with a falling edge. The bar across the top of the blocks indicates that the BKGD line idles in the high state. The time for an 8-bit command is 8×16 target clock cycles.(183)

Note:

183. Target clock cycles are cycles measured using the target MCU's serial clock rate. See Section 5.31.4.6, "BDM Serial Interface" and Section 5.31.3.2.1, "BDM Status Register (BDMSTS)" for information on how serial clock rate is selected.

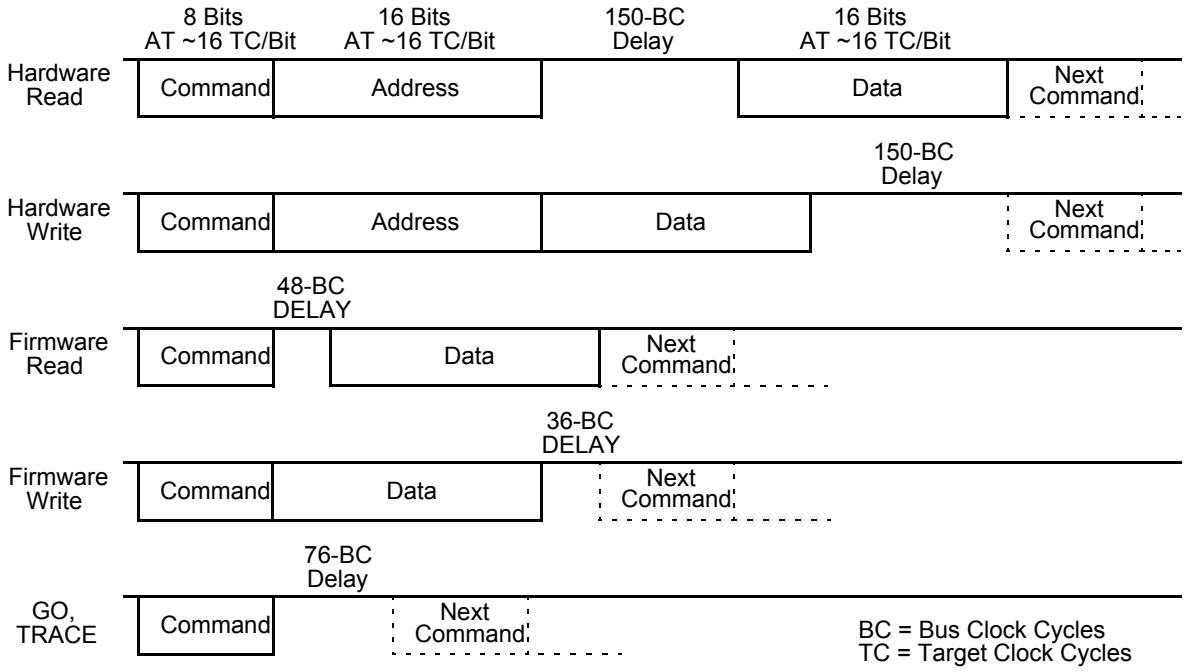


Figure 54. BDM Command Structure

5.31.4.6 BDM Serial Interface

The BDM communicates with external devices serially via the BKGD pin. During reset, this pin is a mode select input which selects between normal and special modes of operation. After reset, this pin becomes the dedicated serial interface pin for the BDM.

Table 291. State1 Sequencer Next State Selection

SC[3:0]	Description (Unspecified matches have no effect)
0010	Match2 to State2
0011	Match1 to State2
0100	Match0 to State2..... Match1 to State3
0101	Match1 to State3.....Match0 to Final State
0110	Match0 to State2..... Match2 to State3
0111	Either Match0 or Match1 to State2
1000	Reserved
1001	Match0 to State3
1010	Reserved
1011	Reserved
1100	Reserved
1101	Either Match0 or Match2 to Final State.....Match1 to State2
1110	Reserved
1111	Reserved

The priorities described in Table 324 dictate that in the case of simultaneous matches, a match leading to final state has priority followed by the match on the lower channel number (0,1,2). Thus with SC[3:0]=1101 a simultaneous match0/match1 transitions to final state.

5.32.3.2.7.2 Debug State Control Register 2 (DBGSCR2)

Table 292. Debug State Control Register 2 (DBGSCR2)

Address: 0x0027

	7	6	5	4	3	2	1	0
R	0	0	0	0	SC3	SC2	SC1	SC0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Read: If COMRV[1:0] = 01

Write: If COMRV[1:0] = 01 and DBG is not armed.

This register is visible at 0x0027 only with COMRV[1:0] = 01. The state control register 2 selects the targeted next state whilst in State2. The matches refer to the match channels of the comparator match control logic as depicted in Figure 62 and described in Section 5.32.3.2.8.1, “Debug Comparator Control Register (DBGXCTL)". Comparators must be enabled by setting the comparator enable bit in the associated DBGXCTL control register.

Table 293. DBGSCR2 Field Descriptions

Field	Description
3–0 SC[3:0]	These bits select the targeted next state whilst in State2, based upon the match event.

Table 294. State2 —Sequencer Next State Selection

SC[3:0]	Description (Unspecified matches have no effect)
0000	Match0 to State1..... Match2 to State3.
0001	Match1 to State3

Field2 Bits in Normal and Loop1 Modes

Figure 65. Information Bits PCH

Bit 3	Bit 2	Bit 1	Bit 0
CSD	CVA	PC17	PC16

Table 328. PCH Field Descriptions

Bit	Description
3 CSD	**Source Destination Indicator** — In Normal and Loop1 mode this bit indicates if the corresponding stored address is a source or destination address. This bit has no meaning in Compressed Pure PC mode. 0 Source Address 1 Destination Address
2 CVA	**Vector Indicator** — In Normal and Loop1 mode this bit indicates if the corresponding stored address is a vector address. Vector addresses are destination addresses, thus if CVA is set, then the corresponding CSD is also set. This bit has no meaning in Compressed Pure PC mode. 0 Non-Vector Destination Address 1 Vector Destination Address
1 PC17	**Program Counter bit 17** — In Normal and Loop1 mode this bit corresponds to program counter bit 17.
0 PC16	**Program Counter bit 16** — In Normal and Loop1 mode this bit corresponds to program counter bit 16.

5.32.4.5.4 Trace Buffer Organization (Compressed Pure PC mode)

Table 329. Trace Buffer Organization Example (Compressed PurePC mode)

Mode	Line Number	2-bits	6-bits	6-bits	6-bits
		Field 3	Field 2	Field 1	Field 0
Compressed Pure PC Mode	Line 1	00	PC1 (Initial 18-bit PC Base Address)		
	Line 2	11	PC4	PC3	PC2
	Line 3	01	0	0	PC5
	Line 4	00	PC6 (New 18-bit PC Base Address)		
	Line 5	10	0	PC8	PC7
	Line 6	00	PC9 (New 18-bit PC Base Address)		

NOTE

Configured for end aligned triggering in compressed PurePC mode, then after rollover it is possible that the oldest base address is overwritten. In this case all entries between the pointer and the next base address have lost their base address following rollover. For example in Table 330 if one line of rollover has occurred, Line 1, PC1, is overwritten with a new entry. Thus the entries on Lines 2 and 3 have lost their base address. For reconstruction of program flow the first base address following the pointer must be used, in the example, Line 4. The pointer points to the oldest entry, Line 2.

Table 447. Flash Reserved3 Register (FRSV3)

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

All bits in the FRSV3 register read 0 and are not writable.

5.40.3.2.16 Flash Reserved4 Register (FRSV4)

This Flash register is reserved for factory testing.

Table 448. Flash Reserved4 Register (FRSV4)

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

All bits in the FRSV4 register read 0 and are not writable.

5.40.3.2.17 Flash Option Register (FOPT)

The FOPT register is the Flash option register.

Table 449. Flash Option Register (FOPT)

	7	6	5	4	3	2	1	0
R	NV[7:0]							
W								
Reset	F	F	F	F	F	F	F	F

= Unimplemented or Reserved

All bits in the FOPT register are readable but are not writable.

During the reset sequence, the FOPT register is loaded from the Flash nonvolatile byte in the Flash configuration field at global address 0x3_FF0E located in P-Flash memory (see Table 411) as indicated by reset condition F in Table 449. If a double bit fault is detected while reading the P-Flash phrase containing the Flash nonvolatile byte during the reset sequence, all bits in the FOPT register will be set.

Table 450. FOPT Field Descriptions

Field	Description
7–0 NV[7:0]	**Nonvolatile Bits** — The NV[7:0] bits are available as nonvolatile bits. Refer to the device user guide for proper use of the NV bits.

Table 489. Erase Verify D-Flash Section Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 010 at command launch
		Set if command not available in current mode (see Table 456)
		Set if an invalid global address [17:0] is supplied
		Set if a misaligned word address is supplied (global address [0] != 0)
		Set if the requested section breaches the end of the D-Flash block
	FPVIOL	None
	MGSTAT1	Set if any errors have been encountered during the read
	MGSTAT0	Set if any non-correctable errors have been encountered during the read

5.40.4.5.15 Program D-Flash Command

The Program D-Flash operation programs one to four previously erased words in the D-Flash block. The Program D-Flash operation will confirm that the targeted location(s) were successfully programmed upon completion.

A Flash word must be in the erased state before being programmed. Cumulative programming of bits within a Flash word is not allowed.

Table 490. Program D-Flash Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
000	0x11	Global address [17:16] to identify the D-Flash block
001	Global address [15:0] of word to be programmed	
010	Word 0 program value	
011	Word 1 program value, if desired	
100	Word 2 program value, if desired	
101	Word 3 program value, if desired	

Upon clearing CCIF to launch the Program D-Flash command, the user-supplied words will be transferred to the Memory Controller and be programmed if the area is unprotected. The CCOBIX index value at Program D-Flash command launch determines how many words will be programmed in the D-Flash block. The CCIF flag is set when the operation has completed.

Table 491. Program D-Flash Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] < 010 at command launch
		Set if CCOBIX[2:0] > 101 at command launch
		Set if command not available in current mode (see Table 456)
		Set if an invalid global address [17:0] is supplied
		Set if a misaligned word address is supplied (global address [0] != 0)
		Set if the requested group of words breaches the end of the D-Flash block
	FPVIOL	Set if the selected area of the D-Flash memory is protected
	MGSTAT1	Set if any errors have been encountered during the verify operation
	MGSTAT0	Set if any non-correctable errors have been encountered during the verify operation