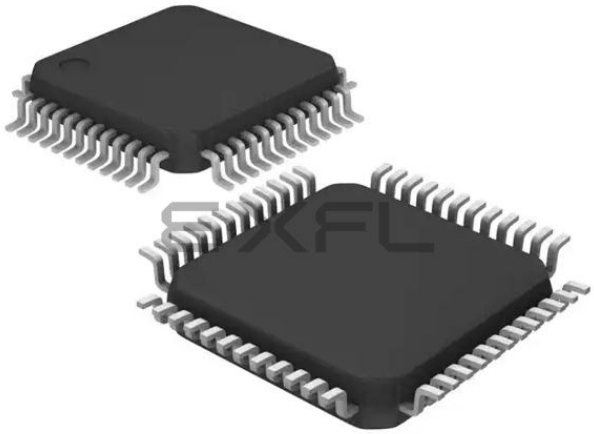

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Application-specific microcontrollers are engineered to

Details	
Product Status	Active
Applications	Automotive
Core Processor	S12
Program Memory Type	FLASH (48kB)
Controller Series	HCS12
RAM Size	2K x 8
Interface	LIN, SCI
Number of I/O	9
Voltage - Supply	2.25V ~ 5.5V
Operating Temperature	-40°C ~ 105°C
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mm912g634dv2apr2

Table 5. Signal Properties Summary

Pin Name Function 1	Pin Name Function 2	Power Supply	Internal Pull Resistor		Description
			CTRL	Reset State	
PA6	—	VDDRX	NA	NA	Port A I/O
PA5	—	VDDRX	NA	NA	Port A I/O
PA4	—	VDDRX	NA	NA	Port A I/O
PA3	SS	VDDRX	NA	NA	Port A I/O, SPI
PA2	SCK	VDDRX	NA	NA	Port A I/O, SPI
PA1	MOSI	VDDRX	NA	NA	Port A I/O, SPI
PA0	MISO	VDDRX	NA	NA	Port A I/O, SPI
PC1	D2DINT	VDDD2D	PUPCE/ D2DEN	Disabled	Port C I/O, D2DI
PC0	D2DCLK	VDDD2D	NA	NA	Port C I/O, D2DI
PD7-0	D2DDAT7-0	VDDD2D	PUPDE/ D2DEN	Disabled	Port D I/O, D2DI

4.3 Operating Conditions

This section describes the operating conditions of the device. Unless otherwise noted those conditions apply to all the following data.

Table 9. Operating Conditions

Ratings	Symbol	Value	Unit
Analog Die Nominal Operating Voltage	V_{SUP}	5.5 to 18	V
Analog Die Functional Operating Voltage - Device is fully functional. All features are operating.	V_{SUPOP}	5.5 to 27	V
MCU I/O and Supply Voltage(17)	V_{DDRX}	4.75 to 5.25	V
MCU Digital Logic Supply Voltage(17)	V_{DDD2D}	2.25 to 2.75	V
MCU Oscillator MM912x634xxxAE MM912x634xxxAP	f_{OSC}	 4.0 to 16 4.0 to 16	MHz
MCU Bus frequency MM912x634xxxAE MM912x634xxxAP	f_{BUS}	f_{BUSMAX}(18)	MHz
Operating Ambient Temperature MM912x634xMxxx MM912x634xVxxx	T_A	 -40 to 125 -40 to 105	°C
Operating Junction Temperature - Analog Die	T_{J_A}	-40 to 150	°C
Operating Junction Temperature - MCU Die	T_{J_M}	-40 to 150	°C

Note:

17. During power up and power down sequence always $V_{DDD2D} < V_{DDRX}$
18. f_{BUSMAX} frequency ratings differ by device and is specified in Table 1

4.7 Thermal Protection Characteristics

Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 18 V, -40 °C ≤ T_A ≤ 125 °C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Table 48. Thermal Characteristics - Voltage Regulators VDD (2.5 V) & VDDX (5.0 V)[58]

Ratings	Symbol	Min	Typ	Max	Unit
VDD/VDDX High-temperature Warning (HTI) Threshold Hysteresis	 T_{HTI} T_{HTI_H}	 110 -	 125 10	 140 -	 °C
VDD/VDDX Over-temperature Shutdown Threshold Hysteresis	 T_{SD} T_{SD_H}	 155 -	 170 10	 185 -	 °C
HSUP Over-temperature Shutdown	T_{HSUPSD}	150	165	180	°C
HSUP Over-temperature Shutdown Hysteresis	T_{HSUPSD_HYS}	-	10	-	°C
HS Over-temperature Shutdown	T_{HSSD}	150	165	180	°C
HS Over-temperature Shutdown Hysteresis	T_{HSSD_HYS}	-	10	-	°C
LS Over-temperature Shutdown	T_{LSSD}	150	165	180	°C
LS Over-temperature Shutdown Hysteresis	T_{LSSD_HYS}	-	10	-	°C
LIN Over-temperature Shutdown	T_{LINSD}	150	165	200	°C
LIN Over-temperature Shutdown Hysteresis	T_{LINSD_HYS}	-	20	-	°C

Note:
58. Guaranteed by characterization. Functionality tested.

4.8 ESD Protection and Latch-up Immunity

All ESD testing is in conformity with CDF-AEC-Q100 stress test qualification for automotive grade integrated circuits. During the device qualification, ESD stresses were performed for the Human Body Model (HBM), Machine Model (MM), Charge Device Model (CDM), as well as LIN transceiver specific specifications.

A device will be defined as a failure if after exposure to ESD pulses, the device no longer meets the device specification. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature, followed by hot temperature, unless specified otherwise in the device specification.

Table 49. ESD and Latch-up Protection Characteristics

Ratings	Symbol	Value	Unit
ESD - Human Body Model (HBM) following AEC-Q100 / JESD22-A114 (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω) - LIN (DGND, PGND, AGND, and LGND shorted) - VS1, VS2, VSENSE, Lx - HSx - All other Pins	V_{HBM}	 ±8000 ±4000 ±3000 ±2000	V
ESD - Charged Device Model (CDM) following AEC-Q100, Corner Pins (1, 12, 13, 24, 25, 36, 37, and 48) All other Pins	V_{CDM}	 ±750 ±500	V
ESD - Machine Model (MM) following AEC-Q100 (C_{ZAP} = 200 pF, R_{ZAP} = 0 Ω), All Pins	V_{MM}	±200	V
Latch-up current at T_A = 125 °C[59]	I_{LAT}	±100	mA

Table 64. 0x00D8–0x00DF Die 2 Die Initiator (D2DI) Map 1 of 3

0x00DD	D2DADRLO	R	ADR[7:0]							
		W								
0x00DE	D2DDATAHI	R	DATA[15:8]							
		W								
0x00DF	D2DDATALO	R	DATA[7:0]							
		W								

Table 65. 0x00E0–0x0E7 Reserved

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00E0- 0x00E7	Reserved	R	0	0	0	0	0	0	0	0
		W								

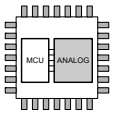
Table 66. 0x00E8–0x00EF Serial Peripheral Interface (SPI)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00E8	SPICR1	R	SPIE	SPE	SPTIE	MSTR	CPOL	CPHA	SSOE	LSBFE
		W								
0x00E9	SPICR2	R	0	XFRW	0	MODFEN	BIDIROE	0	SPISWAI	SPC0
		W								
0x00EA	SPIBR	R	0	SPPR2	SPPR1	SPPR0	0	SPR2	SPR1	SPR0
		W								
0x00EB	SPISR	R	SPIF	0	SPTEF	MODF	0	0	0	0
		W								
0x00EC	SPIDRH	R	R15	R14	R13	R12	R11	R10	R9	R8
		W	T15	T14	T13	T12	T11	T10	T9	T8
0x00ED	SPIDRL	R	R7	R6	R5	R4	R3	R2	R1	R0
		W	T7	T6	T5	T4	T3	T2	T1	T0
0x00EE	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x00EF	Reserved	R	0	0	0	0	0	0	0	0
		W								

Table 67. 0x00F0–0x0FF Reserved

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00E0- 0x00FF	Reserved	R	0	0	0	0	0	0	0	0
		W								

5.7 Interrupts



Interrupts are used to signal a microcontroller that a peripheral needs to be serviced. While in Stop mode, the interrupt signal is used to signal Wake-up events. The interrupts are signaled by an active high level of the D2DINT pin, which will remain high until the interrupt is acknowledged via the D2D-Interface. Interrupts are only asserted while in Normal mode.

5.7.1 Interrupt Source Identification

Once an Interrupt is signalized, there are two options to identify the corresponding source(s).

5.7.1.1 Interrupt Source Mirror

All Interrupt sources in MM912_634 analog die are mirrored to a special Interrupt Source Register (ISR). This register is read only and will indicate all currently pending Interrupts. Reading this register will not acknowledge any interrupt. An additional D2D access is necessary to serve the specific module.

NOTE

The VSI - Voltage Status Interrupt combines the five status flags for the Low Battery Interrupt, Low Voltage Interrupt, High Voltage Interrupt, Voltage Regulator Over-voltage Interrupt, and the Voltage Regulator High Temperature Interrupt. The specific source can be identified by reading the Voltage Status Register - VSR.

5.7.1.1.1 Interrupt Source Register (ISR)

Table 87. Interrupt Source Register (ISR)

Offset[71] 0x00 (0x00 and 0x01 for 8Bit access) Access: User read

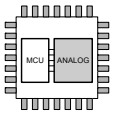
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0	0	HOT	LSOT	HSOT	LINOT	SCI	RX	TX	ERR	TOV	CH3	CH2	CH1	CH0	VSI
W																

Note:
71. Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

Table 88. ISR - Register Field Descriptions

Field	Description
0 - VSI	VSI - Voltage Status Interrupt combining the following sources: • Low Battery Interrupt • Low Voltage Interrupt • High Voltage Interrupt • Voltage Regulator Over-voltage Interrupt • Voltage Regulator High Temperature Interrupt
1 - CH0	CH0 - TIM Channel 0 Interrupt
2 - CH1	CH1 - TIM Channel 1 Interrupt
3 - CH2	CH2 - TIM Channel 2 Interrupt
4 - CH3	CH3 - TIM Channel 3 Interrupt
5 - TOV	TOV - Timer Overflow Interrupt
6 - ERR	ERR - SCI Error Interrupt
7 - TX	TX - SCI Transmit Interrupt
8 - RX	RX - SCI Receive Interrupt
9 - SCI	SCI - ADC Sequence Complete Interrupt
10 - LINOT	LINOT - LIN Driver Over-temperature Interrupt
11 - HSOT	HSOT - High Side Over-temperature Interrupt
12 - LSOT	LSOT - Low Side Over-temperature Interrupt
13 - HOT	HOT - HSUP Over-temperature Interrupt

5.15 LIN Physical Layer Interface - LIN



The LIN bus pin provides a physical layer for single-wire communication in automotive applications. The LIN physical layer is designed to meet the LIN physical layer version 2.1 specification, and has the following features:

- LIN physical layer 2.1 compliant
- Slew rate selection 20 kBit, 10 kBit, and fast Mode (100 kBit)
- Over-temperature Shutdown - HTI
- Permanent Pull-up in Normal mode 30 kΩ, 1.0 MΩ in low power
- Current limitation
- External Rx / Tx access. See Section 5.18, “General Purpose I/O - PTB[0…2]"
- Slew Rate Trim Bit. See Section 5.26, “MM912_634 - Analog Die Trimming"

The LIN driver is a Low Side MOSFET with current limitation and thermal shutdown. An internal pull-up resistor with a serial diode structure is integrated, so no external pull-up components are required for the application in a slave node. The fall time from dominant to recessive and the rise time from recessive to dominant is controlled. The symmetry between both slopes is guaranteed.

5.15.1 LIN Pin

The LIN pin offers high susceptibility immunity level from external disturbance, guaranteeing communication during external disturbance. See Section 4.8, “ESD Protection and Latch-up Immunity".

5.15.2 Slew Rate Selection

The slew rate can be selected for optimized operation at 10 kBit/s and 20 kBit/s as well as a fast baud rate (100 kBit) for test and programming. The slew rate can be adapted with the bits LINSR[1:0] in the LIN Register (LINR). The initial slew rate is 20 kBit/s.

5.15.3 Over-temperature Shutdown (LIN Interrupt)

The output Low Side FET (transmitter) is protected against over-temperature conditions. In case of an over-temperature condition, the transmitter will be shut down and the bit LINOTC in the LIN Register (LINR) is set as long as the condition is present.

If the LINOTIE bit is set in the LIN Register (LINR), an Interrupt IRQ will be generated. Acknowledge the interrupt by reading the LIN Register (LINR). To issue a new interrupt, the condition has to vanish and occur again.

The transmitter is automatically re-enabled once the over-temperature condition is gone and TxD is High.

5.15.4 Low Power Mode and Wake-up Feature

During Low Power mode operation the transmitter of the physical layer is disabled. The receiver is still active and able to detect Wake-up events on the LIN bus line.

A dominant level longer than t_{PROPWL} followed by a rising edge, will generate a wake-up event and be reported in the Wake-up Source Register (WSR).

5.15.5 J2602 Compliance

A Low Voltage Shutdown feature was implemented to allow controlled J2602 compliant LIN driver behavior under Low Voltage conditions (LVSD=0).

When an under-voltage occurs on VS1 (LVI), the LIN stays in recessive mode if it was in recessive state. If it was in a dominant state, it waits until the next dominant to recessive transition, then it stays in the recessive state.

When the under-voltage condition (LVI) is gone, the LIN will start operating when Tx is in a recessive state or on the next dominant to recessive transition.

If the associated error was detected in the received character that caused RDRF to be set, the error flags — noise flag (NF), framing error (FE), and parity error flag (PF) — get set at the same time as RDRF. These flags are not set in overrun cases.

If RDRF was already set when a new character is ready to be transferred from the receive shifter to the receive data buffer, the overrun (OR) flag gets set instead the data along with any associated NF, FE, or PF condition is lost.

At any time, an active edge on the RxD serial data input pin causes the RXEDGIF flag to set. The RXEDGIF flag is cleared by writing a “1” to it. This function does depend on the receiver being enabled (RE = 1).

5.16.3.5 Additional SCI Functions

The following sections describe additional SCI functions.

5.16.3.5.1 8- and 9-Bit Data Modes

The SCI system (transmitter and receiver) can be configured to operate in 9-bit data mode by setting the M control bit in SCIC1. In 9-bit mode, there is a ninth data bit to the left of the MSB of the SCI data register. For the transmit data buffer, this bit is stored in T8 in SCIC3. For the receiver, the ninth bit is held in R8 in SCIC3.

For coherent writes to the transmit data buffer, write to the T8 bit before writing to SCID.

If the bit value to be transmitted as the ninth bit of a new character is the same as for the previous character, it is not necessary to write to T8 again. When data is transferred from the transmit data buffer to the transmit shifter, the value in T8 is copied at the same time data is transferred from SCID to the shifter.

9-bit data mode typically is used in conjunction with parity to allow eight bits of data plus the parity in the ninth bit. Or it is used with address-mark wake-up so the ninth data bit can serve as the wake-up bit. In custom protocols, the ninth bit can also serve as a software-controlled marker.

5.16.3.5.2 Stop Mode Operation

During all stop modes, clocks to the SCI module are halted.

In stop1 and stop2 modes, all SCI register data is lost and must be re-initialized upon recovery from these two stop modes. No SCI module registers are affected in stop3 mode.

The receive input active edge detect circuit is still active in stop3 mode, but not in stop2. An active edge on the receive input brings the CPU out of stop3 mode if the interrupt is not masked (RXEDGIE = 1).

Note that because the clocks are halted, the SCI module will resume operation upon exit from stop (only in stop3 mode). Software should ensure stop mode is not entered while there is a character being transmitted out of or received into the SCI module.

5.16.3.5.3 Loop Mode

When LOOPS = 1, the RSRC bit in the same register chooses between loop mode (RSRC = 0) or single-wire mode (RSRC = 1). Loop mode is sometimes used to check software, independent of connections in the external system, to help isolate system problems. In this mode, the transmitter output is internally connected to the receiver input and the RxD pin is not used by the SCI, so it reverts to a general purpose port I/O pin.

5.16.3.5.4 Single-wire Operation

When LOOPS = 1, the RSRC bit in the same register chooses between loop mode (RSRC = 0) or single-wire mode (RSRC = 1). Single-wire mode is used to implement a half-duplex serial connection. The receiver is internally connected to the transmitter output and to the TxD pin. The RxD pin is not used and reverts to a general purpose port I/O pin.

In single-wire mode, the TXDIR bit in SCIC3 controls the direction of serial data on the TxD pin. When TXDIR = 0, the TxD pin is an input to the SCI receiver and the transmitter is temporarily disconnected from the TxD pin so an external device can send serial data to the receiver. When TXDIR = 1, the TxD pin is an output driven by the transmitter. In single-wire mode, the internal loop back connection from the transmitter to the receiver causes the receiver to receive characters that are sent out by the transmitter.

Table 190. TFLG2 - Register Field Descriptions

Field	Description
7 TOF	Timer Overflow Flag 1 = Indicates that an Interrupt has occurred (Set when 16-bit free-running timer counter overflows from $FFFF to $0000) 0 = Flag indicates an Interrupt has not occurred.

NOTE

The TFLG2 register indicates when an interrupt has occurred. Writing a one to the TOF bit will clear it. Any access to TCNT will clear TOF bit of TFLG2 register if the TFFCA bit in TSCR register is set.

5.19.3.3.14 Timer Input Capture/Output Compare Registers (TC3 - TC0)

Table 191. Timer Input Capture/Output Compare Register 0 (TC0)

Offset[130] 0xCE, 0xCF — Access: User read(anytime)/write [131]

	15	14	13	12	11	10	9	8
R W	tc0_15	tc0_14	tc0_13	tc0_12	tc0_11	tc0_10	tc0_9	tc0_8
Reset	0	0	0	0	0	0	0	0
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
R W	tc0_7	tc0_6	tc0_5	tc0_4	tc0_3	tc0_2	tc0_1	tc0_0
Reset	0	0	0	0	0	0	0	0

Note:
130. Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.
131. TRead anytime. Write anytime for output compare functions Writes to these registers have no effect during input capture.

Table 192. Timer Input Capture/Output Compare Register 1(TC1)

Offset[132] 0xD0, 0xD1 — Access: User read(anytime)/write [133]

	15	14	13	12	11	10	9	8
R W	tc1_15	tc1_14	tc1_13	tc1_12	tc1_11	tc1_10	tc1_9	tc1_8
Reset	0	0	0	0	0	0	0	0
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
R W	tc1_7	tc1_6	tc1_5	tc1_4	tc1_3	tc1_2	tc1_1	tc1_0
Reset	0	0	0	0	0	0	0	0

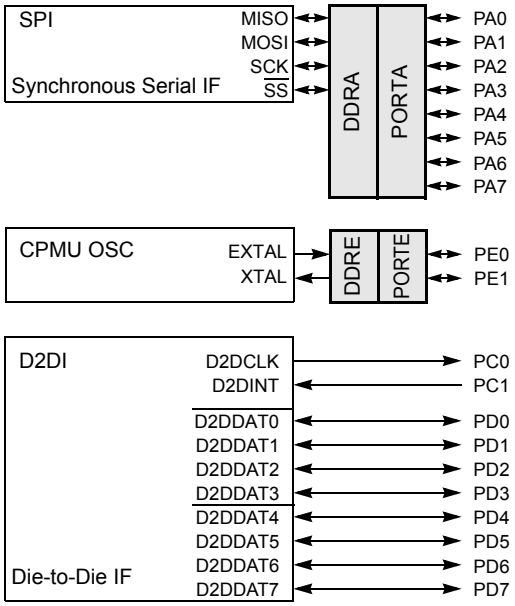
Note:
132. Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.
133. TRead anytime. Write anytime for output compare functions Writes to these registers have no effect during input capture.

5.28 Port Integration Module (S12IPIMV1)

5.28.1 Introduction

The Port Integration Module (PIM) establishes the interface between the MC9S12I64 peripheral modules SPI and Die-To-Die Interface module (D2DI) to the I/O pins of the MCU.

All port A and port E pins support general purpose I/O functionality if not in use with other functions. The PIM controls the signal prioritization and multiplexing on shared pins.



Port Integration Module Elements

Figure 42. Block Diagram

5.28.1.1 Features

- 8-pin port A associated with the SPI module
- 2-pin port C used as D2DI clock output and D2DI interrupt input
- 8-pin port D used as 8 or 4 bit data I/O for the D2DI module
- 2-pin port E associated with the CPMU OSC module
- GPIO function shared on port A, E pins
- Pull-down devices on PC1 and PD7-0 if used as D2DI inputs
- Reduced drive capability on PC0 and PD7-0 on per pin basis

The Port Integration Module includes these distinctive registers:

- Data registers for ports A, E when used as general-purpose I/O
- Data direction registers for ports A, E when used as general-purpose I/O
- Port input register on ports A and E
- Reduced drive register on port C and D

Table 235. DDRE Register Field Descriptions

Field	Description
1–0 DDRE	**Port E Data Direction**— This bit determines whether the associated pin is an input or output. The enabled CPMU OSC function connects the associated pins directly to the oscillator module. In this case the data direction bits will not change. 1 Associated pin is configured as output. 0 Associated pin is configured as input.

5.28.2.6 PIM Reserved Registers

These registers are reserved for factory testing of the PIM module. Writing to these addresses can alter the module functionality.

Table 236. PIM Reserved Registers

Address 0x0004-0x0009 Access: User read(160)

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Note:
160. Read: Always reads 0x00
Write: Not allowed

5.28.2.7 Pull Control Register (PUCR)

Table 237. Pull Control Register (PUCR)

Address 0x0124 Access: User read/write(161)

	7	6	5	4	3	2	1	0
R	0	BKPUE	0	0	0	0	PDPEE	0
W								
Reset	0	1	0	0	0	0	1	0

Note:
161. Read: Anytime.
Write: Anytime.

Table 238. PUCR Register Field Descriptions

Field	Description
6 BKPUE	BKGD pin pull-up Enable—Enable pull-up devices on BKGD pin. This bit configures whether a pull-up device is activated, if the pin is used as input. This bit has no effect if the pin is used as output. Out of reset the pull-up device is enabled. 1 Pull-up device enabled. 0 Pull-up device disabled.
1 PDPEE	Pull-down Port E Enable—Enable pull-down devices on all Port E input pins. This bit configures whether pull-down devices are activated, if the pins are used as inputs. This bit has no effect if the pins are used as outputs. Out of reset the pull-down devices are enabled. If the CPMU OSC function is active the pull-down devices are disabled. In this case the register bit will not change. 1 Pull-down devices enabled. 0 Pull-down devices disabled.

- Four trace modes
  - Normal: change of flow (COF) PC information is stored (see Section 5.32.4.5.2.1, “Normal Mode") for change of flow definition.
  - Loop1: same as Normal but inhibits consecutive duplicate source address entries
  - Detail: address and data for all cycles except free cycles and opcode fetches are stored
  - Compressed Pure PC: all program counter addresses are stored
- 4-stage state sequencer for trace buffer control
  - Tracing session trigger linked to Final State of state sequencer
  - Begin and End alignment of tracing to trigger

5.32.1.4 Modes of Operation

The DBG module can be used in all MCU functional modes.

During BDM hardware accesses and whilst the BDM module is active, CPU monitoring is disabled. When the CPU enters active BDM Mode through a BACKGROUND command, the DBG module, if already armed, remains armed.

The DBG module tracing is disabled if the MCU is secure, however, breakpoints can still be generated

Table 269. Mode Dependent Restriction Summary

BDM Enable	BDM Active	MCU Secure	Comparator Matches Enabled	Breakpoints Possible	Tagging Possible	Tracing Possible
x	x	1	Yes	Yes	Yes	No
0	0	0	Yes	Only SWI	Yes	Yes
0	1	0	Active BDM not possible when not enabled			
1	0	0	Yes	Yes	Yes	Yes
1	1	0	No	No	No	No

5.32.1.5 Block Diagram

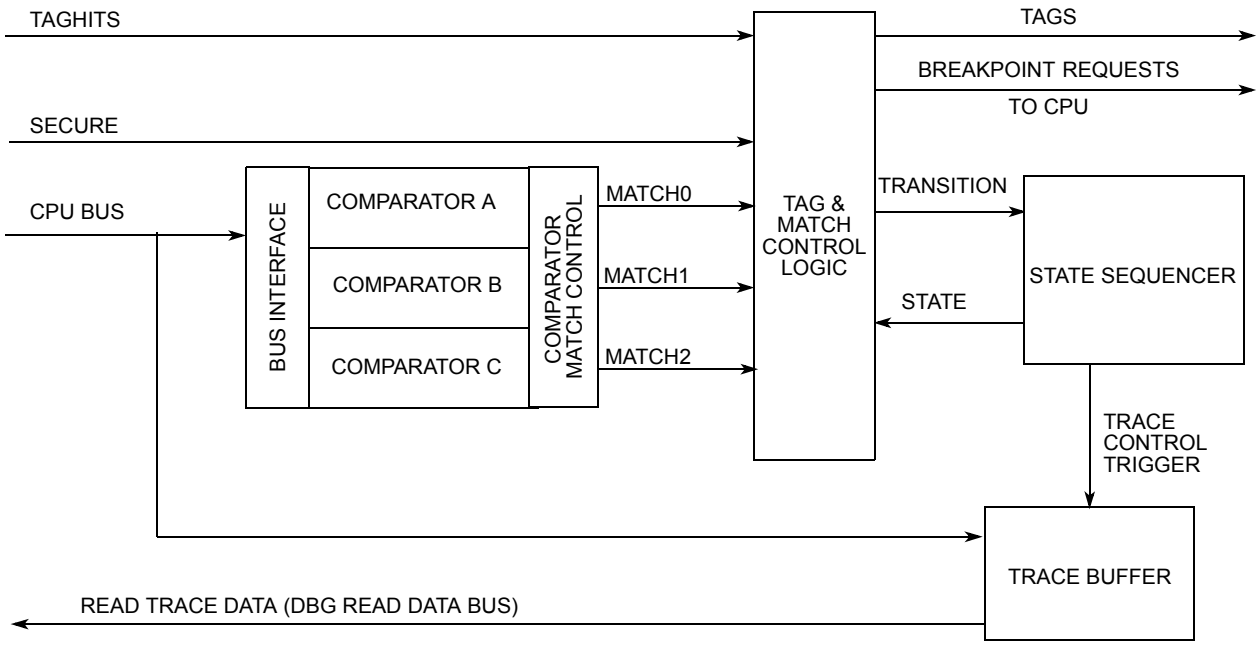


Figure 62. Debug Module Block Diagram

Table 291. State1 Sequencer Next State Selection

SC[3:0]	Description (Unspecified matches have no effect)
0010	Match2 to State2
0011	Match1 to State2
0100	Match0 to State2..... Match1 to State3
0101	Match1 to State3.....Match0 to Final State
0110	Match0 to State2..... Match2 to State3
0111	Either Match0 or Match1 to State2
1000	Reserved
1001	Match0 to State3
1010	Reserved
1011	Reserved
1100	Reserved
1101	Either Match0 or Match2 to Final State.....Match1 to State2
1110	Reserved
1111	Reserved

The priorities described in Table 324 dictate that in the case of simultaneous matches, a match leading to final state has priority followed by the match on the lower channel number (0,1,2). Thus with SC[3:0]=1101 a simultaneous match0/match1 transitions to final state.

5.32.3.2.7.2 Debug State Control Register 2 (DBGSCR2)

Table 292. Debug State Control Register 2 (DBGSCR2)

Address: 0x0027

	7	6	5	4	3	2	1	0
R	0	0	0	0	SC3	SC2	SC1	SC0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Read: If COMRV[1:0] = 01

Write: If COMRV[1:0] = 01 and DBG is not armed.

This register is visible at 0x0027 only with COMRV[1:0] = 01. The state control register 2 selects the targeted next state whilst in State2. The matches refer to the match channels of the comparator match control logic as depicted in Figure 62 and described in Section 5.32.3.2.8.1, “Debug Comparator Control Register (DBGXCTL)". Comparators must be enabled by setting the comparator enable bit in the associated DBGXCTL control register.

Table 293. DBGSCR2 Field Descriptions

Field	Description
3–0 SC[3:0]	These bits select the targeted next state whilst in State2, based upon the match event.

Table 294. State2 —Sequencer Next State Selection

SC[3:0]	Description (Unspecified matches have no effect)
0000	Match0 to State1..... Match2 to State3.
0001	Match1 to State3

One cycle after bdm_unsecure is asserted the secure firmware is disabled from the map.

In secure mode aBDM access to a non register address will be translated to a peripheral register address, and BDM registers are not accessible.

No BDM global access is possible if the chip is secured.

In secured expanded mode or emulation mode, FLASH and EEPROM are disabled by the MMC.

5.34.2 BDM

When security is active and the blank check is performed and failed, only BDM hardware commands are available. If the blank check is succeeds, all BDM commands are available.

The BDM status register contains a bit called UNSEC. This bit is only writable by the secure firmware in special single chip mode. Based on the state of this bit, the BDM generates a signal called “unsecure”. The bit and signal are always reset to 0 (= de-asserted = secure).

If the user resets into special single chip mode with the part secured, an alternate BDM firmware (“SECURE firmware”), is placed in the map along with the standard BDM firmware. The secure firmware has higher priority than the standard firmware, but it is smaller (less bytes). The secure firmware covers the vector space, but does not reach the beginning of the BDM firmware space.

When blank check is successfully performed, UNSEC is asserted. The BDM program jumps to the start of the standard BDM firmware program and the secure firmware is turned off. If the blank check fails, then the ENBDM bit in the BDMSTS register is set without asserting UNSEC, and the BDM firmware code enters a loop. This enables the BDM hardware commands. In secure mode the MMC restricts BDM accesses to the register space.

With UNSEC asserted, security is off and the user can change the state of the secure bits in the FLASH. Note that if the user does not change the state of these bits to “unsecured”, the part will be secured again when it is next taken out of reset.

5.34.3 DBG

S12X_DBG will disable the trace buffer, but breakpoints are still valid.

5.34.4 XGATE

XGATE internal registers XGCCR, XGPC, and XGR1 - XGR7 can not be written and will read zero from IPBI.

Single stepping in XGATE is not possible.

XGATE code residing in the internal RAM cannot be protected:

1. start MCU in NSC, let it run for a while
2. reset into SSC, MASERS the NVM
3. reset into SSC, blank check of BDM secure firmware succeeds
4. MCU is temporarily unsecured
5. BDM can be used to read internal RAM (contents not affected by reset)

5.35 Secure firmware Code Overview

The BDM contains a secure firmware code. This firmware code is invoked when the user comes out of reset in special single chip mode with security enabled. The function of the firmware code is straight forward:

- Verify the FLASH is erased
- Verify the EEPROM is erased
- If both are erased, release security

If either the FLASH or the EEPROM is not erased, then security is not released. The ENBDM bit is set and the code enters a loop. This allows BDM hardware commands, which may be used to erase the EEPROM and FLASH.

Note that erasing the memories and erasing / reprogramming the security bits is NOT part of the firmware code. The user must perform these operations.

The blank check of FLASH and EEPROM is done in the BDM firmware. As such it could be changed on future parts. The current scheme uses the NVM command state-machines (FTX, EETX) to perform the blank check.

5.35.0.2.2 Special Single Chip Mode (SS)

- BDM firmware commands are disabled.
- BDM hardware commands are restricted to the register space.
- Execution of Flash and EEPROM commands is restricted. Please refer to the NVM block guide for details.
- Tracing code execution using the DBG module is disabled.

Special single chip mode means BDM is active after reset. The availability of BDM firmware commands depends on the security state of the device. The BDM secure firmware first performs a blank check of both the Flash memory and the EEPROM. If the blank check succeeds, security will be temporarily turned off and the state of the security bits in the appropriate Flash memory location can be changed If the blank check fails, security will remain active, only the BDM hardware commands will be enabled, and the accessible memory space is restricted to the peripheral register area. This will allow the BDM to be used to erase the EEPROM and Flash memory without giving access to their contents. After erasing both Flash memory and EEPROM, another reset into special single chip mode will cause the blank check to succeed and the options/security byte can be programmed to “unsecured” state via BDM.

While the BDM is executing the blank check, the BDM interface is completely blocked, which means that all BDM commands are temporarily blocked.

5.35.0.2.3 Executing from Internal Memory in Expanded Mode

The user may choose to operate from internal memory while in expanded mode. To do this the user must start in single chip mode and write to the mode bits selecting expanded operation. In this mode internal visibility and IPIPE are blocked. If the users program tries to execute from outside the program memory space (internal space occupied by the FLASH), the FLASH and EEPROM will be disabled. BDM operations will be blocked.

If the user begins operation in single chip mode with security on, the user is constrained to operate out of internal memory - even if the user changes to expanded mode. To accomplish this the MMC needs to register that the part started in single chip mode and was secured. The CPU will provide the state of the two high-order bits of the Program Counter. All this information, plus the firmware size information is used to determine that the part is executing in the proper space. If the program strays, the selects for FLASH and EEPROM are disabled by the MMC until the part goes through reset.

5.35.0.2.4 Unsecuring the Microcontroller

Unsecuring the microcontroller can be done by three different methods:

1. Backdoor key access
2. Reprogramming the security bits
3. Complete memory erase (special modes)

5.35.0.2.5 Unsecuring the MCU Using the Backdoor Key Access

In normal modes (single chip and expanded), security can be temporarily disabled using the backdoor key access method. This method requires that:

- The backdoor key at 0xFF00–0xFF07 (= global addresses 0x7F_FF00–0x7F_FF07) has been programmed to a valid value.
- The KEYEN[1:0] bits within the Flash options/security byte select ‘enabled’.
- In single chip mode, the application program programmed into the microcontroller must be designed to have the capability to write to the backdoor key locations.

The backdoor key values themselves would not normally be stored within the application data, which means the application program would have to be designed to receive the backdoor key values from an external source (e.g. through a serial port).

The backdoor key access method allows debugging of a secured microcontroller without having to erase the Flash. This is particularly useful for failure analysis.

NOTE

No word of the backdoor key is allowed to have the value 0x0000 or 0xFFFF.

5.35.0.3 Reprogramming the Security Bits

In normal single chip mode (NS), security can also be disabled by erasing and reprogramming the security bits within Flash options/security byte to the unsecured value. Because the erase operation will erase the entire sector from 0xFE00–0xFFFF (0x7F_FE00–0x7F_FFFF), the backdoor key and the interrupt vectors will also be erased; this method is not recommended for normal single chip mode. The application software can only erase and program the Flash options/security byte if the Flash sector

Table 342. Reference Clock Frequency Selection if OSC_LCP is enabled

REFCLK Frequency Ranges (OSCE=1)	REFFRQ[1:0]
1.0 MHz <= f_{REF} <= 2.0 MHz	00
2.0 MHz < f_{REF} <= 6.0 MHz	01
6.0 MHz < f_{REF} <= 12.0 MHz	10
f_{REF} >12 MHz	11

5.38.3.2.3 S12CPMU Post Divider Register (CPMUPOSTDIV)

The POSTDIV register controls the frequency ratio between the VCOCLK and the PLLCLK.

Table 343. S12CPMU Post Divider Register (CPMUPOSTDIV)

0x0036

	7	6	5	4	3	2	1	0
R	0	0	0	POSTDIV[4:0]				
W								
Reset	0	0	0	0	0	0	1	1

= Unimplemented or Reserved

Read: Anytime

Write: Anytime if PLLSEL=1. Else write has no effect.

If PLL is locked (LOCK=1) $f_{PLL} = \frac{f_{VCO}}{(POSTDIV + 1)}$

If PLL is not locked (LOCK=0) $f_{PLL} = \frac{f_{VCO}}{4}$

If PLL is selected (PLLSEL=1) $f_{bus} = \frac{f_{PLL}}{2}$

5.38.3.2.4 S12CPMU Flags Register (CPMUFLG)

This register provides S12CPMU status bits and flags.

Table 344. S12CPMU Flags Register (CPMUFLG)

0x0037

	7	6	5	4	3	2	1	0
R	RTIF	PORF	LVRF	LOCKIF	LOCK	ILAF	OSCIF	UPOSC
W								
Reset	0	(193)	(194)	0	0	(195)	0	0

= Unimplemented or Reserved

Note:

193. PORF is set to 1 when a power on reset occurs. Unaffected by System Reset.
194. LVRF is set to 1 when a low voltage reset occurs. Unaffected by System Reset. Set by power on reset.
195. ILAF is set to 1 when an illegal address reset occurs. Unaffected by System Reset. Cleared by power on reset.

Read: Anytime

Write: Refer to each bit for individual write conditions

Table 405. SPISR Field Descriptions

Field	Description
7 SPIF	**SPIF Interrupt Flag** — This bit is set after received data has been transferred into the SPI data register. For information about clearing SPIF Flag, please refer to Table 406. 0 Transfer not yet complete. 1 New data copied to SPIDR.
5 SPTEF	**SPI Transmit Empty Interrupt Flag** — If set, this bit indicates that the transmit data register is empty. For information about clearing this bit and placing data into the transmit data register, please refer to Table 407. 0 SPI data register not empty. 1 SPI data register empty.
4 MODF	**Mode Fault Flag** — This bit is set if the SS input becomes low while the SPI is configured as a master and mode fault detection is enabled, MODFEN bit of SPICR2 register is set. Refer to MODFEN bit description in Section 5.39.3.2.2, “SPI Control Register 2 (SPICR2)". The flag is cleared automatically by a read of the SPI status register (with MODF set) followed by a write to the SPI control register 1. 0 Mode fault has not occurred. 1 Mode fault has occurred.

Table 406. SPIF Interrupt Flag Clearing Sequence

XFRW Bit	SPIF Interrupt Flag Clearing Sequence			
0	Read SPISR with SPIF = 1	then	Read SPIDRL	
1	Read SPISR with SPIF = 1	then	Byte Read SPIDRL (203)	
			or	
			Byte Read SPIDRH (204)	Byte Read SPIDRL
			or	
			Word Read (SPIDRH:SPIDRL)	

Note:

203. Data in SPIDRH is lost in this case.
204. SPIDRH can be read repeatedly without any effect on SPIF. SPIF Flag is cleared only by the read of SPIDRL after reading SPISR with SPIF = 1.

Table 407. SPTEF Interrupt Flag Clearing Sequence

XFRW Bit	SPTEF Interrupt Flag Clearing Sequence			
0	Read SPISR with SPTEF = 1	then	Write to SPIDRL (205)	
1	Read SPISR with SPTEF = 1	then	Byte Write to SPIDRL (205)(206)	
			or	
			Byte Write to SPIDRH (205)(207)	Byte Write to SPIDRL (205)
			or	
			Word Write to (SPIDRH:SPIDRL) (205)	

Note:

205. Any write to SPIDRH or SPIDRL with SPTEF = 0 is effectively ignored.
206. Data in SPIDRH is undefined in this case.
207. SPIDRH can be written repeatedly without any effect on SPTEF. SPTEF Flag is cleared only by writing to SPIDRL after reading SPISR with SPTEF = 1.

5.40.1.2 Features

5.40.1.2.1 P-Flash Features

- Single bit fault correction and double bit fault detection within a 32-bit double word during read operations
- Automated program and erase algorithm with verify and generation of ECC parity bits
- Fast sector erase and phrase program operation
- Ability to read the P-Flash memory while programming a word in the D-Flash memory
- Flexible protection scheme to prevent accidental program or erase of P-Flash memory

5.40.1.2.2 D-Flash Features

- Single bit fault correction and double bit fault detection within a word during read operations
- Automated program and erase algorithm with verify and generation of ECC parity bits
- Fast sector erase and word program operation
- Protection scheme to prevent accidental program or erase of D-Flash memory
- Ability to program up to four words in a burst sequence

5.40.1.2.3 Other Flash Module Features

- No external high-voltage power supply required for Flash memory program and erase operations
- Interrupt generation on Flash command completion and Flash error detection
- Security mechanism to prevent unauthorized access to the Flash memory

5.40.1.3 Block Diagram

The block diagram of the Flash module is shown in Figure 105.

5.40.2 External Signal Description

The Flash module contains no signals that connect off-chip.

5.40.3 Memory Map and Registers

This section describes the memory map and registers for the Flash module. Read data from unimplemented memory space in the Flash module is undefined. Write access to unimplemented or reserved memory space in the Flash module will be ignored by the Flash module.

5.40.3.1 Module Memory Map

The S12 architecture places the P-Flash memory between global addresses .The P-Flash memory map is shown in .

The FPROT register, described in P-Flash Protection Register (FPROT), can be set to protect regions in the Flash memory from accidental program or erase. The Flash memory addresses covered by these protectable regions are shown in the P-Flash memory map. The higher address region is mainly targeted to hold the boot loader code since it covers the vector space. Default protection settings as well as security information that allows the MCU to restrict access to the Flash module are stored in the Flash configuration field as described in Table 411.

Table 411. Flash Configuration Field

Global Address	Size (Bytes)	Description
0x3_FF00-0x3_FF07	8	Backdoor Comparison Key Refer to Section 5.40.4.5.11, “Verify Backdoor Access Key Command", and Section 5.40.5.1, “Unsecuring the MCU using Backdoor Key Access"
0x3_FF08-0x3_FF0B	4	Reserved
0x3_FF0C	1	P-Flash Protection byte. Refer to Section 5.40.3.2.9, “P-Flash Protection Register (FPROT)"
0x3_FF0D	1	D-Flash Protection byte. Refer to Section 5.40.3.2.11, “D-Flash Protection Register (DFPROT)"
0x3_FF0E	1	Flash Nonvolatile byte Refer to Section 5.40.3.2.17, “Flash Option Register (FOPT)"
0x3_FF0F	1	Flash Security byte Refer to Section 5.40.3.2.2, “Flash Security Register (FSEC)"

Note:

212. 0x3FF08-0x3_FF0F form a Flash phrase and must be programmed in a single command write sequence. Each byte in the 0x3_FF08 - 0x3_FF0B reserved field should be programmed to 0xFF.

Table 412. Program IFR Fields

Global Address	Size (Bytes)	Field Description
0x0_4000 – 0x0_4007	8.0	Reserved
0x0_4008 – 0x0_40B5	174	Reserved
0x0_40B6 – 0x0_40B7	2.0	Version ID
0x0_40B8 – 0x0_40BF	8.0	Reserved
0x0_40C0 – 0x0_40FF	64	Program Once Field Refer to Section 5.40.4.5.6, “Program Once Command"

Note:

213. For patch code storage, see Section 5.40.4.2, “IFR Version ID Word"

214. Used to track firmware patch versions, see Section 5.40.4.2, “IFR Version ID Word"

Table 413. D-Flash and Memory Controller Resource Fields

Global Address	Size (Bytes)	Description
0x0_4000 – 0x0_43FF	1,024	Reserved
0x0_4400 – 0x0_53FF	4,096	D-Flash Memory
0x0_5400 – 0x0_57FF	1,024	Reserved
0x0_5800 – 0x0_5AFF	768	Memory Controller Scratch RAM
0x0_5B00 – 0x0_5FFF	1,280	Reserved
0x0_6000 – 0x0_67FF	2,048	Reserved
0x0_6800 – 0x0_7FFF	6,144	Reserved

5.40.3.2.1 Flash Clock Divider Register (FCLKDIV)

The FCLKDIV register is used to control timed events in program and erase algorithms.

Table 415. Flash Clock Divider Register (FCLKDIV)

	7	6	5	4	3	2	1	0
R	FDIVLD	FDIVLCK	FDIV[5:0]					
W								
Reset	0	0	0	0	0	0	0	0

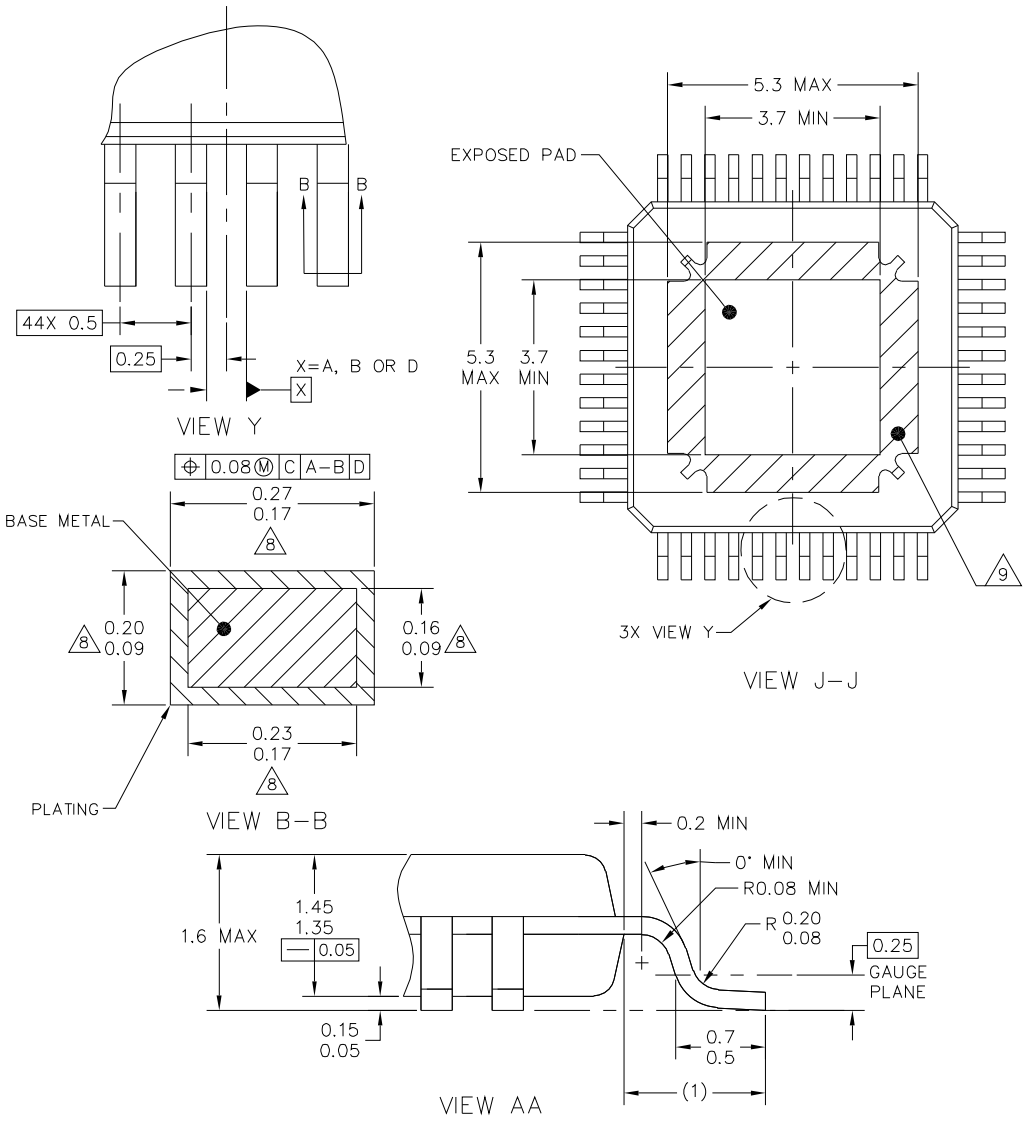
= Unimplemented or Reserved

All bits in the FCLKDIV register are readable, bit 7 is not writable, bit 6 is write-once-hi and controls the writability of the FDIV field.

The FCLKDIV register must never be written to while a Flash command is executing (CCIF=0). The FCLKDIV register is writable during the Flash reset sequence even though CCIF is clear.

Table 416. FCLKDIV Field Descriptions

Field	Description
7 FDIVLD	**Clock Divider Loaded** 0 FCLKDIV register has not been written since the last reset 1 FCLKDIV register has been written since the last reset
6 FDIVLCK	**Clock Divider Locked** 0 FDIV field is open for writing 1 FDIV value is locked and cannot be changed. Once the lock bit is set high, only reset can clear this bit and restore writability to the FDIV field.
5–0 FDIV[5:0]	**Clock Divider Bits** — FDIV[5:0] must be set to effectively divide BUSCLK down to 1 MHz to control timed events during Flash program and erase algorithms. Table 417 shows recommended values for FDIV[5:0] based on the BUSCLK frequency. Please refer to Section 5.40.4.3, “Flash Command Operations", for more information.



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	CASE NUMBER: 2003-01	01 DEC 2009
	STANDARD: JEDEC MS-026 BBC	

AE SUFFIX
48-PIN
LQFP48
REVISION 0