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Details	
Product Status	Active
Applications	Automotive
Core Processor	S12
Program Memory Type	FLASH (64kB)
Controller Series	HCS12
RAM Size	6K x 8
Interface	LIN, SCI
Number of I/O	9
Voltage - Supply	2.25V ~ 5.5V
Operating Temperature	-40°C ~ 105°C
Mounting Type	Surface Mount
Package / Case	48-LQFP Exposed Pad
Supplier Device Package	48-HLQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mm912h634dm1ae

Table 14. Static Electrical Characteristics - Voltage Regulator 5.0 V (VDDX)

Ratings	Symbol	Min	Typ	Max	Unit
Normal Mode Output Voltage 1.0 mA < I_{VDDX} + $I_{VDDXINTERNAL}$ < 80 mA; 5.5 V < V_{SUP} < 27 V (24)	V_{DDXRUN}	4.75	5.00	5.25	V
Normal Mode Output Current Limitation (I_{VDDX})	$I_{VDDXRUN}$	80	130	200	mA
Stop Mode Output Voltage (I_{VDDX} + $I_{VDDXINTERNAL}$ < 500 µA for T_J ≥ 25 °C; I_{VDDX} + $I_{VDDXINTERNAL}$ < 400 µA for T_J < 25 °C) (24)	$V_{DDXSTOP}$	-	5.0	5.5	V
Stop Mode Output Current Limitation (I_{VDDX})	$I_{VDDXSTOP}$	1.0	-	20	mA
Line Regulation Normal Mode, I_{VDDX} = 80 mA Stop Mode, I_{VDDX} = 500 µA	 LR_{XRUN} LR_{XSTOP}	 - -	 20 -	 25 200	mV
Load Regulation Normal Mode, 1.0 mA < I_{VDDX} < 80 mA Normal Mode, V_{SUP} = 3.6 V, 1.0 mA < I_{VDDX} < 40 mA Stop Mode, 0.1 mA < I_{VDDX} < 500 µA	 LD_{XRUN} LD_{XCRK} LD_{XSTOP}	 - - -	 15 - -	 80 200 250	mV
External Capacitor	C_{VDDX}	1.0	-	10	µF
External Capacitor ESR	C_{VDDX_R}	-	-	10	Ohm

Note:

24. $I_{VDDXINTERNAL}$ includes internal consumption from both analog and MCU die.

Table 15. Static Electrical Characteristics - Voltage Regulator 2.5 V (VDD)

Ratings	Symbol	Min	Typ	Max	Unit
Normal Mode Output Voltage 1.0 mA < I_{VDD} + $I_{VDDINTERNAL}$ ≤ 45 mA; 5.5 V < V_{SUP} < 27 V (25)	V_{DDRUN}	2,425	2.5	2,575	V
Normal Mode Output Current Limitation (I_{VDD}) T_J < 25 °C T_J ≥ 25 °C	$I_{VDDLIMRUN}$	 - -	 80 80	 120 143	mA
Stop Mode Output Voltage (I_{VDD} + $I_{VDDINTERNAL}$ < 500 µA for T_J ≥ 25 °C; I_{VDD} + $I_{VDDINTERNAL}$ < 400 µA for T_J < 25 °C) (25)	V_{DDSTOP}	2.25	2.5	2.75	V
Stop Mode Output Current Limitation (I_{VDD})	$I_{VDDLIMSTOP}$	-	-	10	mA
Line Regulation Normal Mode, I_{VDD} = 45 mA Stop Mode, I_{VDD} = 1.0 mA	 LR_{RUN} LR_{STOP}	 - -	 10 -	 12.5 200	mV
Load Regulation Normal Mode, 1.0 mA < I_{VDD} < 45 mA Normal Mode, V_{SUP} = 3.6 V, 1.0 mA < I_{VDD} < 30 mA Stop Mode, 0.1 mA < I_{VDD} < 1.0 mA	 LD_{RUN} LD_{CRK} LD_{STOP}	 - - -	 7.5 - -	 40 40 200	mV
External Capacitor	C_{VDD}	1.0	-	10	µF
External Capacitor ESR	C_{VDD_R}	-	-	10	Ohm

Note:

25. $I_{VDDINTERNAL}$ includes internal consumption from both analog and MCU die.

Table 49. ESD and Latch-up Protection Characteristics (continued)

Ratings	Symbol	Value	Unit
ESD GUN - LIN Conformance Test Specification[61], unpowered, contact discharge, C_{ZAP}= 150 pF, R_{ZAP} = 330 Ω. - LIN (with or without bus filter C_{BUS}=220 pF) - VS1, VS2 with C_{VS} - Lx with serial R_{LX}		 ±15000 ±20000 ±6000	V
ESD GUN - following IEC 61000-4-2 Test Specification[62], unpowered, contact discharge, C_{ZAP}= 150 pF, R_{ZAP} = 330 Ω - LIN (with or without bus filter C_{BUS}=220 pF) - VSENSE with serial R_{VSENSE}[60] - VS1, VS2 with C_{VS} - Lx with serial R_{LX}		 ±8000 ±8000 ±8000 ±8000	V
ESD GUN - following ISO10605 Test Specification[62], unpowered, contact discharge, C_{ZAP}= 150 pF, R_{ZAP} = 2.0 kΩ - LIN (with or without bus filter C_{BUS}=220pF) - VSENSE with serial R_{VSENSE}[60] - VS1, VS2 with C_{VS} - Lx with serial R_{LX}		 ±6000 ±6000 ±6000 ±6000	V
ESD GUN - following ISO10605 Test Specification[62], powered, contact discharge, C_{ZAP}= 330 pF, R_{ZAP} = 2.0 kΩ - LIN (with or without bus filter C_{BUS}=220 pF) - VSENSE with serial R_{VSENSE}[60] - VS1, VS2 with C_{VS} - Lx with serial R_{LX}		 ±8000 ±8000 ±8000 ±8000	V

Note:
59. Input Voltage Limit = -2.5 to 7.5 V.
60. With C_{VBAT} (10…100 nF) as part of the battery path.
61. Certification available on request
62. Tested internally only; certification pending

4.9 Additional Test Information ISO7637-2

Immunity against transients for the LIN, Lx, and VBAT, is specified according to the LIN Conformance Test Specification - Section LIN EMC Test Specification refer to the LIN Conformance Test Certification Report - available as separate document.

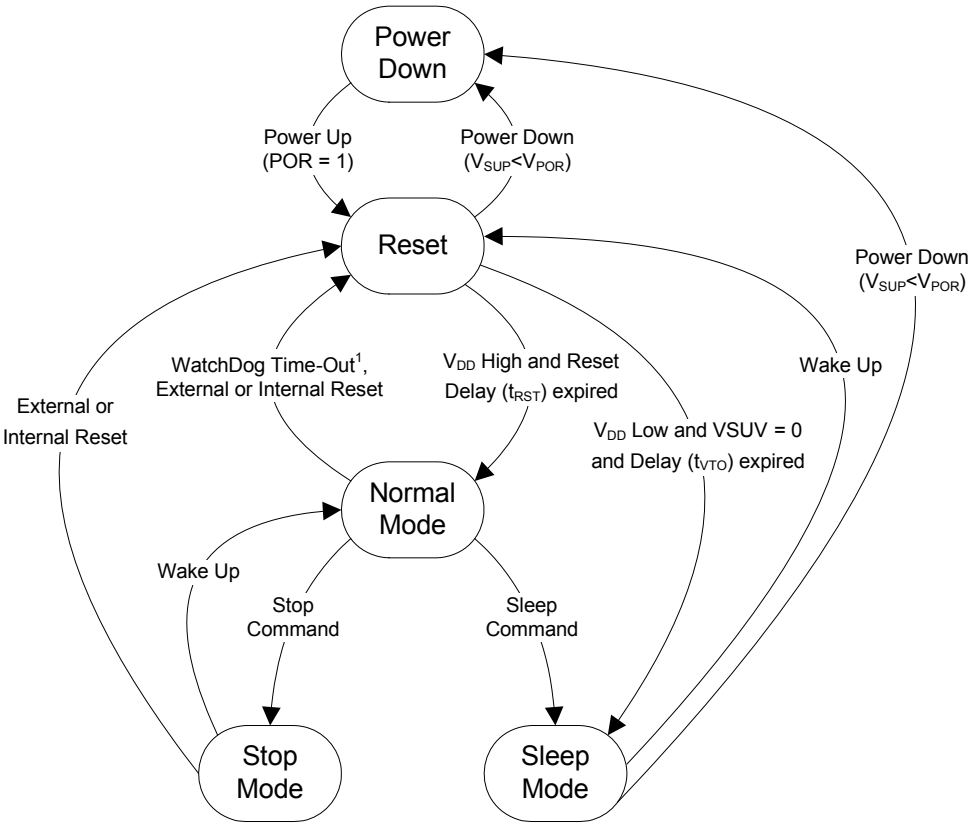
5.4 Modes of Operation

The MM912_634 analog die offers three main operating modes: Normal (Run), Stop, and Sleep. In Normal mode, the device is active and is operating under normal application conditions. In Stop mode, the voltage regulator operates with limited current capability, the external load is expected to be reduced while in Stop mode. In Sleep mode both voltage regulators are turned off (V_{DD} = V_{DDX} = 0 V).

Wake-up from Stop mode is indicated by an interrupt signal. Wake-up from Sleep mode will change the MM912_634 analog die into reset mode while the voltage regulator is turned back on.

The selection of the different modes is controlled by the Mode Control Register (MCR).

Figure 16 describes how transitions are done between the different operating modes.



[1] Initial WD to be served within t_{WDTO} to enable Window WD

Figure 16. Modes of Operation and Transitions

5.4.1 Power Down Mode

For the device power (VS1) below V_{POR}, the MM912_634 analog die is virtually in Power Down mode. Once VS1>VPOR, the MM912_634 analog die will enter Reset mode with the condition “Power On Reset - POR”.

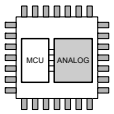
5.4.2 Reset Mode

The MM912_634 analog die enters Reset mode if a reset condition occurs (POR - Power On Reset, LVR- Low Voltage Reset, Low Voltage VDDX Reset - LVRX, WDR - Watchdog Reset, EXR - External Reset, and WUR - Wake-up Sleep Reset).

For internal reset sources, the $\overline{\text{RESET\_A}}$ pin is driven low for tRST after the reset condition is gone. After this delay, the $\overline{\text{RESET\_A}}$ pin is released. With a high detected on the $\overline{\text{RESET\_A}}$ pin, VDD>VLVR and VDDX>VLVRX the MM912_634 analog die enters in Normal mode.

To avoid short-circuit conditions being present for a long time, a tVTO timeout is implemented. Once VDD < VLVR or VDDX < VLVRX with VS1 > (VLVI + VLVI_H) for more than tVTO, the MM912_634 analog die will transit directly to Sleep mode.

5.11 Hall Sensor Supply Output - HSUP



To supply Hall Effect Sensors or similar external loads, the HSUP output is implemented. To reduce power dissipation inside the device, the output is implemented as a switchable Voltage Regulator, internally connected to the VS1 supply input. For protection, an Over-temperature Shutdown and a Current Limitation is implemented. A write to the Hall Supply Register (HSR), when the over-temperature condition is gone, will re-enable the Hall Supply Output.

The HSUP output is active only during Normal mode. A capacitor CHSUP is recommended for operation.

5.11.1 Register Definition

5.11.1.1 Hall Supply Register (HSR)

Table 104. Hall Supply Register (HSR)

Offset[81] 0x38 — Access: User read/write

	7	6	5	4	3	2	1	0
R	HOTIE	HOTC	0	0	0	0	0	HSUPON
W								
Reset	0	0	0	0	0	0	0	0

Note:
81. Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

Table 105. HSR - Register Field Descriptions

Field	Description
7 - HOTIE	Hall Supply Over-temperature Interrupt Enable
6 - HOTC	Hall Supply Over-temperature Condition present. During the event, the Hall Supply is shut down. Reading the register will clear the HOT flag if present. See Section 5.7, “Interrupts" for details.
0 - HSUPON	Hall Supply On: 0 - Hall Supply Regulator disabled 1 - Hall Supply Regulator enabled

5.14.3.1.3 PWM Clock Select (PCLKx)

Each PWM channel has a choice of two clocks to use as the clock source for that channel as described by the following.

NOTE

Register bits PCLK0 and PCLK1 can be written anytime. If a clock select changes while a PWM signal is being generated, a truncated or stretched pulse can occur during the transition.

5.14.3.1.4 PWM Center Align Enable (CAEx)

The CAEx bits select either center aligned outputs or left aligned output for both PWM channels. If the CAEx bit is set to a one, the corresponding PWM output will be center aligned. If the CAEx bit is cleared, the corresponding PWM output will be left aligned. See Section 5.14.4.2.5, “Left Aligned Outputs" and Section 5.14.4.2.6, “Center Aligned Outputs" for a more detailed description of the PWM output modes.

NOTE

Write these bits only when the corresponding channel is disabled.

5.14.3.2 PWM Prescale Clock Select Register (PWMPRCLK)

This register selects the prescale clock source for clocks A and B independently.

Table 121. PWM Prescale Clock Select Register (PWMPRCLK)

Offset(91) 0x61 — Access: User read/write

	7	6	5	4	3	2	1	0
R	0	PCKB2	PCKB1	PCKB0	0	PCKA2	PCKA1	PCKA0
W								
Reset	0	0	0	0	0	0	0	0

Note:
91. Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

Table 122. PWMPRCLK - Register Field Descriptions

Field	Description
6–4 PCKB[2:0]	Prescaler Select for Clock B — Clock B is one of two clock sources which can be used for channel 1. These three bits determine the rate of clock B, as shown in Table 123.
2–0 PCKA[2:0]	Prescaler Select for Clock A — Clock A is one of two clock sources which can be used for channel 0. These three bits determine the rate of clock A, as shown in Table 124.

Table 123. Clock B Prescaler Selects

PCKB2	PCKB1	PCKB0	Value of Clock B
0	0	0	D2D clock
0	0	1	D2D clock / 2
0	1	0	D2D clock / 4
0	1	1	D2D clock / 8
1	0	0	D2D clock / 16
1	0	1	D2D clock / 32
1	1	0	D2D clock / 64
1	1	1	D2D clock / 128

In this way, the output of the PWM will always be either the old waveform or the new waveform, not some variation in between. If the channel is not enabled, then writes to the period and duty registers will go directly to the latches as well as the buffer.

A change in duty or period can be forced into effect “immediately” by writing the new value to the duty and/or period registers, and then writing to the counter. This forces the counter to reset and the new duty and/or period values to be latched. In addition, since the counter is readable, it is possible to know where the count is with respect to the duty value, and software can be used to make adjustments

NOTE

When forcing a new period or duty into effect immediately, an irregular PWM cycle can occur. Depending on the polarity bit, the duty registers will contain the count of either the high time or the low time.

5.14.4.2.4 PWM Timer Counters

Each channel has a dedicated 8-bit up/down counter which runs at the rate of the selected clock source (see Section 5.14.4.1, “PWM Clock Select" for the available clock sources and rates). The counter compares to two registers, a duty register and a period register as shown in Figure 24. When the PWM counter matches the duty register, the output flip-flop changes state, causing the PWM waveform to also change state. A match between the PWM counter and the period register behaves differently depending on what output mode is selected as shown in Figure 24 and described in Section 5.14.4.2.5, “Left Aligned Outputs" and Section 5.14.4.2.6, “Center Aligned Outputs".

Each channel counter can be read at anytime without affecting the count or the operation of the PWM channel.

Any value written to the counter causes the counter to reset to $00, the counter direction to be set to up, the immediate load of both duty and period registers with values from the buffers, and the output to change according to the polarity bit. When the channel is disabled (PWMEx = 0), the counter stops. When a channel becomes enabled (PWMEx = 1), the associated PWM counter continues from the count in the PWMCNTx register. This allows the waveform to continue where it left off when the channel is re-enabled. When the channel is disabled, writing “0” to the period register will cause the counter to reset on the next selected clock.

NOTE

To start a new “clean” PWM waveform without any “history” from the old waveform, writing the channel counter (PWMCNTx) must happen prior to enabling the PWM channel (PWMEx = 1).

Generally, writes to the counter are done prior to enabling a channel in order to start from a known state. However, writing a counter can also be done while the PWM channel is enabled (counting). The effect is similar to writing the counter when the channel is disabled, except that the new period is started immediately with the output set according to the polarity bit.

NOTE

Writing to the counter while the channel is enabled can cause an irregular PWM cycle to occur.

The counter is cleared at the end of the effective period (see Section 5.14.4.2.5, “Left Aligned Outputs" and Section 5.14.4.2.6, “Center Aligned Outputs" for more details).

Table 130. PWM Timer Counter Conditions

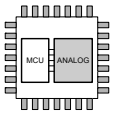
Counter Clears ($00)	Counter Counts	Counter Stops
When PWMCNTx register written to any value	When PWM channel is enabled (PWMEx = 1). Counts from last value in PWMCNTx.	When PWM channel is disabled (PWMEx = 0)
Effective period ends		

5.14.4.2.5 Left Aligned Outputs

The PWM timer provides the choice of two types of outputs, left aligned or center aligned. They are selected with the CAEx bits in the PWMCTL register. If the CAEx bit is cleared (CAEx = 0), the corresponding PWM output will be left aligned.

In left aligned output mode, the 8-bit counter is configured as an up counter only. It compares to two registers, a duty register and a period register as shown in the block diagram in Figure 24. When the PWM counter matches the duty register the output flip-flop changes state causing the PWM waveform to also change state. A match between the PWM counter and the period register resets the counter and the output flip-flop, as shown in Figure 24, as well as performing a load from the double buffer period and duty register to the associated registers, as described in Section 5.14.4.2.3, “PWM Period and Duty". The counter counts from 0 to the value in the period register – 1.

5.15 LIN Physical Layer Interface - LIN



The LIN bus pin provides a physical layer for single-wire communication in automotive applications. The LIN physical layer is designed to meet the LIN physical layer version 2.1 specification, and has the following features:

- LIN physical layer 2.1 compliant
- Slew rate selection 20 kBit, 10 kBit, and fast Mode (100 kBit)
- Over-temperature Shutdown - HTI
- Permanent Pull-up in Normal mode 30 kΩ, 1.0 MΩ in low power
- Current limitation
- External Rx / Tx access. See Section 5.18, “General Purpose I/O - PTB[0…2]"
- Slew Rate Trim Bit. See Section 5.26, “MM912_634 - Analog Die Trimming"

The LIN driver is a Low Side MOSFET with current limitation and thermal shutdown. An internal pull-up resistor with a serial diode structure is integrated, so no external pull-up components are required for the application in a slave node. The fall time from dominant to recessive and the rise time from recessive to dominant is controlled. The symmetry between both slopes is guaranteed.

5.15.1 LIN Pin

The LIN pin offers high susceptibility immunity level from external disturbance, guaranteeing communication during external disturbance. See Section 4.8, “ESD Protection and Latch-up Immunity".

5.15.2 Slew Rate Selection

The slew rate can be selected for optimized operation at 10 kBit/s and 20 kBit/s as well as a fast baud rate (100 kBit) for test and programming. The slew rate can be adapted with the bits LINSR[1:0] in the LIN Register (LINR). The initial slew rate is 20 kBit/s.

5.15.3 Over-temperature Shutdown (LIN Interrupt)

The output Low Side FET (transmitter) is protected against over-temperature conditions. In case of an over-temperature condition, the transmitter will be shut down and the bit LINOTC in the LIN Register (LINR) is set as long as the condition is present.

If the LINOTIE bit is set in the LIN Register (LINR), an Interrupt IRQ will be generated. Acknowledge the interrupt by reading the LIN Register (LINR). To issue a new interrupt, the condition has to vanish and occur again.

The transmitter is automatically re-enabled once the over-temperature condition is gone and TxD is High.

5.15.4 Low Power Mode and Wake-up Feature

During Low Power mode operation the transmitter of the physical layer is disabled. The receiver is still active and able to detect Wake-up events on the LIN bus line.

A dominant level longer than t_{PROPWL} followed by a rising edge, will generate a wake-up event and be reported in the Wake-up Source Register (WSR).

5.15.5 J2602 Compliance

A Low Voltage Shutdown feature was implemented to allow controlled J2602 compliant LIN driver behavior under Low Voltage conditions (LVSD=0).

When an under-voltage occurs on VS1 (LVI), the LIN stays in recessive mode if it was in recessive state. If it was in a dominant state, it waits until the next dominant to recessive transition, then it stays in the recessive state.

When the under-voltage condition (LVI) is gone, the LIN will start operating when Tx is in a recessive state or on the next dominant to recessive transition.

Table 143. SCIS1 Field Descriptions (continued)

Field	Description
4 IDLE	Idle Line Flag — IDLE is set when the SCI receive line becomes idle for a full character time after a period of activity. When ILT = 0, the receiver starts counting idle bit times after the start bit. So if the receive character is all 1s, these bit times and the stop bit time count toward the full character time of logic high (10 or 11 bit times depending on the M control bit) needed for the receiver to detect an idle line. When ILT = 1, the receiver doesn't start counting idle bit times until after the stop bit. So the stop bit and any logic high bit times at the end of the previous character do not count toward the full character time of logic high needed for the receiver to detect an idle line. To clear IDLE, read SCIS1 with IDLE = 1 and then read the SCI data register (SCID). After IDLE has been cleared, it cannot become set again until after a new character has been received and RDRF has been set. IDLE will get set only once even if the receive line remains idle for an extended period. 0 No idle line detected. 1 Idle line was detected.
3 OR	Receiver Overrun Flag — OR is set when a new serial character is ready to be transferred to the receive data register (buffer), but the previously received character has not been read from SCID yet. In this case, the new character (and all associated error information) is lost because there is no room to move it into SCID. To clear OR, read SCIS1 with OR = 1 and then read the SCI data register (SCID). 0 No overrun. 1 Receive overrun (new SCI data lost).
2 NF	Noise Flag — The advanced sampling technique used in the receiver takes seven samples during the start bit and three samples in each data bit and the stop bit. If any of these samples disagrees with the rest of the samples within any bit time in the frame, the flag NF will be set at the same time as the flag RDRF gets set for the character. To clear NF, read SCIS1 and then read the SCI data register (SCID). 0 No noise detected. 1 Noise detected in the received character in SCID.
1 FE	Framing Error Flag — FE is set at the same time as RDRF when the receiver detects a logic 0 where the stop bit was expected. This suggests the receiver was not properly aligned to a character frame. To clear FE, read SCIS1 with FE = 1 and then read the SCI data register (SCID). 0 No framing error detected. This does not guarantee the framing is correct. 1 Framing error.
0 PF	Parity Error Flag — PF is set at the same time as RDRF when parity is enabled (PE = 1) and the parity bit in the received character does not agree with the expected parity value. To clear PF, read SCIS1 and then read the SCI data register (SCID). 0 No parity error. 1 Parity error.

5.16.2.5 SCI Status Register 2 (SCIS2)

This register has one read-only status flag.

Table 144. SCI Status Register 2 (SCIS2)

Offset(104) 0x45 Access: User read/write

	7	6	5	4	3	2	1	0
R	LBKDIF	RXEDGIF	0	RXINV(105)	RWUID	BRK13	LBKDE	RAF
W								
Reset	0	0	0	0	0	0	0	0

Note:
104. Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

5.21 Current Sense Module - ISENSE

The Current Sense Module is implemented to amplify the voltage drop across an external shunt resistor to measure the actual application current using the internal Analog Digital Converter Channel 9. Typical application is the motor current in a window lift control module

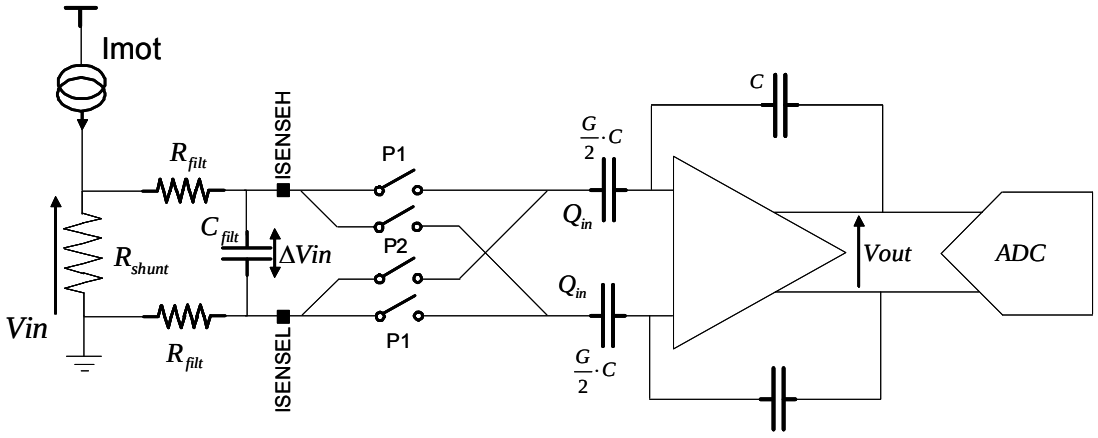


Figure 37. Current Sense Module with External Filter Option

The implementation is based on a switched capacitor solution to eliminate unwanted offset.To fit several application scenarios, eight different GAIN setting are implemented.

5.21.1 Register Definition

5.21.1.1 Current Sense Register (CSR)

Table 210. Current Sense Register (CSR)

Offset[145] 0x3C — Access: User read/write

	7	6	5	4	3	2	1	0
R	CSE	0	0	0	CCD	CSGS		
W								
Reset	0	0	0	0	0	0	0	0

Note:
145. Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

Table 221. CTR3 - Register Field Descriptions

Field	Description
7 OFFCTRE	ADC offset compensation voltage trim enable bit 0 - no trim can be done 1 - trim can be done by setting OFFCTR[2:0] bits
6-4 OFFCTR2…0	ADCOFFC trim - This trim is used to adjust the internal ADC offset compensation voltage 000: 0% 001: +7.98% 010: +15.97% 011: +23.95% 100: -23.95% 101: -15.97% 110: -7.98% 111: 0%
3 CTR3_E	Spare Trim enable bit
2 CTR3_2	Spare Trim bit 2
1 CTR3_1	Spare Trim bit 1
0 CTR3_0	Spare Trim bit 0

Table 250. MODE Field Descriptions

Field	Description
7 MODC	Mode Select Bit — This bit controls the current operating mode during RESET high (inactive). The external mode pin MODC determines the operating mode during $\overline{\text{RESET}}$ low (active). The state of the pin is registered into the respective register bit after the $\overline{\text{RESET}}$ signal goes inactive (see Figure 45). Write restrictions exist to disallow transitions between certain modes. Figure 45 illustrates all allowed mode changes. Attempting non authorized transitions will not change the MODE bit, but it will block further writes to the register bit except in special modes. Write accesses to the MODE register are blocked when the device is secured.

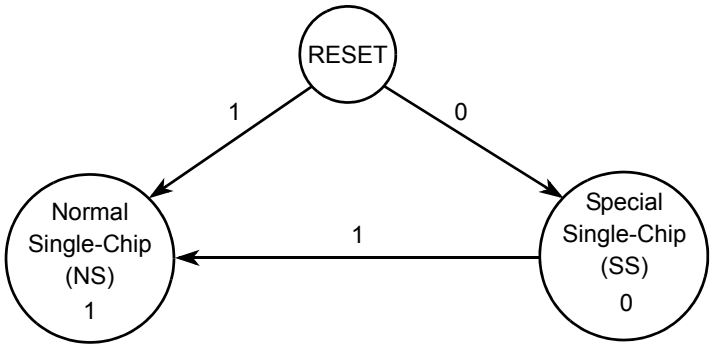


Figure 45. Mode Transition Diagram When MCU is Unsecured

5.29.3.2.2 Direct Page Register (DIRECT)

Table 251. Direct Register (DIRECT)

Address: 0x0011

	7	6	5	4	3	2	1	0
R W	DP15	DP14	DP13	DP12	DP11	DP10	DP9	DP8
Reset	0	0	0	0	0	0	0	0

Read: Anytime

Write: anytime in special SS, write-one in NS.

This register determines the position of the 256 Byte direct page within the memory map.It is valid for both global and local mapping scheme.

Table 252. DIRECT Field Descriptions

Field	Description
7–0 DP[15:8]	Direct Page Index Bits 15–8 — These bits are used by the CPU when performing accesses using the direct addressing mode. These register bits form bits [15:8] of the local address (see Figure 46).

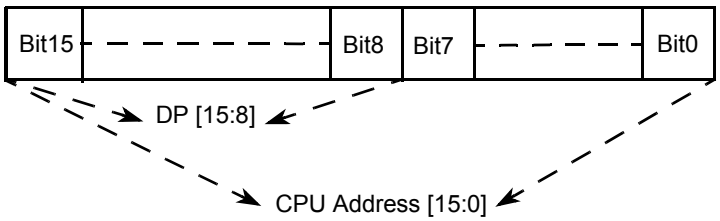


Figure 46. DIRECT Address Mapping

Table 254. PPAGE Field Descriptions

Field	Description
3–0 PIX[3:0]	Program Page Index Bits 3–0 — These page index bits are used to select which of the 256 P-Flash or ROM array pages is to be accessed in the Program Page Window.

The fixed 16 kB page from 0x0000 to 0x3FFF is the page number 0x0C. Parts of this page are covered by Registers, D-Flash and RAM space. See SoC Guide for details.

The fixed 16 kB page from 0x4000–0x7FFF is the page number 0x0D.

The reset value of 0x0E ensures that there is linear Flash space available between addresses 0x0000 and 0xFFFF out of reset.

The fixed 16 kB page from 0xC000-0xFFFF is the page number 0x0F.

5.29.4 Functional Description

The S12PMMC block performs several basic functions of the S12I sub-system operation: MCU operation modes, priority control, address mapping, select signal generation and access limitations for the system. Each aspect is described in the following subsections.

5.29.4.1 MCU Operating Modes

- Normal single chip mode
  This is the operation mode for running application code. There is no external bus in this mode.
- Special single chip mode
  This mode is generally used for debugging operation, boot-strapping or security related operations. The active background debug mode is in control of the CPU code execution and the BDM firmware is waiting for serial commands sent through the BKGD pin.

5.29.4.2 Memory Map Scheme

5.29.4.2.1 CPU and BDM Memory Map Scheme

The BDM firmware lookup tables and BDM register memory locations share addresses with other modules; however they are not visible in the memory map during user's code execution. The BDM memory resources are enabled only during the READ_BD and WRITE_BD access cycles to distinguish between accesses to the BDM memory area and accesses to the other modules. (Refer to BDM Block Guide for further details).

When the MCU enters active BDM mode, the BDM firmware lookup tables and the BDM registers become visible in the local memory map in the range 0xFF00-0xFFFF (global address 0x3_FF00 - 0x3_FFFF) and the CPU begins execution of firmware commands or the BDM begins execution of hardware commands. The resources which share memory space with the BDM module will not be visible in the memory map during active BDM mode.

Please note that after the MCU enters active BDM mode the BDM firmware lookup tables and the BDM registers will also be visible between addresses 0xBF00 and 0xBFFF if the PPAGE register contains value of 0x0F.

5.29.4.2.1.1 Expansion of the Local Address Map

Expansion of the CPU Local Address Map

The program page index register in S12PMMC allows accessing up to 256 kB of P-Flash in the global memory map by using the four index bits (PPAGE[3:0]) to page 16x16 kB blocks into the program page window located from address 0x8000 to address 0xBFFF in the local CPU memory map.

The page value for the program page window is stored in the PPAGE register. The value of the PPAGE register can be read or written by normal memory accesses as well as by the CALL and RTC instructions (see Section 5.29.6.1, "CALL and RTC Instructions").

Control registers, vector space and parts of the on-chip memories are located in unpaged portions of the 64 kB local CPU address space.

The starting address of an interrupt service routine must be located in unpaged memory unless the user is certain that the PPAGE register will be set to the appropriate value when the service routine is called. However an interrupt service routine can call other routines that are in paged memory. The upper 16 kB block of the local CPU memory space (0xC000–0xFFFF) is unpaged. It is

- Four trace modes
  - Normal: change of flow (COF) PC information is stored (see Section 5.32.4.5.2.1, “Normal Mode") for change of flow definition.
  - Loop1: same as Normal but inhibits consecutive duplicate source address entries
  - Detail: address and data for all cycles except free cycles and opcode fetches are stored
  - Compressed Pure PC: all program counter addresses are stored
- 4-stage state sequencer for trace buffer control
  - Tracing session trigger linked to Final State of state sequencer
  - Begin and End alignment of tracing to trigger

5.32.1.4 Modes of Operation

The DBG module can be used in all MCU functional modes.

During BDM hardware accesses and whilst the BDM module is active, CPU monitoring is disabled. When the CPU enters active BDM Mode through a BACKGROUND command, the DBG module, if already armed, remains armed.

The DBG module tracing is disabled if the MCU is secure, however, breakpoints can still be generated

Table 269. Mode Dependent Restriction Summary

BDM Enable	BDM Active	MCU Secure	Comparator Matches Enabled	Breakpoints Possible	Tagging Possible	Tracing Possible
x	x	1	Yes	Yes	Yes	No
0	0	0	Yes	Only SWI	Yes	Yes
0	1	0	Active BDM not possible when not enabled			
1	0	0	Yes	Yes	Yes	Yes
1	1	0	No	No	No	No

5.32.1.5 Block Diagram

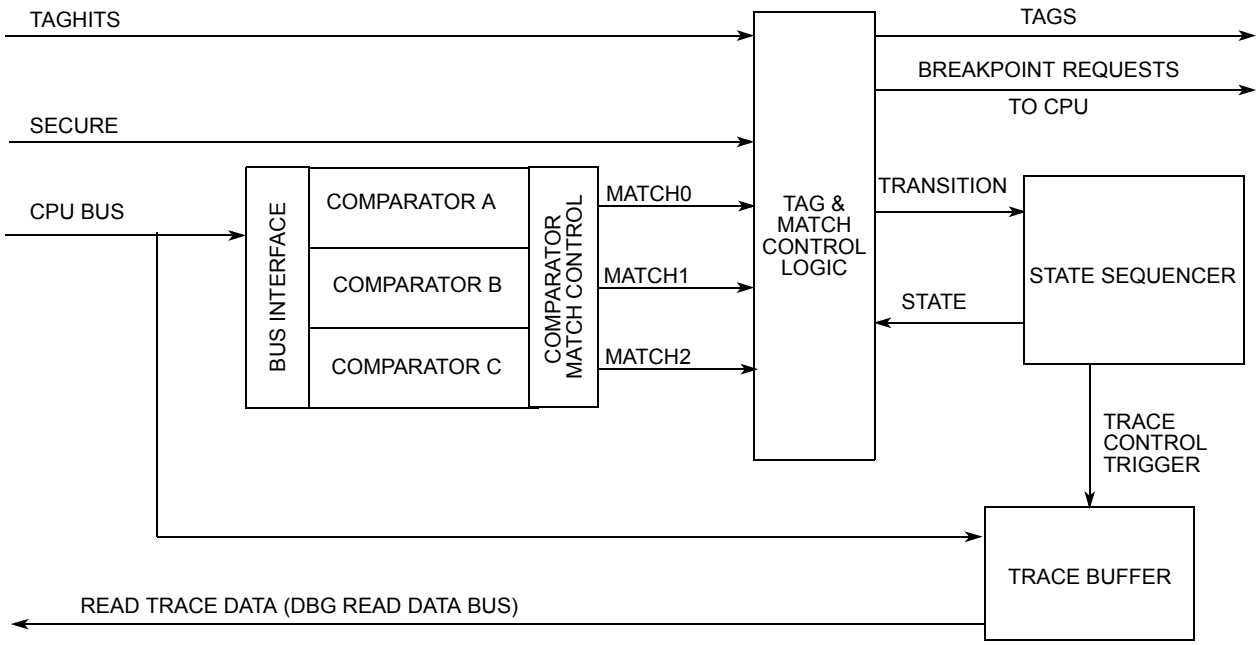


Figure 62. Debug Module Block Diagram

Table 299. Comparator Register Layout

0x0028	CONTROL	Read/Write	Comparators A,B and C
0x0029	ADDRESS HIGH	Read/Write	Comparators A,B and C
0x002A	ADDRESS MEDIUM	Read/Write	Comparators A,B and C
0x002B	ADDRESS LOW	Read/Write	Comparators A,B and C
0x002C	DATA HIGH COMPARATOR	Read/Write	Comparator A only
0x002D	DATA LOW COMPARATOR	Read/Write	Comparator A only
0x002E	DATA HIGH MASK	Read/Write	Comparator A only
0x002F	DATA LOW MASK	Read/Write	Comparator A only

5.32.3.2.8.1 Debug Comparator Control Register (DBGXCTL)

The contents of this register bits 7 and 6 differ depending upon which comparator registers are visible in the 8-byte window of the DBG module register address map.

Table 300. Debug Comparator Control Register DBGACTL (Comparator A)

Address: 0x0028

	7	6	5	4	3	2	1	0
R W	SZE	SZ	TAG	BRK	RW	RWE	NDB	COMPE
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Table 301. Debug Comparator Control Register DBGBCTL (Comparator B)

Address: 0x0028

	7	6	5	4	3	2	1	0
R W	SZE	SZ	TAG	BRK	RW	RWE	0	COMPE
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Table 302. Debug Comparator Control Register DBGCCTL (Comparator C)

Address: 0x0028

	7	6	5	4	3	2	1	0
R W	0	0	TAG	BRK	RW	RWE	0	COMPE
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Read: DBGACTL if COMRV[1:0] = 00
DBGBCTL if COMRV[1:0] = 01
DBGCCTL if COMRV[1:0] = 10

Write: DBGACTL if COMRV[1:0] = 00 and DBG not armed
DBGBCTL if COMRV[1:0] = 01 and DBG not armed
DBGCCTL if COMRV[1:0] = 10 and DBG not armed

A match can initiate a transition to another state sequencer state (see Section 5.32.4.4, “State Sequence Control"). The comparator control register also allows the type of access to be included in the comparison through the use of the RWE, RW, SZE, and SZ bits. The RWE bit controls whether read or write comparison is enabled for the associated comparator and the RW bit selects either a read or write access for a valid match. Similarly the SZE and SZ bits allow the size of access (word or byte) to be considered in the compare. Only comparators A and B feature SZE and SZ.

The TAG bit in each comparator control register is used to determine the match condition. By setting TAG, the comparator qualifies a match with the output of opcode tracking logic and a state sequencer transition occurs when the tagged instruction reaches the CPU execution stage. Whilst tagging the RW, RWE, SZE, and SZ bits and the comparator data registers are ignored; the comparator address register must be loaded with the exact opcode address.

If the TAG bit is clear (forced type match) a comparator match is generated when the selected address appears on the system address bus. If the selected address is an opcode address, the match is generated when the opcode is fetched from the memory, which precedes the instruction execution by an indefinite number of cycles due to instruction pipelining. For a comparator match of an opcode at an odd address when TAG = 0, the corresponding even address must be contained in the comparator register. Thus for an opcode at odd address (n), the comparator register must contain address (n–1).

Once a successful comparator match has occurred, the condition that caused the original match is not verified again on subsequent matches. Thus if a particular data value is verified at a given address, this address may not still contain that data value when a subsequent match occurs.

Match[0, 1, 2] map directly to Comparators [A, B, C] respectively, except in range modes (see Section 5.32.3.2.4, “Debug Control Register2 (DBGC2)"). Comparator channel priority rules are described in the priority section (Section 5.32.4.3.4, “Channel Priorities").

5.32.4.2.1 Single Address Comparator Match

With range comparisons disabled, the match condition is an exact equivalence of address bus with the value stored in the comparator address registers. Further qualification of the type of access (R/W, word/byte) and data bus contents is possible, depending on comparator channel.

5.32.4.2.1.1 Comparator C

Comparator C offers only address and direction (R/W) comparison. The exact address is compared, thus with the comparator address register loaded with address (n) a word access of address (n–1) also accesses (n) but does not cause a match.

Table 320. Comparator C Access Considerations

Condition For Valid Match	Comp C Address	RWE	RW	Examples
Read and write accesses of ADDR[n]	ADDR[n](189)	0	X	LDAA ADDR[n] STAA #$BYTE ADDR[n]
Write accesses of ADDR[n]	ADDR[n]	1	0	STAA #$BYTE ADDR[n]
Read accesses of ADDR[n]	ADDR[n]	1	1	LDAA #$BYTE ADDR[n]

Note:
189. A word access of ADDR[n-1] also accesses ADDR[n] but does not generate a match. The comparator address register must contain the exact address from the code.

5.32.4.2.1.2 Comparator B

Comparator B offers address, direction (R/W) and access size (word/byte) comparison. If the SZE bit is set the access size (word or byte) is compared with the SZ bit value such that only the specified size of access causes a match. Thus if configured for a byte access of a particular address, a word access covering the same address does not lead to match.

Assuming the access direction is not qualified (RWE=0), for simplicity, the size access considerations are shown in Table 321.

It is possible to set both TRIG and ARM simultaneously to generate an immediate trigger, independent of the current state of ARM.

5.32.4.3.4 Channel Priorities

In case of simultaneous matches the priority is resolved according to Table 324. The lower priority is suppressed. It is thus possible to miss a lower priority match if it occurs simultaneously with a higher priority. The priorities described in Table 324 dictate that in the case of simultaneous matches, the match pointing to final state has highest priority followed by the lower channel number (0,1,2).

Table 324. Channel Priorities

Priority	Source	Action
Highest	TRIG	Enter Final State
	Channel pointing to Final State	Transition to next state as defined by state control registers
	Match0 (force or tag hit)	Transition to next state as defined by state control registers
	Match1 (force or tag hit)	Transition to next state as defined by state control registers
Lowest	Match2 (force or tag hit)	Transition to next state as defined by state control registers

5.32.4.4 State Sequence Control

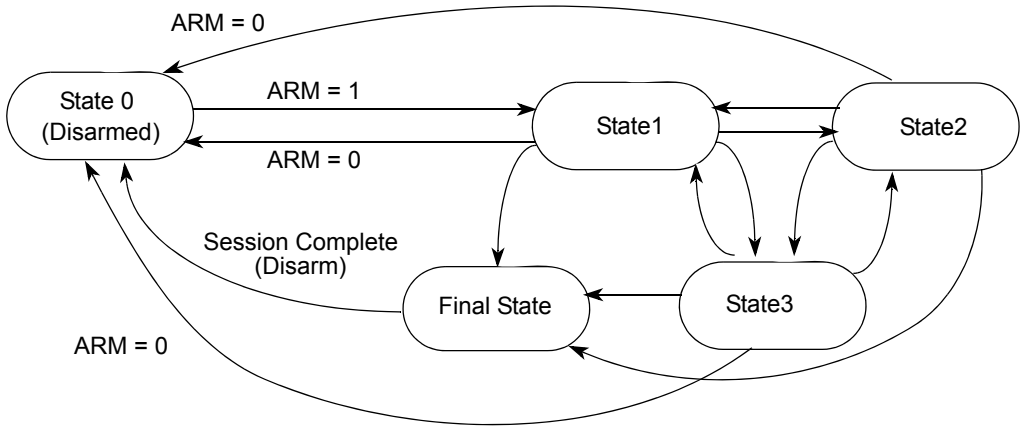


Figure 64. State Sequencer Diagram

The state sequencer allows a defined sequence of events to provide a trigger point for tracing of data in the trace buffer. Once the DBG module has been armed by setting the ARM bit in the DBGC1 register, then state1 of the state sequencer is entered. Further transitions between the states are then controlled by the state control registers and channel matches. From Final State the only permitted transition is back to the disarmed state0. Transition between any of the states 1 to 3 is not restricted. Each transition updates the SSF[2:0] flags in DBGSR accordingly to indicate the current state.

Alternatively writing to the TRIG bit in DBGSC1, provides an immediate trigger independent of comparator matches.

Independent of the state sequencer, each comparator channel can be individually configured to generate an immediate breakpoint when a match occurs through the use of the BRK bits in the DBGxCTL registers. Thus it is possible to generate an immediate breakpoint on selected channels, whilst a state sequencer transition can be initiated by a match on other channels. If a debug session is ended by a match on a channel the state sequencer transitions through Final State for a clock cycle to state0. This is independent of tracing and breakpoint activity, thus with tracing and breakpoints disabled, the state sequencer enters state0 and the debug module is disarmed.

5.32.4.4.1 Final State

On entering Final State a trigger may be issued to the trace buffer according to the trace alignment control as defined by the TALIGN bit (see Section 5.32.3.2.3, “Debug Trace Control Register (DBGTCR)"). If the TSOURCE bit in DBGTCR is clear then the trace buffer is disabled and the transition to Final State can only generate a breakpoint request. In this case or upon completion of a tracing session when tracing is enabled, the ARM bit in the DBGC1 register is cleared, returning the module to

Table 349. CPMUCLKS Descriptions

Field	Description
7 PLLSEL	**PLL Select Bit** This bit selects the PLLCLK as source of the System Clocks (Core Clock and Bus Clock). PLLSEL can only be set to 0, if UPOSC=1. UPOSC= 0 sets the PLLSEL bit. Entering Full Stop Mode sets the PLLSEL bit. 0 System clocks are derived from OSCCLK if oscillator is up (UPOSC=1, $f_{BUS} = f_{OSC} / 2$. 1 System clocks are derived from PLLCLK, $f_{BUS} = f_{PLL} / 2$.
6 PSTP	**Pseudo Stop Bit** This bit controls the functionality of the oscillator during Stop Mode. 0 Oscillator is disabled in Stop Mode (Full Stop Mode). 1 Oscillator continues to run in Stop Mode (Pseudo Stop Mode), option to run RTI and COP. Note: Pseudo Stop Mode allows for faster STOP recovery and reduces the mechanical stress and aging of the resonator in case of frequent STOP conditions at the expense of a slightly increased power consumption. Note: When starting up the external oscillator (either by programming OSCE bit to 1 or on exit from Full Stop Mode with OSCE bit is already 1) the software must wait for a minimum time equivalent to the startup-time of the external oscillator t_{UPOSC} before entering Pseudo Stop Mode.
3 PRE	**RTI Enable During Pseudo Stop Bit** — PRE enables the RTI during Pseudo Stop Mode. 0 RTI stops running during Pseudo Stop Mode. 1 RTI continues running during Pseudo Stop Mode if RTIOSCSEL=1. Note: If PRE=0 or RTIOSCSEL=0 then the RTI will go static while Stop Mode is active. The RTI counter will not be reset.
2 PCE	**COP Enable During Pseudo Stop Bit** — PCE enables the COP during Pseudo Stop Mode. 0 COP stops running during Pseudo Stop Mode 1 COP continues running during Pseudo Stop Mode if COPOSCSEL=1 Note: If PCE=0 or COPOSCSEL=0 then the COP will go static while Stop Mode is active. The COP counter will not be reset.
1 RTIOSCSEL	**RTI Clock Select** — RTIOSCSEL selects the clock source to the RTI. Either IRCCLK or OSCCLK. Changing the RTIOSCSEL bit re-starts the RTI timeout period. RTIOSCSEL can only be set to 1, if UPOSC=1. UPOSC= 0 clears the RTIOSCSEL bit. 0 RTI clock source is IRCCLK. 1 RTI clock source is OSCCLK.
0 COPOSCSEL	**COP Clock Select** — COPOSCSEL selects the clock source to the COP. Either IRCCLK or OSCCLK. Changing the COPOSCSEL bit re-starts the COP timeout period. COPOSCSEL can only be set to 1, if UPOSC=1. UPOSC= 0 clears the COPOSCSEL bit. 0 COP clock source is IRCCLK. 1 COP clock source is OSCCLK

5.38.3.2.7 S12CPMU PLL Control Register (CPMUPLL)

This register controls the PLL functionality.

Table 350. S12CPMU PLL Control Register (CPMUPLL)

0x003A

	7	6	5	4	3	2	1	0
R	0	0	FM1	FM0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

Read: Anytime

Write: Anytime if PROT=0 (CPMUPROT register) and PLLSEL=1 (CPMUCLKS register). Else write has no effect.

Table 370. CPMUAPICTL Field Descriptions

Field	Description
7 APICLK	**Autonomous Periodical Interrupt Clock Select Bit** — Selects the clock source for the API. Writable only if APIFE = 0. APICLK cannot be changed if APIFE is set by the same write operation. 0 Autonomous periodical interrupt clock used as source. 1 Bus Clock used as source.
4 APIES	**Autonomous Periodical Interrupt External Select Bit** — Selects the waveform at the external pin API_EXTCLK as shown in Figure . See device level specification for connectivity of API_EXTCLK pin. 0 If APIEA and APIFE are set, at the external pin API_EXTCLK periodic high pulses are visible at the end of every selected period with the size of half of the minimum period (APIR=0x0000 in Table 377). 1 If APIEA and APIFE are set, at the external pin API_EXTCLK a clock is visible with 2 times the selected API Period.
3 APIEA	**Autonomous Periodical Interrupt External Access Enable Bit** — If set, the waveform selected by bit APIES can be accessed externally. See device level specification for connectivity. 0 Waveform selected by APIES can not be accessed externally. 1 Waveform selected by APIES can be accessed externally, if APIFE is set.
2 APIFE	**Autonomous Periodical Interrupt Feature Enable Bit** — Enables the API feature and starts the API timer when set. 0 Autonomous periodical interrupt is disabled. 1 Autonomous periodical interrupt is enabled and timer starts running.
1 APIE	Autonomous Periodical Interrupt Enable Bit 0 API interrupt request is disabled. 1 API interrupt will be requested whenever APIF is set.
0 APIF	**Autonomous Periodical Interrupt Flag** — APIF is set to 1 when the in the API configured time has elapsed. This flag can only be cleared by writing a 1. Writing a 0 has no effect. If enabled (APIE = 1), APIF causes an interrupt request. 0 API time-out has not yet occurred. 1 API time-out has occurred.

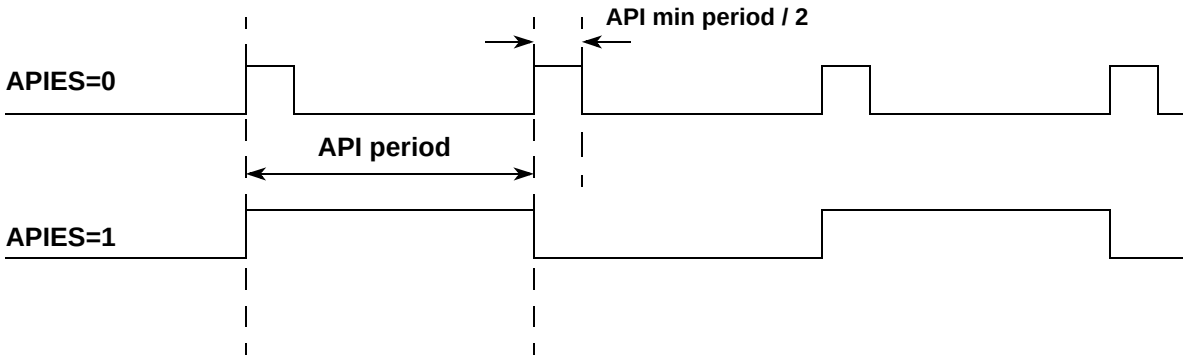


Figure 84. Waveform selected on API_EXTCLK pin (APIEA=1, APIFE=1)

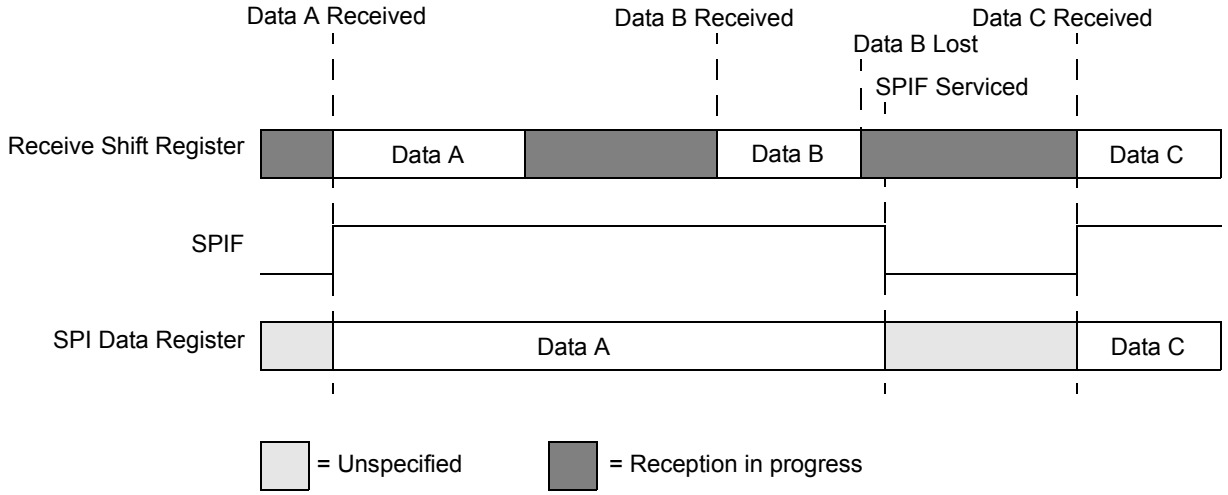


Figure 98. Reception with SPIF Serviced Too Late

5.39.4 Functional Description

The SPI module allows a duplex, synchronous, serial communication between the MCU and peripheral devices. Software can poll the SPI status flags or SPI operation can be interrupt driven.

The SPI system is enabled by setting the SPI enable (SPE) bit in SPI control register 1. While SPE is set, the four associated SPI port pins are dedicated to the SPI function as:

- Slave select ($\overline{SS}$)
- Serial clock (SCK)
- Master out/slave in (MOSI)
- Master in/slave out (MISO)

The main element of the SPI system is the SPI data register. The n-bit(208) data register in the master and the n-bit(208) data register in the slave are linked by the MOSI and MISO pins to form a distributed 2n-bit(208) register. When a data transfer operation is performed, this 2n-bit(208) register is serially shifted n(208) bit positions by the S-clock from the master, so data is exchanged between the master and the slave. Data written to the master SPI data register becomes the output data for the slave, and data read from the master SPI data register after a transfer operation is the input data from the slave.

A read of SPISR with SPTEF = 1 followed by a write to SPIDR puts data into the transmit data register. When a transfer is complete and SPIF is cleared, received data is moved into the receive data register. This data register acts as the SPI receive data register for reads and as the SPI transmit data register for writes. A common SPI data register address is shared for reading data from the read data buffer and for writing data to the transmit data register.

The clock phase control bit (CPHA) and a clock polarity control bit (CPOL) in the SPI control register 1 (SPICR1) select one of four possible clock formats to be used by the SPI system. The CPOL bit simply selects a non-inverted or inverted clock. The CPHA bit is used to accommodate two fundamentally different protocols by sampling data on odd numbered SCK edges or on even numbered SCK edges (see Section 5.39.4.3, “Transmission Formats").

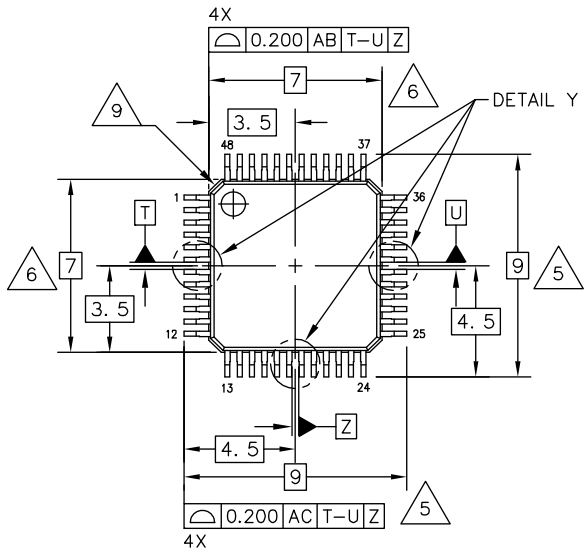
The SPI can be configured to operate as a master or as a slave. When the MSTR bit in SPI control register1 is set, master mode is selected, when the MSTR bit is clear, slave mode is selected.

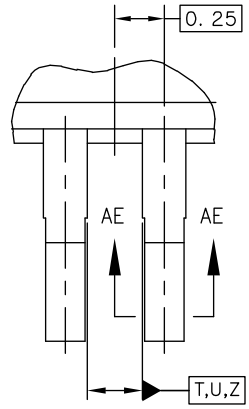
Note:

208. n depends on the selected transfer width, refer to Section 5.39.3.2.2, “SPI Control Register 2 (SPICR2)"

NOTE

A change of CPOL or MSTR bit while there is a received byte pending in the receive shift register will destroy the received byte and must be avoided.





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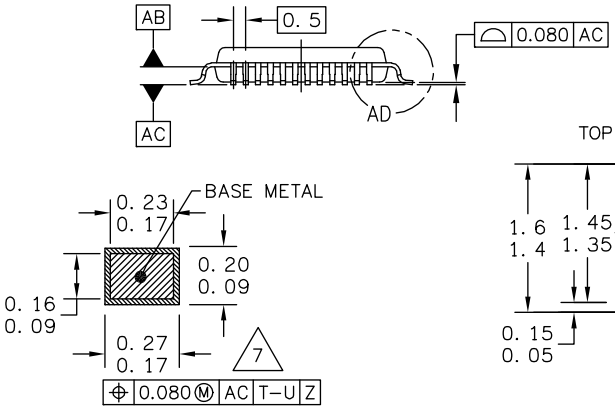
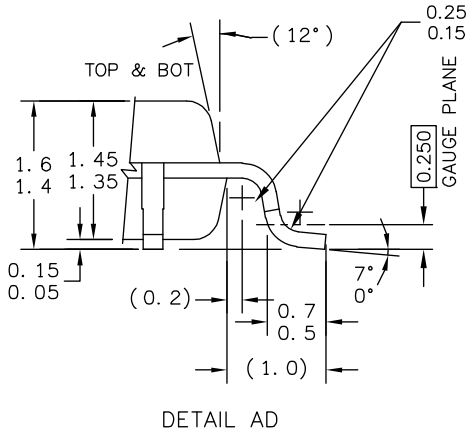


SECTION AE–AE



DETAIL AD

© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: LQFP, 48 LEAD, 0.50 PITCH (7.0 X 7.0 X 1.4)	DOCUMENT NO: 98ASH00962A	REV: G
	CASE NUMBER: 932-03	14 APR 2005
	STANDARD: JEDEC MS-026-BBC	

AP SUFFIX
48-PIN
98ASH00962A
REVISION G