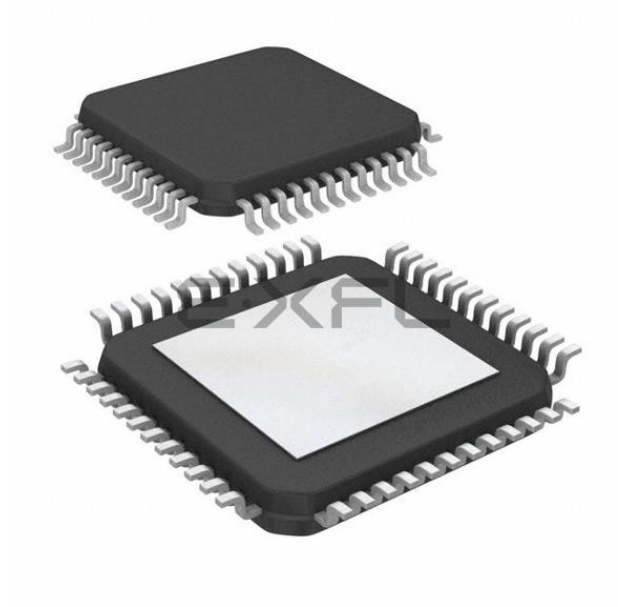

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Application-specific microcontrollers are engineered to

Details	
Product Status	Active
Applications	Automotive
Core Processor	S12
Program Memory Type	FLASH (64kB)
Controller Series	HCS12
RAM Size	6K x 8
Interface	LIN, SCI
Number of I/O	9
Voltage - Supply	2.25V ~ 5.5V
Operating Temperature	-40°C ~ 105°C
Mounting Type	Surface Mount
Package / Case	48-LQFP Exposed Pad
Supplier Device Package	48-HLQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mm912h634dm1aer2

Assuming that no non-blank location is found, then the time to erase verify a D-Flash block is given by:

$$t_{dcheck} = 2800 \cdot \frac{1}{f_{NVMBUS}}$$

4.6.2.1.1.3 Erase Verify P-Flash Section (FCMD=0x03)

The maximum time to erase verify a section of P-Flash depends on the number of phrases being verified (N_{VP}) and is given by:

$$t \approx (450 + N_{VP}) \cdot \frac{1}{f_{NVMBUS}}$$

4.6.2.1.1.4 Read Once (FCMD=0x04)

The maximum read once time is given by:

$$t = 400 \cdot \frac{1}{f_{NVMBUS}}$$

4.6.2.1.1.5 Program P-Flash (FCMD=0x06)

The programming time for a single phrase of four P-Flash words and the two seven-bit ECC fields is dependent on the bus frequency, f_{NVMBUS}, as well as on the NVM operating frequency, f_{NVMOP}.

The typical phrase programming time is given by:

$$t_{ppgm} \approx 164 \cdot \frac{1}{f_{NVMOP}} + 2000 \cdot \frac{1}{f_{NVMBUS}}$$

The maximum phrase programming time is given by:

$$t_{ppgm} \approx 164 \cdot \frac{1}{f_{NVMOP}} + 2500 \cdot \frac{1}{f_{NVMBUS}}$$

4.6.2.1.1.6 Program Once (FCMD=0x07)

The maximum time required to program a P-Flash Program Once field is given by:

$$t \approx 164 \cdot \frac{1}{f_{NVMOP}} + 2150 \cdot \frac{1}{f_{NVMBUS}}$$

4.6.2.1.1.7 Erase All Blocks (FCMD=0x08)

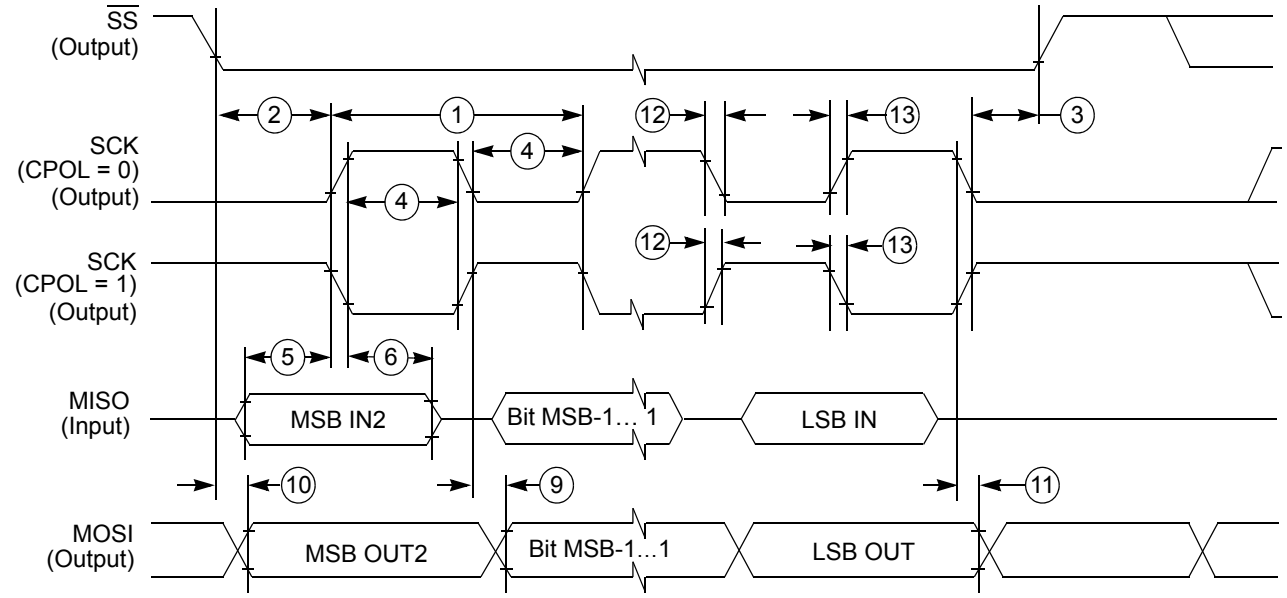
The time required to erase all blocks is given by:

$$t_{mass} \approx 100100 \cdot \frac{1}{f_{NVMOP}} + 38000 \cdot \frac{1}{f_{NVMBUS}}$$

4.6.2.1.1.8 Erase P-Flash Block (FCMD=0x09)

The time required to erase the P-Flash block is given by:

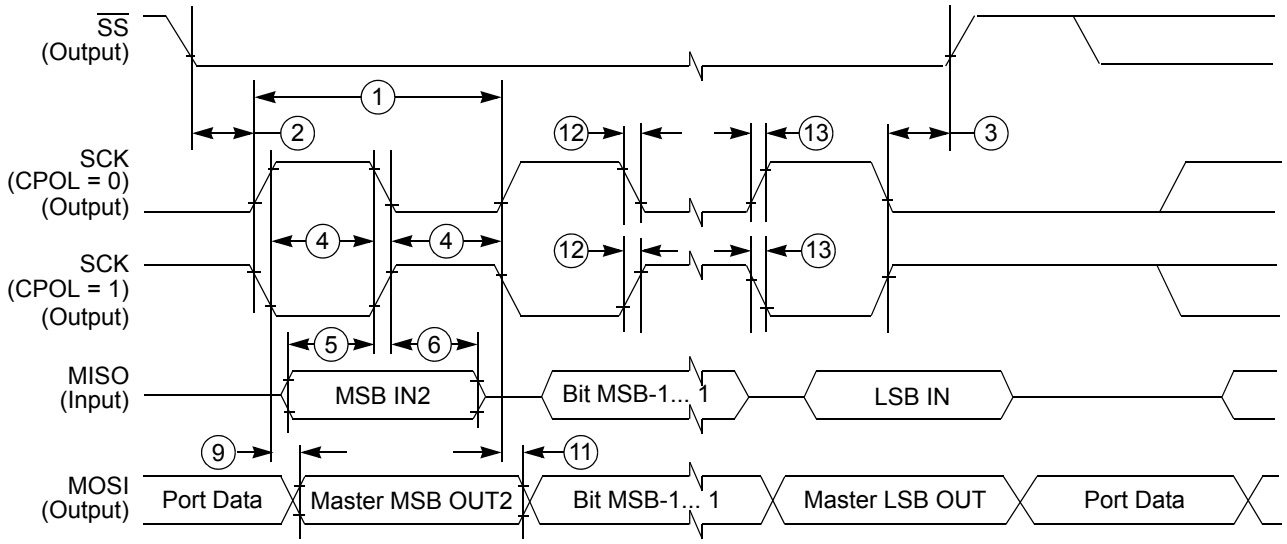
$$t_{pmass} \approx 100100 \cdot \frac{1}{f_{NVMOP}} + 35000 \cdot \frac{1}{f_{NVMBUS}}$$



1. If configured as an output.
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, bit 2... MSB.

Figure 12. SPI Master Timing (CPHA = 0)

In Figure 13 the timing diagram for master mode with transmission format CPHA=1 is depicted.



1.If configured as output
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1,bit 2... MSB.

Figure 13. SPI Master Timing (CPHA = 1)

In Table 46 the timing characteristics for master mode are listed.

5.3.3.2.2 Register Considerations

The Lx - Bit for the not available Lx input in the Lx Status Register must be ignored.

Offset	Name		7	6	5	4	3	2	1	0
0x08	LXR	R	0	0	L5	L4	L3	L2	L1	L0
	Lx Status Register	W								

The Lx Control register for the not available Lx input must be written 0.

0x09	LXCR	R	0	0	L5DS	L4DS	L3DS	L2DS	L1DS	L0DS
	Lx Control Register	W								

A not available Lx input can not be selected as Wake-up Source and must have its LxWE bit set to 0.

0x12	WCR	R	CSSEL		L5WE	L4WE	L3WE	L2WE	L1WE	L0WE
	Wake Up Control Register	W								

The Wake-up Source Register for not available Lx inputs must be ignored.

0x14	WSR	R	FWU	LINWU	L5WU	L4WU	L3WU	L2WU	L1WU	L0WU
	Wake Up Source Register	W								

The Conversion Control Register for the not available Lx analog input (3…8) must always be written 0.

0x82	ACCR (hi)	R	CH15	CH14	0	CH12	CH11	CH10	CH9	CH8
	ADC Conversion Ctrl Reg	W								
0x83	ACCR (lo)	R	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
	ADC Conversion Ctrl Reg	W								

The Conversion Complete Register for the not available Lx analog input (3.8) must be ignored.

0x84	ACCSR (hi)	R	CC15	CC14	0	CC12	CC11	CC10	CC9	CC8
	ADC Conv Complete Reg	W								
0x85	ACCSR (lo)	R	CC7	CC6	CC5	CC4	CC3	CC2	CC1	CC0
	ADC Conv Complete Reg	W								

The ADC Data Result Register for the not available Lx analog input (3.8) must be ignored.

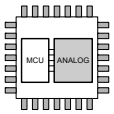
0x8C-0x97	ADRx (hi)	R	adrx 9	adrx 8	adrx 7	adrx 6	adrx 5	adrx 4	adrx 3	adrx 2
	ADC Data Result Register x	W								
	ADRx (lo)	R	adrx 1	adrx 0	0	0	0	0	0	0
	ADC Data Result Register x	W								

5.3.3.2.3 Functional Considerations

For the not available Lx inputs, the following functions are limited:

- No Wake-up feature / Cyclic Sense
- No Digital Input
- No Analog Input and conversion via ADC

5.11 Hall Sensor Supply Output - HSUP



To supply Hall Effect Sensors or similar external loads, the HSUP output is implemented. To reduce power dissipation inside the device, the output is implemented as a switchable Voltage Regulator, internally connected to the VS1 supply input. For protection, an Over-temperature Shutdown and a Current Limitation is implemented. A write to the Hall Supply Register (HSR), when the over-temperature condition is gone, will re-enable the Hall Supply Output.

The HSUP output is active only during Normal mode. A capacitor CHSUP is recommended for operation.

5.11.1 Register Definition

5.11.1.1 Hall Supply Register (HSR)

Table 104. Hall Supply Register (HSR)

Offset[81] 0x38 — Access: User read/write

	7	6	5	4	3	2	1	0
R	HOTIE	HOTC	0	0	0	0	0	HSUPON
W								
Reset	0	0	0	0	0	0	0	0

Note:
81. Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

Table 105. HSR - Register Field Descriptions

Field	Description
7 - HOTIE	Hall Supply Over-temperature Interrupt Enable
6 - HOTC	Hall Supply Over-temperature Condition present. During the event, the Hall Supply is shut down. Reading the register will clear the HOT flag if present. See Section 5.7, “Interrupts" for details.
0 - HSUPON	Hall Supply On: 0 - Hall Supply Regulator disabled 1 - Hall Supply Regulator enabled

Once an over-voltage condition on one of the voltage regulators occurs, the LSx control bits in the Low Side Control Register (LSCR) will be reset to 0. The Voltage Regulator Over-voltage Condition Bit (VROVC) in the Voltage Status Register (VSR) will stay set as long as the condition is present. If the Voltage Regulator Over-voltage Interrupt was enabled (VROVIE=1), the VROV-Interrupt will be issued. Reading the Voltage Regulator Over-voltage Condition Bit (VROVC) in the Voltage Status Register (VSR) will clear the interrupt. To issue another VROV - Interrupt, the condition has to vanish and be present again.

To re-enable the Low Side Drivers after a Voltage Regulator Over-voltage condition occurred, first the LSCEN register has to be written with “0x05” - this information is processed through the main digital blocks, and would secure a minimum functionality before enabling the LS drivers again. In a second step, the LSx Control Bits in the Low Side Control Register (LSCR) must be enabled again after the over-voltage condition has vanished (VROVC=0).

NOTE

The over-voltage threshold has to be trimmed at system power up. Please refer to Section 5.26.1.2.3, “Trimming Register 2 (CTR2)" for details. The default trim is worst case and may have disabled the LS function already. An initial LS enable would be needed.

5.13.4.2 Open Load Detection

Each low side driver signals an OpenLoad condition if the current through the low side is below the OpenLoad current threshold. The OpenLoad condition is indicated with the bits LS1OL and LS2OL in the Low Side Status Register (LSSR). When the low side is in OFF state, the OpenLoad Detection function is not operating. When reading the LSSR register while the low side is operating in PWM and is in the OFF state, the LS1OL and LS2OL bits will not indicate OpenLoad.

5.13.4.3 Current Limitation

Each Low Side driver has a current limitation. In combination with the over-temperature shutdown, the Low Side drivers are protected against over-current and short-circuit failures.

The driver operates in current limitation, and is indicated with the bits LS1CL and LS2CL in the Low Side Status Register (LSSR).

Note: If the drivers is operating in current limitation mode excessive power might be dissipated.

5.13.4.4 Over-temperature Protection (LS Interrupt)

Both Low Side drivers are protected against over-temperature. In case of an over-temperature condition, both Low Side drivers are shut down and the event is latched in the Interrupt Control Module. The shutdown is indicated as LS Interrupt in the Interrupt Source Register (ISR).

If the bit LSM is set in the Interrupt Mask Register (IMR) than an Interrupt (IRQ) is generated.

A write to the Low Side Control Register (LSCR) will re-enable the Low Side drivers when the over-temperature condition is gone.

5.13.5 PWM Capability

See Section 5.14, “PWM Control Module (PWM8B2C)".

5.14 PWM Control Module (PWM8B2C)

5.14.1 Introduction

To control the High Side (HS1, HS2) and the Low Side (LS1, LS2) duty cycle as well as the PTB2 output, the PWM module is implemented. Refer to the individual driver section for details on the use of the internal PWM1 and PWM0 signal (Section 5.12, “High Side Drivers - HS", Section 5.13, “Low Side Drivers - LSx" and Section 5.18, “General Purpose I/O - PTB[0…2]")

The PWM definition is based on the HC12 PWM definitions with some of the simplifications incorporated. The PWM module has two channels with independent controls of left and center aligned outputs on each channel.

Each of the two channels has a programmable period and duty cycle as well as a dedicated counter. A flexible clock select scheme allows a total of four different clock sources to be used with the counters. Each of the modulators can create independent continuous waveforms with software-selectable duty rates from 0% to 100%.

5.14.1.1 Features

The PWM block includes these distinctive features:

- Two independent PWM channels with programmable periods and duty cycles
- Dedicated counter for each PWM channel
- Programmable PWM enable/disable for each channel
- Software selection of PWM duty pulse polarity for each channel
- Period and duty cycle are double buffered. Change takes effect when the end of the effective period is reached (PWM counter reaches zero), or when the channel is disabled
- Programmable center or left aligned outputs on individual channels
- Four clock sources (A, B, SA, and SB) provide for a wide range of frequencies
- Programmable clock select logic

5.14.1.2 Modes of Operation

The PWM8B2C module does operate in Normal mode only.

5.14.1.3 Block Diagram

Figure 22 shows the block diagram for the 8-bit 2-channel PWM block.

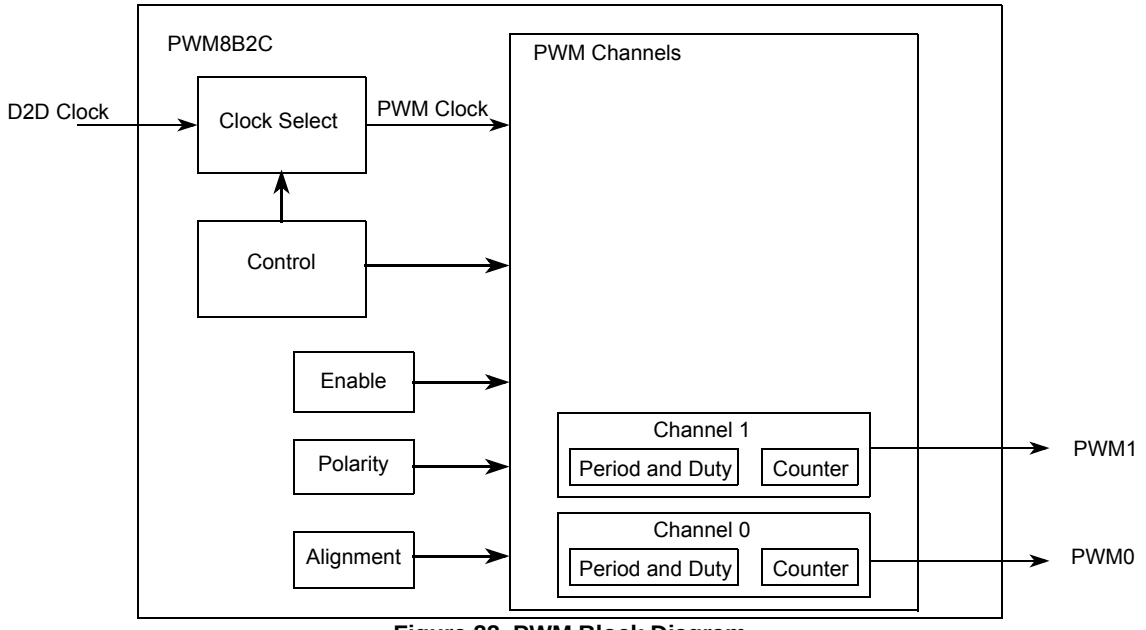


Figure 22. PWM Block Diagram

Table 126. PWM Scale B Register (PWMSCLB)

Offset[93] 0x63 — Access: User read/write

	7	6	5	4	3	2	1	0
R W	Bit 7	6	5	4	3	2	1	Bit 0
Reset	0	0	0	0	0	0	0	0

Note:
93. Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

5.14.3.5 PWM Channel Counter Registers (PWMCNTx)

Each channel has a dedicated 8-bit up/down counter, which runs at the rate of the selected clock source. The counter can be read at any time without affecting the count or the operation of the PWM channel. In left aligned output mode, the counter counts from 0 to the value in the period register - 1. In center aligned output mode, the counter counts from 0 up to the value in the period register and then back down to 0.

Any value written to the counter causes the counter to reset to $00, the counter direction to be set to up, the immediate load of both duty and period registers with values from the buffers, and the output to change according to the polarity bit. The counter is also cleared at the end of the effective period (see Section 5.14.4.2.5, “Left Aligned Outputs" and Section 5.14.4.2.6, “Center Aligned Outputs" for more details). When the channel is disabled (PWMEx = 0), the PWMCNTx register does not count. When a channel becomes enabled (PWMEx = 1), the associated PWM counter starts at the count in the PWMCNTx register. For more detailed information on the operation of the counters, see Section 5.14.4.2.4, “PWM Timer Counters".

NOTE

Writing to the counter while the channel is enabled can cause an irregular PWM cycle to occur.

Table 127. PWM Channel Counter Registers (PWMCNTx)

Offset[94] 0x64/0x65 — Access: User read/write

	7	6	5	4	3	2	1	0
R	Bit 7	6	5	4	3	2	1	Bit 0
W	0	0	0	0	0	0	0	0
Reset	0	0	0	0	0	0	0	0

Note:
94. Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

5.14.3.6 PWM Channel Period Registers (PWMPERx)

There is a dedicated period register for each channel. The value in this register determines the period of the associated PWM channel.

The period registers for each channel are double buffered, so if they change while the channel is enabled, the change will NOT take effect until one of the following occurs:

- The effective period ends
- The counter is written (counter resets to $00)
- The channel is disabled

In this way, the output of the PWM will always be either the old waveform or the new waveform, not some variation in between. If the channel is not enabled, then writes to the period register will go directly to the latches as well as the buffer.

NOTE

Reads of this register return the most recent value written. Reads do not necessarily return the value of the currently active period due to the double buffering scheme.

NOTE

Changing the PWM output mode from left aligned to center aligned output (or vice versa) while channels are operating can cause irregularities in the PWM output. It is recommended to program the output mode before enabling the PWM channel.

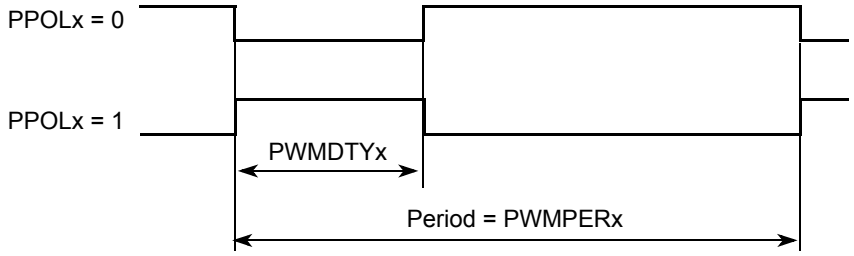


Figure 25. PWM Left Aligned Output Waveform

To calculate the output frequency in left aligned output mode for a particular channel, take the selected clock source frequency for the channel (A, B, SA, or SB), and divide it by the value in the period register for that channel.

- PWMx Frequency = Clock (A, B, SA, or SB) / PWMPERx
- PWMx Duty Cycle (high time as a % of period):
  - Polarity = 0 (PPOLx = 0)
- Duty Cycle = [(PWMPERx-PWMDTYx)/PWMPERx] * 100%
  - Polarity = 1 (PPOLx = 1)

  Duty Cycle = [PWMDTYx / PWMPERx] * 100%

As an example of a left aligned output, consider the following case:

Clock Source = E, where E = 10 kHz (100 µs period)

PPOLx = 0

PWMPERx = 4

PWMDTYx = 1

PWMx Frequency = 10 kHz/4 = 2.5 kHz

PWMx Period = 400 µs

PWMx Duty Cycle = 3/4 *100% = 75%

The output waveform generated is shown in Figure 26.

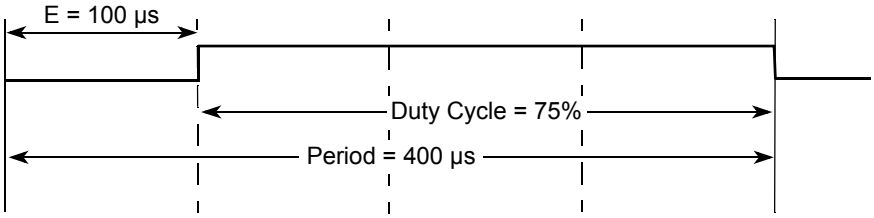


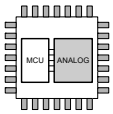
Figure 26. PWM Left Aligned Output Example Waveform

5.14.4.2.6 Center Aligned Outputs

For a center aligned output mode selection, set the CAEx bit (CAEx = 1) in the PWMCTL register, and the corresponding PWM output will be center aligned.

The 8-bit counter operates as an up/down counter in this mode, and is set to up whenever the counter is equal to $00. The counter compares to two registers, a duty register and a period register, as shown in the block diagram in Figure 24. When the PWM counter matches the duty register, the output flip-flop changes state, causing the PWM waveform to also change state. A match between the PWM counter and the period register changes the counter direction from an up-count to a down-count. When the PWM counter decrements and matches the duty register again, the output flip-flop changes state, causing the PWM output to also change state. When the PWM counter decrements and reaches zero, the counter direction changes from a down-count back to an up-count, and a load from the double buffer period and duty registers to the associated registers is performed, as described

5.16 Serial Communication Interface (S08SCIV4)



5.16.1 Introduction

5.16.1.1 Features

Features of the SCI module include:

- Full-duplex, standard non-return-to-zero (NRZ) format
- Double-buffered transmitter and receiver with separate enables
- Programmable baud rates (13-bit modulo divider)
- Interrupt-driven or polled operation:
  - Transmit data register empty and transmission complete
  - Receive data register full
  - Receive overrun, parity error, framing error, and noise error
  - Idle receiver detect
  - Active edge on receive pin
  - Break detect supporting LIN
- Hardware parity generation and checking
- Programmable 8-bit or 9-bit character length
- Receiver wake-up by idle-line or address-mark
- Optional 13-bit break character generation / 11-bit break character detection
- Selectable transmitter output polarity

5.16.1.2 Modes of Operation

See Section 5.16.3, “Functional Description", for details concerning SCI operation in these modes:

- 8 and 9-bit data modes
- Loop mode
- Single-wire mode

5.16.1.3 Block Diagram

Figure 29 shows the transmitter portion of the SCI.

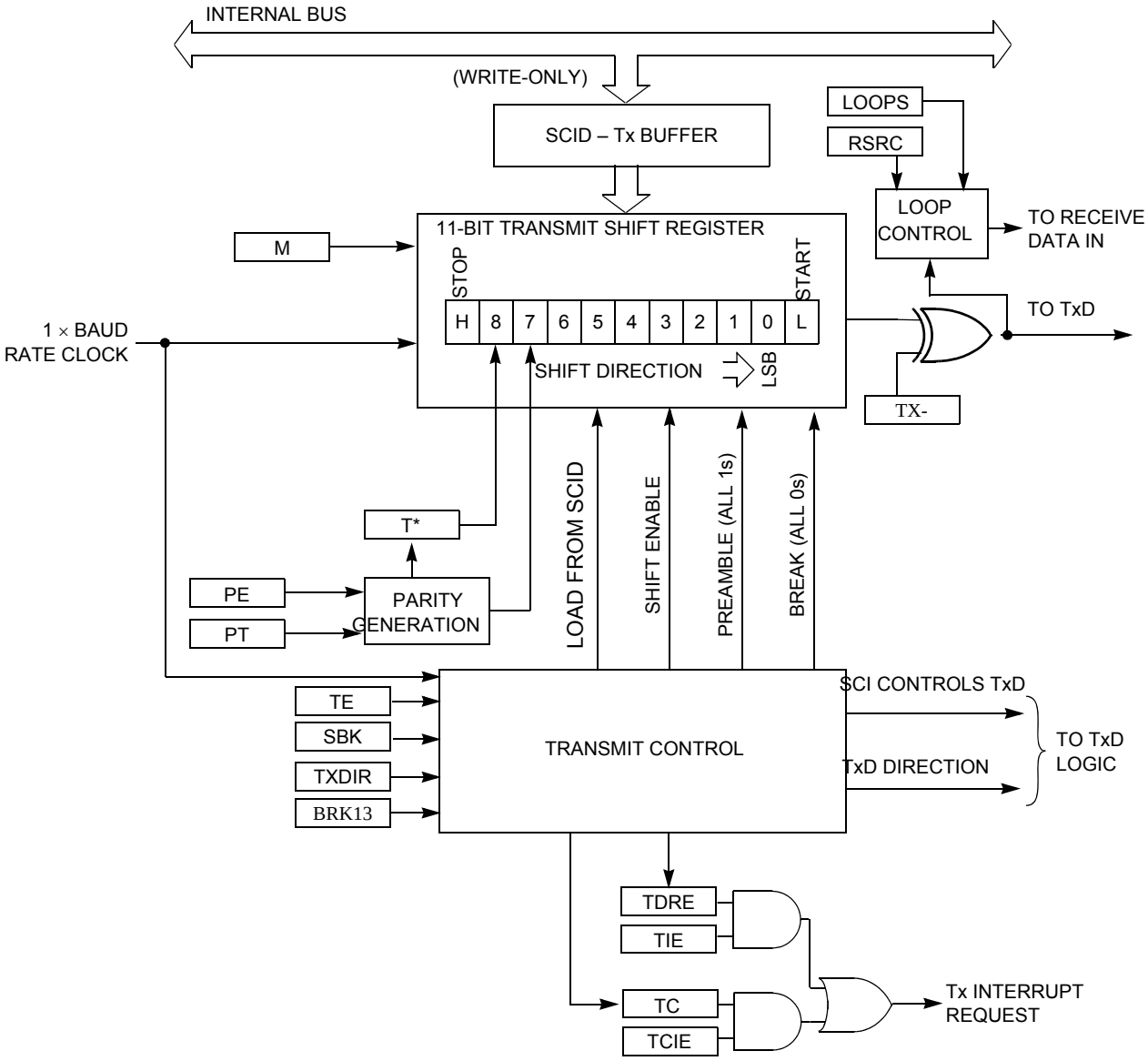


Figure 29. SCI Transmitter Block Diagram

Figure 30 shows the receiver portion of the SCI.

If the associated error was detected in the received character that caused RDRF to be set, the error flags — noise flag (NF), framing error (FE), and parity error flag (PF) — get set at the same time as RDRF. These flags are not set in overrun cases.

If RDRF was already set when a new character is ready to be transferred from the receive shifter to the receive data buffer, the overrun (OR) flag gets set instead the data along with any associated NF, FE, or PF condition is lost.

At any time, an active edge on the RxD serial data input pin causes the RXEDGIF flag to set. The RXEDGIF flag is cleared by writing a “1” to it. This function does depend on the receiver being enabled (RE = 1).

5.16.3.5 Additional SCI Functions

The following sections describe additional SCI functions.

5.16.3.5.1 8- and 9-Bit Data Modes

The SCI system (transmitter and receiver) can be configured to operate in 9-bit data mode by setting the M control bit in SCIC1. In 9-bit mode, there is a ninth data bit to the left of the MSB of the SCI data register. For the transmit data buffer, this bit is stored in T8 in SCIC3. For the receiver, the ninth bit is held in R8 in SCIC3.

For coherent writes to the transmit data buffer, write to the T8 bit before writing to SCID.

If the bit value to be transmitted as the ninth bit of a new character is the same as for the previous character, it is not necessary to write to T8 again. When data is transferred from the transmit data buffer to the transmit shifter, the value in T8 is copied at the same time data is transferred from SCID to the shifter.

9-bit data mode typically is used in conjunction with parity to allow eight bits of data plus the parity in the ninth bit. Or it is used with address-mark wake-up so the ninth data bit can serve as the wake-up bit. In custom protocols, the ninth bit can also serve as a software-controlled marker.

5.16.3.5.2 Stop Mode Operation

During all stop modes, clocks to the SCI module are halted.

In stop1 and stop2 modes, all SCI register data is lost and must be re-initialized upon recovery from these two stop modes. No SCI module registers are affected in stop3 mode.

The receive input active edge detect circuit is still active in stop3 mode, but not in stop2. An active edge on the receive input brings the CPU out of stop3 mode if the interrupt is not masked (RXEDGIE = 1).

Note that because the clocks are halted, the SCI module will resume operation upon exit from stop (only in stop3 mode). Software should ensure stop mode is not entered while there is a character being transmitted out of or received into the SCI module.

5.16.3.5.3 Loop Mode

When LOOPS = 1, the RSRC bit in the same register chooses between loop mode (RSRC = 0) or single-wire mode (RSRC = 1). Loop mode is sometimes used to check software, independent of connections in the external system, to help isolate system problems. In this mode, the transmitter output is internally connected to the receiver input and the RxD pin is not used by the SCI, so it reverts to a general purpose port I/O pin.

5.16.3.5.4 Single-wire Operation

When LOOPS = 1, the RSRC bit in the same register chooses between loop mode (RSRC = 0) or single-wire mode (RSRC = 1). Single-wire mode is used to implement a half-duplex serial connection. The receiver is internally connected to the transmitter output and to the TxD pin. The RxD pin is not used and reverts to a general purpose port I/O pin.

In single-wire mode, the TXDIR bit in SCIC3 controls the direction of serial data on the TxD pin. When TXDIR = 0, the TxD pin is an input to the SCI receiver and the transmitter is temporarily disconnected from the TxD pin so an external device can send serial data to the receiver. When TXDIR = 1, the TxD pin is an output driven by the transmitter. In single-wire mode, the internal loop back connection from the transmitter to the receiver causes the receiver to receive characters that are sent out by the transmitter.

5.21 Current Sense Module - ISENSE

The Current Sense Module is implemented to amplify the voltage drop across an external shunt resistor to measure the actual application current using the internal Analog Digital Converter Channel 9. Typical application is the motor current in a window lift control module

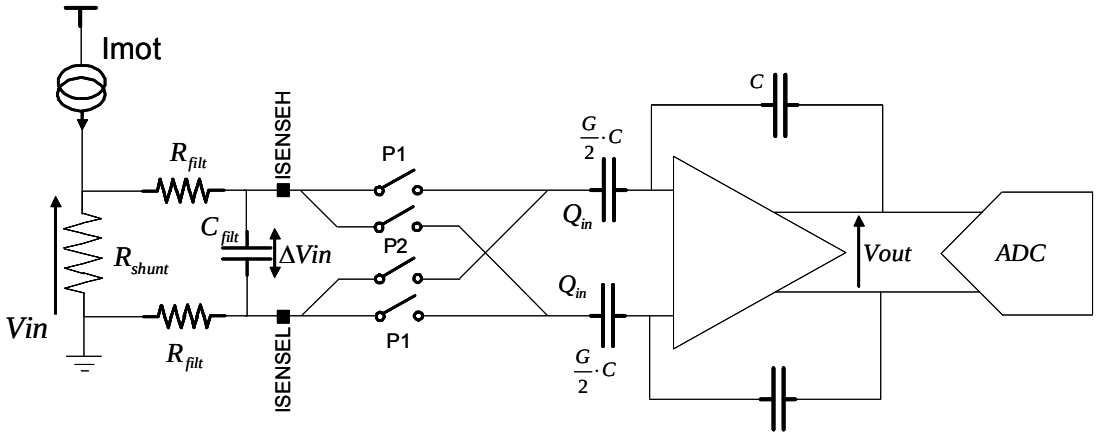


Figure 37. Current Sense Module with External Filter Option

The implementation is based on a switched capacitor solution to eliminate unwanted offset.To fit several application scenarios, eight different GAIN setting are implemented.

5.21.1 Register Definition

5.21.1.1 Current Sense Register (CSR)

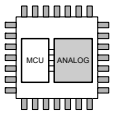
Table 210. Current Sense Register (CSR)

Offset[145] 0x3C — Access: User read/write

	7	6	5	4	3	2	1	0
R	CSE	0	0	0	CCD	CSGS		
W								
Reset	0	0	0	0	0	0	0	0

Note:
145. Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

5.22 Temperature Sensor - TSENSE



To be able to measure the current MM912_634 analog die chip temperature, the TSENSE feature is implemented. A constant temperature related gain of TSG can be routed to the internal Analog Digital Converter (Channel 11).

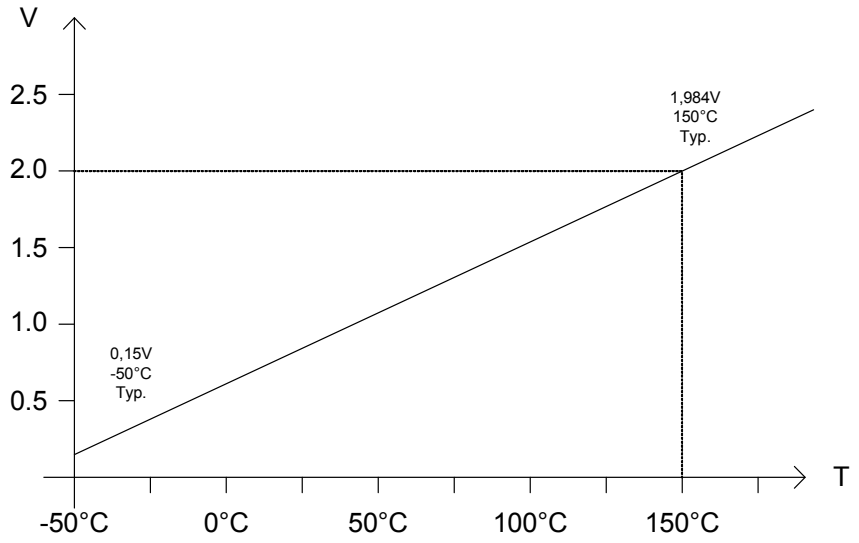


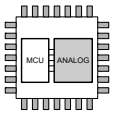
Figure 38. TSENSE - Graph

Refer to the Section 5.20, “Analog Digital Converter - ADC" for details on the channel selection and analog measurement.

NOTE

Due to internal capacitor charging, temperature measurements are valid 200 ms (max) after system power up and wake-up.

5.26 MM912_634 - Analog Die Trimming



A trimming option is implemented to increase some device parameter accuracy. As the MM912_634 analog die is exclusively combined with a FLASH- MCU, the required trimming values can be calculated during the final test of the device, and stored to a fixed position in the FLASH memory. During start-up of the system, the trimming values have to be copied into the MM912_634 analog die trimming registers.

The trimming registers will maintain their content during Low Power mode, Reset will set the default value.

5.26.1 Memory Map and Register Definition

5.26.1.1 Module Memory Map

There are four trimming registers implemented (CTR0…CTR3), with CTR2 being reserved for future use. The following table shows the registers used.

Table 212. MM912_634 Analog Die Trimming Registers

Offset	Name		7	6	5	4	3	2	1	0
0xF0	CTR0	R	LINTRE	LINTR	WDCTRE	CTR0_4	CTR0_3	WDCTR2	WDCTR1	WDCTR0
	Trimming Reg 0	W								
0xF1	CTR1	R	BGTRE	CTR1_6	BGTRIMUP	BGTRIMDN	IREFTRE	IREFTR2	IREFTR1	IREFTR0
	Trimming Reg 1	W								
0xF2	CTR2	R	0	0	0	SLPBGTRE	SLPBG_LOCK	SLPBGTR2	SLPBGTR1	SLPBGTR0
	Trimming Reg 2	W								
0xF3	CTR3	R	OFFCTRE	OFFCTR2	OFFCTR1	OFFCTR0	CTR3_E	CTR3_2	CTR3_1	CTR3_0
	Trimming Reg 3	W								

Note:
148. Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

At system startup, the trimming information have to be copied from the MCU IFR Flash location to the corresponding MM912_634 analog die trimming registers. The following table shows the register correlation.

Table 213. MM912_634 - MCU vs. Analog Die Trimming Register Correlation

Name	MCU IFR Address	Analog Offset[149]
CTR0	0x0_40C0	0xF0
CTR1	0x0_40C1	0xF1
CTR2	0x0_40C2	0xF2
CTR3	0x0_40C3	0xF3

Note:
149. Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

NOTE

Two word (16-Bit) transfers including CTR2 are recommended at system startup. The IFR register has to be enabled for reading (Program Page Index Register (PPAGE))

NOTE

To trim the bg1p25sleep there is two steps:

Step 1: First choose the right trim step by adjusting SLPBGTR[2:0] with SLPBGTRE=1, SLPBG_LOCK bit has to stay at 0.

Step 2: Once the trim value is known, correct SLPBGTR[2:0], SLPBGTRE and SLPBG_LOCK bits have to be set at the same time to apply and lock the trim. Once the trim is locked, no other trim on the parameter is possible.

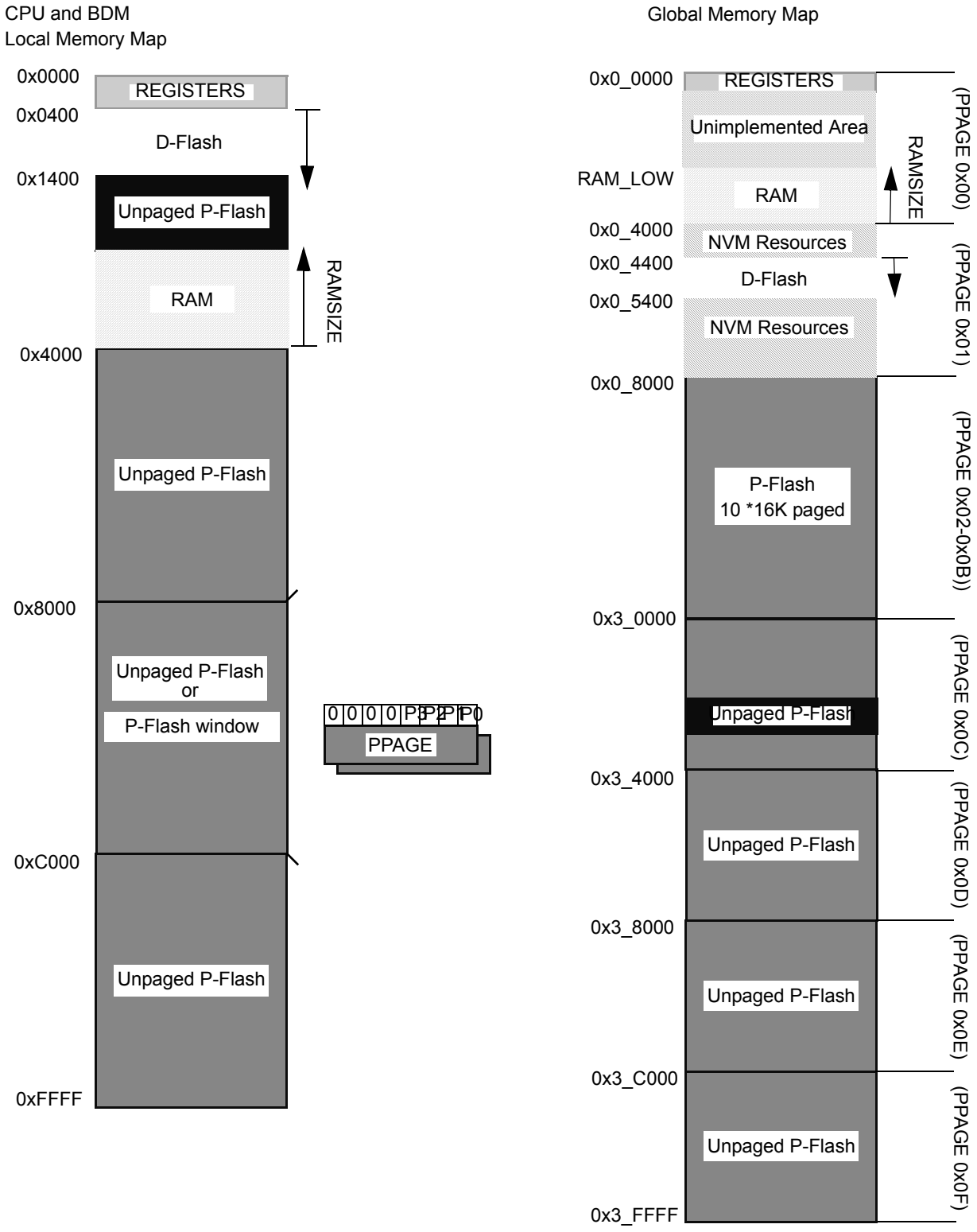


Figure 49. Local to Global Address Mapping

5.32 S12S Debug Module (S12SDBGV2)

5.32.1 Introduction

The S12SDBG module provides an on-chip trace buffer with flexible triggering capability to allow non-intrusive debug of application software. The S12SDBG module is optimized for S12SCPU debugging.

Typically the S12SDBG module is used in conjunction with the S12SBDM module, whereby the user configures the S12SDBG module for a debugging session over the BDM interface. Once configured the S12SDBG module is armed and the device leaves BDM returning control to the user program, which is then monitored by the S12SDBG module. Alternatively the S12SDBG module can be configured over a serial interface using SWI routines.

5.32.1.1 Glossary Of Terms

COF: Change Of Flow. Change in the program flow due to a conditional branch, indexed jump or interrupt.

BDM: Background Debug Mode

S12SBDM: Background Debug Module

DUG: Device User Guide, describing the features of the device into which the DBG is integrated.

WORD: 16 bit data entity

Data Line: 20 bit data entity

CPU: S12SCPU module

DBG: S12SDBG module

POR: Power On Reset

Tag: Tags can be attached to CPU opcodes as they enter the instruction pipe. If the tagged opcode reaches the execution stage a tag hit occurs.

5.32.1.2 Overview

The comparators monitor the bus activity of the CPU module. A match can initiate a state sequencer transition. On a transition to the Final State, bus tracing is triggered and/or a breakpoint can be generated.

Independent of comparator matches a transition to Final State with associated tracing and breakpoint can be triggered immediately by writing to the TRIG control bit.

The trace buffer is visible through a 2-byte window in the register address map and can be read out using standard 16-bit word reads. Tracing is disabled when the MCU system is secured.

5.32.1.3 Features

- Three comparators (A, B and C)
  - — Comparators A compares the full address bus and full 16-bit data bus
  - — Comparator A features a data bus mask register
  - — Comparators B and C compare the full address bus only
  - — Each comparator features selection of read or write access cycles
  - — Comparator B allows selection of byte or word access cycles
  - — Comparator matches can initiate state sequencer transitions
- Three comparator modes
  - — Simple address/data comparator match mode
  - — Inside address range mode, Addmin $\leq$ Address $\leq$ Addmax
  - — Outside address range match mode, Address $<$ Addmin or Address $>$ Addmax
- Two types of matches
  - — Tagged — This matches just before a specific instruction begins execution
  - — Force — This is valid on the first instruction boundary after a match occurs
- Two types of breakpoints
  - — CPU breakpoint entering BDM on breakpoint (BDM)
  - — CPU breakpoint executing SWI on breakpoint (SWI)
- Trigger mode independent of comparators
  - — TRIG Immediate software trigger

Table 284. DBGTB Field Descriptions

Field	Description
15–0 Bit[15:0]	**Trace Buffer Data Bits** — The Trace Buffer Register is a window through which the 20-bit wide data lines of the Trace Buffer may be read 16 bits at a time. Each valid read of DBGTB increments an internal trace buffer pointer which points to the next address to be read. When the ARM bit is set the trace buffer is locked to prevent reading. The trace buffer can only be unlocked for reading by writing to DBGTB with an aligned word write when the module is disarmed. The DBGTB register can be read only as an aligned word, any byte reads or misaligned access of these registers return 0 and do not cause the trace buffer pointer to increment to the next trace buffer address. Similarly reads while the debugger is armed or with the TSOURCE bit clear, return 0 and do not affect the trace buffer pointer. The POR state is undefined. Other resets do not affect the trace buffer contents.

5.32.3.2.6 Debug Count Register (DBGCNT)

Table 285. Debug Count Register (DBGCNT)

Address: 0x0026

	7	6	5	4	3	2	1	0
R	TBF	0	CNT					
W								
Reset	—	—	—	—	—	—	—	—
POR	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Read: Anytime

Write: Never

Table 286. DBGCNT Field Descriptions

Field	Description
7 TBF	**Trace Buffer Full** — The TBF bit indicates that the trace buffer has stored 64 or more lines of data since it was last armed. If this bit is set, then all 64 lines will be valid data, regardless of the value of DBGCNT bits. The TBF bit is cleared when ARM in DBGC1 is written to a one. The TBF is cleared by the power on reset initialization. Other system generated resets have no affect on this bit This bit is also visible at DBGSR[7]
5–0 CNT[5:0]	**Count Value** — The CNT bits indicate the number of valid data 20-bit data lines stored in the Trace Buffer. Table 287 shows the correlation between the CNT bits and the number of valid data lines in the Trace Buffer. When the CNT rolls over to zero, the TBF bit in DBGSR is set and incrementing of CNT will continue in end-trigger mode. The DBGCNT register is cleared when ARM in DBGC1 is written to a one. The DBGCNT register is cleared by power-on-reset initialization but is not cleared by other system resets. Thus should a reset occur during a debug session, the DBGCNT register still indicates after the reset, the number of valid trace buffer entries stored before the reset occurred. The DBGCNT register is not decremented when reading from the trace buffer.

Table 287. CNT Decoding Table

TBF	CNT[5:0]	Description
0	000000	No data valid
0	000001	1 line valid
	000010	2 lines valid
	000100	4 lines valid
	000110	6 lines valid
	…	…
	111111	63 lines valid

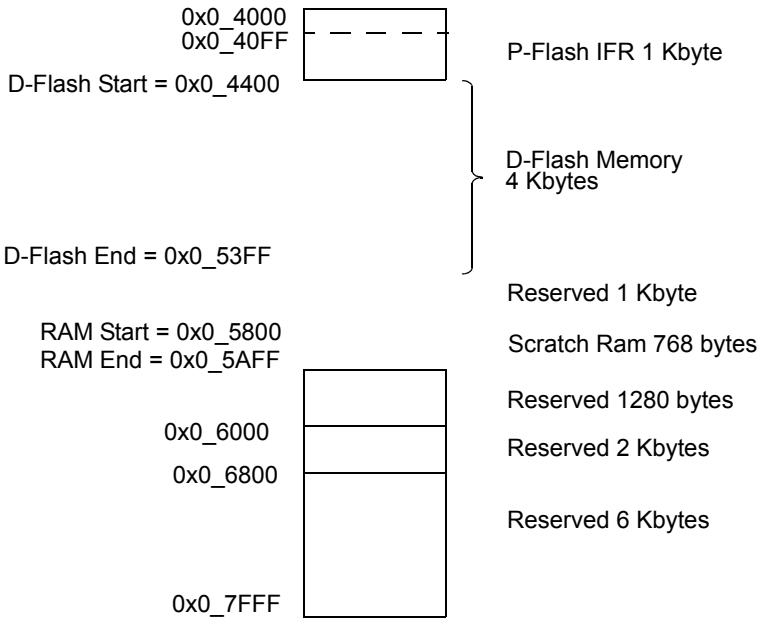


Figure 105. D-Flash and Memory Controller Resource Memory Map

5.40.3.2 Register Descriptions

The Flash module contains a set of 20 control and status registers located between Flash module base + 0x0000 and 0x0013. A summary of the Flash module registers is given in Figure 414 with detailed descriptions in the following subsections.

Writes to any Flash register must be avoided while a Flash command is active (CCIF=0) to prevent corruption of Flash register contents and adversely affect Memory Controller behavior.

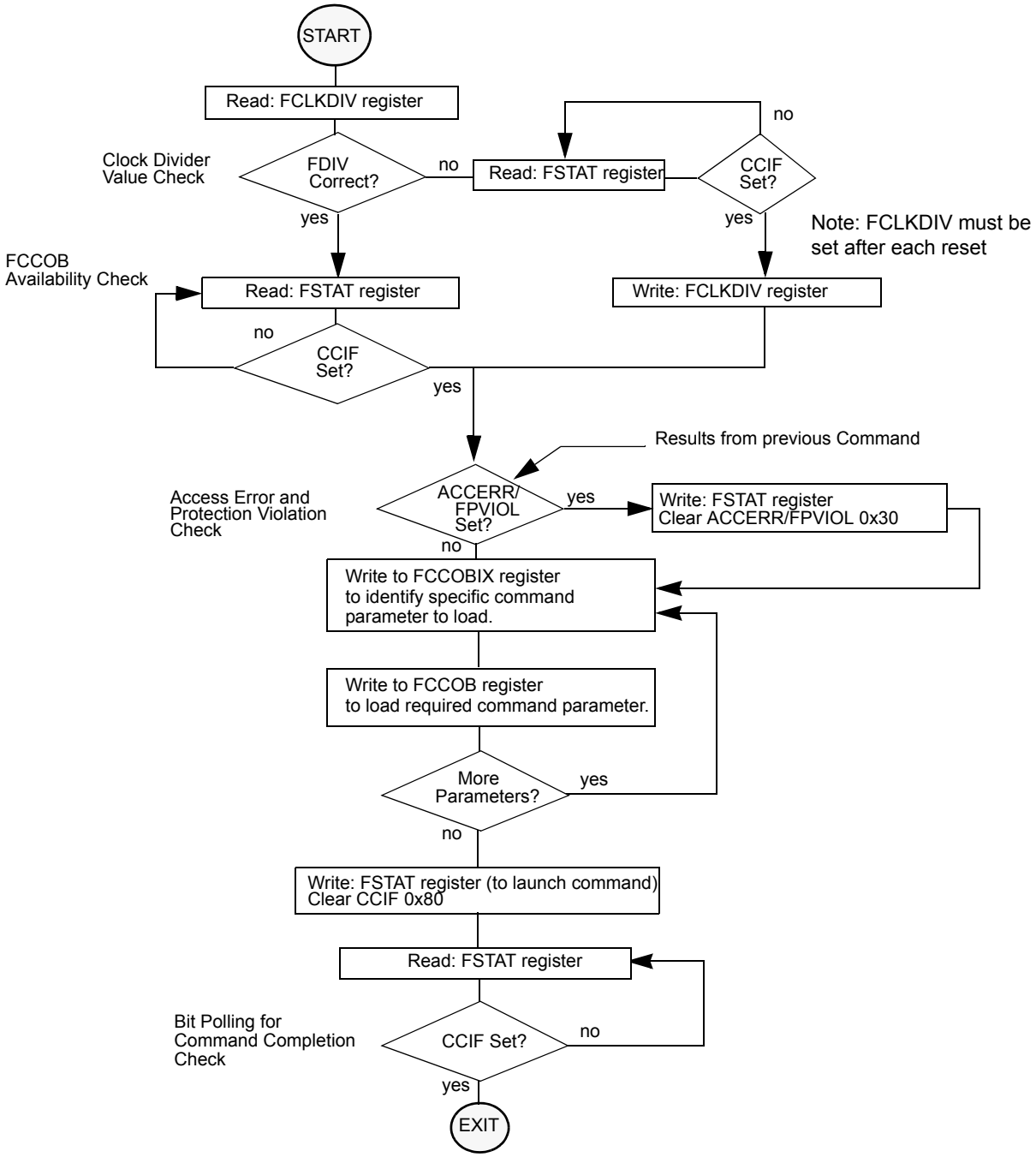


Figure 107. Generic Flash Command Write Sequence Flowchart

5.41.1.3.2 D2DI in special modes

The MCU can enter a special mode (used for test and debugging purposes as well as programming the FLASH). In the D2DI the “write-once” feature is disabled. See the MCU description for details.

5.41.2 External Signal Description

The D2DI optionally uses 6 or 10 port pins. The functions of those pins depends on the settings in the D2DCTL0 register, when the D2DI module is enabled.

5.41.2.1 D2DCLK

When the D2DI is enabled this pin is the clock output. This signal is low if the initiator is disabled, in STOP mode (with D2DSWAI asserted), otherwise it is a continuos clock. This pin may be shared with general purpose functionality if the D2DI is disabled.

5.41.2.2 D2DDAT[7:4]

When the D2DI is enabled and the interface connection width D2DCW is set to be 8-bit wide, those lines carry the data bits 7:4 acting as outputs or inputs. When they act as inputs pull-down elements are enabled. If the D2DI is disabled or if the interface connection width is set as 4-bit wide, the pins may be shared with general purpose pin functionality.

5.41.2.3 D2DDAT[3:0]

When the D2DI is enabled those lines carry the data bits 3:0 acting as outputs or inputs. When they act as inputs pull-down elements are enabled. If the D2DI is disabled the pins and may be shared with general purpose pin functionality.

5.41.2.4 D2DINT

The D2DINT is an active input interrupt input driven by the target device. The pin has an active pull-down device. If the D2DI is disabled the pin may be shared with general purpose pin functionality.

Table 497. Signal Properties

Name	Primary (D2DEN=1)	I/O	Secondary (D2DEN=0)	Reset	Comment	Pull down
D2DDAT[7:0]	Bi-directional Data Lines	I/O	GPIO	0	driven low if in STOP mode	Active(236)
D2DCLK	Interface Clock Signal	O	GPIO	0	low if in STOP mode	—
$\overline{\text{D2DINT}}$	Active High Interrupt	I	GPIO	—	—	Active(237)

Note:
236. Active if in input state, only if D2DEN=1
237. only if D2DEN=1

See the port interface module (PIM) guide for details of the GPIO function.

5.41.3 Memory Map and Register Definition

5.41.3.1 Memory Map

The D2DI memory map is split into three sections.

1. An eight-byte set of control registers
2. A 256 byte window for blocking transactions
3. A 256 byte window for non-blocking transactions

See the chapter “Device Memory Map” for the register layout (distribution of these sections).