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Application-specific microcontrollers are engineered to

Details	
Product Status	Active
Applications	Automotive
Core Processor	S12
Program Memory Type	FLASH (64kB)
Controller Series	HCS12
RAM Size	6K x 8
Interface	LIN, SCI
Number of I/O	9
Voltage - Supply	2.25V ~ 5.5V
Operating Temperature	-40°C ~ 105°C
Mounting Type	Surface Mount
Package / Case	48-LQFP Exposed Pad
Supplier Device Package	48-HLQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mm912h634dv1ae

Table 16. Static Electrical Characteristics - Hall Sensor Supply Output - HSUP

Ratings	Symbol	Min	Typ	Max	Unit
Current Limitation	I_{HSUP}	40	70	90	mA
Output Drain-to-Source On resistance T_J = 150 °C, ILOAD = 30 mA; 5.5 V ≤ VSUP ≤ 16 V T_J = 150 °C, ILOAD = 30 mA; 3.7 V ≤ VSUP < 5.5 V	$R_{DS(ON)}$	- -	- -	10 12	Ohm
Output Voltage: (18 V ≤ V_{SUP} ≤ 27 V)	$VHSUP_{MAX}$	16	17.5	18	V
Load Regulation (1.0 mA < I_{HSUP} < 30 mA; V_{SUP} > 18 V)	LD_{HSUP}	-	-	500	mV
Hall Supply Capacitor Range	C_{HSUP}	0.22	-	10	µF
External Capacitor ESR	C_{HSUP_R}	-	-	10	Ohm

Table 17. Static Electrical Characteristics - High Side Drivers - HS

Ratings	Symbol	Min	Typ	Max	Unit
Output Drain-to-Source On resistance T_J = 25 °C, I_{LOAD} = 50 mA; V_{SUP} > 9.0 V T_J = 150 °C, I_{LOAD} = 50 mA; V_{SUP} > 9.0 V T_J = 150 °C, I_{LOAD} = 30 mA; 5.5 V < V_{SUP} < 9.0 V	$R_{DS(ON)}$	- - -	- - -	7.0 10 14	Ohm
Output Current Limitation (0 V < V_{OUT} < V_{SUP} - 2.0 V)	I_{LIMHSX}	60	110	250	mA
Open Load Current Detection	I_{OLHSX}	-	5.0	7.5	mA
Leakage Current (-0.2 V < V_{HSx} < V_{S2} + 0.2 V)	I_{LEAK}	-	-	10	µA
Current Limitation Flag Threshold (5.5 V < V_{SUP} < 27 V)	V_{THSC}	V_{SUP} -2	-	-	V

Table 18. Static Electrical Characteristics - Low Side Drivers - LS

Ratings	Symbol	Min	Typ	Max	Unit
Output Drain-to-Source On resistance T_J = 25 °C, I_{LOAD} = 150 mA, V_{SUP} > 9.0 V T_J = 150 °C, I_{LOAD} = 150 mA, V_{SUP} > 9.0 V T_J = 150 °C, I_{LOAD} = 120 mA, 5.5 V < V_{SUP} < 9.0 V	$R_{DS(ON)}$	– – –	– – –	2.5 4.5 10	Ohm
Output Current Limitation (2.0 V < V_{OUT} < V_{SUP})	I_{LIMLSX}	180	275	380	mA
Open Load Current Detection	I_{OLLSX}	-	8.0	12	mA
Leakage Current (-0.2 V < V_{OUT} < VS1)	I_{LEAK}	-	-	10	µA
Active Output Energy Clamp (I_{OUT} = 150 mA)	V_{CLAMP}	40	-	45	V
Coil Series Resistance (I_{OUT} = 150 mA)	R_{COIL}	120	-		Ohm
Coil Inductance (I_{OUT} = 150 mA)	R_{COIL}	-	-	400	mH
Current Limitation Flag Threshold (5.5 V < V_{SUP} < 27 V)	V_{THSC}	2.0	-	-	V

Table 19. Static Electrical Characteristics - LIN Physical Layer Interface - LIN

Ratings	Symbol	Min	Typ	Max	Unit
Current Limitation for Driver dominant state. V_{BUS} = 18 V	I_{BUSLIM}	40	120	200	mA
Input Leakage Current at the Receiver incl. Pull-up Resistor RSLAVE; Driver OFF; V_{BUS} = 0 V; V_{BAT} = 12 V	$I_{BUS\_PAS\_DOM}$	-1.0	-	-	mA
Input Leakage Current at the Receiver incl. Pull-up Resistor RSLAVE; Driver OFF; 8.0 V < V_{BAT} < 18 V; 8.0 V < V_{BUS} < 18 V; V_{BUS} ≥ V_{BAT}	$I_{BUS\_PAS\_REC}$	-	-	20	µA

Table 21. Static Electrical Characteristics - General Purpose I/O - PTB[0…2]

Ratings	Symbol	Min	Typ	Max	Unit
Input Low Voltage (VS1 = 3.7 V)	$V_{IL3.7}$	V_{SS}-0.3	-	1.4	V
Input Hysteresis (VS1 = 3.7 V)	$V_{HYS3.7}$	100	200	300	mV
Input Leakage Current (pins in high-impedance input mode) (V_{IN} = V_{DDX} or V_{SSX})	I_{IN}	-1.0	-	1.0	µA
Output High Voltage (pins in output mode) Full drive I_{OH} = -10 mA	V_{OH}	V_{DDX}-0.8	-	-	V
Output Low Voltage (pins in output mode) Full drive I_{OL} = 10 mA	V_{OL}	-	-	0.8	V
Internal Pull-up Resistance (V_{IH} min > Input voltage > V_{IL} max)	R_{PUL}	26.25	37.5	48.75	kOhm
Input Capacitance	C_{IN}	-	6.0	-	pF
Clamp Voltage when selected as analog input	V_{CL_AIN}	VDD	-	-	V
Analog Input impedance = 10 kOhm max, Capacitance = 12 pF	R_{AIN}	-	-	10	kOhm
Analog Input Capacitance = 12 pF	C_{AIN}	-	12	-	pF
Maximum current all PTB combined (VDDX capability)	I_{BMAX}	-15	-	15	mA
Output Drive strength at 10 MHz	C_{OUT}	-	-	100	pF

Table 22. Static Electrical Characteristics - Analog Digital Converter - ADC(27)

Ratings	Symbol	Min	Typ	Max	Unit
ADC2p5 Reference Voltage 5.5 V < V_{SUP} < 27 V	$V_{ADC2p5RUN}$	2,45	2.5	2.55	V
ADC2p5 Reference Stop Mode Output Voltage	$V_{ADC2p5STOP}$	-	-	100	mV
Line Regulation, Normal Mode	LR_{RUNA}	-	10	12.5	mV
External Capacitor	C_{ADC2p5}	0.1	-	1.0	µF
External Capacitor ESR	C_{VDD_R}	-	-	10	Ohm
Scale Factor Error	E_{SCALE}	-1	-	1	LSB
Differential Linearity Error	E_{DNL}	-1.5	-	1.5	LSB
Integral Linearity Error	E_{INL}	-1.5	-	1.5	LSB
Zero Offset Error	E_{OFF}	-2.0	-	2.0	LSB
Quantization Error	E_Q	-0.5	-	0.5	LSB
Total Error with offset compensation	TE	-5.0	-	5.0	LSB
Bandgap measurement Channel (CH14) Valid Result Range (including ±7.0% bg1p25sleep accuracy + high-impedance measurement error of ±5.0% at f_{ADC})(28)	AD_{CH14}	1.1	1.25	1.4	V

Note:
27. No external load allowed on the ADC2p5 pin.
28. Reduced ADC frequency will lower measurement error.

5.3.3.1 Current Sense Module

For device options with the current sense module not available, the following considerations are to be made.

5.3.3.1.1 Pinout considerations

Table 78. ISENSE - Pin Considerations

PIN	PIN name for option 1	New PIN name	Comment
40	ISENSEL	NC	ISENSE feature not bonded and/or not tested. Connect PINs 40 and 41 (NC) to GND.
41	ISENSEH	NC	

5.3.3.1.2 Register Considerations

The Current Sense Register must remain in default (0x00) state.

Offset	Name		7	6	5	4	3	2	1	0
0x3C	CSR	R	CSE	0	0	0	CCD	CSGS		
	Current Sense Register	W								

The Conversion Control Register - Bit 9 must always be written 0.

0x82	ACCR (hi)	R	CH15	CH14	0	CH12	CH11	CH10	CH9	CH8
	ADC Conversion Ctrl Reg	W								

The Conversion Complete Register - Bit 9 must be ignored.

0x84	ACCSR (hi)	R	CC15	CC14	0	CC12	CC11	CC10	CC9	CC8
	ADC Conv Complete Reg	W								

The ADC Data Result Reg 9 must be ignored.

0x98	ADR9 (hi)	R	adr9 9	adr9 8	adr9 7	adr9 6	adr9 5	adr9 4	adr9 3	adr9 2
	ADC Data Result Register 9	W								
0x99	ADR9 (lo)	R	adr9 1	adr9 0	0	0	0	0	0	0
	ADC Data Result Register 9	W								

5.3.3.1.3 Functional Considerations

- The complete Current Sense Module is not available.
- The ADC Channel 9 is not available.

5.3.3.2 Wake-up Inputs (Lx)

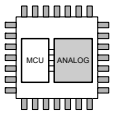
For device options with reduced number of wake up inputs (Lx), the following considerations are to be made.

5.3.3.2.1 Pinout considerations

Table 79. Lx - Pin Considerations

PIN	PIN Name for Option 1	New PIN name	Comment
31…36	Lx	NC	One or more Lx wake up inputs are not available based on the analog die option. Not available Lx inputs are not bonded and/or not tested. Connect not available Lx pins (NC) to GND. RLx is not required on those pins.

5.5 Power Supply



The MM912_634 analog die supplies VDD (2.5 V), VDDX (5.0 V), and HSUP, based on the supply voltage applied to the VS1 pin. VDD is cascaded of the VDDX regulator. To separate the High Side outputs from the main power supply, the VS2 pin does only power the High Side drivers. Both supply pins have to be externally protected against reverse battery conditions. To supply external Hall Effect Sensors, the HSUP pin will supply a switchable regulated supply. See Section 5.11, “Hall Sensor Supply Output - HSUP".

A reverse battery protected input (VSENSE) is implemented to measure the Battery Voltage directly. A serial resistor (R_{VSENSE}) is required on this pin. See Section 5.23, “Supply Voltage Sense - VSENSE". In addition, the VS1 supply can be routed to the ADC (VS1SENSE) to measure the VS1 pin voltage directly. See Section 5.24, “Internal Supply Voltage Sense - VS1SENSE".

To have an independent ADC verification, the internal sleep mode bandgap voltage can be routed to the ADC (BANDGAP). As this node is independent from the ADC reference, any out of range result would indicate malfunctioning ADC or Bandgap reference. See Section 5.25, “Internal Bandgap Reference Voltage Sense - BANDGAP".

To stabilize the internal ADC reference voltage for higher precision measurements, the current limited ADC2p5 pin needs to be connected to an external filter capacitor (C_{ADC2p5}). It is not recommended to connect additional loads to this pin. See Section 5.20, “Analog Digital Converter - ADC".

The following safety features are implemented:

- LBI - Low Battery Interrupt, internally measured at VSENSE
- LVI - Low Voltage Interrupt, internally measured at VS1
- HVI - High Voltage Interrupt, internally measured at VS2
- VROVI - Voltage Regulator Over-voltage Interrupt internally measured at VDD and VDDX
- LVR - Low Voltage Reset, internally measured at VDD
- LVRX - Low Voltage Reset, internally measured at VDDX
- HTI - High Temperature Interrupt measured between the VDD and VDDX regulators
- Over-temperature Shutdown measured between the VDD and VDDX regulators

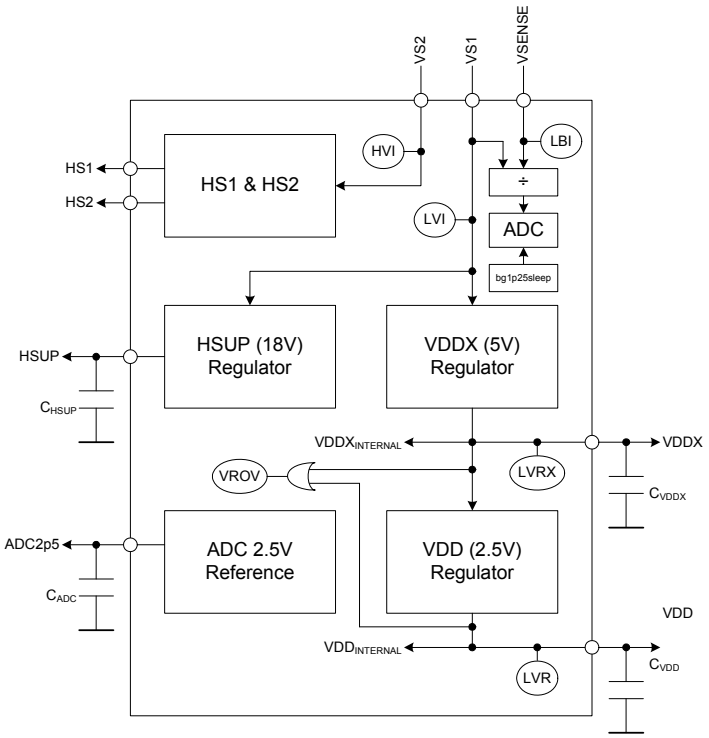


Figure 17. MM912_634 Power Supply

5.14.3.1.3 PWM Clock Select (PCLKx)

Each PWM channel has a choice of two clocks to use as the clock source for that channel as described by the following.

NOTE

Register bits PCLK0 and PCLK1 can be written anytime. If a clock select changes while a PWM signal is being generated, a truncated or stretched pulse can occur during the transition.

5.14.3.1.4 PWM Center Align Enable (CAEx)

The CAEx bits select either center aligned outputs or left aligned output for both PWM channels. If the CAEx bit is set to a one, the corresponding PWM output will be center aligned. If the CAEx bit is cleared, the corresponding PWM output will be left aligned. See Section 5.14.4.2.5, “Left Aligned Outputs" and Section 5.14.4.2.6, “Center Aligned Outputs" for a more detailed description of the PWM output modes.

NOTE

Write these bits only when the corresponding channel is disabled.

5.14.3.2 PWM Prescale Clock Select Register (PWMPRCLK)

This register selects the prescale clock source for clocks A and B independently.

Table 121. PWM Prescale Clock Select Register (PWMPRCLK)

Offset(91) 0x61 — Access: User read/write

	7	6	5	4	3	2	1	0
R	0	PCKB2	PCKB1	PCKB0	0	PCKA2	PCKA1	PCKA0
W								
Reset	0	0	0	0	0	0	0	0

Note:
91. Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

Table 122. PWMPRCLK - Register Field Descriptions

Field	Description
6–4 PCKB[2:0]	Prescaler Select for Clock B — Clock B is one of two clock sources which can be used for channel 1. These three bits determine the rate of clock B, as shown in Table 123.
2–0 PCKA[2:0]	Prescaler Select for Clock A — Clock A is one of two clock sources which can be used for channel 0. These three bits determine the rate of clock A, as shown in Table 124.

Table 123. Clock B Prescaler Selects

PCKB2	PCKB1	PCKB0	Value of Clock B
0	0	0	D2D clock
0	0	1	D2D clock / 2
0	1	0	D2D clock / 4
0	1	1	D2D clock / 8
1	0	0	D2D clock / 16
1	0	1	D2D clock / 32
1	1	0	D2D clock / 64
1	1	1	D2D clock / 128

5.16.2.3 SCI Control Register 2 (SCIC2)

This register can be read or written at any time.

Table 140. SCI Control Register 2 (SCIC2)

Offset(102) 0x43 Access: User read/write

	7	6	5	4	3	2	1	0
R W	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK
Reset	0	0	0	0	0	0	0	0

Note:
102. Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

Table 141. SCIC2 Field Descriptions

Field	Description
7 TIE	Transmit Interrupt Enable (for TDRE) 0 Hardware interrupts from TDRE disabled (use polling). 1 Hardware interrupt requested when TDRE flag is 1.
6 TCIE	Transmission Complete Interrupt Enable (for TC) 0 Hardware interrupts from TC disabled (use polling). 1 Hardware interrupt requested when TC flag is 1.
5 RIE	Receiver Interrupt Enable (for RDRF) 0 Hardware interrupts from RDRF disabled (use polling). 1 Hardware interrupt requested when RDRF flag is 1.
4 LIE	Idle Line Interrupt Enable (for IDLE) 0 Hardware interrupts from IDLE disabled (use polling). 1 Hardware interrupt requested when IDLE flag is 1.
3 TE	Transmitter Enable 0 Transmitter off. 1 Transmitter on. TE must be 1 in order to use the SCI transmitter. When TE = 1, the SCI forces the TxD pin to act as an output for the SCI system. When the SCI is configured for single-wire operation (LOOPS = RSRC = 1), TXDIR controls the direction of traffic on the single SCI communication line (TxD pin). TE also can be used to queue an idle character by writing TE = 0 then TE = 1 while a transmission is in progress. Refer to Section 5.16.3.2.1, “Send Break and Queued Idle" for more details. When TE is written to 0, the transmitter keeps control of the port TxD pin until any data, queued idle, or queued break character finishes transmitting before allowing the pin to revert to a general-purpose I/O pin.
2 RE	Receiver Enable — When the SCI receiver is off, the RxD pin reverts to being a general-purpose port I/O pin. If LOOPS = 1 the RxD pin reverts to being a general-purpose I/O pin even if RE = 1. 0 Receiver off. 1 Receiver on.

Table 173. TSCR1 - Register Field Descriptions

Field	Description
7 TEN	Timer Enable 1 = Enables the timer. 0 = Disables the timer. (Used for reducing power consumption).
4 TFFCA	Timer Fast Flag Clear All 1 = For TFLG1 register, a read from an input capture or a write to the output compare channel [TC 3:0] causes the corresponding channel flag, CnF, to be cleared.For TFLG2 register, any access to the TCNT register clears the TOF flag. Any access to the PACNT registers clears the PAOVF and PAIF bits in the PAFLG register. This has the advantage of eliminating software overhead in a separate clear sequence. Extra care is required to avoid accidental flag clearing due to unintended accesses. 0 = Allows the timer flag clearing.

5.19.3.3.7 Timer Toggle On Overflow Register 1 (TTOV)

Table 174. Timer Toggle On Overflow Register 1 (TTOV)

Offset(123) 0xC7 Access: User read/write

	7	6	5	4	3	2	1	0
R	0	0	0	0	TOV3	TOV2	TOV1	TOV0
W								
Reset	0	0	0	0	0	0	0	0

Note:
123. Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

Table 175. TTOV - Register Field Descriptions

Field	Description
3-0 TOV[3-0]	Toggle On Overflow Bits 1 = Toggle output compare pin on overflow feature enabled. 0 = Toggle output compare pin on overflow feature disabled.

NOTE

TOVn toggles output compare pin on overflow. This feature only takes effect when the corresponding channel is configured for an output compare mode. When set, an overflow toggle on the output compare pin takes precedence over forced output compare events.

5.19.3.3.8 Timer Control Register 1 (TCTL1)

Table 176. Timer Control Register 1 (TCTL1)

Offset(124) 0xC8 Access: User read/write

	7	6	5	4	3	2	1	0
R W	OM3	OL3	OM2	OL2	OM1	OL1	OM0	OL0
Reset	0	0	0	0	0	0	0	0

Note:
124. Offset related to 0x0200 for blocking access and 0x300 for non blocking access within the global address space.

5.19.4 Functional Description

5.19.4.1 General

This section provides a complete functional description of the timer TIM16B4C block. Refer to the detailed timer block diagram in Figure 34 as necessary.

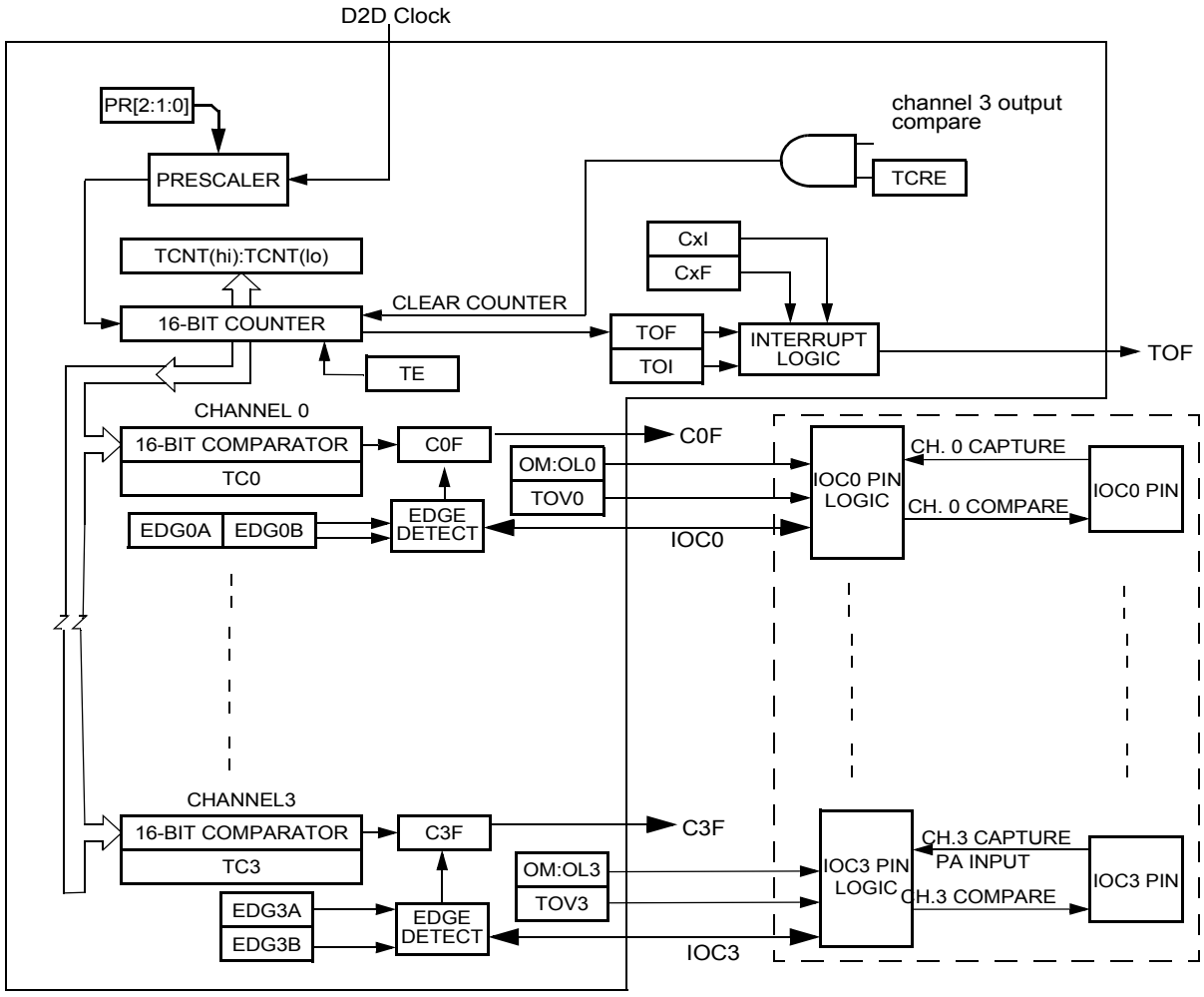


Figure 34. Detailed Timer Block Diagram

5.19.4.2 Prescaler

The prescaler divides the bus clock by 1, 2, 4, 8, 16, 32, 64, or 128. The prescaler select bits, PR[2:0], select the prescaler divisor. PR[2:0] are in the timer system control register 2 (TSCR2).

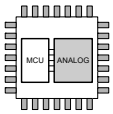
5.19.4.3 Input Capture

Clearing the I/O (input/output) select bit, IOSn, configures channel n as an input capture channel. The input capture function captures the time at which an external event occurs. When an active edge occurs on the pin of an input capture channel, the timer transfers the value in the timer counter into the timer channel registers, TCn.

The minimum pulse width for the input capture input is greater than two bus clocks.

An input capture on channel n sets the CnF flag. The CnI bit enables the CnF flag to generate interrupt requests.

5.20 Analog Digital Converter - ADC



5.20.1 Introduction

5.20.1.1 Overview

In order to sample the MM912_634 analog die analog sources, a 10-bit resolution successive approximation Analog to Digital Converter has been implemented. Controlled by the A/D Control Logic (ADC Wrapper), the Analog Digital Converter allows fast and high precision conversions.

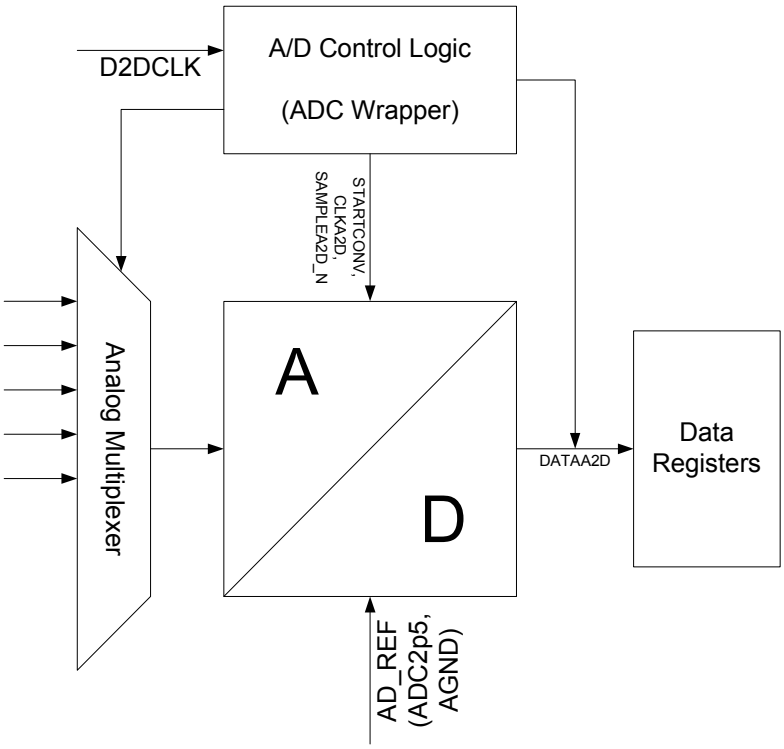


Figure 35. Analog Digital Converter Block Diagram

5.20.1.2 Features

- 10-bit resolution
- 13 µs (typ.), 10-bit Single Sample + Conversion Time
- External ADC2p5 pin with over-current protection to filter the analog reference voltage
- Total Error (TE) of ± 5 LSB without offset calibration active
- Integrated selectable offset compensation
- 14 + 1 analog channels (AD0…8; ISENSE, TSENSE and VSENSE, VS1SENSE, BANDGAP, plus calibration channel)
- Sequence- and Continuous Conversion Mode with IRQ for Sequence Complete indication
- Dedicated Result register for each channel

5.20.2 Modes of Operation

The Analog Digital Converter Module is active only in normal mode; it is disabled in Sleep and Stop mode.

5.20.3 External Signal Description

This section lists and describes the signals that do connect off-chip. Table 197 shows all the pins and their functions that are controlled by the Analog Digital Converter Module.

Table 197. ADC - Pin Functions and Priorities

Pin Name	Pin Function & Priority	I/O	Description	Pin Function after Reset
AGND	Analog Ground	-	Analog Ground Connection	-
ADC2p5	Analog Regulator	-	Analog Digital Converter Regulator Filter Terminal. A capacitor C_{ADC2p5} is required for operation.	-

5.20.4 Memory Map and Register Definition

5.20.4.1 Module Memory Map

Table 198 shows the register map of the Analog Digital Converter Module. All Register addresses given are referenced to the D2D interface offset.

Table 198. Analog Digital Converter Module - Memory Map

Register / Offset[138]		Bit 7	6	5	4	3	2	1	Bit 0
0x80 ACR	R	SCIE	CCE	OCE	ADCRST	0	PS2	PS1	PS0
	W								
0x81 ASR	R	SCF	2p5CLF	0	0	CCNT3	CCNT2	CCNT1	CCNT0
	W								
0x82 ACCR (hi)	R	CH15	CH14	0	CH12	CH11	CH10	CH9	CH8
	W								
0x83 ACCR (lo)	R	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
	W								
0x84 ACCSR (hi)	R	CC15	CC14	0	CC12	CC11	CC10	CC9	CC8
	W								
0x85 ACCSR (lo)	R	CC7	CC6	CC5	CC4	CC3	CC2	CC1	CC0
	W								
0x86 ADR0 (hi)	R	ADR0[9:2]							
	W								
0x87 ADR0 (lo)	R	ADR0[1:0]							
	W								
0x88 ADR1 (hi)	R	ADR1[9:2]							
	W								
0x89 ADR1 (lo)	R	ADR1[1:0]							
	W								
0x8A ADR2 (hi)	R	ADR2[9:2]							
	W								
0x8B ADR2 (lo)	R	ADR2[1:0]							
	W								
0x8C ADR3 (hi)	R	ADR3[9:2]							
	W								
0x8D ADR3 (lo)	R	ADR3[1:0]							
	W								
0x8E ADR4 (hi)	R	ADR4[9:2]							
	W								

5.27.8 Resets and Interrupts

Consult the S12 CPU manual and the S12SINT section for information on exception processing.

5.27.8.1 Resets

Table 224 lists all Reset sources and the vector locations. Resets are explained in detail in the 5.38, “S12 Clock, Reset and Power Management Unit (S12CPMU)”.

Table 224. Reset Sources and Vector Locations

Vector Address	Reset Source	CCR Mask	Local Enable
$FFFE	Power-On Reset (POR)	None	None
$FFFE	Low Voltage Reset (LVR)	None	None
$FFFE	External pin $\overline{\text{RESET}}$	None	None
$FFFE	Illegal Address Reset	None	None
$FFFC	Clock monitor reset	None	OSCE Bit in CPMUOSC register
$FFFA	COP watchdog reset	None	CR[2:0] in CPMUCOP register

5.27.8.2 Interrupt Vectors

Table 225 lists all interrupt sources and vectors in the default order of priority. The interrupt module (see 5.30, “Interrupt Module (S12SINTV1)”) provides an interrupt vector base register (IVBR) to relocate the vectors.

Table 225. Interrupt Vector Locations (Sheet 1 of 2)

Vector Address[155]	Interrupt Source	CCR Mask	Local Enable	Wake-up from STOP
Vector base + $F8	Unimplemented instruction trap	None	None	-
Vector base+ $F6	SWI	None	None	-
Vector base+ $F4	D2DI Error Interrupt	X Bit	None	Yes
Vector base+ $F2	D2DI External Error Interrupt	I bit	D2DCTL (D2DIE)	Yes
Vector base+ $F0	RTI timeout interrupt	I bit	CPMUINT (RTIE)	
Vector base + $EE to Vector base + $DA	Reserved			
Vector base + $D8	SPI	I bit	SPICR1 (SPIE, SPTIE)	No
Vector base + $D6 to Vector base + $CA	Reserved			
Vector base + $C8	Oscillator status interrupt	I bit	CPMUINT (OSCIE)	No
Vector base + $C6	PLL lock interrupt	I bit	CPMUINT (LOCKIE)	No
Vector base + $C4 to Vector base + $BC	Reserved			
Vector base + $BA	FLASH error	I bit	FERCNFG (SFDIE, DFDIE)	No
Vector base + $B8	FLASH command	I bit	FCNFG (CCIE)	No
Vector base + $B6 to Vector base + $8C	Reserved			
Vector base + $8A	Low-voltage interrupt (LVI)	I bit	CPMUCTRL (LVIE)	No
Vector base + $88 to Vector base + $82	Reserved			

5.29.5 Implemented Memory in the System Memory Architecture

Each memory can be implemented in its maximum allowed size. But some devices have been defined for smaller sizes, which means less implemented pages. All non implemented pages are called unimplemented areas.

- Registers has a fixed size of 1.0 kB, accessible via xbus0.
- SRAM has a maximum size of 11 kB, accessible via xbus0.
- D-Flash has a fixed size of 4.0 kB accessible via xbus0.
- P-Flash has a maximum size of 224 kB, accessible via xbus0.
- NVM resources (IFR, Scratch-RAM, ROM) including D-Flash have maximum size of 16 kB (PPAGE 0x01).

5.29.5.0.1 Implemented Memory Map

The global memory spaces reserved for the internal resources (RAM, D-Flash, and P-Flash) are not determined by the MMC module. Size of the individual internal resources are however fixed in the design of the device cannot be changed by the user. Please refer to the SoC Guide for further details. Figure 50 and Table 255 show the memory spaces occupied by the on-chip resources. Please note that the memory spaces have fixed top addresses.

Table 255. Global Implemented Memory Space

Internal Resource	Bottom Address	Top Address
Registers	0x0_0000	0x0_03FF
System RAM	RAM_LOW = 0x0_4000 minus RAMSIZE(169)	0x0_3FFF
D-Flash	0x0_4400	0x0_53FF
P-Flash	PF_LOW = 0x4_0000 minus FLASHSIZE(170)	0x3_FFFF

Note:
169. RAMSIZE is the hexadecimal value of RAM SIZE in bytes
170. FLASHSIZE is the hexadecimal value of FLASH SIZE in bytes

In single-chip modes accesses by the CPU12 (except for firmware commands) to any of the unimplemented areas (see Figure 50) will result in an illegal access reset (system reset). BDM accesses to the unimplemented areas are allowed but the data will be undefined.

No misaligned word access from the BDM module will occur; these accesses are blocked in the BDM module (Refer to BDM Block Guide).

5.31.4.7 Serial Interface Hardware Handshake Protocol

BDM commands that require CPU execution are ultimately treated at the MCU bus rate. Since the BDM clock source can be modified , it is very helpful to provide a handshake protocol in which the host could determine when an issued command is executed by the CPU. . The alternative is to always wait the amount of time equal to the appropriate number of cycles at the slowest possible rate the clock could be running. This sub-section will describe the hardware handshake protocol.

The hardware handshake protocol signals to the host controller when an issued command was successfully executed by the target. This protocol is implemented by a 16 serial clock cycle low pulse followed by a brief speedup pulse in the BKGD pin. This pulse is generated by the target MCU when a command, issued by the host, has been successfully executed (see Figure 58). This pulse is referred to as the ACK pulse. After the ACK pulse has finished: the host can start the bit retrieval if the last issued command was a read command, or start a new command if the last command was a write command or a control command (BACKGROUND, GO, GO_UNTIL(182) or TRACE1). The ACK pulse is not issued earlier than 32 serial clock cycles after the BDM command was issued. The end of the BDM command is assumed to be the 16th tick of the last bit. This minimum delay assures enough time for the host to perceive the ACK pulse. Note also that, there is no upper limit for the delay between the command and the related ACK pulse, since the command execution depends upon the CPU bus, which in some cases could be very slow due to long accesses taking place.This protocol allows a great flexibility for the POD designers, since it does not rely on any accurate time measurement or short response time to any event in the serial communication.

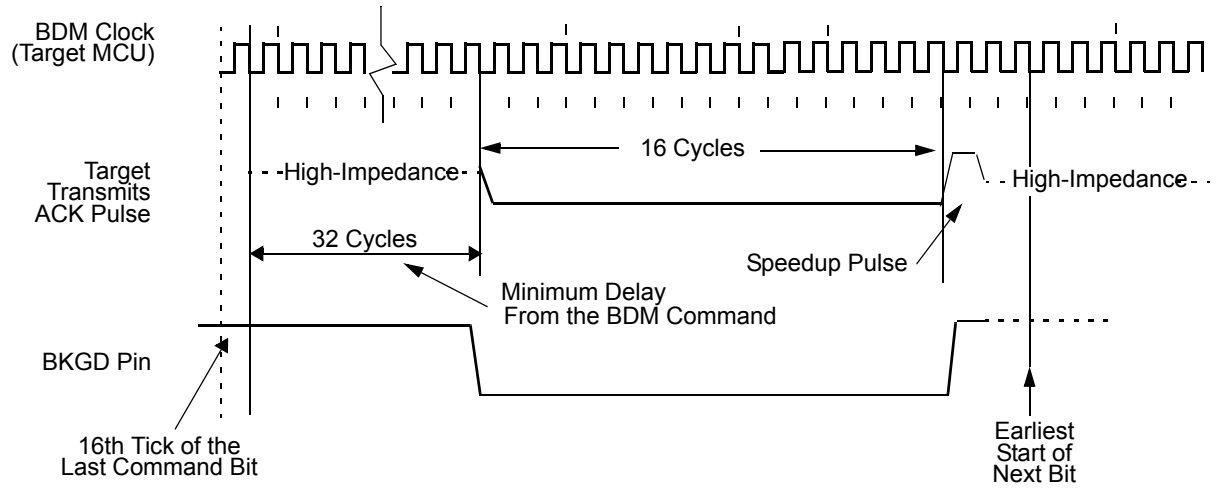


Figure 58. Target Acknowledge Pulse (ACK)

NOTE

If the ACK pulse was issued by the target, the host assumes the previous command was executed. If the CPU enters stop prior to executing a hardware command, the ACK pulse will not be issued meaning that the BDM command was not executed. After entering stop mode, the BDM command is no longer pending.

Figure 59 shows the ACK handshake protocol in a command level timing diagram. The READ_BYTE instruction is used as an example. First, the 8-bit instruction opcode is sent by the host, followed by the address of the memory location to be read. The target BDM decodes the instruction. A bus cycle is grabbed (free or stolen) by the BDM and it executes the READ_BYTE operation. Having retrieved the data, the BDM issues an ACK pulse to the host controller, indicating that the addressed byte is ready to be retrieved. After detecting the ACK pulse, the host initiates the byte retrieval process. Note that data is sent in the form of a word and the host needs to determine which is the appropriate byte based on whether the address was odd or even.

has been reached. Hence after a system stop mode the handshake feature must be enabled again by sending the ACK_ENABLE command.

5.31.4.11 Serial Communication Timeout

The host initiates a host-to-target serial transmission by generating a falling edge on the BKGD pin. If BKGD is kept low for more than 128 target clock cycles, the target understands that a SYNC command was issued. In this case, the target will keep waiting for a rising edge on BKGD in order to answer the SYNC request pulse. If the rising edge is not detected, the target will keep waiting forever without any timeout limit.

Consider now the case where the host returns BKGD to logic one before 128 cycles. This is interpreted as a valid bit transmission, and not as a SYNC request. The target will keep waiting for another falling edge marking the start of a new bit. If, however, a new falling edge is not detected by the target within 512 clock cycles since the last falling edge, a timeout occurs and the current command is discarded without affecting memory or the operating mode of the MCU. This is referred to as a soft-reset.

If a read command is issued but the data is not retrieved within 512 serial clock cycles, a soft-reset will occur causing the command to be disregarded. The data is not available for retrieval after the timeout has occurred. This is the expected behavior if the handshake protocol is not enabled. In order to allow the data to be retrieved even with a large clock frequency mismatch (between BDM and CPU) when the hardware handshake protocol is enabled, the time out between a read command and the data retrieval is disabled. Therefore, the host could wait for more then 512 serial clock cycles and still be able to retrieve the data from an issued read command. However, once the handshake pulse (ACK pulse) is issued, the timeout feature is re-activated, meaning that the target will time out after 512 clock cycles. Therefore, the host needs to retrieve the data within a 512 serial clock cycles time frame after the ACK pulse had been issued. After that period, the read command is discarded and the data is no longer available for retrieval. Any negative edge in the BKGD pin after the timeout period is considered to be a new command or a SYNC request.

Note that whenever a partially issued command, or partially retrieved data, has occurred the timeout in the serial communication is active. This means that if a time frame higher than 512 serial clock cycles is observed between two consecutive negative edges and the command being issued or data being retrieved is not complete, a soft-reset will occur causing the partially received command or data retrieved to be disregarded. The next negative edge in the BKGD pin, after a soft-reset has occurred, is considered by the target as the start of a new BDM command, or the start of a SYNC request pulse.

5.32 S12S Debug Module (S12SDBGV2)

5.32.1 Introduction

The S12SDBG module provides an on-chip trace buffer with flexible triggering capability to allow non-intrusive debug of application software. The S12SDBG module is optimized for S12SCPU debugging.

Typically the S12SDBG module is used in conjunction with the S12SBDM module, whereby the user configures the S12SDBG module for a debugging session over the BDM interface. Once configured the S12SDBG module is armed and the device leaves BDM returning control to the user program, which is then monitored by the S12SDBG module. Alternatively the S12SDBG module can be configured over a serial interface using SWI routines.

5.32.1.1 Glossary Of Terms

COF: Change Of Flow. Change in the program flow due to a conditional branch, indexed jump or interrupt.

BDM: Background Debug Mode

S12SBDM: Background Debug Module

DUG: Device User Guide, describing the features of the device into which the DBG is integrated.

WORD: 16 bit data entity

Data Line: 20 bit data entity

CPU: S12SCPU module

DBG: S12SDBG module

POR: Power On Reset

Tag: Tags can be attached to CPU opcodes as they enter the instruction pipe. If the tagged opcode reaches the execution stage a tag hit occurs.

5.32.1.2 Overview

The comparators monitor the bus activity of the CPU module. A match can initiate a state sequencer transition. On a transition to the Final State, bus tracing is triggered and/or a breakpoint can be generated.

Independent of comparator matches a transition to Final State with associated tracing and breakpoint can be triggered immediately by writing to the TRIG control bit.

The trace buffer is visible through a 2-byte window in the register address map and can be read out using standard 16-bit word reads. Tracing is disabled when the MCU system is secured.

5.32.1.3 Features

- Three comparators (A, B and C)
  - — Comparators A compares the full address bus and full 16-bit data bus
  - — Comparator A features a data bus mask register
  - — Comparators B and C compare the full address bus only
  - — Each comparator features selection of read or write access cycles
  - — Comparator B allows selection of byte or word access cycles
  - — Comparator matches can initiate state sequencer transitions
- Three comparator modes
  - — Simple address/data comparator match mode
  - — Inside address range mode, Addmin $\leq$ Address $\leq$ Addmax
  - — Outside address range match mode, Address $<$ Addmin or Address $>$ Addmax
- Two types of matches
  - — Tagged — This matches just before a specific instruction begins execution
  - — Force — This is valid on the first instruction boundary after a match occurs
- Two types of breakpoints
  - — CPU breakpoint entering BDM on breakpoint (BDM)
  - — CPU breakpoint executing SWI on breakpoint (SWI)
- Trigger mode independent of comparators
  - — TRIG Immediate software trigger

5.32.4.7.3.1 DBG Breakpoint Priorities And BDM Interfacing

Breakpoint operation is dependent on the state of the BDM module. If the BDM module is active, the CPU is executing out of BDM firmware, thus comparator matches and associated breakpoints are disabled. In addition, while executing a BDM TRACE command, tagging into BDM is disabled. If BDM is not active, the breakpoint gives priority to BDM requests over SWI requests if the breakpoint happens to coincide with a SWI instruction in user code. On returning from BDM, the SWI from user code gets executed.

Table 332. Breakpoint Mapping Summary

DBGBRK	BDM Bit (DBGC1[4])	BDM Enabled	BDM Active	Breakpoint Mapping
0	X	X	X	No Breakpoint
1	0	X	0	Breakpoint to SWI
X	X	1	1	No Breakpoint
1	1	0	X	Breakpoint to SWI
1	1	1	0	Breakpoint to BDM

BDM cannot be entered from a breakpoint unless the ENABLE bit is set in the BDM. If entry to BDM via a BGND instruction is attempted and the ENABLE bit in the BDM is cleared, the CPU actually executes the BDM firmware code, checks the ENABLE and returns if ENABLE is not set. If not serviced by the monitor then the breakpoint is re-asserted when the BDM returns to normal CPU flow.

If the comparator register contents coincide with the SWI/BDM vector address then an SWI in user code could coincide with a DBG breakpoint. The CPU ensures that BDM requests have a higher priority than SWI requests. Returning from the BDM/SWI service routine care must be taken to avoid a repeated breakpoint at the same address.

Should a tagged or forced breakpoint coincide with a BGND in user code, then the instruction that follows the BGND instruction is the first instruction executed when normal program execution resumes.

NOTE

When program control returns from a tagged breakpoint using an RTI or BDM GO command without program counter modification it returns to the instruction whose tag generated the breakpoint. To avoid a repeated breakpoint at the same location reconfigure the DBG module in the SWI routine, if configured for an SWI breakpoint, or over the BDM interface by executing a TRACE command before the GO to increment the program flow past the tagged instruction.

5.32.5 Application Information

5.32.5.1 State Machine scenarios

Defining the state control registers as SCR1,SCR2, SCR3 and M0,M1,M2 as matches on channels 0,1,2 respectively. SCR encoding supported by S12SDBGV1 are shown in black. SCR encoding supported only in S12SDBGV2 are shown in red. For backwards compatibility the new scenarios use a 4th bit in each SCR register. Thus the existing encoding for SCRx[2:0] is not changed.

5.32.5.2 Scenario 1

A trigger is generated if a given sequence of 3 code events is executed.

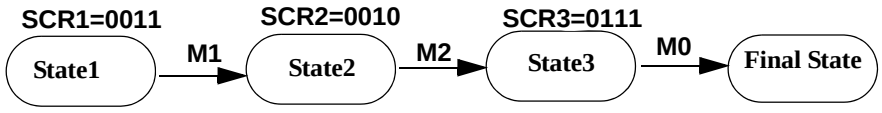


Figure 66. Scenario 1

Scenario 1 is possible with S12SDBGV1 SCR encoding

Table 354. CPMURTI Field Descriptions

Field	Description
7 RTDEC	**Decimal or Binary Divider Select Bit** — RTDEC selects decimal or binary based prescaler values. 0 Binary based divider value. See Table 355 1 Decimal based divider value. See Table 356
6–4 RTR[6:4]	**Real Time Interrupt Prescale Rate Select Bits** — These bits select the prescale rate for the RTI. See Table 355 and Table 356.
3–0 RTR[3:0]	**Real Time Interrupt Modulus Counter Select Bits** — These bits select the modulus counter target value to provide additional granularity.Table 355 and Table 356 show all possible divide values selectable by the CPMURTI register.

Table 355. RTI Frequency Divide Rates for RTDEC = 0

RTR[3:0]	RTR[6:4] =							
	000 (OFF)	**001 (2^{10})**	**010 (2^{11})**	**011 (2^{12})**	**100 (2^{13})**	**101 (2^{14})**	**110 (2^{15})**	**111 (2^{16})**
0000 (÷1)	OFF(196)	2^{10}	2^{11}	2^{12}	2^{13}	2^{14}	2^{15}	2^{16}
0001 (÷2)	OFF	$2x2^{10}$	$2x2^{11}$	$2x2^{12}$	$2x2^{13}$	$2x2^{14}$	$2x2^{15}$	$2x2^{16}$
0010 (÷3)	OFF	$3x2^{10}$	$3x2^{11}$	$3x2^{12}$	$3x2^{13}$	$3x2^{14}$	$3x2^{15}$	$3x2^{16}$
0011 (÷4)	OFF	$4x2^{10}$	$4x2^{11}$	$4x2^{12}$	$4x2^{13}$	$4x2^{14}$	$4x2^{15}$	$4x2^{16}$
0100 (÷5)	OFF	$5x2^{10}$	$5x2^{11}$	$5x2^{12}$	$5x2^{13}$	$5x2^{14}$	$5x2^{15}$	$5x2^{16}$
0101 (÷6)	OFF	$6x2^{10}$	$6x2^{11}$	$6x2^{12}$	$6x2^{13}$	$6x2^{14}$	$6x2^{15}$	$6x2^{16}$
0110 (÷7)	OFF	$7x2^{10}$	$7x2^{11}$	$7x2^{12}$	$7x2^{13}$	$7x2^{14}$	$7x2^{15}$	$7x2^{16}$
0111 (÷8)	OFF	$8x2^{10}$	$8x2^{11}$	$8x2^{12}$	$8x2^{13}$	$8x2^{14}$	$8x2^{15}$	$8x2^{16}$
1000 (÷9)	OFF	$9x2^{10}$	$9x2^{11}$	$9x2^{12}$	$9x2^{13}$	$9x2^{14}$	$9x2^{15}$	$9x2^{16}$
1001 (÷10)	OFF	$10x2^{10}$	$10x2^{11}$	$10x2^{12}$	$10x2^{13}$	$10x2^{14}$	$10x2^{15}$	$10x2^{16}$
1010 (÷11)	OFF	$11x2^{10}$	$11x2^{11}$	$11x2^{12}$	$11x2^{13}$	$11x2^{14}$	$11x2^{15}$	$11x2^{16}$
1011 (÷12)	OFF	$12x2^{10}$	$12x2^{11}$	$12x2^{12}$	$12x2^{13}$	$12x2^{14}$	$12x2^{15}$	$12x2^{16}$
1100 (÷13)	OFF	$13x2^{10}$	$13x2^{11}$	$13x2^{12}$	$13x2^{13}$	$13x2^{14}$	$13x2^{15}$	$13x2^{16}$
1101 (÷14)	OFF	$14x2^{10}$	$14x2^{11}$	$14x2^{12}$	$14x2^{13}$	$14x2^{14}$	$14x2^{15}$	$14x2^{16}$
1110 (÷15)	OFF	$15x2^{10}$	$15x2^{11}$	$15x2^{12}$	$15x2^{13}$	$15x2^{14}$	$15x2^{15}$	$15x2^{16}$
1111 (÷16)	OFF	$16x2^{10}$	$16x2^{11}$	$16x2^{12}$	$16x2^{13}$	$16x2^{14}$	$16x2^{15}$	$16x2^{16}$

Note:
196. Denotes the default value out of reset.This value should be used to disable the RTI to ensure future backwards compatibility.

Table 356. RTI Frequency Divide Rates for RTDEC=1

RTR[3:0]	RTR[6:4] =							
	000 ($1x10^3$)	**001 ($2x10^3$)**	**010 ($5x10^3$)**	**011 ($10x10^3$)**	**100 ($20x10^3$)**	**101 ($50x10^3$)**	**110 ($100x10^3$)**	**111 ($200x10^3$)**
0000 (÷1)	$1x10^3$	$2x10^3$	$5x10^3$	$10x10^3$	$20x10^3$	$50x10^3$	$100x10^3$	$200x10^3$
0001 (÷2)	$2x10^3$	$4x10^3$	$10x10^3$	$20x10^3$	$40x10^3$	$100x10^3$	$200x10^3$	$400x10^3$

Table 360. Reserved Register (CPMUTEST0)

0x003D

	7	6	5	4	3	2	1	0
R	fmcs_reg_sel0	cpmu_test_gfe0	cpmu_test_xfc_en0	fc_force_en0	vcofrq20	0	fm_test0	test_sqw_osc0
W								
Reset	0	Note 10	0	0	0	0	0	0

1) Power on reset clears the crg_test_gfe bit

= Unimplemented or Reserved

Read: Anytime

Write: Only in Special Mode

Table 361. CPMUTEST0 Field Descriptions

Field	Description
7 fmcs_reg_sel	**FMCS Register Select Bit**— This bit switches either CPMUTEST1 or CPMUFMCS test register to address 0x003E. 0 CPMUTEST1 register is visible on address 0x003E, fm_cs[7:0] of hardmacro driven dynamically (triangular) if fm_enable=1. 1 CPMUFMCS register is visible on address 0x003E, fm_cs[7:0] of hardmacro driven to value of FMCS register.
6 cpmu_test_gfe	**Glitch Filter Enable Test Bit** — This bit goes to the PTI controller, it is intended to enable the RESET pad glitch filter in functional test mode (where it is by default disabled). 0 Glitch Filter disable request 1 Glitch Filter enable request
5 cpmu_test_xfc_en	**XFC Test Pin Enable** — This bit routes the external XFC test pin to the internal filter node. Using this test feature make sure that only one source is driving the internal filter node (FC). So for this case write fc_force_en=0, pfd_force_en=1, pfd_force_up=pfd_force_down=0. 0 external XFC test pin not connected to internal filter node 1 external XFC test pin connected to internal filter node
4 fc_force_en	**FC Force Enable Bit** — This bit allows to force the internal filter node FC to defined values. If fc_force_en=1, REFFRQ[1] bit (in CPMUREFDIV register) selects either 1/2 or 1/3 V_{DDPLL} voltage to be driven on FC node. Using this test feature make sure that only one source is driving the internal filter node (FC). So for this case write cpmu_test_xfc_en=0, pfd_force_en=1, pfd_force_up=pfd_force_down=0. 0 Internal filter node (FC) not driven from defined values (1/2 or 1/3 V_{DDPLL}) 1 If REFFRQ[1]=1 then internal filter node (FC) is driven to $V_{DDPLL}/3$. If REFFRQ[1]=0 then internal filter node (FC) is driven to $V_{DDPLL}/2$.
3 vcofrq2	**VCO gain Bit 2** — This bit selects together with the VCOFRQ[1:0] bits of the CPMUSYNR register the gain of the VtoI converter in the PLL. Setting vcofrq2-0 all to 1 is intended for 160MHz VCOCLK generation.
1 fm_test	**FM test amplitude Bit** — This bit multiplies FM amplitude determined by FM1,FM0 and CPMUFMCS[7:0] by 4. This is to amplify frequency variation on VCOCLK when using PLL test modes (pfd_force_en, fc_force_en). A higher frequency variation is easier to measure on tester. 0 FM amplitude multiplied by 1 1 FM amplitude multiplied by 4
0 test_sqw_osc	**Test square wave enable Bit** — Enables XTAL pin digital input data used for Oscillator test. 0 XTAL pin as digital input disabled 1 XTAL pin as digital input enabled

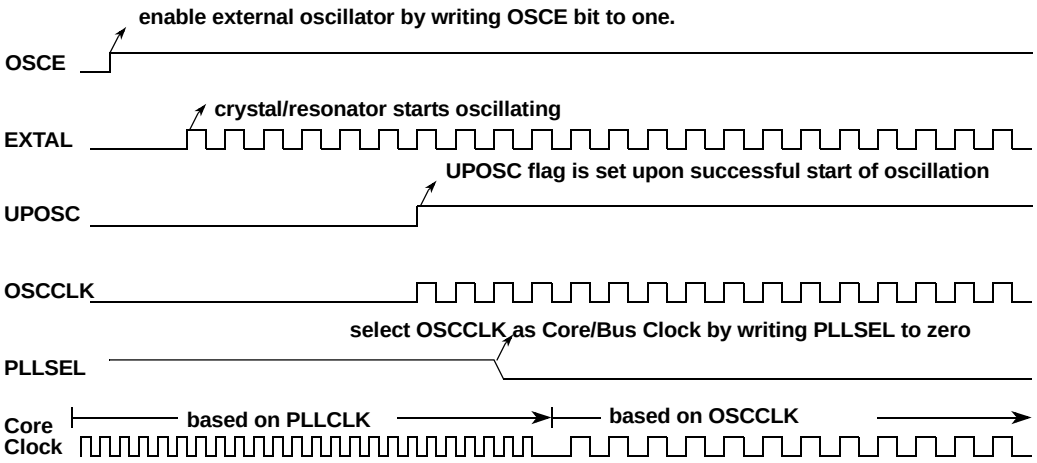


Figure 90. Enabling the External Oscillator

5.38.4.5.2 The Adaptive Oscillator Filter

A spike in the oscillator clock can disturb the function of the modules driven by this clock.

The Adaptive Oscillator Filter includes two features:

1. Filter noise (spikes) from the incoming external oscillator clock. The filter feature is illustrated in Figure 91.

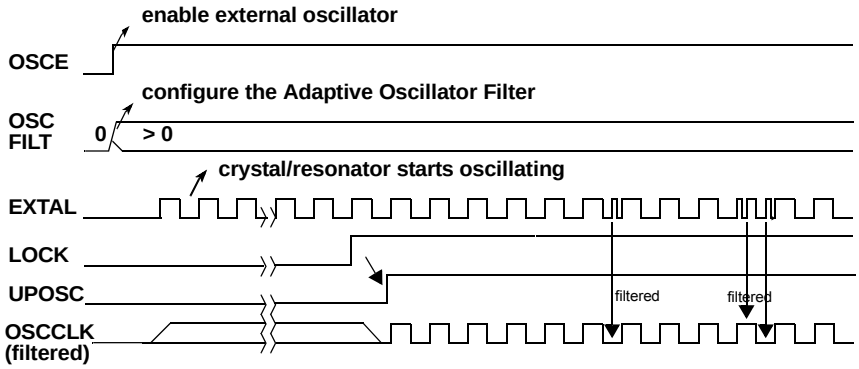


Figure 91. Noise Filtered by the Adaptive Oscillator Filter

2. Detect severe noise disturbance on external oscillator clock which can not be filtered and indicate the critical situation to the software by clearing the UPOSC and LOCK status bit and setting the OSCIF and LOCKIF flag. An example for the detection of critical noise is illustrated in Figure 92

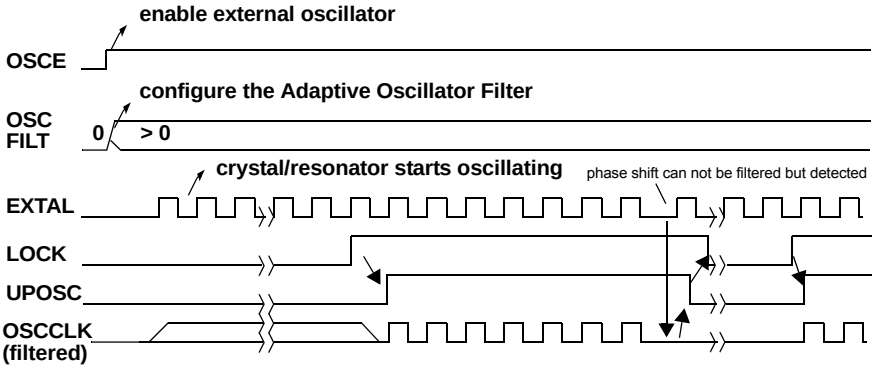


Figure 92. Critical Noise Detected by the Adaptive Oscillator Filter

5.41.1.3.2 D2DI in special modes

The MCU can enter a special mode (used for test and debugging purposes as well as programming the FLASH). In the D2DI the “write-once” feature is disabled. See the MCU description for details.

5.41.2 External Signal Description

The D2DI optionally uses 6 or 10 port pins. The functions of those pins depends on the settings in the D2DCTL0 register, when the D2DI module is enabled.

5.41.2.1 D2DCLK

When the D2DI is enabled this pin is the clock output. This signal is low if the initiator is disabled, in STOP mode (with D2DSWAI asserted), otherwise it is a continuos clock. This pin may be shared with general purpose functionality if the D2DI is disabled.

5.41.2.2 D2DDAT[7:4]

When the D2DI is enabled and the interface connection width D2DCW is set to be 8-bit wide, those lines carry the data bits 7:4 acting as outputs or inputs. When they act as inputs pull-down elements are enabled. If the D2DI is disabled or if the interface connection width is set as 4-bit wide, the pins may be shared with general purpose pin functionality.

5.41.2.3 D2DDAT[3:0]

When the D2DI is enabled those lines carry the data bits 3:0 acting as outputs or inputs. When they act as inputs pull-down elements are enabled. If the D2DI is disabled the pins and may be shared with general purpose pin functionality.

5.41.2.4 D2DINT

The D2DINT is an active input interrupt input driven by the target device. The pin has an active pull-down device. If the D2DI is disabled the pin may be shared with general purpose pin functionality.

Table 497. Signal Properties

Name	Primary (D2DEN=1)	I/O	Secondary (D2DEN=0)	Reset	Comment	Pull down
D2DDAT[7:0]	Bi-directional Data Lines	I/O	GPIO	0	driven low if in STOP mode	Active(236)
D2DCLK	Interface Clock Signal	O	GPIO	0	low if in STOP mode	—
$\overline{\text{D2DINT}}$	Active High Interrupt	I	GPIO	—	—	Active(237)

Note:
236. Active if in input state, only if D2DEN=1
237. only if D2DEN=1

See the port interface module (PIM) guide for details of the GPIO function.

5.41.3 Memory Map and Register Definition

5.41.3.1 Memory Map

The D2DI memory map is split into three sections.

1. An eight-byte set of control registers
2. A 256 byte window for blocking transactions
3. A 256 byte window for non-blocking transactions

See the chapter “Device Memory Map” for the register layout (distribution of these sections).