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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	256
Total RAM Bits	2048
Number of I/O	62
Number of Gates	10000
Voltage - Supply	3V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TC)
Package / Case	84-LCC (J-Lead)
Supplier Device Package	84-PLCC (29.31x29.31)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at40k05al-1ajc

Table 1. AT40KAL Family⁽¹⁾

Device	AT40K05AL	AT40K10AL	AT40K20AL	AT40K40AL
Usable Gates	5K - 10K	10K - 20K	20K - 30K	40K - 50K
Rows x Columns	16 x 16	24 x 24	32 x 32	48 x 48
Cells	256	576	1,024	2,304
Registers	496 ⁽¹⁾	954 ⁽¹⁾	1,520 ⁽¹⁾	3,048 ⁽¹⁾
RAM Bits	2,048	4,608	8,192	18,432
I/O (Maximum)	128	192	256	384

Note: 1. Packages with FCK will have 8 less registers.

Description

The AT40KAL is a family of fully PCI-compliant, SRAM-based FPGAs with distributed 10 ns programmable synchronous/asynchronous, dual-port/single-port SRAM, 8 global clocks, Cache Logic ability (partially or fully reconfigurable without loss of data), automatic component generators, and range in size from 5,000 to 50,000 usable gates. I/O counts range from 128 to 384 in industry standard packages ranging from 84-pin PLCC to 352-ball Square BGA, and support 3.3V designs.

The AT40KAL is designed to quickly implement high-performance, large gate count designs through the use of synthesis and schematic-based tools used on a PC or Sun platform. Atmel's design tools provide seamless integration with industry standard tools such as Synplicity, ModelSim, Exemplar and Viewlogic. See the "IDS Datasheet" available on the Atmel web site (<http://www.atmel.com/atmel/acrobat/doc1421.pdf>) for a list of other supported tools.

The AT40KAL can be used as a coprocessor for high-speed (DSP/processor-based) designs by implementing a variety of computation intensive, arithmetic functions. These include adaptive finite impulse response (FIR) filters, fast Fourier transforms (FFT), convolvers, interpolators and discrete-cosine transforms (DCT) that are required for video compression and decompression, encryption, convolution and other multimedia applications.

Fast, Flexible and Efficient SRAM

The AT40KAL FPGA offers a patented distributed 10 ns SRAM capability where the RAM can be used without losing logic resources. Multiple independent, synchronous or asynchronous, dual-port or single-port RAM functions (FIFO, scratch pad, etc.) can be created using Atmel's macro generator tool.

Fast, Efficient Array and Vector Multipliers

The AT40KAL's patented 8-sided core cell with direct horizontal, vertical and diagonal cell-to-cell connections implements ultra fast array multipliers without using any busing resources. The AT40KAL's Cache Logic capability enables a large number of design coefficients and variables to be implemented in a very small amount of silicon, enabling vast improvement in system speed at much lower cost than conventional FPGAs.

Cache Logic Design

The AT40KAL, AT6000 and FPSLIC families are capable of implementing Cache Logic (dynamic full/partial logic reconfiguration, without loss of data, on-the-fly) for building adaptive logic and systems. As new logic functions are required, they can be loaded into the logic cache without losing the data already there or disrupting the operation of the rest of the chip; replacing or complementing the active logic. The AT40KAL can act as a reconfigurable coprocessor.

Automatic Component Generators

The AT40KAL FPGA family is capable of implementing user-defined, automatically generated, macros in multiple designs; speed and functionality are unaffected by the macro orientation or density of the target device. This enables the fastest, most predictable and efficient FPGA design approach and minimizes design risk by reusing already proven functions. The Automatic Component Generators work seamlessly with industry standard schematic and synthesis tools to create the fastest, most efficient designs available.

The patented AT40KAL series architecture employs a symmetrical grid of small yet powerful cells connected to a flexible busing network. Independently controlled clocks and resets govern every column of cells. The array is surrounded by programmable I/O.

Devices range in size from 5,000 to 50,000 usable gates in the family, and have 256 to 3,048 registers. Pin locations are consistent throughout the AT40KAL series for easy design migration in the same package footprint. The AT40KAL series FPGAs utilize a reliable 0.35 μ triple-metal, CMOS process and are 100% factory-tested. Atmel's PC- and workstation-based integrated development system (IDS) is used to create AT40KAL series designs. Multiple design entry methods are supported.

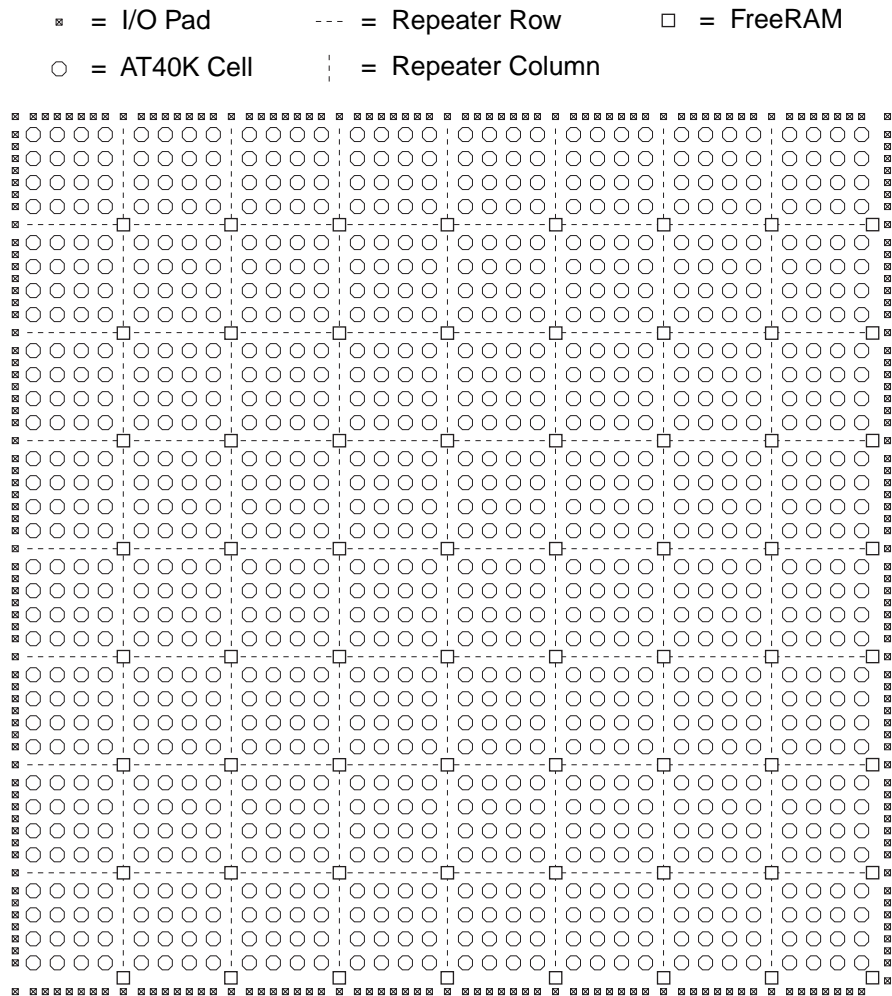
The Atmel architecture was developed to provide the highest levels of performance, functional density and design flexibility in an FPGA. The cells in the Atmel array are small, efficient and can implement any pair of Boolean functions of (the same) three inputs or any single Boolean function of four inputs. The cell's small size leads to arrays with large numbers of cells, greatly multiplying the functionality in each cell. A simple, high-speed busing network provides fast, efficient communication over medium and long distances.

The Symmetrical Array

At the heart of the Atmel architecture is a symmetrical array of identical cells, see Figure 1. The array is continuous from one edge to the other, except for bus repeaters spaced every four cells, see Figure 2 on page 5. At the intersection of each repeater row and column there is a 32 x 4 RAM block accessible by adjacent buses. The RAM can be configured as either a single-ported or dual-ported RAM⁽¹⁾, with either synchronous or asynchronous operation.

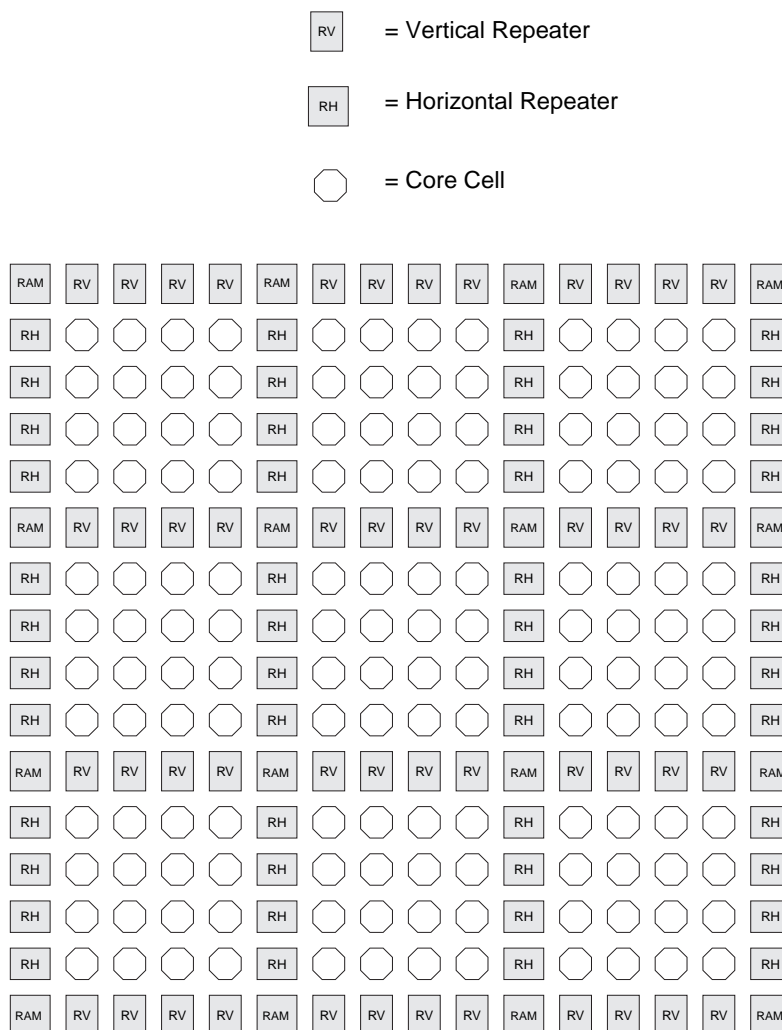
Note: 1. The right-most column can only be used as single-port RAM.

Figure 1. Symmetrical Array Surrounded by I/O (AT40K20AL)⁽¹⁾



Note: 1. AT40KAL has registered I/Os. Group enable on every sector for tri-states on obufe's.

Figure 2. Floor Plan (Representative Portion)⁽¹⁾



Note: 1. Repeaters regenerate signals and can connect any bus to any other bus (all pathways are legal) on the same plane. Each repeater has connections to two adjacent local-bus segments and two express-bus segments. This is done automatically using the integrated development system (IDS) tool.

The Busing Network

Figure 3 on page 7 depicts one of five identical busing planes. Each plane has three bus resources: a local-bus resource (the middle bus) and two express-bus (both sides) resources. Bus resources are connected via repeaters. Each repeater has connections to two adjacent local-bus segments and two express-bus segments. Each local-bus segment spans four cells and connects to consecutive repeaters. Each express-bus segment spans eight cells and “leapfrogs” or bypasses a repeater. Repeaters regenerate signals and can connect any bus to any other bus (all pathways are legal) on the same plane. Although not shown, a local bus can bypass a repeater via a programmable pass gate allowing long on-chip tri-state buses to be created. Local/Local turns are implemented through pass gates in the cell-bus interface. Express/Express turns are implemented through separate pass gates distributed throughout the array.

Some of the bus resources on the AT40KAL are used as a dual-function resources. Table 2 shows which buses are used in a dual-function mode and which bus plane is used. The AT40KAL software tools are designed to accommodate dual-function buses in an efficient manner.

Table 2. Dual-function Buses

Function	Type	Plane(s)	Direction	Comments
Cell Output Enable	Local	5	Horizontal and Vertical	
RAM Output Enable	Express	2	Vertical	Bus full length at array edge Bus in first column to left of RAM block
RAM Write Enable	Express	1	Vertical	Bus full length at array edge Bus in first column to left of RAM block
RAM Address	Express	1 - 5	Vertical	Buses full length at array edge Buses in second column to left of RAM block
RAM Data In	Local	1	Horizontal	Data In connects to local bus plane 1
RAM Data Out	Local	2	Horizontal	Data out connects to local bus plane 2
Clocking	Express	4	Vertical	Bus half length at array edge
Set/Reset	Express	5	Vertical	Bus half length at array edge

Set/Reset Scheme

The AT40KAL family reset scheme is essentially the same as the clock scheme except that there is only one Global Reset. A dedicated Global Set/Reset bus can be driven by any User I/O, except those used for clocking (Global Clocks or Fast Clocks). The automatic placement tool will choose the reset net with the most connections to use the global resources. You can change this by using an RSBUF component in your design to indicate the global reset. Additional resets will use the express bus network.

The Global Set/Reset is distributed to each column of the array. Like Sector Clock mux, there is Sector Set/Reset mux at every four cells. Each sector column of four cells is set/reset by a Plane 5 express bus or Global Set/Reset using the Sector Set/Reset mux, see Figure 11 on page 17. The set/reset provided to each sector column of four cells is either inverted or non-inverted using the Sector Reset mux.

The function of the Set/Reset input of a register is determined by a configuration bit in each cell. The Set/Reset input of a register is active low (logic 0) by default. Setting or Resetting of a register is asynchronous. Before configuration on power-up, a logic 1 (a high) is provided by each register (i.e., all registers are set at power-up).

Absolute Maximum Ratings – 3.3V Commercial/Industrial*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-0.5V to $V_{CC} + 7V$
Supply Voltage (V_{CC})	-0.5V to +7.0V
Maximum Soldering Temp. (10 sec. @ 1/16 in.)	250°C
ESD ($R_{ZAP} = 1.5K$, $C_{ZAP} = 100$ pF)	2000V

*NOTICE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those listed under operating conditions is not implied. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect device reliability.

DC and AC Operating Range – 3.3V Operation

		Commercial	Industrial
Operating Temperature (Case)		0°C - 70°C	-40°C - 85°C
V_{CC} Power Supply		3.3V \pm 0.3V	3.3V \pm 0.3V
Input Voltage Level (CMOS)	High (V_{IHC})	70% - 100% V_{CC}	70% - 100% V_{CC}
	Low (V_{ILC})	0 - 30% V_{CC}	0 - 30% V_{CC}

AC Timing Characteristics – 3.3V Operation

Delays are based on fixed loads and are described in the notes.

Maximum times based on worst case: $V_{CC} = 3.00V$, temperature = $70^{\circ}C$

Minimum times based on best case: $V_{CC} = 3.60V$, temperature = $0^{\circ}C$

Maximum delays are the average of $t_{PD\text{LH}}$ and $t_{PD\text{HL}}$.

Cell Function	Parameter	Path	-1	Units	Notes
Core					
2-input Gate	t_{PD} (Maximum)	x/y -> x/y	1.8	ns	1 unit load
3-input Gate	t_{PD} (Maximum)	x/y/z -> x/y	2.1	ns	1 unit load
3-input Gate	t_{PD} (Maximum)	x/y/w -> x/y	2.2	ns	1 unit load
4-input Gate	t_{PD} (Maximum)	x/y/w/z -> x/y	2.2	ns	1 unit load
Fast Carry	t_{PD} (Maximum)	y -> y	1.4	ns	1 unit load
Fast Carry	t_{PD} (Maximum)	x -> y	1.7	ns	1 unit load
Fast Carry	t_{PD} (Maximum)	y -> x	1.8	ns	1 unit load
Fast Carry	t_{PD} (Maximum)	x -> x	1.5	ns	1 unit load
Fast Carry	t_{PD} (Maximum)	w -> y	2.2	ns	1 unit load
Fast Carry	t_{PD} (Maximum)	w -> x	2.3	ns	1 unit load
Fast Carry	t_{PD} (Maximum)	z -> y	2.3	ns	1 unit load
Fast Carry	t_{PD} (Maximum)	z -> x	1.7	ns	1 unit load
DFF	t_{PD} (Maximum)	q -> x/y	1.8	ns	1 unit load
DFF	t_{PD} (Maximum)	R -> x/y	2.2	ns	1 unit load
DFF	t_{PD} (Maximum)	S -> x/y	2.2	ns	1 unit load
DFF	t_{PD} (Maximum)	q -> w	1.8	ns	
Incremental -> L	t_{PD} (Maximum)	x/y -> L	1.5	ns	1 unit load
Local Output Enable	t_{PZX} (Maximum)	oe -> L	1.4	ns	1 unit load
Local Output Enable	t_{PXZ} (Maximum)	oe -> L	1.8	ns	

AC Timing Characteristics – 3.3V Operation

Delays are based on fixed loads and are described in the notes.

Maximum times based on worst case: $V_{CC} = 3.0V$, temperature = $70^{\circ}C$

Minimum times based on best case: $V_{CC} = 3.6V$, temperature = $0^{\circ}C$

Maximum delays are the average of t_{PDLH} and t_{PDHL} .

All input IO characteristics measured from a V_{IH} of 50% of V_{DD} at the pad (CMOS threshold) to the internal V_{IH} of 50% of V_{DD} . All output IO characteristics are measured as the average of t_{PDLH} and t_{PDHL} to the pad V_{IH} of 50% of V_{DD} .

Cell Function	Parameter	Path	-1	Units	Notes
Repeaters					
Repeater	t_{PD} (Maximum)	L -> E	1.3	ns	1 unit load
Repeater	t_{PD} (Maximum)	E -> E	1.3	ns	1 unit load
Repeater	t_{PD} (Maximum)	L -> L	1.3	ns	1 unit load
Repeater	t_{PD} (Maximum)	E -> L	1.3	ns	1 unit load
Repeater	t_{PD} (Maximum)	E -> IO	0.8	ns	1 unit load
Repeater	t_{PD} (Maximum)	L -> IO	0.8	ns	1 unit load

All input IO characteristics measured from a V_{IH} of 50% of V_{DD} at the pad (CMOS threshold) to the internal V_{IH} of 50% of V_{DD} . All output IO characteristics are measured as the average of t_{PDLH} and t_{PDHL} to the pad V_{IH} of 50% of V_{DD} .

Cell Function	Parameter	Path	-1	Units	Notes
IO					
Input	t_{PD} (Maximum)	pad -> x/y	1.2	ns	No extra delay
Input	t_{PD} (Maximum)	pad -> x/y	3.6	ns	1 extra delay
Input	t_{PD} (Maximum)	pad -> x/y	7.3	ns	2 extra delays
Input	t_{PD} (Maximum)	pad -> x/y	10.8	ns	3 extra delays
Output, Slow	t_{PD} (Maximum)	x/y/E/L -> pad	5.9	ns	50 pf load
Output, Medium	t_{PD} (Maximum)	x/y/E/L -> pad	4.8	ns	50 pf load
Output, Fast	t_{PD} (Maximum)	x/y/E/L -> pad	3.9	ns	50 pf load
Output, Slow	t_{PZX} (Maximum)	oe -> pad	6.2	ns	50 pf load
Output, Slow	t_{PXZ} (Maximum)	oe -> pad	1.3	ns	50 pf load
Output, Medium	t_{PZX} (Maximum)	oe -> pad	4.8	ns	50 pf load
Output, Medium	t_{PXZ} (Maximum)	oe -> pad	1.9	ns	50 pf load
Output, Fast	t_{PZX} (Maximum)	oe -> pad	3.7	ns	50 pf load
Output, Fast	t_{PXZ} (Maximum)	oe -> pad	1.6	ns	50 pf load

AT40K05AL	AT40K10AL	AT40K20AL	AT40K40AL	Left Side (Top to Bottom)				
128 I/O	192 I/O	256 I/O	384 I/O	84 PLCC	100 TQFP	144 LQFP	208 PQFP	240 PQFP
GND	GND	GND	GND	12	1	1	2	1
I/O1, GCK1 (A16)	I/O1, GCK1 (A16)	I/O1, GCK1 (A16)	I/O1, GCK1 (A16)	13	2	2	4	2
I/O2 (A17)	I/O2 (A17)	I/O2 (A17)	I/O2 (A17)	14	3	3	5	3
I/O3	I/O3	I/O3	I/O3			4	6	4
I/O4	I/O4	I/O4	I/O4			5	7	5
I/O5 (A18)	I/O5 (A18)	I/O5 (A18)	I/O5 (A18)	15	4	6	8	6
I/O6 (A19)	I/O6 (A19)	I/O6 (A19)	I/O6 (A19)	16	5	7	9	7
			GND					
			I/O7					
			I/O8					
			I/O9					
			I/O10					
		I/O7	I/O11					
		I/O8	I/O12					
		VCC	VCC					
		GND	GND					
			I/O13					
			I/O14					
I/O7	I/O7	I/O9	I/O15				10	8
I/O8	I/O8	I/O10	I/O16				11	9
	I/O9	I/O11	I/O17				12	10
	I/O10	I/O12	I/O18				13	11
			GND					
			I/O19					
			I/O20					
	I/O11	I/O13	I/O21					12
	I/O12	I/O14	I/O22					13
		I/O15	I/O23					
		I/O16	I/O24					
GND	GND	GND	GND			8	14	14

Note: 1. On-chip tri-state

AT40K05AL	AT40K10AL	AT40K20AL	AT40K40AL	Left Side (Top to Bottom)				
128 I/O	192 I/O	256 I/O	384 I/O	84 PLCC	100 TQFP	144 LQFP	208 PQFP	240 PQFP
I/O9, FCK1	I/O13, FCK1	I/O17, FCK1	I/O25, FCK1			9	15	15
I/O10	I/O14	I/O18	I/O26			10	16	16
I/O11 (A20)	I/O15 (A20)	I/O19 (A20)	I/O27 (A20)	17	6	11	17	17
I/O12 (A21)	I/O16 (A21)	I/O20 (A21)	I/O28 (A21)	18	7	12	18	18
	VCC	VCC	VCC					19
	I/O17	I/O21	I/O29					20
	I/O18	I/O22	I/O30					21
			GND					
			I/O31					
			I/O32					
			I/O33					
			I/O34					
		I/O23	I/O35					
		I/O24	I/O36					
		GND	GND					22
			VCC					
			I/O37					
			I/O38					
		I/O25	I/O39					
		I/O26	I/O40					
	I/O19	I/O27	I/O41				19	23
	I/O20	I/O28	I/O42				20	24
			GND					
I/O13	I/O21	I/O29	I/O43			13	21	25
I/O14	I/O22	I/O30	I/O44		8	14	22	26
			I/O45					
			I/O46					
I/O15 (A22)	I/O23 (A22)	I/O31 (A22)	I/O47 (A22)	19	9	15	23	27
I/O16 (A23)	I/O24 (A23)	I/O32 (A23)	I/O48 (A23)	20	10	16	24	28
GND	GND	GND	GND	21	11	17	25	29
VCC	VCC	VCC	VCC	22	12	18	26	30

Note: 1. On-chip tri-state

AT40K05AL	AT40K10AL	AT40K20AL	AT40K40AL	Bottom Side (Left to Right)				
128 I/O	192 I/O	256 I/O	384 I/O	84 PLCC	100 TQFP	144 LQFP	208 PQFP	240 PQFP
VCC	VCC	VCC	VCC	33	25	37	55	61
M2	M2	M2	M2	34	26	38	56	62
I/O33, GCK3	I/O49, GCK3	I/O65, GCK3	I/O97, GCK3	35	27	39	57	63
I/O34 (HDC)	I/O50 (HDC)	I/O66 (HDC)	I/O98 (HDC)	36	28	40	58	64
I/O35	I/O51	I/O67	I/O99			41	59	65
I/O36	I/O52	I/O68	I/O100			42	60	66
I/O37	I/O53	I/O69	I/O101		29	43	61	67
I/O38 (LDC)	I/O54 (LDC)	I/O70 (LDC)	I/O102 (LDC)	37	30	44	62	68
			GND					
			I/O103					
			I/O104					
			I/O105					
			I/O106					
		I/O71	I/O107					
		I/O72	I/O108					
		VCC	VCC					
		GND	GND					
I/O39	I/O55	I/O73	I/O109				63	69
I/O40	I/O56	I/O74	I/O110				64	70
	I/O57	I/O75	I/O111				65	71
	I/O58	I/O76	I/O112				66	72
			I/O113					
			I/O114					
			GND					
		I/O77	I/O115					
		I/O78	I/O116					
	I/O59	I/O79	I/O117					73
	I/O60	I/O80	I/O118					74
			I/O119					
			I/O120					
GND	GND	GND	GND			45	67	75
I/O41	I/O61	I/O81	I/O121			46	68	76

AT40K05AL	AT40K10AL	AT40K20AL	AT40K40AL	Bottom Side (Left to Right)				
128 I/O	192 I/O	256 I/O	384 I/O	84 PLCC	100 TQFP	144 LQFP	208 PQFP	240 PQFP
I/O42	I/O62	I/O82	I/O122			47	69	77
I/O43	I/O63	I/O83	I/O123	38	31	48	70	78
I/O44	I/O64	I/O84	I/O124	39	32	49	71	79
	VCC	VCC	VCC					80
	I/O65	I/O85	I/O125				72	81
	I/O66	I/O86	I/O126				73	82
			GND					
			I/O127					
			I/O128					
			I/O129					
			I/O130					
		I/O87	I/O131					
		I/O88	I/O132					
		GND	GND					83
			VCC					
		I/O89	I/O133					
		I/O90	I/O134					
	I/O67	I/O91	I/O135					84
	I/O68	I/O92	I/O136					85
I/O45	I/O69	I/O93	I/O137		33	50	74	86
I/O46	I/O70	I/O94	I/O138		34	51	75	87
			GND					
			I/O139					
			I/O140					
			I/O141					
			I/O142					
I/O47 (D15)	I/O71 (D15)	I/O95 (D15)	I/O143 (D15)	40	35	52	76	88
I/O48 (INIT)	I/O72 (INIT)	I/O96 (INIT)	I/O144 (INIT)	41	36	53	77	89
VCC	VCC	VCC	VCC	42	37	54	78	90
GND	GND	GND	GND	43	38	55	79	91
I/O49 (D14)	I/O73 (D14)	I/O97 (D14)	I/O145 (D14)	44	39	56	80	92
I/O50 (D13)	I/O74 (D13)	I/O98 (D13)	I/O146 (D13)	45	40	57	81	93

AT40K05AL	AT40K10AL	AT40K20AL	AT40K40AL	Bottom Side (Left to Right)				
128 I/O	192 I/O	256 I/O	384 I/O	84 PLCC	100 TQFP	144 LQFP	208 PQFP	240 PQFP
			I/O174					
			GND					
			I/O175					
			I/O176					
	I/O87	I/O117	I/O177				91	109
	I/O88	I/O118	I/O178				92	110
I/O57	I/O89	I/O119	I/O179				93	111
I/O58	I/O90	I/O120	I/O180				94	112
		GND	GND					
		VCC	VCC					
		I/O121	I/O181					
		I/O122	I/O182					
I/O59 (D10)	I/O91 (D10)	I/O123 (D10)	I/O183 (D10)	48	45	65	95	113
I/O60 (D9)	I/O92 (D9)	I/O124 (D9)	I/O184 (D9)	49	46	66	96	114
			I/O185					
			I/O186					
			GND					
			I/O187					
			I/O188					
I/O61	I/O93	I/O125	I/O189			67	97	115
I/O62	I/O94	I/O126	I/O190			68	98	116
I/O63 (D8)	I/O95 (D8)	I/O127 (D8)	I/O191 (D8)	50	47	69	99	117
I/O64, GCK4	I/O96, GCK4	I/O128, GCK4	I/O192, GCK4	51	48	70	100	118
GND	GND	GND	GND	52	49	71	101	119
$\overline{\text{CON}}$	$\overline{\text{CON}}$	$\overline{\text{CON}}$	$\overline{\text{CON}}$	53	50	72	103	120

AT40K05AL	AT40K10AL	AT40K20AL	AT40K40AL	Top Side (Right to Left)				
128 I/O	192 I/O	256 I/O	384 I/O	84 PLCC	100 TQFP	144 LQFP	208 PQFP	240 PQFP
GND	GND	GND	GND	76	77	110	160	182
I/O97 (A0)	I/O145 (A0)	I/O193 (A0)	I/O289 (A0)	77	78	111	161	183
I/O98, GCK7 (A1)	I/O146, GCK7 (A1)	I/O194, GCK7 (A1)	I/O290, GCK7 (A1)	78	79	112	162	184
I/O99	I/O147	I/O195	I/O291			113	163	185
I/O100	I/O148	I/O196	I/O292			114	164	186
			I/O293					
			I/O294					
			GND					
			I/O295					
			I/O296					
I/O101 ($\overline{\text{CS1}}$, A2)	I/O149 ($\overline{\text{CS1}}$, A2)	I/O197 ($\overline{\text{CS1}}$, A2)	I/O297 ($\overline{\text{CS1}}$, A2)	79	80	115	165	187
I/O102 (A3)	I/O150 (A3)	I/O198 (A3)	I/O298 (A3)	80	81	116	166	188
		I/O199	I/O299					
		I/O200	I/O300					
		VCC	VCC					
		GND	GND					
	I/O151 ⁽¹⁾	I/O201 ⁽¹⁾	I/O301 ⁽¹⁾	75 ⁽¹⁾ NC	76 ⁽¹⁾ NC	109 ⁽¹⁾ NC	159 ⁽¹⁾ NC	189 ⁽¹⁾ NC
	I/O152	I/O202	I/O302					190
I/O103	I/O153	I/O203	I/O303			117	167	191
I/O104 ⁽¹⁾	I/O154	I/O204	I/O304				168	192
			I/O305					
			I/O306					
			GND					
			I/O307					
			I/O308					
	I/O155	I/O205	I/O309				169	193
	I/O156	I/O206	I/O310				170	194
		I/O207	I/O311					195
		I/O208	I/O312					
GND	GND	GND	GND			118	171	196

Note: 1. Shared with TSTCLK. No Connect.



AT40K05AL	AT40K10AL	AT40K20AL	AT40K40AL	Top Side (Right to Left)				
128 I/O	192 I/O	256 I/O	384 I/O	84 PLCC	100 TQFP	144 LQFP	208 PQFP	240 PQFP
I/O105	I/O157	I/O209	I/O313			119	172	197
I/O106	I/O158	I/O210	I/O314			120	173	198
	I/O159	I/O211	I/O315					199
	I/O160	I/O212	I/O316					200
	VCC	VCC	VCC					201
		I/O213	I/O317					
		I/O214	I/O318					
			GND					
			I/O319					
			I/O320					
			I/O321					
			I/O322					
		I/O215	I/O323					
		I/O216	I/O324					
		GND	GND					
			VCC					
I/O107 (A4)	I/O161 (A4)	I/O217 (A4)	I/O325 (A4)	81	82	121	174	202
I/O108 (A5)	I/O162 (A5)	I/O218 (A5)	I/O326 (A5)	82	83	122	175	203
	I/O163	I/O219	I/O327				176	205
	I/O164	I/O220	I/O328				177	206
I/O109	I/O165	I/O221	I/O329		84	123	178	207
I/O110	I/O166	I/O222	I/O330		85	124	179	208
			GND					
			I/O331					
			I/O332					
			I/O333					
			I/O334					
I/O111 (A6)	I/O167 (A6)	I/O223 (A6)	I/O335 (A6)	83	86	125	180	209
I/O112 (A7)	I/O168 (A7)	I/O224 (A7)	I/O336 (A7)	84	87	126	181	210
GND	GND	GND	GND	1	88	127	182	211
VCC	VCC	VCC	VCC	2	89	128	183	212

Note: 1. Shared with TSTCLK. No Connect.

AT40K05AL	AT40K10AL	AT40K20AL	AT40K40AL	Top Side (Right to Left)				
128 I/O	192 I/O	256 I/O	384 I/O	84 PLCC	100 TQFP	144 LQFP	208 PQFP	240 PQFP
		I/O242	I/O362					
	I/O181	I/O243	I/O363				195	228
	I/O182	I/O244	I/O364				196	229
			I/O365					
			I/O366					
			GND					
			I/O367					
			I/O368					
I/O121	I/O183	I/O245	I/O369				197	230
I/O122	I/O184	I/O246	I/O370				198	231
I/O123 (A12)	I/O185 (A12)	I/O247 (A12)	I/O371 (A12)	7	96	138	199	232
I/O124 (A13)	I/O186 (A13)	I/O248 (A13)	I/O372 (A13)	8	97	139	200	233
		GND	GND					
		VCC	VCC					
		I/O249	I/O373					
		I/O250	I/O374					
			I/O375					
			I/O376					
			I/O377					
			I/O378					
			GND					
	I/O187	I/O251	I/O379					234
	I/O188	I/O252	I/O380					235
I/O125	I/O189	I/O253	I/O381			140	201	236
I/O126	I/O190	I/O254	I/O382			141	202	237
I/O127 (A14)	I/O191 (A14)	I/O255 (A14)	I/O383 (A14)	9	98	142	203	238
I/O128, GCK8 (A15)	I/O192, GCK8 (A15)	I/O256, GCK8 (A15)	I/O384, GCK8 (A15)	10	99	143	204	239
VCC	VCC	VCC	VCC	11	100	144	205	240

Note: 1. Shared with TSTCLK. No Connect.

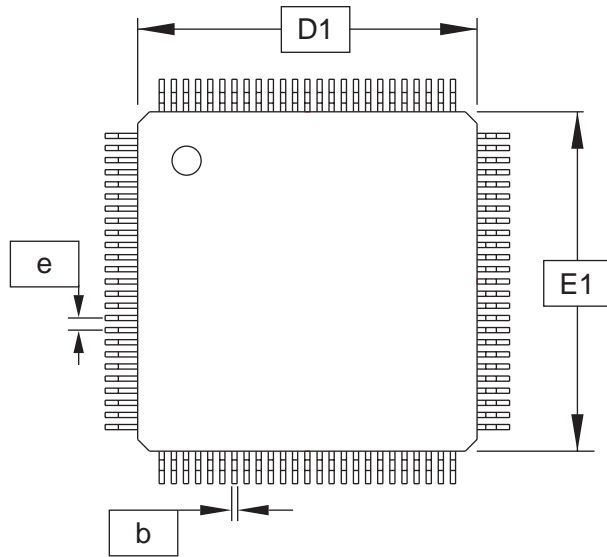
Part/Package Availability and User I/O Counts (including Dual-function Pins)

Package ⁽¹⁾	AT40K05AL	AT40K10AL	AT40K20AL	AT40K40AL
84 PLCC	62	62	–	62
100 TQFP	78	78	78	–
144 LQFP	114	114	114	114
208 PQFP	128	161	161	161
240 PQFP	–	–	–	193

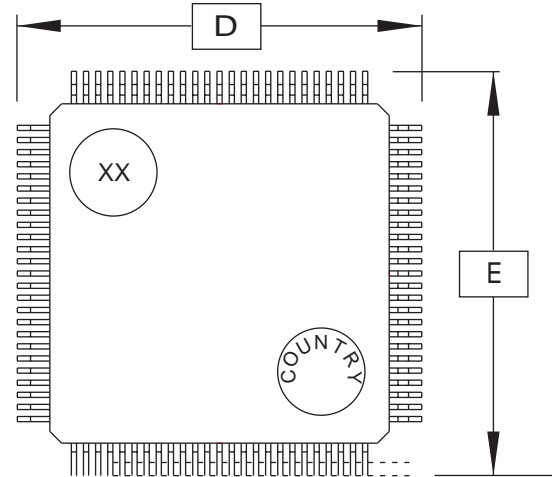
Note: 1. Devices in same package are pin-to-pin compatible.

Package Type	
84J	84-lead, Plastic J-leaded Chip Carrier (PLCC)
100T1	100-lead, Thin (1.0 mm) Plastic Quad Flat Package (TQFP)
144L1	144-lead, Low-profile (1.4 mm) Plastic Quad Flat Package (LQFP)
208Q1	208-lead, Plastic Quad Flat Package (PQFP)
240Q1	240-lead, Plastic Quad Flat Package (PQFP)

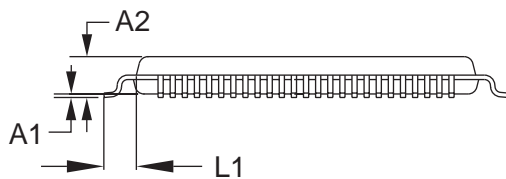
100T1 – TQFP



Top View



Bottom View



Side View

COMMON DIMENSIONS (Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A1	0.05		0.15	6
A2	0.95	1.00	1.05	
D	16.00 BSC			
D1	14.00 BSC			2, 3
E	16.00 BSC			
E1	14.00 BSC			2, 3
e	0.50 BSC			
b	0.17	0.22	0.27	4, 5
L1	1.00 REF			

- Notes: 1. This drawing is for general information only. Refer to JEDEC Drawing MO-153, Variation AA, for proper dimensions, tolerances, datums, etc.
2. The top package body size may be smaller than the bottom package size by as much as 0.15 mm.
3. Dimensions D1 and E1 do not include mold protrusions. Allowable protrusion is 0.25 mm per side. D1 and E1 are maximum plastic body size dimensions, including mold mismatch.
4. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall not cause the lead width to exceed the maximum b dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 and 0.5 mm pitch packages.
5. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
6. A1 is defined as the distance from the seating place to the lowest point on the package body.

11/30/01



2325 Orchard Parkway
San Jose, CA 95131

TITLE

100T1, 100-lead (14 x 14 x 1.0 mm Body), Thin Plastic
Quad Flat Pack (TQFP)

DRAWING NO.

100T1

REV.

A



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