Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	256
Total RAM Bits	2048
Number of I/O	128
Number of Gates	10000
Voltage - Supply	3V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TC)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at40k05al-1dqc

Cache Logic Design

The AT40KAL, AT6000 and FPSLIC families are capable of implementing Cache Logic (dynamic full/partial logic reconfiguration, without loss of data, on-the-fly) for building adaptive logic and systems. As new logic functions are required, they can be loaded into the logic cache without losing the data already there or disrupting the operation of the rest of the chip; replacing or complementing the active logic. The AT40KAL can act as a reconfigurable coprocessor.

Automatic Component Generators

The AT40KAL FPGA family is capable of implementing user-defined, automatically generated, macros in multiple designs; speed and functionality are unaffected by the macro orientation or density of the target device. This enables the fastest, most predictable and efficient FPGA design approach and minimizes design risk by reusing already proven functions. The Automatic Component Generators work seamlessly with industry standard schematic and synthesis tools to create the fastest, most efficient designs available.

The patented AT40KAL series architecture employs a symmetrical grid of small yet powerful cells connected to a flexible busing network. Independently controlled clocks and resets govern every column of cells. The array is surrounded by programmable I/O.

Devices range in size from 5,000 to 50,000 usable gates in the family, and have 256 to 3,048 registers. Pin locations are consistent throughout the AT40KAL series for easy design migration in the same package footprint. The AT40KAL series FPGAs utilize a reliable 0.35µ triple-metal, CMOS process and are 100% factory-tested. Atmel's PC- and workstation-based integrated development system (IDS) is used to create AT40KAL series designs. Multiple design entry methods are supported.

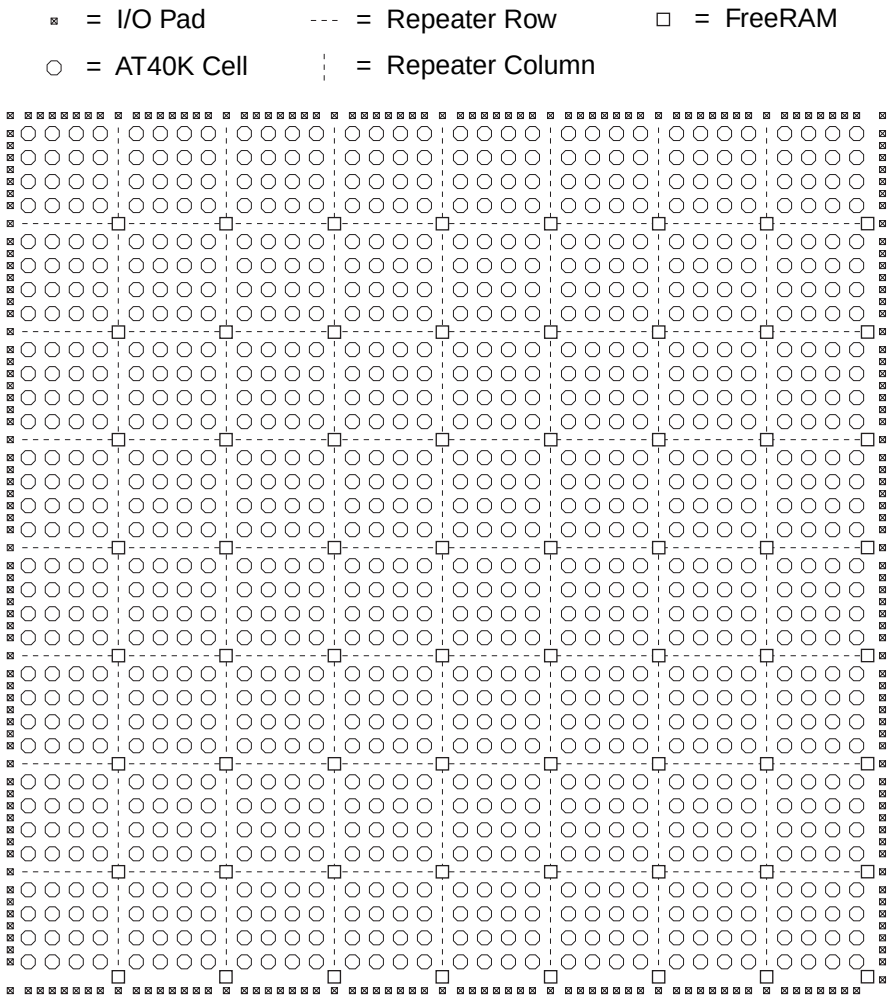
The Atmel architecture was developed to provide the highest levels of performance, functional density and design flexibility in an FPGA. The cells in the Atmel array are small, efficient and can implement any pair of Boolean functions of (the same) three inputs or any single Boolean function of four inputs. The cell's small size leads to arrays with large numbers of cells, greatly multiplying the functionality in each cell. A simple, high-speed busing network provides fast, efficient communication over medium and long distances.

The Symmetrical Array

At the heart of the Atmel architecture is a symmetrical array of identical cells, see Figure 1. The array is continuous from one edge to the other, except for bus repeaters spaced every four cells, see Figure 2 on page 5. At the intersection of each repeater row and column there is a 32 x 4 RAM block accessible by adjacent buses. The RAM can be configured as either a single-ported or dual-ported RAM(1), with either synchronous or asynchronous operation.

Note: 1. The right-most column can only be used as single-port RAM.

Figure 1. Symmetrical Array Surrounded by I/O (AT40K20AL)(1)



Note: 1. AT40KAL has registered I/Os. Group enable on every sector for tri-states on obufe's.

The Busing Network

Figure 3 on page 7 depicts one of five identical busing planes. Each plane has three bus resources: a local-bus resource (the middle bus) and two express-bus (both sides) resources. Bus resources are connected via repeaters. Each repeater has connections to two adjacent local-bus segments and two express-bus segments. Each local-bus segment spans four cells and connects to consecutive repeaters. Each express-bus segment spans eight cells and “leapfrogs” or bypasses a repeater. Repeaters regenerate signals and can connect any bus to any other bus (all pathways are legal) on the same plane. Although not shown, a local bus can bypass a repeater via a programmable pass gate allowing long on-chip tri-state buses to be created. Local/Local turns are implemented through pass gates in the cell-bus interface. Express/Express turns are implemented through separate pass gates distributed throughout the array.

Some of the bus resources on the AT40KAL are used as a dual-function resources. Table 2 shows which buses are used in a dual-function mode and which bus plane is used. The AT40KAL software tools are designed to accommodate dual-function buses in an efficient manner.

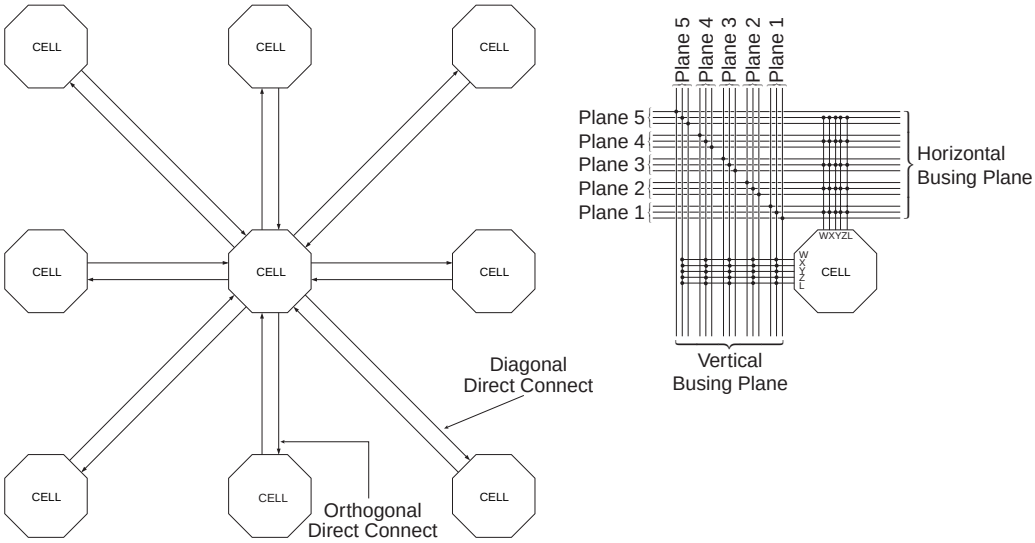
Table 2. Dual-function Buses

Function	Type	Plane(s)	Direction	Comments
Cell Output Enable	Local	5	Horizontal and Vertical	
RAM Output Enable	Express	2	Vertical	Bus full length at array edge Bus in first column to left of RAM block
RAM Write Enable	Express	1	Vertical	Bus full length at array edge Bus in first column to left of RAM block
RAM Address	Express	1 - 5	Vertical	Buses full length at array edge Buses in second column to left of RAM block
RAM Data In	Local	1	Horizontal	Data In connects to local bus plane 1
RAM Data Out	Local	2	Horizontal	Data out connects to local bus plane 2
Clocking	Express	4	Vertical	Bus half length at array edge
Set/Reset	Express	5	Vertical	Bus half length at array edge

Cell Connections

Figure 4(a) depicts direct connections between a cell and its eight nearest neighbors. Figure 4(b) shows the connections between a cell and five horizontal local buses (1 per busing plane) and five vertical local buses (1 per busing plane).

Figure 4. Cell Connections



(a) Cell-to-cell Connections

(b) Cell-to-bus Connections

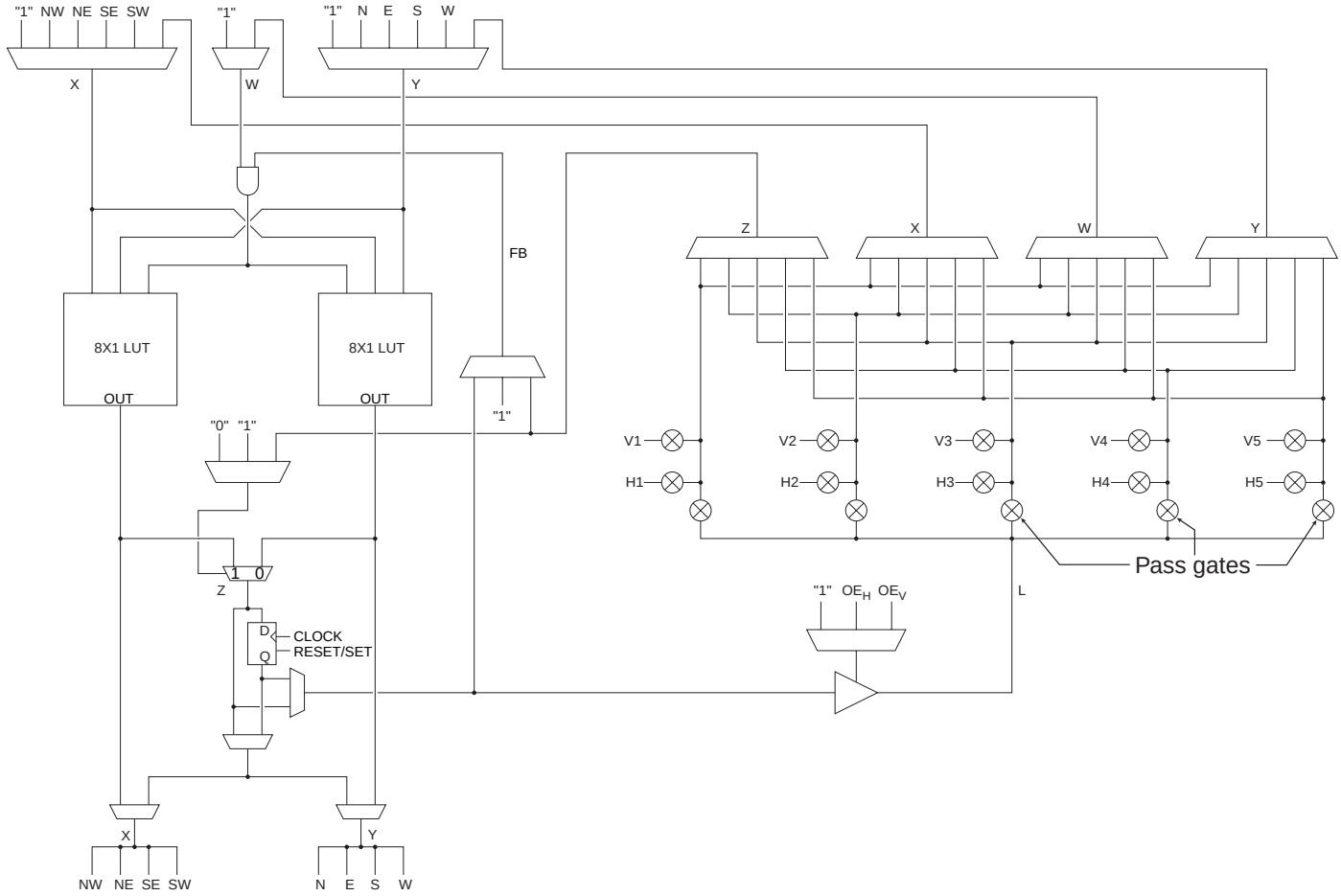
The Cell

Figure 5 depicts the AT40KAL cell. Configuration bits for separate muxes and pass gates are independent. All permutations of programmable muxes and pass gates are legal. V_n (V_1 - V_5) is connected to the vertical local bus in plane n. H_n (H_1 - H_5) is connected to the horizontal local bus in plane *n*. A local/local turn in plane n is achieved by turning on the two pass gates connected to V_n and H_n. Pass gates are opened to let signals into the cell from a local bus or to drive a signal out onto a local bus. Signals coming into the logic cell on one local bus plane can be switched onto another plane by opening two of the pass gates. This allows bus signals to switch planes to achieve greater route ability. Up to five simultaneous local/local turns are possible.

The AT40KAL FPGA core cell is a highly configurable logic block based around two 3-input LUTs (8 x 1 ROM), which can be combined to produce one 4-input LUT. This means that any core cell can implement two functions of 3 inputs or one function of 4 inputs. There is a Set/Reset D flip-flop in every cell, the output of which may be tri-stated and fed back internally within the core cell. There is also a 2-to-1 multiplexer in every cell, and an upstream AND gate in the “front end” of the cell. This AND gate is an important feature in the implementation of efficient array multipliers.

With this functionality in each core cell, the core cell can be configured in several “modes”. The core cell flexibility makes the AT40KAL architecture well suited to most digital design application areas, see Figure 6.

Figure 5. The Cell



X = Diagonal Direct Connect or Bus
Y = Orthogonal Direct Connect or Bus
W = Bus Connection
Z = Bus Connection
FB = Internal Feedback

Clocking Scheme

There are eight Global Clock buses (GCK1 - GCK8) on the AT40KAL FPGA. Each of the eight dedicated Global Clock buses is connected to one of the dual-use Global Clock pins. Any clocks used in the design should use global clocks where possible: this can be done by using Assign Pin Locks to lock the clocks to the Global Clock locations. In addition to the eight Global Clocks, there are four Fast Clocks (FCK1 - FCK4), two per edge column of the array for PCI specification. For AT40KAL FPGAs, even the derived clocks can be routed through the Global network. Access points are provided in the corners of the array to route the derived clocks into the global clock network. The IDS software tools handle derived clocks to global clock connections automatically if used.

Each column of an array has a “Column Clock mux” and a “Sector Clock mux”. The Column Clock mux is at the top of every column of an array and the Sector Clock mux is at every four cells. The Column Clock mux is selected from one of the eight Global Clock buses. The clock provided to each sector column of four cells is inverted, non-inverted or tied off to “0”, using the Sector Clock mux to minimize the power consumption in a sector that has no clocks. The clock can either come from the Column Clock or from the Plane 4 express bus, see Figure 10 on page 15. The extreme-left Column Clock mux has two additional inputs, FCK1 and FCK2, to provide fast clocking to left-side I/Os. The extreme-right Column Clock mux has two additional inputs as well, FCK3 and FCK4, to provide fast clocking to right-side I/Os.

The register in each cell is triggered on a rising clock edge by default. Before configuration on power-up, constant “0” is provided to each register’s clock pins. After configuration on power-up, the registers either set or reset, depending on the user’s choice.

The clocking scheme is designed to allow efficient use of multiple clocks with low clock skew, both within a column and across the core cell array.

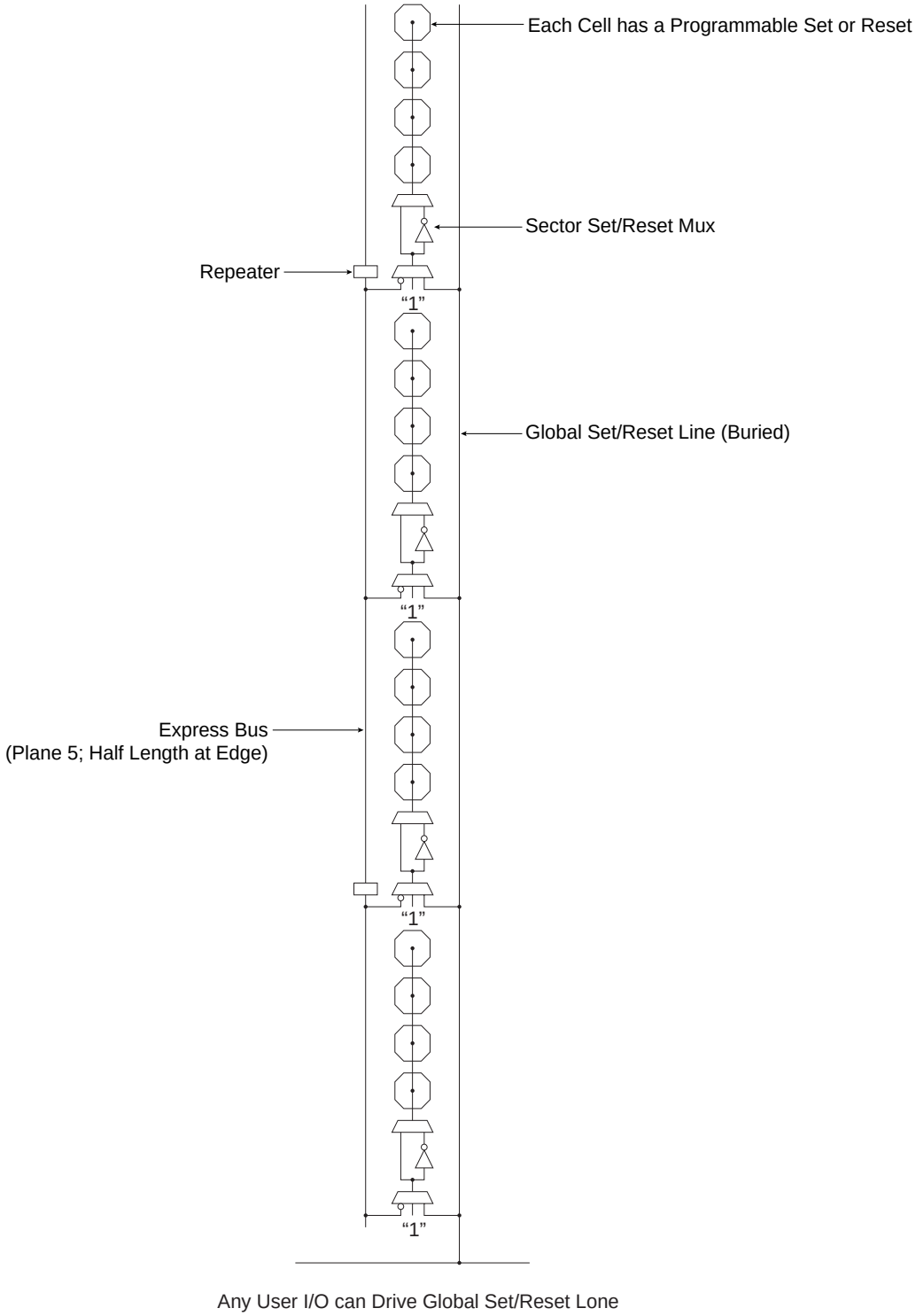
Set/Reset Scheme

The AT40KAL family reset scheme is essentially the same as the clock scheme except that there is only one Global Reset. A dedicated Global Set/Reset bus can be driven by any User I/O, except those used for clocking (Global Clocks or Fast Clocks). The automatic placement tool will choose the reset net with the most connections to use the global resources. You can change this by using an RSBUF component in your design to indicate the global reset. Additional resets will use the express bus network.

The Global Set/Reset is distributed to each column of the array. Like Sector Clock mux, there is Sector Set/Reset mux at every four cells. Each sector column of four cells is set/reset by a Plane 5 express bus or Global Set/Reset using the Sector Set/Reset mux, see Figure 11 on page 17. The set/reset provided to each sector column of four cells is either inverted or non-inverted using the Sector Reset mux.

The function of the Set/Reset input of a register is determined by a configuration bit in each cell. The Set/Reset input of a register is active low (logic 0) by default. Setting or Resetting of a register is asynchronous. Before configuration on power-up, a logic 1 (a high) is provided by each register (i.e., all registers are set at power-up).

Figure 11. Set/Reset (for One Column of Cells)



DC Characteristics – 3.3V Operation Commercial/Industrial

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{IH}	High-level Input Voltage	CMOS	0.7 V_{CC}		5.5V	V
V_{IL}	Low-level Input Voltage	CMOS	-0.3		30% V_{CC}	V
V_{OH}	High-level Output Voltage	I_{OH} = 4 mA V_{CC} = V_{CC} minimum	2.1			V
		I_{OH} = 12 mA V_{CC} = 3.0V	2.1			V
		I_{OH} = 16 mA V_{CC} = 3.0V	2.1			V
V_{OL}	Low-level Output Voltage	I_{OL} = -4 mA V_{CC} = 3.0V			0.4	V
		I_{OL} = -12 mA V_{CC} = 3.0V			0.4	V
		I_{OL} = -16 mA V_{CC} = 3.0V			0.4	V
I_{IH}	High-level Input Current	V_{IN} = V_{CC} Maximum			10.0	µA
		With pull-down, V_{IN} = V_{CC}	75.0	150.0	300.0	µA
I_{IL}	Low-level Input Current	V_{IN} = V_{SS}	-10.0			µA
		With pull-up, V_{IN} = V_{SS}	-300.0	-150.0	-75.0	µA
I_{OZH}	High-level Tri-state Output Leakage Current	Without pull-down, V_{IN} = V_{CC} Maximum			10.0	µA
		With pull-down, V_{IN} = V_{CC} Maximum	75.0	150.0	300.0	µA
I_{OZL}	Low-level Tri-state Output Leakage Current	Without pull-up, V_{IN} = V_{SS}	-10.0			mA
		With pull-up, V_{IN} = V_{SS}	CON = -500 µA TO -125 µA	-150.0	CON = -500 µA TO -125 µA	µA
I_{CC}	Standby Current Consumption	Standby, unprogrammed		0.6	1.0	mA
C_{IN}	Input Capacitance	All pins			10.0	pF

Note: 1. Parameter based on characterization and simulation; it is not tested in production.

Power-On Power Supply Requirements

Atmel FPGAs require a minimum rated power supply current capacity to insure proper initialization, and the power supply ramp-up time does affect the current required. A fast ramp-up time requires more current than a slow ramp-up time.

Table 3. Power-On Power Supply Requirements[1]

Device	Description	Maximum Current[2][3]
AT40K05AL AT40K10AL	Maximum Current Supply	50 mA
AT40K20AL AT40K40AL	Maximum Current Supply	100 mA

Notes:
1. This specification applies to Commercial and Industrial grade products only.
2. Devices are guaranteed to initialize properly at 50% of the minimum current listed above. A larger capacity power supply may result in a larger initialization current.
3. Ramp-up time is measured from 0 V DC to 3.6 V DC. Peak current required lasts less than 2 ms, and occurs near the internal power on reset threshold voltage.

AC Timing Characteristics – 3.3V Operation

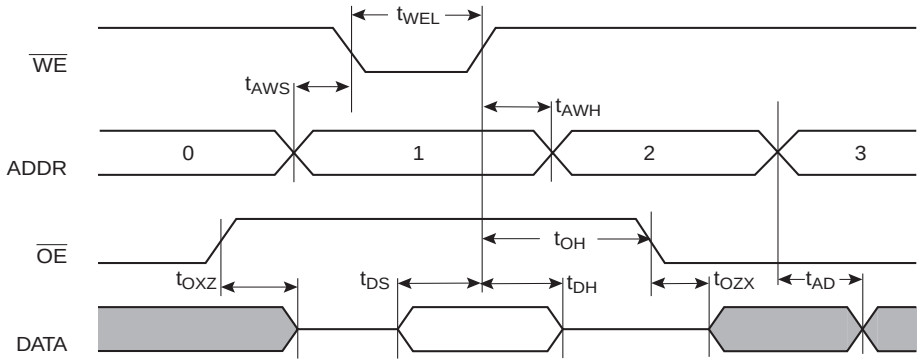
Delays are based on fixed loads and are described in the notes.
Maximum times based on worst case: V_{CC} = 3.0V, temperature = 70°C
Minimum times based on best case: V_{CC} = 3.6V, temperature = 0°C

Cell Function	Parameter	Path	-1	Units	Notes
Async RAM					
Write	t_{WECYC} (Minimum)	cycle time	12.0	ns	
Write	t_{WEL} (Minimum)	we	5.0	ns	Pulse width low
Write	t_{WEH} (Minimum)	we	5.0	ns	Pulse width high
Write	t_{AWS} (Minimum)	wr addr setup -> we	5.3	ns	
Write	t_{AWH} (Minimum)	wr addr hold -> we	0.0	ns	
Write	t_{DS} (Minimum)	din setup -> we	5.0	ns	
Write	t_{DH} (Minimum)	din hold -> we	0.0	ns	
Write/Read	t_{DD} (Maximum)	din -> dout	8.7	ns	rd addr = wr addr
Read	t_{AD} (Maximum)	rd addr -> dout	6.3	ns	
Read	t_{OZX} (Maximum)	oe -> dout	2.9	ns	
Read	t_{OXZ} (Maximum)	oe -> dout	3.5	ns	
Sync RAM					
Write	t_{CYC} (Minimum)	cycle time	12.0	ns	
Write	t_{CLKL} (Minimum)	clk	5.0	ns	Pulse width low
Write	t_{CLKH} (Minimum)	clk	5.0	ns	Pulse width high
Write	t_{WCS} (Minimum)	we setup -> clk	3.2	ns	
Write	t_{WCH} (Minimum)	we hold -> clk	0.0	ns	
Write	t_{ACS} (Minimum)	wr addr setup -> clk	5.0	ns	
Write	t_{ACH} (Minimum)	wr addr hold -> clk	0.0	ns	
Write	t_{DCS} (Minimum)	wr data setup -> clk	3.9	ns	
Write	t_{DCH} (Minimum)	wr data hold -> clk	0.0	ns	
Write/Read	t_{CD} (Maximum)	clk -> dout	5.8	ns	rd addr = wr addr
Read	t_{AD} (Maximum)	rd addr -> dout	6.3	ns	
Read	t_{OZX} (Maximum)	oe -> dout	2.9	ns	
Read	t_{OXZ} (Maximum)	oe -> dout	3.5	ns	

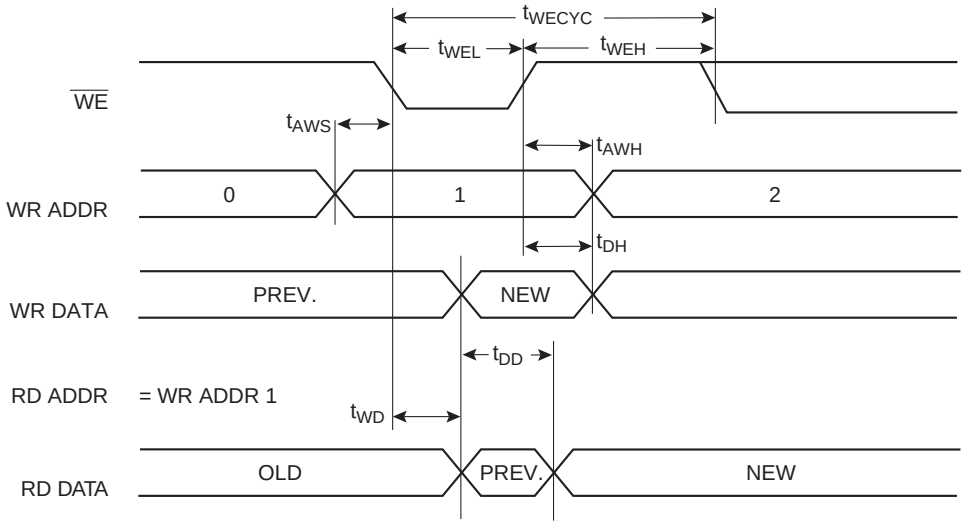
Notes:
1. CMOS buffer delays are measured from a V_{IH} of 1/2 V_{CC} at the pad to the internal V_{IH} at A. The input buffer load is constant.
2. Buffer delay is to a pad voltage of 1.5V with one output switching.
3. Parameter based on characterization and simulation; not tested in production.
4. Exact power calculation is available in Atmel FPGA Designer software.

FreeRAM Asynchronous Timing Characteristics

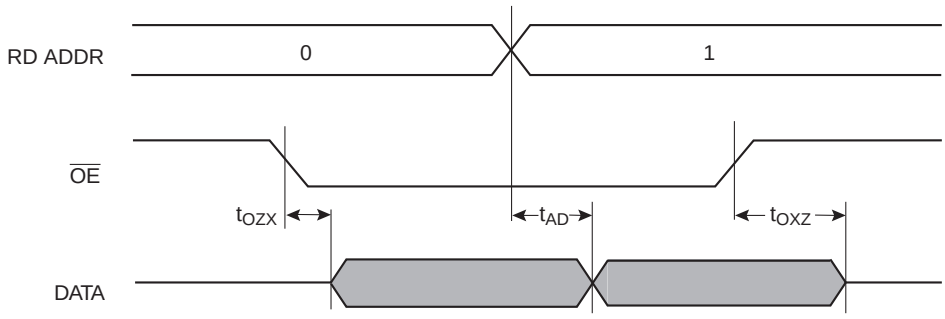
Single-port Write/Read



Dual-port Write with Read



Dual-port Read



AT40K05AL	AT40K10AL	AT40K20AL	AT40K40AL	Left Side (Top to Bottom)				
128 I/O	192 I/O	256 I/O	384 I/O	84 PLCC	100 TQFP	144 LQFP	208 PQFP	240 PQFP
GND	GND	GND	GND	12	1	1	2	1
I/O1, GCK1 (A16)	I/O1, GCK1 (A16)	I/O1, GCK1 (A16)	I/O1, GCK1 (A16)	13	2	2	4	2
I/O2 (A17)	I/O2 (A17)	I/O2 (A17)	I/O2 (A17)	14	3	3	5	3
I/O3	I/O3	I/O3	I/O3			4	6	4
I/O4	I/O4	I/O4	I/O4			5	7	5
I/O5 (A18)	I/O5 (A18)	I/O5 (A18)	I/O5 (A18)	15	4	6	8	6
I/O6 (A19)	I/O6 (A19)	I/O6 (A19)	I/O6 (A19)	16	5	7	9	7
			GND					
			I/O7					
			I/O8					
			I/O9					
			I/O10					
		I/O7	I/O11					
		I/O8	I/O12					
		VCC	VCC					
		GND	GND					
			I/O13					
			I/O14					
I/O7	I/O7	I/O9	I/O15				10	8
I/O8	I/O8	I/O10	I/O16				11	9
	I/O9	I/O11	I/O17				12	10
	I/O10	I/O12	I/O18				13	11
			GND					
			I/O19					
			I/O20					
	I/O11	I/O13	I/O21					12
	I/O12	I/O14	I/O22					13
		I/O15	I/O23					
		I/O16	I/O24					
GND	GND	GND	GND			8	14	14

Note: 1. On-chip tri-state

AT40K05AL	AT40K10AL	AT40K20AL	AT40K40AL	Left Side (Top to Bottom)				
128 I/O	192 I/O	256 I/O	384 I/O	84 PLCC	100 TQFP	144 LQFP	208 PQFP	240 PQFP
I/O17	I/O25	I/O33	I/O49	23	13	19	27	31
I/O18	I/O26	I/O34	I/O50	24	14	20	28	32
			I/O51					
			I/O52					
I/O19	I/O27	I/O35	I/O53		15	21	29	33
I/O20	I/O28	I/O36	I/O54			22	30	34
			GND					
	I/O29	I/O37	I/O55				31	35
	I/O30	I/O38	I/O56				32	36
		I/O39	I/O57					
		I/O40	I/O58					
			I/O59					
			I/O60					
			VCC					
		GND	GND					37
		I/O41	I/O61					
		I/O42	I/O62					
			I/O63					
			I/O64					
			I/O65					
			I/O66					
			GND					
	I/O31	I/O43	I/O67					38
	I/O32	I/O44	I/O68					39
	VCC	VCC	VCC					40
I/O21	I/O33	I/O45	I/O69	25	16	23	33	41
I/O22	I/O34	I/O46	I/O70	26	17	24	34	42
I/O23	I/O35	I/O47	I/O71			25	35	43
I/O24, FCK2	I/O36, FCK2	I/O48, FCK2	I/O72, FCK2			26	36	44
GND	GND	GND	GND			27	37	45
		I/O49	I/O73					
		I/O50	I/O74					
	I/O37	I/O51	I/O75					46

Note: 1. On-chip tri-state

AT40K05AL	AT40K10AL	AT40K20AL	AT40K40AL	Left Side (Top to Bottom)				
128 I/O	192 I/O	256 I/O	384 I/O	84 PLCC	100 TQFP	144 LQFP	208 PQFP	240 PQFP
	I/O38	I/O52	I/O76					47
			I/O77					
			I/O78					
			GND					
			I/O79					
			I/O80					
	I/O39	I/O53	I/O81				38	48
	I/O40	I/O54	I/O82				39	49
I/O25	I/O41	I/O55	I/O83				40	50
I/O26	I/O42	I/O56	I/O84				41	51
		GND	GND					
		VCC	VCC					
		I/O57	I/O85					
		I/O58	I/O86					
			I/O87					
			I/O88					
I/O27	I/O43	I/O59	I/O89	27	18	28	42	52
I/O28	I/O44	I/O60	I/O90		19	29	43	53
			GND					
			I/O91					
			I/O92					
I/O29	I/O45	I/O61	I/O93			30	44	54
I/O30	I/O46	I/O62	I/O94			31	45	55
I/O31 ($\overline{OTS}$)[1]	I/O47 ($\overline{OTS}$)[1]	I/O63 ($\overline{OTS}$)[1]	I/O95 ($\overline{OTS}$)[1]	28	20	32	46	56
I/O32, GCK2	I/O48, GCK2	I/O64, GCK2	I/O96, GCK2	29	21	33	47	57
M1	M1	M1	M1	30	22	34	48	58
GND	GND	GND	GND	31	23	35	49	59
M0	M0	M0	M0	32	24	36	50	60

Note: 1. On-chip tri-state

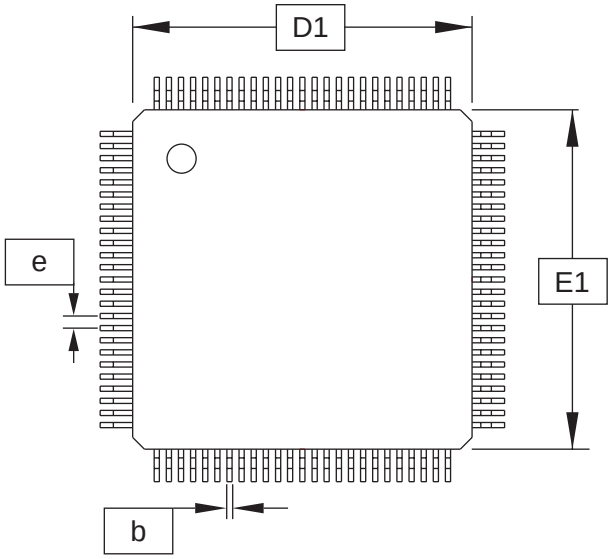
AT40K05AL	AT40K10AL	AT40K20AL	AT40K40AL	Bottom Side (Left to Right)				
128 I/O	192 I/O	256 I/O	384 I/O	84 PLCC	100 TQFP	144 LQFP	208 PQFP	240 PQFP
			I/O174					
			GND					
			I/O175					
			I/O176					
	I/O87	I/O117	I/O177				91	109
	I/O88	I/O118	I/O178				92	110
I/O57	I/O89	I/O119	I/O179				93	111
I/O58	I/O90	I/O120	I/O180				94	112
		GND	GND					
		VCC	VCC					
		I/O121	I/O181					
		I/O122	I/O182					
I/O59 (D10)	I/O91 (D10)	I/O123 (D10)	I/O183 (D10)	48	45	65	95	113
I/O60 (D9)	I/O92 (D9)	I/O124 (D9)	I/O184 (D9)	49	46	66	96	114
			I/O185					
			I/O186					
			GND					
			I/O187					
			I/O188					
I/O61	I/O93	I/O125	I/O189			67	97	115
I/O62	I/O94	I/O126	I/O190			68	98	116
I/O63 (D8)	I/O95 (D8)	I/O127 (D8)	I/O191 (D8)	50	47	69	99	117
I/O64, GCK4	I/O96, GCK4	I/O128, GCK4	I/O192, GCK4	51	48	70	100	118
GND	GND	GND	GND	52	49	71	101	119
$\overline{\text{CON}}$	$\overline{\text{CON}}$	$\overline{\text{CON}}$	$\overline{\text{CON}}$	53	50	72	103	120

AT40K05AL	AT40K10AL	AT40K20AL	AT40K40AL	Right Side (Bottom to Top)				
128 I/O	192 I/O	256 I/O	384 I/O	84 PLCC	100 TQFP	144 LQFP	208 PQFP	240 PQFP
I/O73, FCK3	I/O111, FCK3	I/O147, FCK3	I/O219, FCK3			82	120	138
I/O74	I/O112	I/O148	I/O220			83	121	139
	VCC	VCC	VCC					140
I/O75 (D5)	I/O113 (D5)	I/O149 (D5)	I/O221 (D5)	59	57	84	122	141
I/O76 (CS0)	I/O114 (CS0)	I/O150 (CS0)	I/O222 (CS0)	60	58	85	123	142
			GND					
			I/O223					
			I/O224					
			I/O225					
			I/O226					
		I/O151	I/O227					
		I/O152	I/O228					
		GND	GND					143
			VCC					
			I/O229					
			I/O230					
		I/O153	I/O231					
		I/O154	I/O232					
	I/O115	I/O155	I/O233				124	144
	I/O116	I/O156	I/O234				125	145
			GND					
I/O77	I/O117	I/O157	I/O235		59	86	126	146
I/O78	I/O118	I/O158	I/O236		60	87	127	147
			I/O237					
			I/O238					
I/O79(D4)	I/O119(D4)	I/O159(D4)	I/O239(D4)	61	61	88	128	148
I/O80	I/O120	I/O160	I/O240	62	62	89	129	149
VCC	VCC	VCC	VCC	63	63	90	130	150
GND	GND	GND	GND	64	64	91	131	151
I/O81 (D3)	I/O121 (D3)	I/O161 (D3)	I/O241 (D3)	65	65	92	132	152
I/O82 ($\overline{\text{CHECK}}$)	I/O122 ($\overline{\text{CHECK}}$)	I/O162 ($\overline{\text{CHECK}}$)	I/O242 ($\overline{\text{CHECK}}$)	66	66	93	133	153

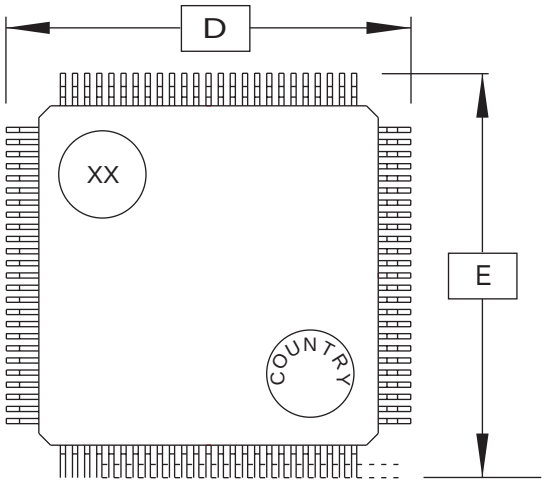
AT40K05AL	AT40K10AL	AT40K20AL	AT40K40AL	Top Side (Right to Left)				
128 I/O	192 I/O	256 I/O	384 I/O	84 PLCC	100 TQFP	144 LQFP	208 PQFP	240 PQFP
		I/O242	I/O362					
	I/O181	I/O243	I/O363				195	228
	I/O182	I/O244	I/O364				196	229
			I/O365					
			I/O366					
			GND					
			I/O367					
			I/O368					
I/O121	I/O183	I/O245	I/O369				197	230
I/O122	I/O184	I/O246	I/O370				198	231
I/O123 (A12)	I/O185 (A12)	I/O247 (A12)	I/O371 (A12)	7	96	138	199	232
I/O124 (A13)	I/O186 (A13)	I/O248 (A13)	I/O372 (A13)	8	97	139	200	233
		GND	GND					
		VCC	VCC					
		I/O249	I/O373					
		I/O250	I/O374					
			I/O375					
			I/O376					
			I/O377					
			I/O378					
			GND					
	I/O187	I/O251	I/O379					234
	I/O188	I/O252	I/O380					235
I/O125	I/O189	I/O253	I/O381			140	201	236
I/O126	I/O190	I/O254	I/O382			141	202	237
I/O127 (A14)	I/O191 (A14)	I/O255 (A14)	I/O383 (A14)	9	98	142	203	238
I/O128, GCK8 (A15)	I/O192, GCK8 (A15)	I/O256, GCK8 (A15)	I/O384, GCK8 (A15)	10	99	143	204	239
VCC	VCC	VCC	VCC	11	100	144	205	240

Note: 1. Shared with TSTCLK. No Connect.

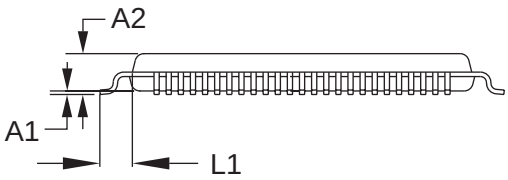
100T1 – TQFP



Top View



Bottom View



Side View

COMMON DIMENSIONS
(Unit of Measure = mm)

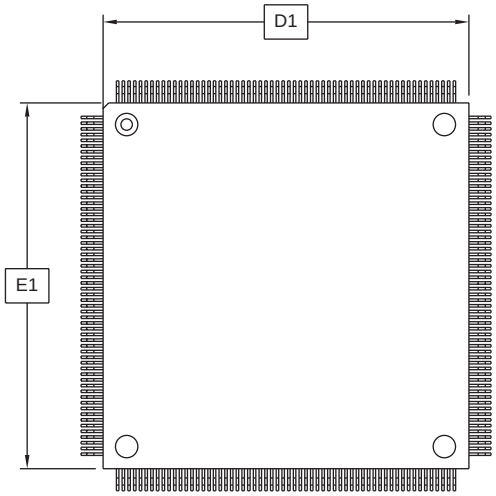
SYMBOL	MIN	NOM	MAX	NOTE
A1	0.05		0.15	6
A2	0.95	1.00	1.05	
D		16.00 BSC		
D1		14.00 BSC		2, 3
E		16.00 BSC		
E1		14.00 BSC		2, 3
e		0.50 BSC		
b	0.17	0.22	0.27	4, 5
L1		1.00 REF		

Notes:
1. This drawing is for general information only. Refer to JEDEC Drawing MO-153, Variation AA, for proper dimensions, tolerances, datums, etc.
2. The top package body size may be smaller than the bottom package size by as much as 0.15 mm.
3. Dimensions D1 and E1 do not include mold protrusions. Allowable protrusion is 0.25 mm per side. D1 and E1 are maximum plastic body size dimensions, including mold mismatch.
4. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall not cause the lead width to exceed the maximum b dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 and 0.5 mm pitch packages.
5. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
6. A1 is defined as the distance from the seating place to the lowest point on the package body.

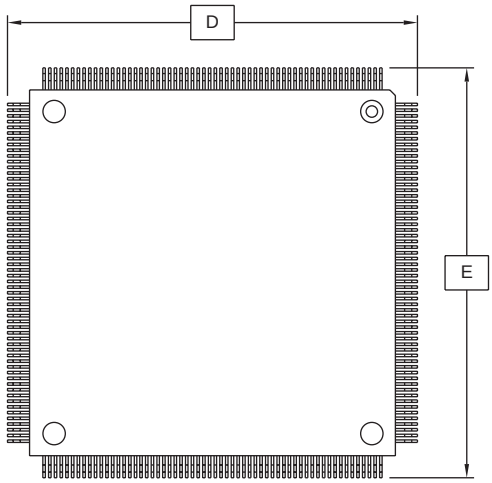
11/30/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**100T1**, 100-lead (14 x 14 x 1.0 mm Body), Thin Plastic Quad Flat Pack (TQFP)	100T1	A

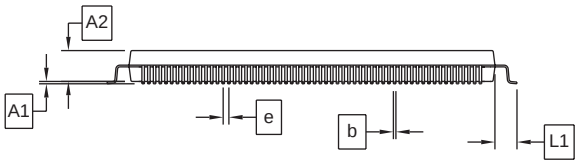
240Q1 – PQFP



Top View



Bottom View



Side View

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A1	0.25	–	0.50	
A2	3.20	3.40	3.60	
D		34.60 BSC		3
D1		32.00 BSC		2, 4
E		34.60 BSC		3
E1		32.00 BSC		2, 4
e		0.50 BSC		
b	0.17	–	0.27	5
L1		1.30 REF		

Notes:
1. This drawing is for general information only. Refer to JEDEC Drawing MS-029, Variation GA, for additional information.
2. All dimensioning and tolerancing conforms to ASME Y14.5M-1994.
3. To be determined at seating plane.
4. Dimensions D1 and E1 do not include mold protrusions. Allowable protrusion is 0.25 mm per side. D1 and E1 are maximum plastic body size dimensions including mold mismatch. Dimensions D1 and E1 shall be determined at datum plane.
5. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall not cause the lead width to exceed the maximum b dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. The minimum space between protrusion and an adjacent lead shall not be less than 0.07 mm.

3/29/02

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**240Q1,** 240-lead, 32 x 32 mm Body, 2.6 Form Opt., Plastic Quad Flat Pack (PQFP)	240Q1	A