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Understanding Embedded - FPGAs (Field Programmable Gate Array)

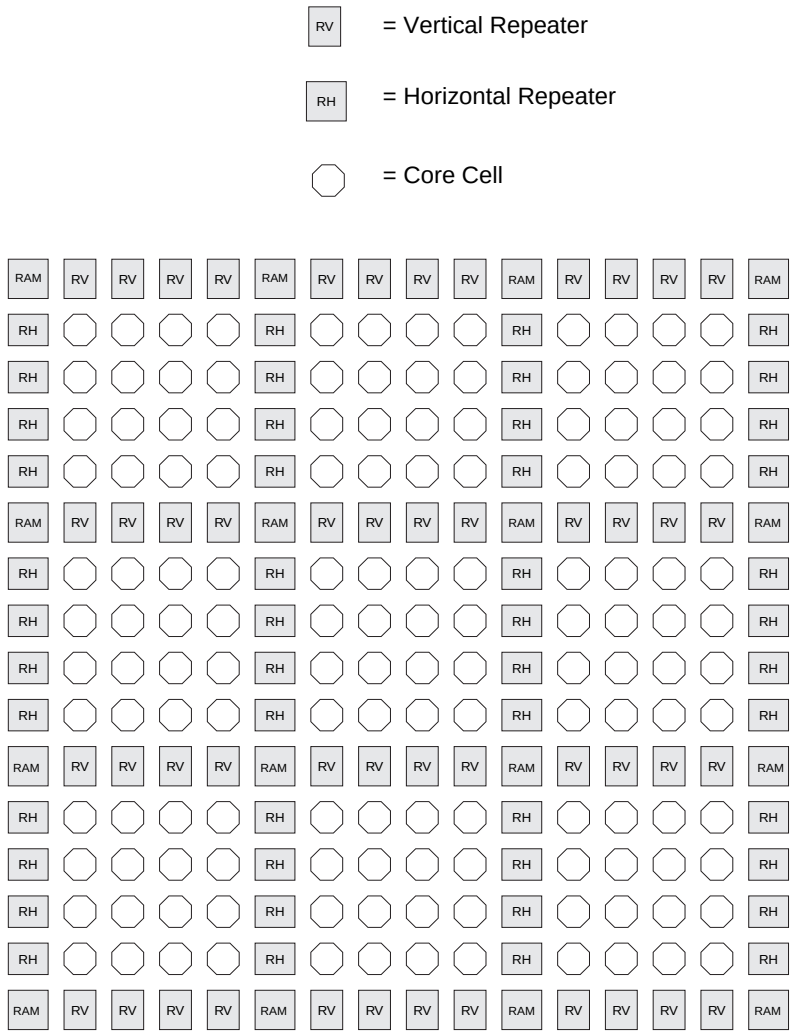
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	576
Total RAM Bits	4608
Number of I/O	161
Number of Gates	20000
Voltage - Supply	3V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at40k10al-1dqc

Figure 2. Floor Plan (Representative Portion)[1]



Note: 1. Repeaters regenerate signals and can connect any bus to any other bus (all pathways are legal) on the same plane. Each repeater has connections to two adjacent local-bus segments and two express-bus segments. This is done automatically using the integrated development system (IDS) tool.

The Busing Network

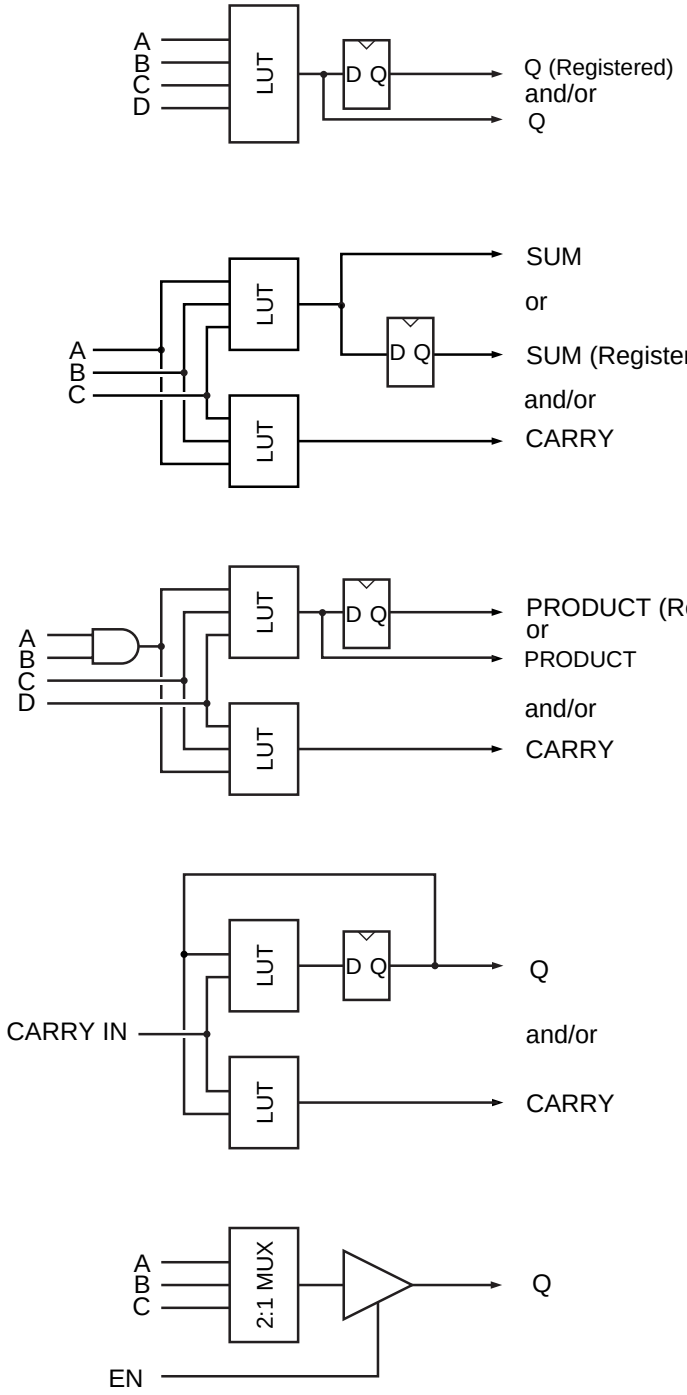
Figure 3 on page 7 depicts one of five identical busing planes. Each plane has three bus resources: a local-bus resource (the middle bus) and two express-bus (both sides) resources. Bus resources are connected via repeaters. Each repeater has connections to two adjacent local-bus segments and two express-bus segments. Each local-bus segment spans four cells and connects to consecutive repeaters. Each express-bus segment spans eight cells and “leapfrogs” or bypasses a repeater. Repeaters regenerate signals and can connect any bus to any other bus (all pathways are legal) on the same plane. Although not shown, a local bus can bypass a repeater via a programmable pass gate allowing long on-chip tri-state buses to be created. Local/Local turns are implemented through pass gates in the cell-bus interface. Express/Express turns are implemented through separate pass gates distributed throughout the array.

Some of the bus resources on the AT40KAL are used as a dual-function resources. Table 2 shows which buses are used in a dual-function mode and which bus plane is used. The AT40KAL software tools are designed to accommodate dual-function buses in an efficient manner.

Table 2. Dual-function Buses

Function	Type	Plane(s)	Direction	Comments
Cell Output Enable	Local	5	Horizontal and Vertical	
RAM Output Enable	Express	2	Vertical	Bus full length at array edge Bus in first column to left of RAM block
RAM Write Enable	Express	1	Vertical	Bus full length at array edge Bus in first column to left of RAM block
RAM Address	Express	1 - 5	Vertical	Buses full length at array edge Buses in second column to left of RAM block
RAM Data In	Local	1	Horizontal	Data In connects to local bus plane 1
RAM Data Out	Local	2	Horizontal	Data out connects to local bus plane 2
Clocking	Express	4	Vertical	Bus half length at array edge
Set/Reset	Express	5	Vertical	Bus half length at array edge

Figure 6. Some Single Cell Modes



Synthesis Mode. This mode is particularly important for the use of VHDL/Verilog design. VHDL/Verilog Synthesis tools generally will produce as their output large amounts of random logic functions. Having a 4-input LUT structure gives efficient random logic optimization without the delays associated with larger LUT structures. The output of any cell may be registered, tri-stated and/or fed back into a core cell.

Arithmetic Mode is frequently used in many designs. As can be seen in the figure, the AT40KAL core cell can implement a 1-bit full adder (2-input adder with both Carry In and Carry Out) in one core cell. Note that the sum output in this diagram is registered. This output could then be tri-stated and/or fed back into the cell.

DSP/Multiplier Mode. This mode is used to efficiently implement array multipliers. An array multiplier is an array of bitwise multipliers, each implemented as a full adder with an upstream AND gate. Using this AND gate and the diagonal interconnects between cells, the array multiplier structure fits very well into the AT40KAL architecture.

Counter Mode. Counters are fundamental to almost all digital designs. They are the basis of state machines, timing chains and clock dividers. A counter is essentially an increment by one function (i.e., an adder), with the input being an output (or a decode of an output) from the previous stage. A 1-bit counter can be implemented in one core cell. Again, the output can be registered, tri-stated and/or fed back.

Tri-state/Mux Mode. This mode is used in many telecommunications applications, where data needs to be routed through more than one possible path. The output of the core cell is very often tri-statable for many inputs to many outputs data switching.

Reading and writing of the 10 ns 32 x 4 dual-port FreeRAM are independent of each other. Reading the 32 x 4 dual-port RAM is completely asynchronous. Latches are transparent; when Load is logic 1, data flows through; when Load is logic 0, data is latched. These latches are used to synchronize Write Address, $\overline{\text{Write Enable Not}}$, and Din signals for a synchronous RAM. Each bit in the 32 x 4 dual-port RAM is also a transparent latch. The front-end latch and the memory latch together form an edge-triggered flip flop. When a nibble (bit = 7) is (Write) addressed and LOAD is logic 1 and $\overline{\text{WE}}$ is logic 0, data flows through the bit. When a nibble is not (Write) addressed or LOAD is logic 0 or $\overline{\text{WE}}$ is logic 1, data is latched in the nibble. The two CLOCK muxes are controlled together; they both select CLOCK (for a synchronous RAM) or they both select "1" (for an asynchronous RAM). CLOCK is obtained from the clock for the sector-column immediately to the left and immediately above the RAM block. Writing any value to the RAM clear byte during configuration clears the RAM (see the "AT40K/40KAL Configuration Series" application note at www.atmel.com).

Figure 8. RAM Logic

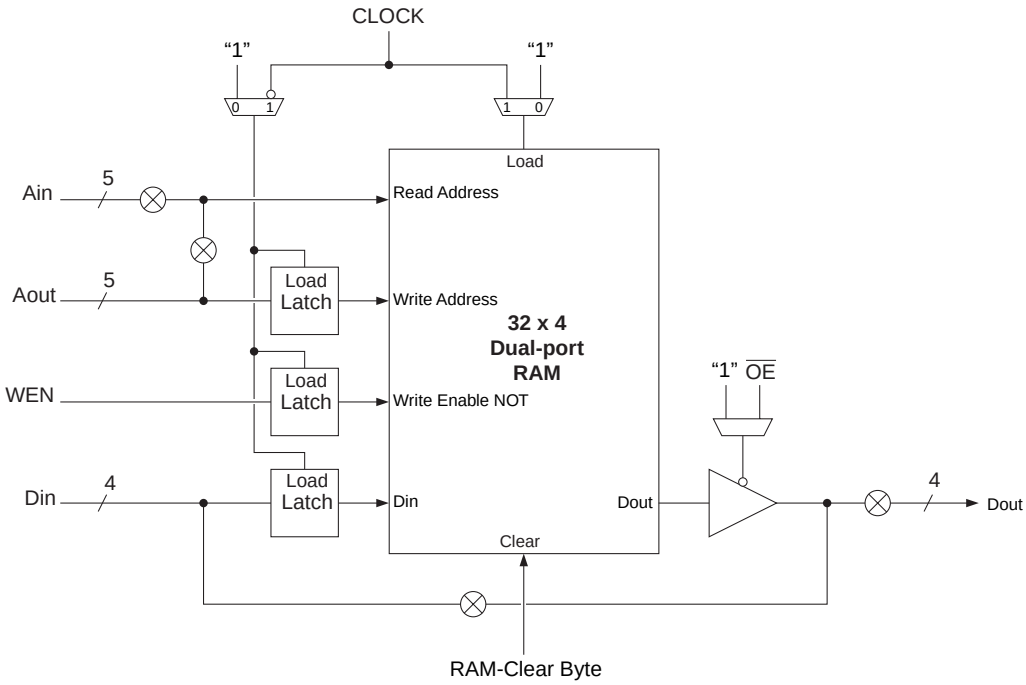
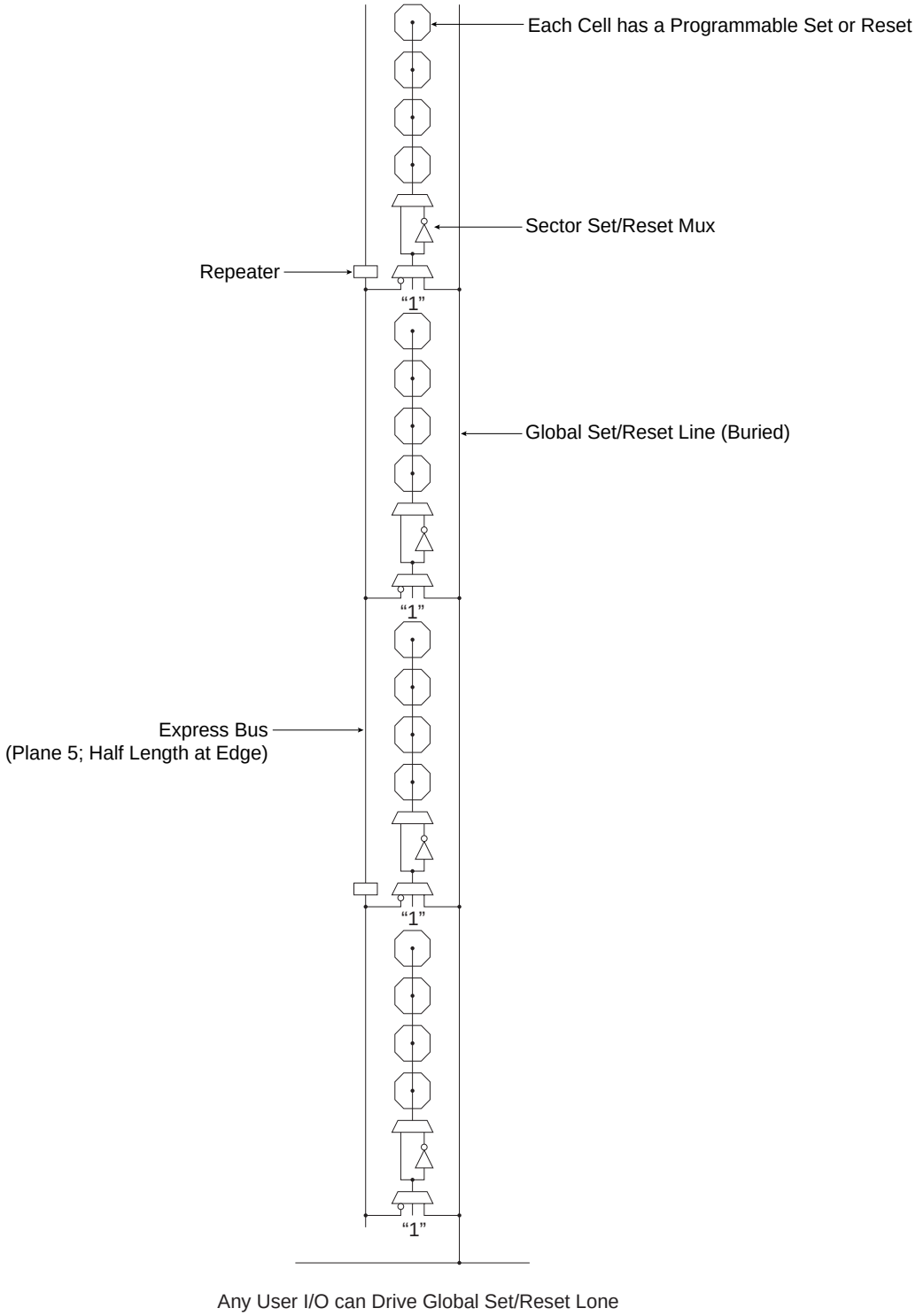


Figure 9 on page 13 shows an example of a RAM macro constructed using the AT40KAL's FreeRAM cells. The macro shown is a 128 x 8 dual-ported asynchronous RAM. Note the very small amount of external logic required to complete the address decoding for the macro. Most of the logic cells (core cells) in the sectors occupied by the RAM will be unused: they can be used for other logic in the design. This logic can be automatically generated using the macro generators.

Figure 11. Set/Reset (for One Column of Cells)



Primary, Secondary and Corner I/Os

The AT40KAL has three kinds of I/Os: Primary I/O, Secondary I/O and a Corner I/O. Every edge cell except corner cells on the AT40KAL has access to one Primary I/O and two Secondary I/Os.

Primary I/O

Every logic cell at the edge of the FPGA array has a direct orthogonal connection to and from a Primary I/O cell. The Primary I/O interfaces directly to its adjacent core cell. It also connects into the repeaters on the row immediately above and below the adjacent core cell. In addition, each Primary I/O also connects into the busing network of the three nearest edge cells. This is an extremely powerful feature, as it provides logic cells toward the center of the array with fast access to I/Os via local and express buses. It can be seen from the diagram that a given Primary I/O can be accessed from any logic cell on three separate rows or columns of the FPGA. See Figure 12 on page 20.

Secondary I/O

Every logic cell at the edge of the FPGA array has two direct diagonal connections to a Secondary I/O cell. The Secondary I/O is located between core cell locations. This I/O connects on the diagonal inputs to the cell above and the cell below. It also connects to the repeater of the cell above and below. In addition, each Secondary I/O also connects into the busing network of the two nearest edge cells. This is an extremely powerful feature, as it provides logic cells toward the center of the array with fast access to I/Os via local and express buses. It can be seen from the diagram that a given Secondary I/O can be accessed from any logic cell on two rows or columns of the FPGA. See Figure 13 on page 20.

Corner I/O

Logic cells at the corner of the FPGA array have direct-connect access to five separate I/Os: 2 Primary, 2 Secondary and 1 Corner I/O. Corner I/Os are like an extra Secondary I/O at each corner of the array. With the inclusion of Corner I/Os, an AT40KAL FPGA with n x n core cells always has 8n I/Os. As the diagram shows, Corner I/Os can be accessed both from the corner logic cell and the horizontal and vertical busing networks running along the edges of the array. This means that many different edge logic cells can access the Corner I/Os. See Figure 14 on page 21.

Absolute Maximum Ratings – 3.3V Commercial/Industrial*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-0.5V to V_{CC} +7V
Supply Voltage (V_{CC})	-0.5V to +7.0V
Maximum Soldering Temp. (10 sec. @ 1/16 in.)	250°C
ESD (R_{ZAP} = 1.5K, C_{ZAP} = 100 pF)	2000V

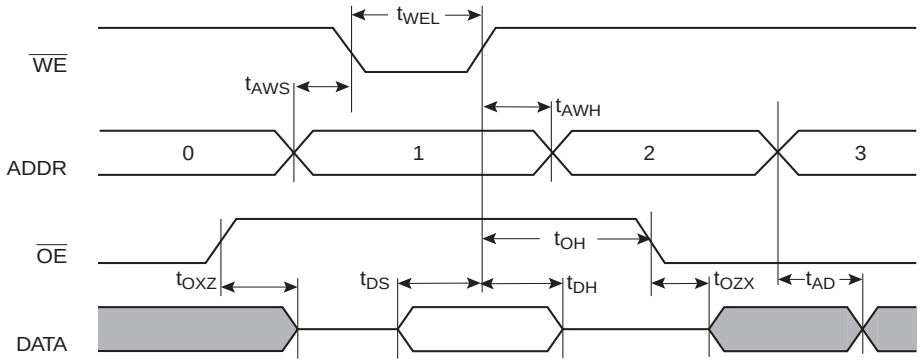
*NOTICE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those listed under operating conditions is not implied. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect device reliability.

DC and AC Operating Range – 3.3V Operation

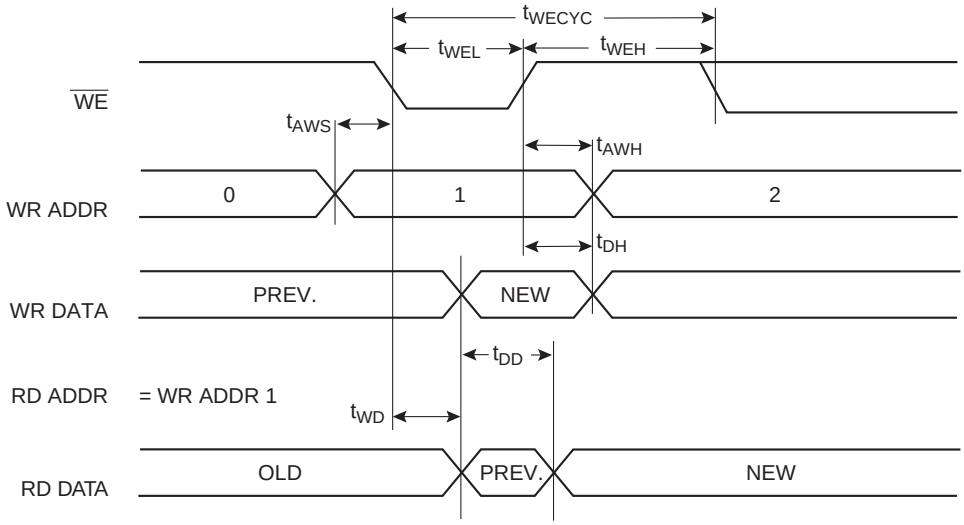
		Commercial	Industrial
Operating Temperature (Case)		0°C - 70°C	-40°C - 85°C
V_{CC} Power Supply		3.3V ± 0.3V	3.3V ± 0.3V
Input Voltage Level (CMOS)	High (V_{IHC})	70% - 100% V_{CC}	70% - 100% V_{CC}
	Low (V_{ILC})	0 - 30% V_{CC}	0 - 30% V_{CC}

FreeRAM Asynchronous Timing Characteristics

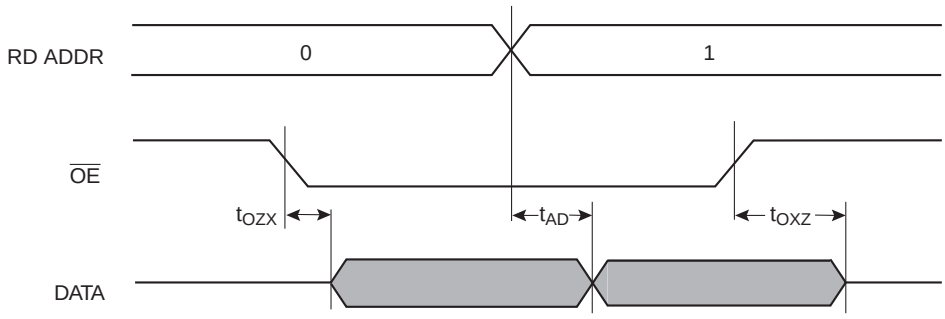
Single-port Write/Read



Dual-port Write with Read

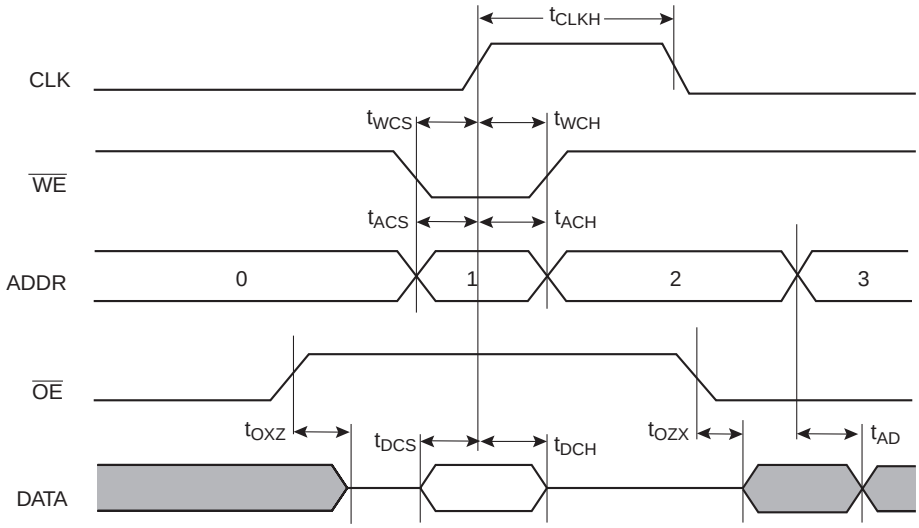


Dual-port Read

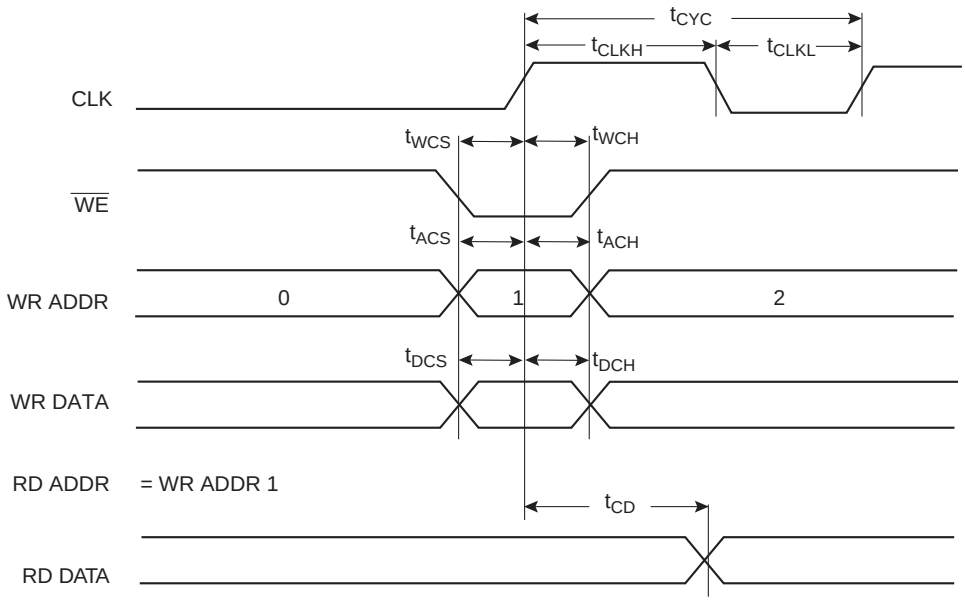


FreeRAM Synchronous Timing Characteristics

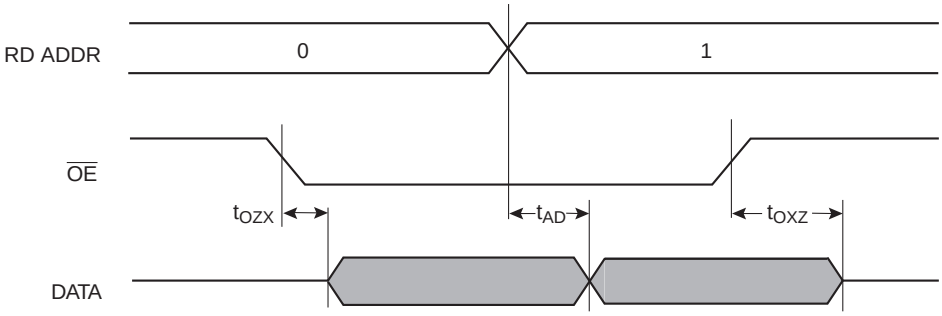
Single-port Write/Read



Dual-port Write with Read



Dual-port Read



AT40K05AL	AT40K10AL	AT40K20AL	AT40K40AL	Left Side (Top to Bottom)				
128 I/O	192 I/O	256 I/O	384 I/O	84 PLCC	100 TQFP	144 LQFP	208 PQFP	240 PQFP
I/O17	I/O25	I/O33	I/O49	23	13	19	27	31
I/O18	I/O26	I/O34	I/O50	24	14	20	28	32
			I/O51					
			I/O52					
I/O19	I/O27	I/O35	I/O53		15	21	29	33
I/O20	I/O28	I/O36	I/O54			22	30	34
			GND					
	I/O29	I/O37	I/O55				31	35
	I/O30	I/O38	I/O56				32	36
		I/O39	I/O57					
		I/O40	I/O58					
			I/O59					
			I/O60					
			VCC					
		GND	GND					37
		I/O41	I/O61					
		I/O42	I/O62					
			I/O63					
			I/O64					
			I/O65					
			I/O66					
			GND					
	I/O31	I/O43	I/O67					38
	I/O32	I/O44	I/O68					39
	VCC	VCC	VCC					40
I/O21	I/O33	I/O45	I/O69	25	16	23	33	41
I/O22	I/O34	I/O46	I/O70	26	17	24	34	42
I/O23	I/O35	I/O47	I/O71			25	35	43
I/O24, FCK2	I/O36, FCK2	I/O48, FCK2	I/O72, FCK2			26	36	44
GND	GND	GND	GND			27	37	45
		I/O49	I/O73					
		I/O50	I/O74					
	I/O37	I/O51	I/O75					46

Note: 1. On-chip tri-state

AT40K05AL	AT40K10AL	AT40K20AL	AT40K40AL	Left Side (Top to Bottom)				
128 I/O	192 I/O	256 I/O	384 I/O	84 PLCC	100 TQFP	144 LQFP	208 PQFP	240 PQFP
	I/O38	I/O52	I/O76					47
			I/O77					
			I/O78					
			GND					
			I/O79					
			I/O80					
	I/O39	I/O53	I/O81				38	48
	I/O40	I/O54	I/O82				39	49
I/O25	I/O41	I/O55	I/O83				40	50
I/O26	I/O42	I/O56	I/O84				41	51
		GND	GND					
		VCC	VCC					
		I/O57	I/O85					
		I/O58	I/O86					
			I/O87					
			I/O88					
I/O27	I/O43	I/O59	I/O89	27	18	28	42	52
I/O28	I/O44	I/O60	I/O90		19	29	43	53
			GND					
			I/O91					
			I/O92					
I/O29	I/O45	I/O61	I/O93			30	44	54
I/O30	I/O46	I/O62	I/O94			31	45	55
I/O31 ($\overline{OTS}$)[1]	I/O47 ($\overline{OTS}$)[1]	I/O63 ($\overline{OTS}$)[1]	I/O95 ($\overline{OTS}$)[1]	28	20	32	46	56
I/O32, GCK2	I/O48, GCK2	I/O64, GCK2	I/O96, GCK2	29	21	33	47	57
M1	M1	M1	M1	30	22	34	48	58
GND	GND	GND	GND	31	23	35	49	59
M0	M0	M0	M0	32	24	36	50	60

Note: 1. On-chip tri-state

AT40K05AL	AT40K10AL	AT40K20AL	AT40K40AL	Bottom Side (Left to Right)				
128 I/O	192 I/O	256 I/O	384 I/O	84 PLCC	100 TQFP	144 LQFP	208 PQFP	240 PQFP
VCC	VCC	VCC	VCC	33	25	37	55	61
M2	M2	M2	M2	34	26	38	56	62
I/O33, GCK3	I/O49, GCK3	I/O65, GCK3	I/O97, GCK3	35	27	39	57	63
I/O34 (HDC)	I/O50 (HDC)	I/O66 (HDC)	I/O98 (HDC)	36	28	40	58	64
I/O35	I/O51	I/O67	I/O99			41	59	65
I/O36	I/O52	I/O68	I/O100			42	60	66
I/O37	I/O53	I/O69	I/O101		29	43	61	67
I/O38 (LDC)	I/O54 (LDC)	I/O70 (LDC)	I/O102 (LDC)	37	30	44	62	68
			GND					
			I/O103					
			I/O104					
			I/O105					
			I/O106					
		I/O71	I/O107					
		I/O72	I/O108					
		VCC	VCC					
		GND	GND					
I/O39	I/O55	I/O73	I/O109				63	69
I/O40	I/O56	I/O74	I/O110				64	70
	I/O57	I/O75	I/O111				65	71
	I/O58	I/O76	I/O112				66	72
			I/O113					
			I/O114					
			GND					
		I/O77	I/O115					
		I/O78	I/O116					
	I/O59	I/O79	I/O117					73
	I/O60	I/O80	I/O118					74
			I/O119					
			I/O120					
GND	GND	GND	GND			45	67	75
I/O41	I/O61	I/O81	I/O121			46	68	76

AT40K05AL	AT40K10AL	AT40K20AL	AT40K40AL	Bottom Side (Left to Right)				
128 I/O	192 I/O	256 I/O	384 I/O	84 PLCC	100 TQFP	144 LQFP	208 PQFP	240 PQFP
			I/O174					
			GND					
			I/O175					
			I/O176					
	I/O87	I/O117	I/O177				91	109
	I/O88	I/O118	I/O178				92	110
I/O57	I/O89	I/O119	I/O179				93	111
I/O58	I/O90	I/O120	I/O180				94	112
		GND	GND					
		VCC	VCC					
		I/O121	I/O181					
		I/O122	I/O182					
I/O59 (D10)	I/O91 (D10)	I/O123 (D10)	I/O183 (D10)	48	45	65	95	113
I/O60 (D9)	I/O92 (D9)	I/O124 (D9)	I/O184 (D9)	49	46	66	96	114
			I/O185					
			I/O186					
			GND					
			I/O187					
			I/O188					
I/O61	I/O93	I/O125	I/O189			67	97	115
I/O62	I/O94	I/O126	I/O190			68	98	116
I/O63 (D8)	I/O95 (D8)	I/O127 (D8)	I/O191 (D8)	50	47	69	99	117
I/O64, GCK4	I/O96, GCK4	I/O128, GCK4	I/O192, GCK4	51	48	70	100	118
GND	GND	GND	GND	52	49	71	101	119
$\overline{\text{CON}}$	$\overline{\text{CON}}$	$\overline{\text{CON}}$	$\overline{\text{CON}}$	53	50	72	103	120

AT40K05AL	AT40K10AL	AT40K20AL	AT40K40AL	Right Side (Bottom to Top)				
128 I/O	192 I/O	256 I/O	384 I/O	84 PLCC	100 TQFP	144 LQFP	208 PQFP	240 PQFP
I/O73, FCK3	I/O111, FCK3	I/O147, FCK3	I/O219, FCK3			82	120	138
I/O74	I/O112	I/O148	I/O220			83	121	139
	VCC	VCC	VCC					140
I/O75 (D5)	I/O113 (D5)	I/O149 (D5)	I/O221 (D5)	59	57	84	122	141
I/O76 (CS0)	I/O114 (CS0)	I/O150 (CS0)	I/O222 (CS0)	60	58	85	123	142
			GND					
			I/O223					
			I/O224					
			I/O225					
			I/O226					
		I/O151	I/O227					
		I/O152	I/O228					
		GND	GND					143
			VCC					
			I/O229					
			I/O230					
		I/O153	I/O231					
		I/O154	I/O232					
	I/O115	I/O155	I/O233				124	144
	I/O116	I/O156	I/O234				125	145
			GND					
I/O77	I/O117	I/O157	I/O235		59	86	126	146
I/O78	I/O118	I/O158	I/O236		60	87	127	147
			I/O237					
			I/O238					
I/O79(D4)	I/O119(D4)	I/O159(D4)	I/O239(D4)	61	61	88	128	148
I/O80	I/O120	I/O160	I/O240	62	62	89	129	149
VCC	VCC	VCC	VCC	63	63	90	130	150
GND	GND	GND	GND	64	64	91	131	151
I/O81 (D3)	I/O121 (D3)	I/O161 (D3)	I/O241 (D3)	65	65	92	132	152
I/O82 ($\overline{\text{CHECK}}$)	I/O122 ($\overline{\text{CHECK}}$)	I/O162 ($\overline{\text{CHECK}}$)	I/O242 ($\overline{\text{CHECK}}$)	66	66	93	133	153

AT40K05AL	AT40K10AL	AT40K20AL	AT40K40AL	Right Side (Bottom to Top)				
128 I/O	192 I/O	256 I/O	384 I/O	84 PLCC	100 TQFP	144 LQFP	208 PQFP	240 PQFP
			I/O243					
			I/O244					
I/O83	I/O123	I/O163	I/O245		67	94	134	154
I/O84	I/O124	I/O164	I/O246			95	135	155
			GND					
	I/O125	I/O165	I/O247				136	156
	I/O126	I/O166	I/O248				137	157
		I/O167	I/O249					
		I/O168	I/O250					
			I/O251					
			I/O252					
			VCC					
		GND	GND					158
		I/O169	I/O253					
		I/O170	I/O254					
			I/O255					
			I/O256					
			I/O257					
			I/O258					
			GND					
I/O85 (D2)	I/O127 (D2)	I/O171 (D2)	I/O259 (D2)	67	68	96	138	159
I/O86	I/O128	I/O172	I/O260	68	69	97	139	160
	VCC	VCC	VCC					161
I/O87	I/O129	I/O173	I/O261			98	140	162
I/O88, FCK4	I/O130, FCK4	I/O174, FCK4	I/O262, FCK4			99	141	163
	I/O131	I/O175	I/O263					164
	I/O132	I/O176	I/O264					165
GND	GND	GND	GND			100	142	166
		I/O177	I/O265					
		I/O178	I/O266					
	I/O133	I/O179	I/O267					167
	I/O134	I/O180	I/O268					168
			I/O269					

AT40K05AL	AT40K10AL	AT40K20AL	AT40K40AL	Top Side (Right to Left)				
128 I/O	192 I/O	256 I/O	384 I/O	84 PLCC	100 TQFP	144 LQFP	208 PQFP	240 PQFP
I/O105	I/O157	I/O209	I/O313			119	172	197
I/O106	I/O158	I/O210	I/O314			120	173	198
	I/O159	I/O211	I/O315					199
	I/O160	I/O212	I/O316					200
	VCC	VCC	VCC					201
		I/O213	I/O317					
		I/O214	I/O318					
			GND					
			I/O319					
			I/O320					
			I/O321					
			I/O322					
		I/O215	I/O323					
		I/O216	I/O324					
		GND	GND					
			VCC					
I/O107 (A4)	I/O161 (A4)	I/O217 (A4)	I/O325 (A4)	81	82	121	174	202
I/O108 (A5)	I/O162 (A5)	I/O218 (A5)	I/O326 (A5)	82	83	122	175	203
	I/O163	I/O219	I/O327				176	205
	I/O164	I/O220	I/O328				177	206
I/O109	I/O165	I/O221	I/O329		84	123	178	207
I/O110	I/O166	I/O222	I/O330		85	124	179	208
			GND					
			I/O331					
			I/O332					
			I/O333					
			I/O334					
I/O111 (A6)	I/O167 (A6)	I/O223 (A6)	I/O335 (A6)	83	86	125	180	209
I/O112 (A7)	I/O168 (A7)	I/O224 (A7)	I/O336 (A7)	84	87	126	181	210
GND	GND	GND	GND	1	88	127	182	211
VCC	VCC	VCC	VCC	2	89	128	183	212

Note: 1. Shared with TSTCLK. No Connect.

AT40K05AL Ordering Information

Usable Gates	Operating Voltage	Speed Grade (ns)	Ordering Code	Package	Operation Range[1]
5,000 - 10,000	3.3V	1	AT40K05AL-1AJC AT40K05AL-1AQC AT40K05AL-1BQC AT40K05AL-1DQC	84J 100T1 144L1 208Q1	Commercial (0°C to 70°C)
5,000 - 10,000	3.3V	1	AT40K05AL-1AJI AT40K05AL-1AQI AT40K05AL-1BQI AT40K05AL-1DQI	84J 100T1 144L1 208Q1	Industrial (-40°C to 85°C)

AT40K10AL Ordering Information

Usable Gates	Operating Voltage	Speed Grade (ns)	Ordering Code	Package	Operation Range[1]
10,000 - 20,000	3.3V	1	AT40K10AL-1AJC AT40K10AL-1AQC AT40K10AL-1BQC AT40K10AL-1DQC	84J 100T1 144L1 208Q1	Commercial (0°C to 70°C)
10,000 - 20,000	3.3V	1	AT40K10AL-1AJI AT40K10AL-1AQI AT40K10AL-1BQI AT40K10AL-1DQI	84J 100T1 144L1 208Q1	Industrial (-40°C to 85°C)

AT40K20AL Ordering Information

Usable Gates	Operating Voltage	Speed Grade (ns)	Ordering Code	Package	Operation Range[1]
20,000 - 30,000	3.3V	1	AT40K20AL-1AJC AT40K20AL-1AQC AT40K20AL-1BQC AT40K20AL-1DQC	84J 100T1 144L1 208Q1	Commercial (0°C to 70°C)
20,000 - 30,000	3.3V	1	AT40K20AL-1AJI AT40K20AL-1AQI AT40K20AL-1BQI AT40K20AL-1DQI	84J 100T1 144L1 208Q1	Industrial (-40°C to 85°C)

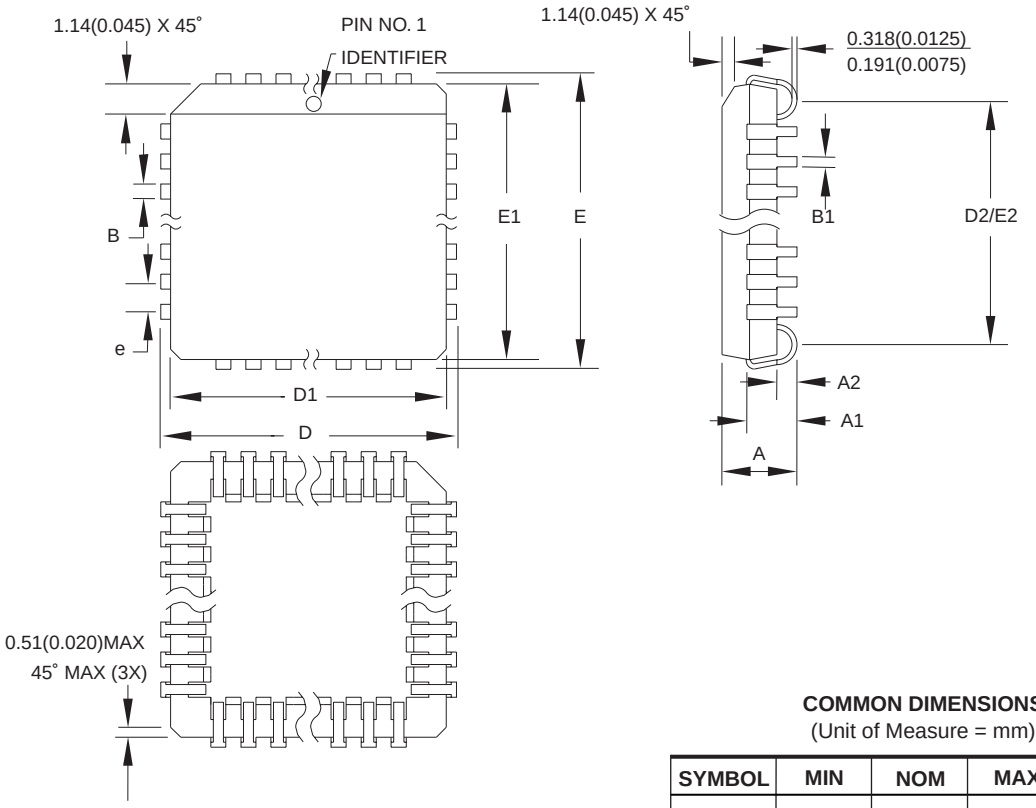
AT40K40AL Ordering Information

Usable Gates	Operating Voltage	Speed Grade (ns)	Ordering Code	Package	Operation Range[1]
40,000 - 50,000	3.3V	1	AT40K40AL-1BQC AT40K40AL-1DQC AT40K40AL-1EQC	144L1 208Q1 240Q1	Commercial (0°C to 70°C)
40,000 - 50,000	3.3V	1	AT40K40AL-1BQI AT40K40AL-1DQI AT40K40AL-1EQI	144L1 208Q1 240Q1	Industrial (-40°C to 85°C)

Note: 1. For military parts, contact Atmel at fpga@atmel.com.

Packaging Information

84J – PLCC



COMMON DIMENSIONS
(Unit of Measure = mm)

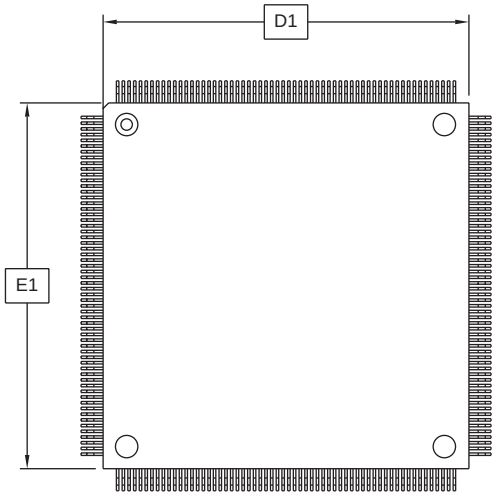
SYMBOL	MIN	NOM	MAX	NOTE
A	4.191	–	4.572	
A1	2.286	–	3.048	
A2	0.508	–	–	
D	30.099	–	30.353	
D1	29.210	–	29.413	Note 2
E	30.099	–	30.353	
E1	29.210	–	29.413	Note 2
D2/E2	27.686	–	28.702	
B	0.660	–	0.813	
B1	0.330	–	0.533	
e	1.270 TYP			

Notes:
1. This package conforms to JEDEC reference MS-018, Variation AF.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010"(0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
3. Lead coplanarity is 0.004" (0.102 mm) maximum.

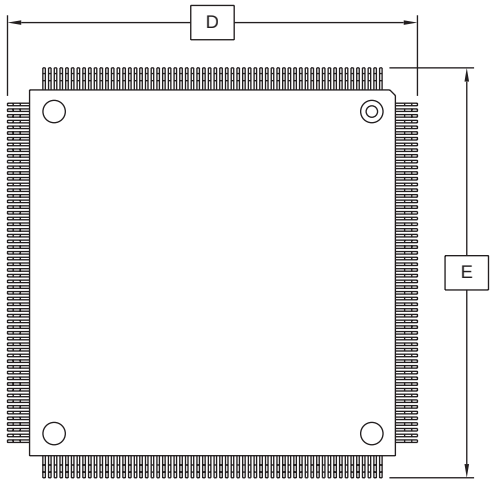
10/04/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**84J**, 84-lead, Plastic J-leaded Chip Carrier (PLCC)	84J	B

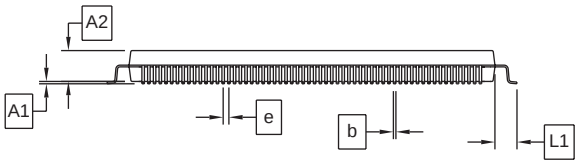
240Q1 – PQFP



Top View



Bottom View



Side View

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A1	0.25	–	0.50	
A2	3.20	3.40	3.60	
D		34.60 BSC		3
D1		32.00 BSC		2, 4
E		34.60 BSC		3
E1		32.00 BSC		2, 4
e		0.50 BSC		
b	0.17	–	0.27	5
L1		1.30 REF		

Notes:
1. This drawing is for general information only. Refer to JEDEC Drawing MS-029, Variation GA, for additional information.
2. All dimensioning and tolerancing conforms to ASME Y14.5M-1994.
3. To be determined at seating plane.
4. Dimensions D1 and E1 do not include mold protrusions. Allowable protrusion is 0.25 mm per side. D1 and E1 are maximum plastic body size dimensions including mold mismatch. Dimensions D1 and E1 shall be determined at datum plane.
5. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall not cause the lead width to exceed the maximum b dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. The minimum space between protrusion and an adjacent lead shall not be less than 0.07 mm.

3/29/02

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**240Q1,** 240-lead, 32 x 32 mm Body, 2.6 Form Opt., Plastic Quad Flat Pack (PQFP)	240Q1	A

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