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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

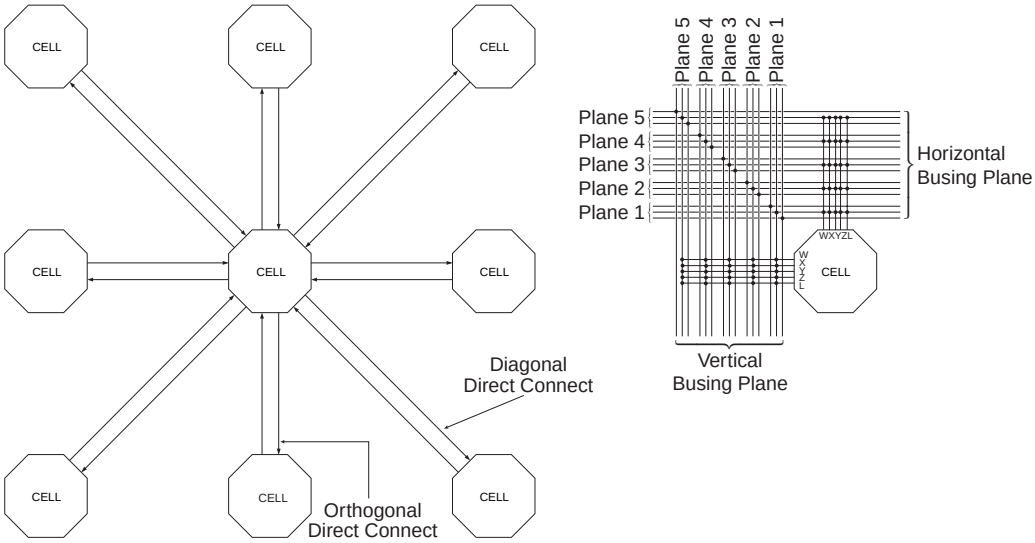
The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	1024
Total RAM Bits	8192
Number of I/O	256
Number of Gates	30000
Voltage - Supply	3V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C
Package / Case	352-LBGA
Supplier Device Package	352-SBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at40k20al-1bgc

Cell Connections

Figure 4(a) depicts direct connections between a cell and its eight nearest neighbors. Figure 4(b) shows the connections between a cell and five horizontal local buses (1 per busing plane) and five vertical local buses (1 per busing plane).

Figure 4. Cell Connections



(a) Cell-to-cell Connections

(b) Cell-to-bus Connections

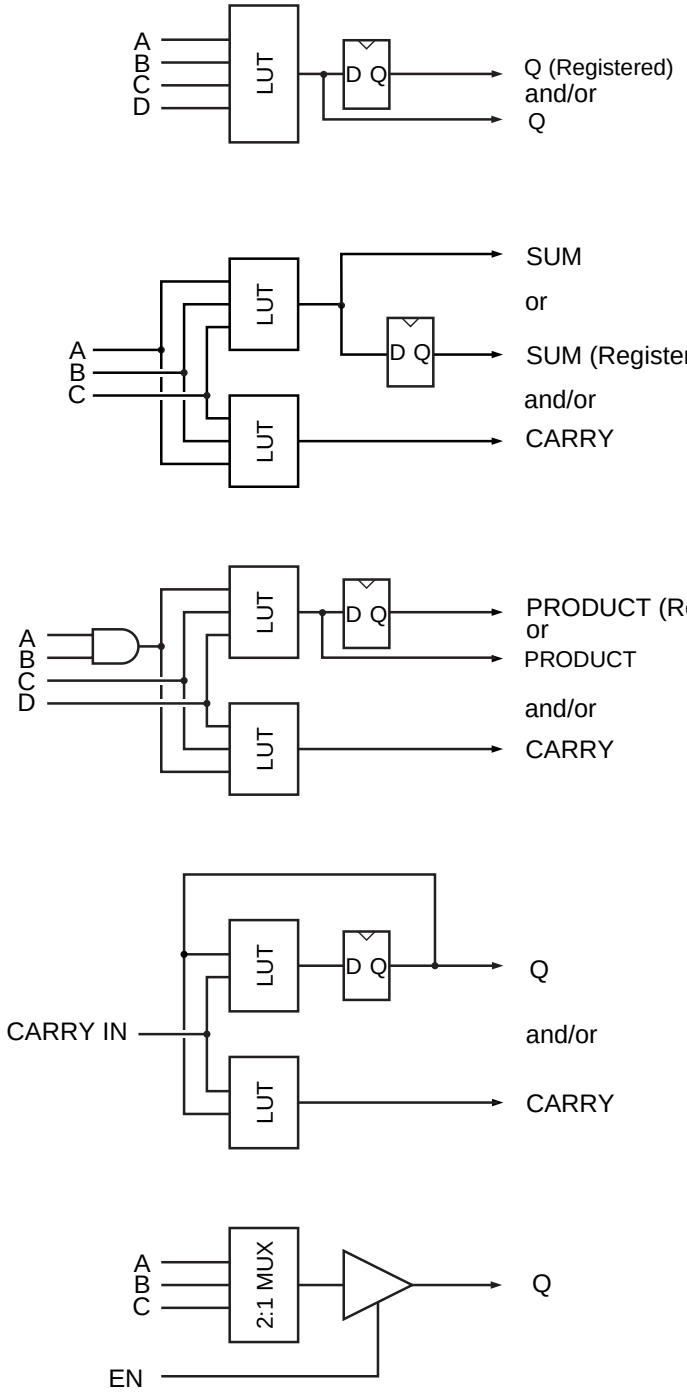
The Cell

Figure 5 depicts the AT40KAL cell. Configuration bits for separate muxes and pass gates are independent. All permutations of programmable muxes and pass gates are legal. V_n (V_1 - V_5) is connected to the vertical local bus in plane n. H_n (H_1 - H_5) is connected to the horizontal local bus in plane *n*. A local/local turn in plane n is achieved by turning on the two pass gates connected to V_n and H_n. Pass gates are opened to let signals into the cell from a local bus or to drive a signal out onto a local bus. Signals coming into the logic cell on one local bus plane can be switched onto another plane by opening two of the pass gates. This allows bus signals to switch planes to achieve greater route ability. Up to five simultaneous local/local turns are possible.

The AT40KAL FPGA core cell is a highly configurable logic block based around two 3-input LUTs (8 x 1 ROM), which can be combined to produce one 4-input LUT. This means that any core cell can implement two functions of 3 inputs or one function of 4 inputs. There is a Set/Reset D flip-flop in every cell, the output of which may be tri-stated and fed back internally within the core cell. There is also a 2-to-1 multiplexer in every cell, and an upstream AND gate in the “front end” of the cell. This AND gate is an important feature in the implementation of efficient array multipliers.

With this functionality in each core cell, the core cell can be configured in several “modes”. The core cell flexibility makes the AT40KAL architecture well suited to most digital design application areas, see Figure 6.

Figure 6. Some Single Cell Modes



Synthesis Mode. This mode is particularly important for the use of VHDL/Verilog design. VHDL/Verilog Synthesis tools generally will produce as their output large amounts of random logic functions. Having a 4-input LUT structure gives efficient random logic optimization without the delays associated with larger LUT structures. The output of any cell may be registered, tri-stated and/or fed back into a core cell.

Arithmetic Mode is frequently used in many designs. As can be seen in the figure, the AT40KAL core cell can implement a 1-bit full adder (2-input adder with both Carry In and Carry Out) in one core cell. Note that the sum output in this diagram is registered. This output could then be tri-stated and/or fed back into the cell.

DSP/Multiplier Mode. This mode is used to efficiently implement array multipliers. An array multiplier is an array of bitwise multipliers, each implemented as a full adder with an upstream AND gate. Using this AND gate and the diagonal interconnects between cells, the array multiplier structure fits very well into the AT40KAL architecture.

Counter Mode. Counters are fundamental to almost all digital designs. They are the basis of state machines, timing chains and clock dividers. A counter is essentially an increment by one function (i.e., an adder), with the input being an output (or a decode of an output) from the previous stage. A 1-bit counter can be implemented in one core cell. Again, the output can be registered, tri-stated and/or fed back.

Tri-state/Mux Mode. This mode is used in many telecommunications applications, where data needs to be routed through more than one possible path. The output of the core cell is very often tri-statable for many inputs to many outputs data switching.

RAM

32 x 4 dual-ported RAM blocks are dispersed throughout the array, see Figure 7. A 4-bit Input Data Bus connects to four horizontal local buses distributed over four sector rows (plane 1). A 4-bit Output Data Bus connects to four horizontal local buses distributed over four sector rows (plane 2). A 5-bit Input Address Bus connects to five vertical express buses in the same column. A 5-bit Output Address Bus connects to five vertical express buses in the same column. Ain (input address) and Aout (output address) alternate positions in horizontally aligned RAM blocks. For the left-most RAM blocks, Aout is on the left and Ain is on the right. For the right-most RAM blocks, Ain is on the left and Aout is tied off, thus it can only be configured as a single port. For single-ported RAM, Ain is the READ/WRITE address port and Din is the (bi-directional) data port. Right-most RAM blocks can be used only for single-ported memories. WEN and OEN connect to the vertical express buses in the same column.

Figure 7. RAM Connections (One Ram Block)

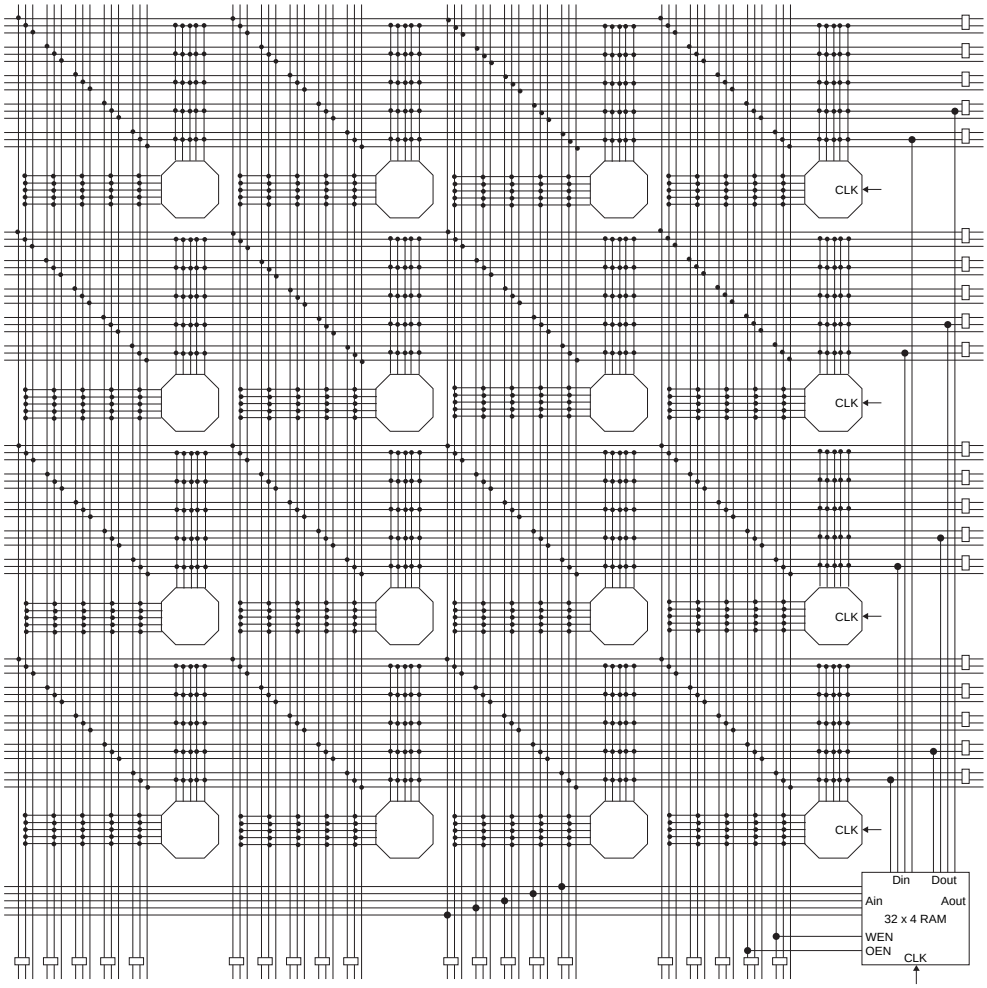


Figure 9. RAM Example: 128 x 8 Dual-ported RAM (Asynchronous)

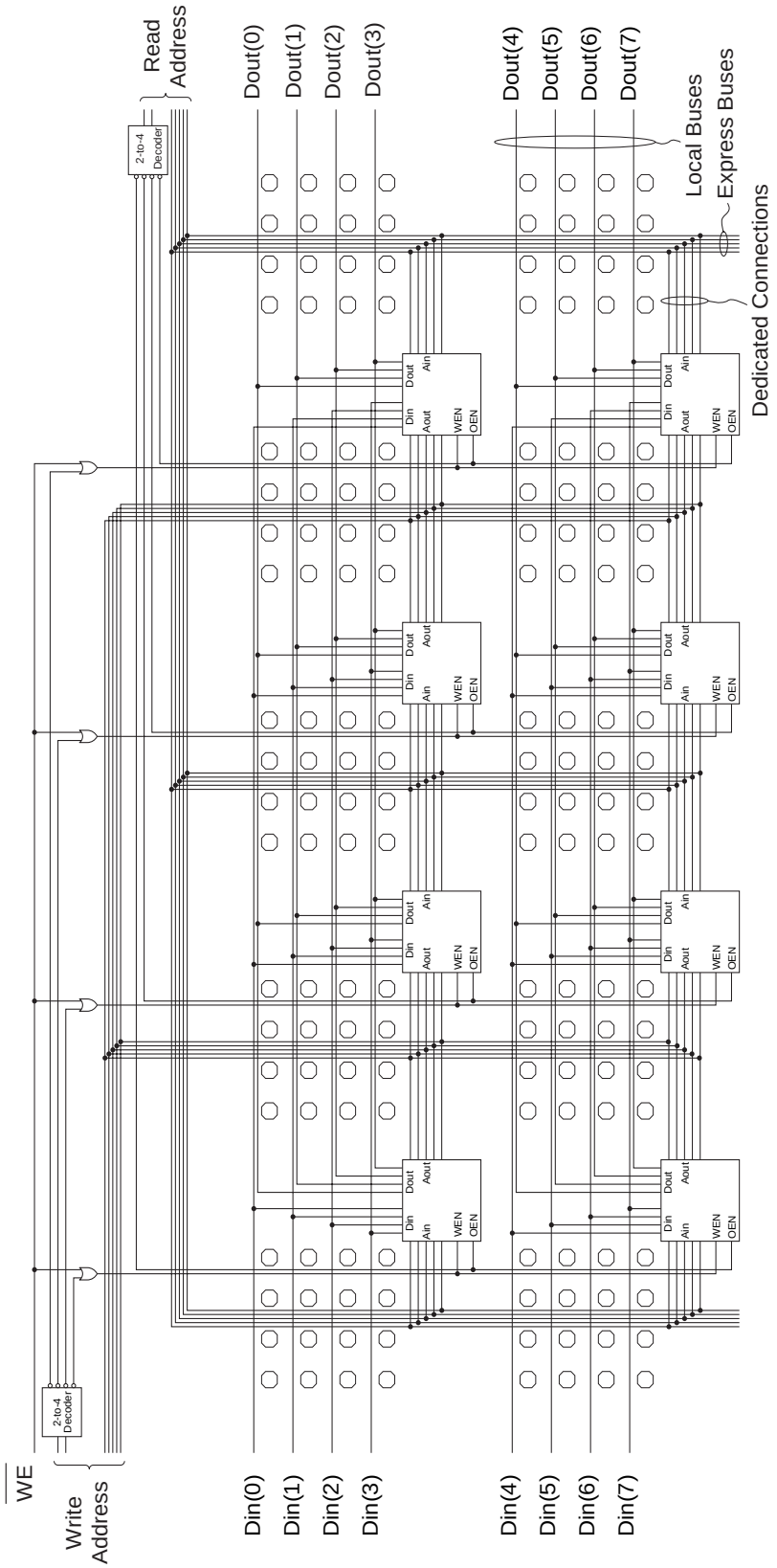
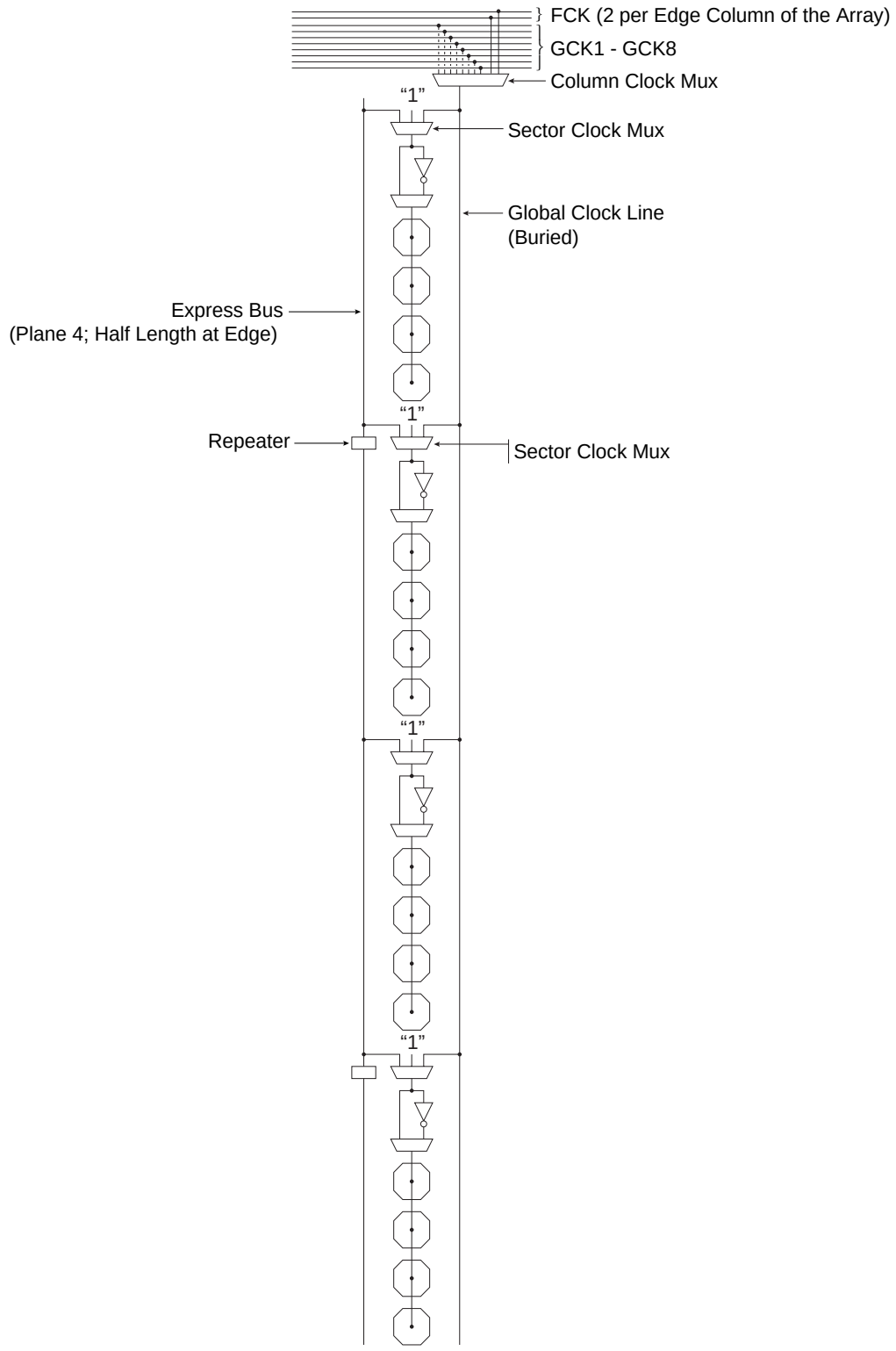


Figure 10. Clocking (for One Column of Cells)



Set/Reset Scheme

The AT40KAL family reset scheme is essentially the same as the clock scheme except that there is only one Global Reset. A dedicated Global Set/Reset bus can be driven by any User I/O, except those used for clocking (Global Clocks or Fast Clocks). The automatic placement tool will choose the reset net with the most connections to use the global resources. You can change this by using an RSBUF component in your design to indicate the global reset. Additional resets will use the express bus network.

The Global Set/Reset is distributed to each column of the array. Like Sector Clock mux, there is Sector Set/Reset mux at every four cells. Each sector column of four cells is set/reset by a Plane 5 express bus or Global Set/Reset using the Sector Set/Reset mux, see Figure 11 on page 17. The set/reset provided to each sector column of four cells is either inverted or non-inverted using the Sector Reset mux.

The function of the Set/Reset input of a register is determined by a configuration bit in each cell. The Set/Reset input of a register is active low (logic 0) by default. Setting or Resetting of a register is asynchronous. Before configuration on power-up, a logic 1 (a high) is provided by each register (i.e., all registers are set at power-up).

Primary, Secondary and Corner I/Os

The AT40KAL has three kinds of I/Os: Primary I/O, Secondary I/O and a Corner I/O. Every edge cell except corner cells on the AT40KAL has access to one Primary I/O and two Secondary I/Os.

Primary I/O

Every logic cell at the edge of the FPGA array has a direct orthogonal connection to and from a Primary I/O cell. The Primary I/O interfaces directly to its adjacent core cell. It also connects into the repeaters on the row immediately above and below the adjacent core cell. In addition, each Primary I/O also connects into the busing network of the three nearest edge cells. This is an extremely powerful feature, as it provides logic cells toward the center of the array with fast access to I/Os via local and express buses. It can be seen from the diagram that a given Primary I/O can be accessed from any logic cell on three separate rows or columns of the FPGA. See Figure 12 on page 20.

Secondary I/O

Every logic cell at the edge of the FPGA array has two direct diagonal connections to a Secondary I/O cell. The Secondary I/O is located between core cell locations. This I/O connects on the diagonal inputs to the cell above and the cell below. It also connects to the repeater of the cell above and below. In addition, each Secondary I/O also connects into the busing network of the two nearest edge cells. This is an extremely powerful feature, as it provides logic cells toward the center of the array with fast access to I/Os via local and express buses. It can be seen from the diagram that a given Secondary I/O can be accessed from any logic cell on two rows or columns of the FPGA. See Figure 13 on page 20.

Corner I/O

Logic cells at the corner of the FPGA array have direct-connect access to five separate I/Os: 2 Primary, 2 Secondary and 1 Corner I/O. Corner I/Os are like an extra Secondary I/O at each corner of the array. With the inclusion of Corner I/Os, an AT40KAL FPGA with n x n core cells always has 8n I/Os. As the diagram shows, Corner I/Os can be accessed both from the corner logic cell and the horizontal and vertical busing networks running along the edges of the array. This means that many different edge logic cells can access the Corner I/Os. See Figure 14 on page 21.

AC Timing Characteristics – 3.3V Operation

Delays are based on fixed loads and are described in the notes.
Maximum times based on worst case: V_{CC} = 3.00V, temperature = 70°C
Minimum times based on best case: V_{CC} = 3.60V, temperature = 0°C
Maximum delays are the average of t_{PDLH} and t_{PDHL}.

Cell Function	Parameter	Path	-1	Units	Notes
Core					
2-input Gate	t_{PD} (Maximum)	x/y -> x/y	1.8	ns	1 unit load
3-input Gate	t_{PD} (Maximum)	x/y/z -> x/y	2.1	ns	1 unit load
3-input Gate	t_{PD} (Maximum)	x/y/w -> x/y	2.2	ns	1 unit load
4-input Gate	t_{PD} (Maximum)	x/y/w/z -> x/y	2.2	ns	1 unit load
Fast Carry	t_{PD} (Maximum)	y -> y	1.4	ns	1 unit load
Fast Carry	t_{PD} (Maximum)	x -> y	1.7	ns	1 unit load
Fast Carry	t_{PD} (Maximum)	y -> x	1.8	ns	1 unit load
Fast Carry	t_{PD} (Maximum)	x -> x	1.5	ns	1 unit load
Fast Carry	t_{PD} (Maximum)	w -> y	2.2	ns	1 unit load
Fast Carry	t_{PD} (Maximum)	w -> x	2.3	ns	1 unit load
Fast Carry	t_{PD} (Maximum)	z -> y	2.3	ns	1 unit load
Fast Carry	t_{PD} (Maximum)	z -> x	1.7	ns	1 unit load
DFF	t_{PD} (Maximum)	q -> x/y	1.8	ns	1 unit load
DFF	t_{PD} (Maximum)	R -> x/y	2.2	ns	1 unit load
DFF	t_{PD} (Maximum)	S -> x/y	2.2	ns	1 unit load
DFF	t_{PD} (Maximum)	q -> w	1.8	ns	
Incremental -> L	t_{PD} (Maximum)	x/y -> L	1.5	ns	1 unit load
Local Output Enable	t_{PZX} (Maximum)	oe -> L	1.4	ns	1 unit load
Local Output Enable	t_{PXZ} (Maximum)	oe -> L	1.8	ns	

AC Timing Characteristics – 3.3V Operation

Delays are based on fixed loads and are described in the notes.
Maximum times based on worst case: V_{CC} = 3.0V, temperature = 70°C
Minimum times based on best case: V_{CC} = 3.6V, temperature = 0°C
Maximum delays are the average of t_{PDLH} and t_{PDHL}.

All input IO characteristics measured from a V_{IH} of 50% of V_{DD} at the pad (CMOS threshold) to the internal V_{IH} of 50% of V_{DD}. All output IO characteristics are measured as the average of t_{PDLH} and t_{PDHL} to the pad V_{IH} of 50% of V_{DD}.

Cell Function	Parameter	Path	-1	Units	Notes
Repeaters					
Repeater	t_{PD} (Maximum)	L -> E	1.3	ns	1 unit load
Repeater	t_{PD} (Maximum)	E -> E	1.3	ns	1 unit load
Repeater	t_{PD} (Maximum)	L -> L	1.3	ns	1 unit load
Repeater	t_{PD} (Maximum)	E -> L	1.3	ns	1 unit load
Repeater	t_{PD} (Maximum)	E -> IO	0.8	ns	1 unit load
Repeater	t_{PD} (Maximum)	L -> IO	0.8	ns	1 unit load

All input IO characteristics measured from a V_{IH} of 50% of V_{DD} at the pad (CMOS threshold) to the internal V_{IH} of 50% of V_{DD}. All output IO characteristics are measured as the average of t_{PDLH} and t_{PDHL} to the pad V_{IH} of 50% of V_{DD}.

Cell Function	Parameter	Path	-1	Units	Notes
IO					
Input	t_{PD} (Maximum)	pad -> x/y	1.2	ns	No extra delay
Input	t_{PD} (Maximum)	pad -> x/y	3.6	ns	1 extra delay
Input	t_{PD} (Maximum)	pad -> x/y	7.3	ns	2 extra delays
Input	t_{PD} (Maximum)	pad -> x/y	10.8	ns	3 extra delays
Output, Slow	t_{PD} (Maximum)	x/y/E/L -> pad	5.9	ns	50 pf load
Output, Medium	t_{PD} (Maximum)	x/y/E/L -> pad	4.8	ns	50 pf load
Output, Fast	t_{PD} (Maximum)	x/y/E/L -> pad	3.9	ns	50 pf load
Output, Slow	t_{PZX} (Maximum)	oe -> pad	6.2	ns	50 pf load
Output, Slow	t_{PXZ} (Maximum)	oe -> pad	1.3	ns	50 pf load
Output, Medium	t_{PZX} (Maximum)	oe -> pad	4.8	ns	50 pf load
Output, Medium	t_{PXZ} (Maximum)	oe -> pad	1.9	ns	50 pf load
Output, Fast	t_{PZX} (Maximum)	oe -> pad	3.7	ns	50 pf load
Output, Fast	t_{PXZ} (Maximum)	oe -> pad	1.6	ns	50 pf load

AC Timing Characteristics – 3.3V Operation

Delays are based on fixed loads and are described in the notes.
Maximum times based on worst case: V_{CC} = 3.0V, temperature = 70°C
Minimum times based on best case: V_{CC} = 3.6V, temperature = 0°C

Cell Function	Parameter	Path	-1	Units	Notes
Async RAM					
Write	t_{WECYC} (Minimum)	cycle time	12.0	ns	
Write	t_{WEL} (Minimum)	we	5.0	ns	Pulse width low
Write	t_{WEH} (Minimum)	we	5.0	ns	Pulse width high
Write	t_{AWS} (Minimum)	wr addr setup -> we	5.3	ns	
Write	t_{AWH} (Minimum)	wr addr hold -> we	0.0	ns	
Write	t_{DS} (Minimum)	din setup -> we	5.0	ns	
Write	t_{DH} (Minimum)	din hold -> we	0.0	ns	
Write/Read	t_{DD} (Maximum)	din -> dout	8.7	ns	rd addr = wr addr
Read	t_{AD} (Maximum)	rd addr -> dout	6.3	ns	
Read	t_{OZX} (Maximum)	oe -> dout	2.9	ns	
Read	t_{OXZ} (Maximum)	oe -> dout	3.5	ns	
Sync RAM					
Write	t_{CYC} (Minimum)	cycle time	12.0	ns	
Write	t_{CLKL} (Minimum)	clk	5.0	ns	Pulse width low
Write	t_{CLKH} (Minimum)	clk	5.0	ns	Pulse width high
Write	t_{WCS} (Minimum)	we setup -> clk	3.2	ns	
Write	t_{WCH} (Minimum)	we hold -> clk	0.0	ns	
Write	t_{ACS} (Minimum)	wr addr setup -> clk	5.0	ns	
Write	t_{ACH} (Minimum)	wr addr hold -> clk	0.0	ns	
Write	t_{DCS} (Minimum)	wr data setup -> clk	3.9	ns	
Write	t_{DCH} (Minimum)	wr data hold -> clk	0.0	ns	
Write/Read	t_{CD} (Maximum)	clk -> dout	5.8	ns	rd addr = wr addr
Read	t_{AD} (Maximum)	rd addr -> dout	6.3	ns	
Read	t_{OZX} (Maximum)	oe -> dout	2.9	ns	
Read	t_{OXZ} (Maximum)	oe -> dout	3.5	ns	

Notes:
1. CMOS buffer delays are measured from a V_{IH} of 1/2 V_{CC} at the pad to the internal V_{IH} at A. The input buffer load is constant.
2. Buffer delay is to a pad voltage of 1.5V with one output switching.
3. Parameter based on characterization and simulation; not tested in production.
4. Exact power calculation is available in Atmel FPGA Designer software.

AT40K05AL	AT40K10AL	AT40K20AL	AT40K40AL	Left Side (Top to Bottom)				
128 I/O	192 I/O	256 I/O	384 I/O	84 PLCC	100 TQFP	144 LQFP	208 PQFP	240 PQFP
I/O9, FCK1	I/O13, FCK1	I/O17, FCK1	I/O25, FCK1			9	15	15
I/O10	I/O14	I/O18	I/O26			10	16	16
I/O11 (A20)	I/O15 (A20)	I/O19 (A20)	I/O27 (A20)	17	6	11	17	17
I/O12 (A21)	I/O16 (A21)	I/O20 (A21)	I/O28 (A21)	18	7	12	18	18
	VCC	VCC	VCC					19
	I/O17	I/O21	I/O29					20
	I/O18	I/O22	I/O30					21
			GND					
			I/O31					
			I/O32					
			I/O33					
			I/O34					
		I/O23	I/O35					
		I/O24	I/O36					
		GND	GND					22
			VCC					
			I/O37					
			I/O38					
		I/O25	I/O39					
		I/O26	I/O40					
	I/O19	I/O27	I/O41				19	23
	I/O20	I/O28	I/O42				20	24
			GND					
I/O13	I/O21	I/O29	I/O43			13	21	25
I/O14	I/O22	I/O30	I/O44		8	14	22	26
			I/O45					
			I/O46					
I/O15 (A22)	I/O23 (A22)	I/O31 (A22)	I/O47 (A22)	19	9	15	23	27
I/O16 (A23)	I/O24 (A23)	I/O32 (A23)	I/O48 (A23)	20	10	16	24	28
GND	GND	GND	GND	21	11	17	25	29
VCC	VCC	VCC	VCC	22	12	18	26	30

Note: 1. On-chip tri-state

AT40K05AL	AT40K10AL	AT40K20AL	AT40K40AL	Bottom Side (Left to Right)				
128 I/O	192 I/O	256 I/O	384 I/O	84 PLCC	100 TQFP	144 LQFP	208 PQFP	240 PQFP
VCC	VCC	VCC	VCC	33	25	37	55	61
M2	M2	M2	M2	34	26	38	56	62
I/O33, GCK3	I/O49, GCK3	I/O65, GCK3	I/O97, GCK3	35	27	39	57	63
I/O34 (HDC)	I/O50 (HDC)	I/O66 (HDC)	I/O98 (HDC)	36	28	40	58	64
I/O35	I/O51	I/O67	I/O99			41	59	65
I/O36	I/O52	I/O68	I/O100			42	60	66
I/O37	I/O53	I/O69	I/O101		29	43	61	67
I/O38 (LDC)	I/O54 (LDC)	I/O70 (LDC)	I/O102 (LDC)	37	30	44	62	68
			GND					
			I/O103					
			I/O104					
			I/O105					
			I/O106					
		I/O71	I/O107					
		I/O72	I/O108					
		VCC	VCC					
		GND	GND					
I/O39	I/O55	I/O73	I/O109				63	69
I/O40	I/O56	I/O74	I/O110				64	70
	I/O57	I/O75	I/O111				65	71
	I/O58	I/O76	I/O112				66	72
			I/O113					
			I/O114					
			GND					
		I/O77	I/O115					
		I/O78	I/O116					
	I/O59	I/O79	I/O117					73
	I/O60	I/O80	I/O118					74
			I/O119					
			I/O120					
GND	GND	GND	GND			45	67	75
I/O41	I/O61	I/O81	I/O121			46	68	76

AT40K05AL	AT40K10AL	AT40K20AL	AT40K40AL	Bottom Side (Left to Right)				
128 I/O	192 I/O	256 I/O	384 I/O	84 PLCC	100 TQFP	144 LQFP	208 PQFP	240 PQFP
I/O42	I/O62	I/O82	I/O122			47	69	77
I/O43	I/O63	I/O83	I/O123	38	31	48	70	78
I/O44	I/O64	I/O84	I/O124	39	32	49	71	79
	VCC	VCC	VCC					80
	I/O65	I/O85	I/O125				72	81
	I/O66	I/O86	I/O126				73	82
			GND					
			I/O127					
			I/O128					
			I/O129					
			I/O130					
		I/O87	I/O131					
		I/O88	I/O132					
		GND	GND					83
			VCC					
		I/O89	I/O133					
		I/O90	I/O134					
	I/O67	I/O91	I/O135					84
	I/O68	I/O92	I/O136					85
I/O45	I/O69	I/O93	I/O137		33	50	74	86
I/O46	I/O70	I/O94	I/O138		34	51	75	87
			GND					
			I/O139					
			I/O140					
			I/O141					
			I/O142					
I/O47 (D15)	I/O71 (D15)	I/O95 (D15)	I/O143 (D15)	40	35	52	76	88
I/O48 (INIT)	I/O72 (INIT)	I/O96 (INIT)	I/O144 (INIT)	41	36	53	77	89
VCC	VCC	VCC	VCC	42	37	54	78	90
GND	GND	GND	GND	43	38	55	79	91
I/O49 (D14)	I/O73 (D14)	I/O97 (D14)	I/O145 (D14)	44	39	56	80	92
I/O50 (D13)	I/O74 (D13)	I/O98 (D13)	I/O146 (D13)	45	40	57	81	93

AT40K05AL	AT40K10AL	AT40K20AL	AT40K40AL	Right Side (Bottom to Top)				
128 I/O	192 I/O	256 I/O	384 I/O	84 PLCC	100 TQFP	144 LQFP	208 PQFP	240 PQFP
VCC	VCC	VCC	VCC	54	51	73	106	121
$\overline{\text{RESET}}$	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$	55	52	74	108	122
I/O65 (D7)	I/O97 (D7)	I/O129 (D7)	I/O193 (D7)	56	53	75	109	123
I/O66, GCK5	I/O98, GCK5	I/O130, GCK5	I/O194, GCK5	57	54	76	110	124
I/O67	I/O99	I/O131	I/O195			77	111	125
I/O68	I/O100	I/O132	I/O196			78	112	126
		I/O133	I/O197					
		I/O134	I/O198					
			GND					
	I/O101	I/O135	I/O199					127
	I/O102	I/O136	I/O200					128
			I/O201					
			I/O202					
			I/O203					
			I/O204					
		VCC	VCC					
		GND	GND					
I/O69 (D6)	I/O103 (D6)	I/O137 (D6)	I/O205 (D6)	58	55	79	113	129
I/O70	I/O104	I/O138	I/O206		56	80	114	130
I/O71	I/O105	I/O139	I/O207				115	131
I/O72	I/O106	I/O140	I/O208				116	132
			I/O209					
			I/O210					
			GND					
			I/O211					
			I/O212					
	I/O107	I/O141	I/O213				117	133
	I/O108	I/O142	I/O214				118	134
		I/O143	I/O215					
		I/O144	I/O216					
GND	GND	GND	GND			81	119	135
	I/O109	I/O145	I/O217					136
	I/O110	I/O146	I/O218					137

AT40K05AL	AT40K10AL	AT40K20AL	AT40K40AL	Right Side (Bottom to Top)				
128 I/O	192 I/O	256 I/O	384 I/O	84 PLCC	100 TQFP	144 LQFP	208 PQFP	240 PQFP
			I/O243					
			I/O244					
I/O83	I/O123	I/O163	I/O245		67	94	134	154
I/O84	I/O124	I/O164	I/O246			95	135	155
			GND					
	I/O125	I/O165	I/O247				136	156
	I/O126	I/O166	I/O248				137	157
		I/O167	I/O249					
		I/O168	I/O250					
			I/O251					
			I/O252					
			VCC					
		GND	GND					158
		I/O169	I/O253					
		I/O170	I/O254					
			I/O255					
			I/O256					
			I/O257					
			I/O258					
			GND					
I/O85 (D2)	I/O127 (D2)	I/O171 (D2)	I/O259 (D2)	67	68	96	138	159
I/O86	I/O128	I/O172	I/O260	68	69	97	139	160
	VCC	VCC	VCC					161
I/O87	I/O129	I/O173	I/O261			98	140	162
I/O88, FCK4	I/O130, FCK4	I/O174, FCK4	I/O262, FCK4			99	141	163
	I/O131	I/O175	I/O263					164
	I/O132	I/O176	I/O264					165
GND	GND	GND	GND			100	142	166
		I/O177	I/O265					
		I/O178	I/O266					
	I/O133	I/O179	I/O267					167
	I/O134	I/O180	I/O268					168
			I/O269					

AT40K05AL	AT40K10AL	AT40K20AL	AT40K40AL	Top Side (Right to Left)				
128 I/O	192 I/O	256 I/O	384 I/O	84 PLCC	100 TQFP	144 LQFP	208 PQFP	240 PQFP
GND	GND	GND	GND	76	77	110	160	182
I/O97 (A0)	I/O145 (A0)	I/O193 (A0)	I/O289 (A0)	77	78	111	161	183
I/O98, GCK7 (A1)	I/O146, GCK7 (A1)	I/O194, GCK7 (A1)	I/O290, GCK7 (A1)	78	79	112	162	184
I/O99	I/O147	I/O195	I/O291			113	163	185
I/O100	I/O148	I/O196	I/O292			114	164	186
			I/O293					
			I/O294					
			GND					
			I/O295					
			I/O296					
I/O101 ($\overline{CS1}$,A2)	I/O149 ($\overline{CS1}$,A2)	I/O197 ($\overline{CS1}$,A2)	I/O297 ($\overline{CS1}$,A2)	79	80	115	165	187
I/O102 (A3)	I/O150 (A3)	I/O198 (A3)	I/O298 (A3)	80	81	116	166	188
		I/O199	I/O299					
		I/O200	I/O300					
		VCC	VCC					
		GND	GND					
	I/O151[1]	I/O201[1]	I/O301[1]	75[1] NC	76[1] NC	109[1] NC	159[1] NC	189[1] NC
	I/O152	I/O202	I/O302					190
I/O103	I/O153	I/O203	I/O303			117	167	191
I/O104[1]	I/O154	I/O204	I/O304				168	192
			I/O305					
			I/O306					
			GND					
			I/O307					
			I/O308					
	I/O155	I/O205	I/O309				169	193
	I/O156	I/O206	I/O310				170	194
		I/O207	I/O311					195
		I/O208	I/O312					
GND	GND	GND	GND			118	171	196

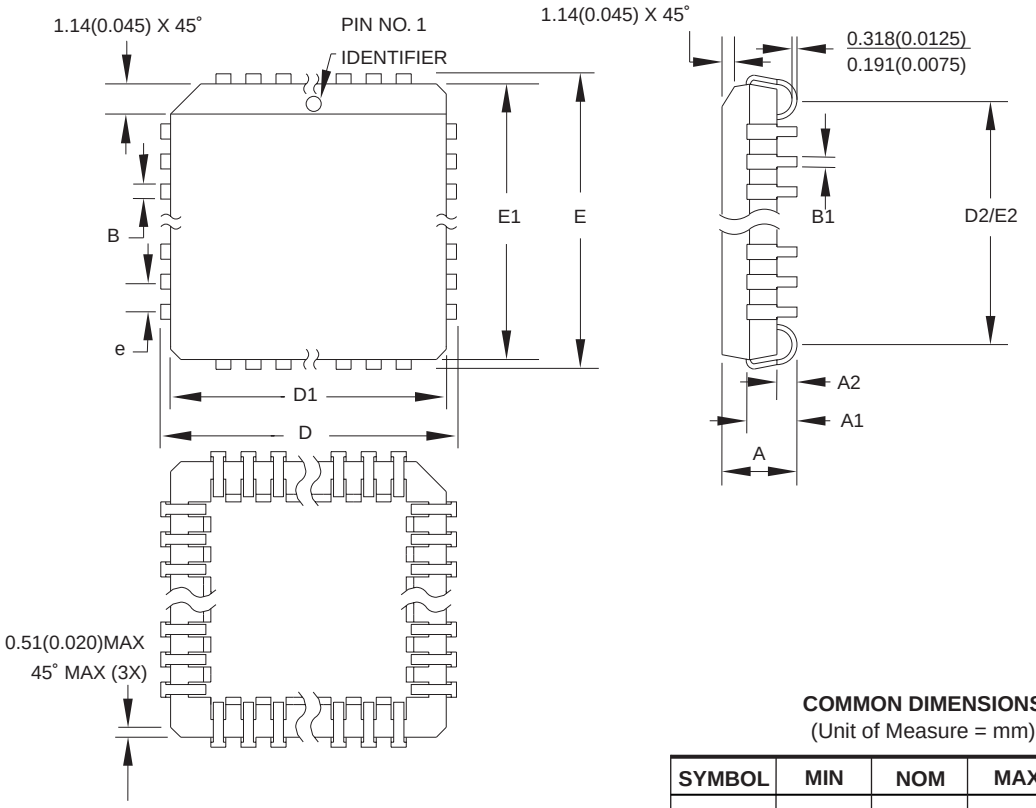
Note: 1. Shared with TSTCLK. No Connect.

AT40K05AL	AT40K10AL	AT40K20AL	AT40K40AL	Top Side (Right to Left)				
128 I/O	192 I/O	256 I/O	384 I/O	84 PLCC	100 TQFP	144 LQFP	208 PQFP	240 PQFP
I/O113 (A8)	I/O169 (A8)	I/O225 (A8)	I/O337 (A8)	3	90	129	184	213
I/O114 (A9)	I/O170 (A9)	I/O226 (A9)	I/O338 (A9)	4	91	130	185	214
			I/O339					
			I/O340					
			I/O341					
			I/O342					
			GND					
I/O115	I/O171	I/O227	I/O343		92	131	186	215
I/O116	I/O172	I/O228	I/O344		93	132	187	216
	I/O173	I/O229	I/O345				188	217
	I/O174	I/O230	I/O346				189	218
I/O117 (A10)	I/O175 (A10)	I/O231 (A10)	I/O347 (A10)	5	94	133	190	220
I/O118 (A11)	I/O176 (A11)	I/O232 (A11)	I/O348 (A11)	6	95	134	191	221
			VCC					
		GND	GND					
		I/O233	I/O349					
		I/O234	I/O350					
			I/O351					
			I/O352					
			I/O353					
			I/O354					
			GND					
		I/O235	I/O355					
		I/O236	I/O356					
	VCC	VCC	VCC					222
	I/O177	I/O237	I/O357					223
	I/O178	I/O238	I/O358					224
I/O119	I/O179	I/O239	I/O359			135	192	225
I/O120	I/O180	I/O240	I/O360			136	193	226
GND	GND	GND	GND			137	194	227
		I/O241	I/O361					

Note: 1. Shared with TSTCLK. No Connect.

Packaging Information

84J – PLCC



COMMON DIMENSIONS
(Unit of Measure = mm)

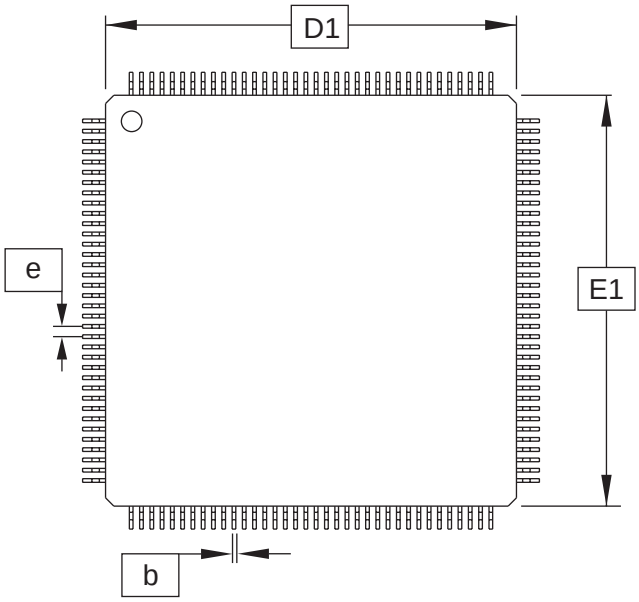
SYMBOL	MIN	NOM	MAX	NOTE
A	4.191	–	4.572	
A1	2.286	–	3.048	
A2	0.508	–	–	
D	30.099	–	30.353	
D1	29.210	–	29.413	Note 2
E	30.099	–	30.353	
E1	29.210	–	29.413	Note 2
D2/E2	27.686	–	28.702	
B	0.660	–	0.813	
B1	0.330	–	0.533	
e	1.270 TYP			

Notes:
1. This package conforms to JEDEC reference MS-018, Variation AF.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010"(0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
3. Lead coplanarity is 0.004" (0.102 mm) maximum.

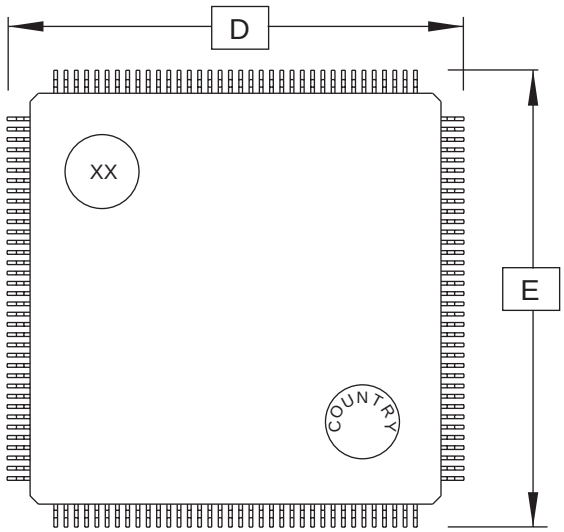
10/04/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**84J**, 84-lead, Plastic J-leaded Chip Carrier (PLCC)	84J	B

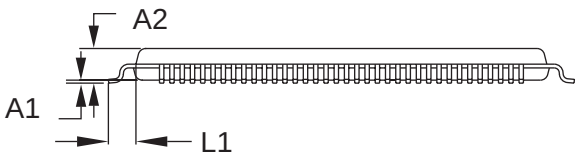
144L1 – LQFP



Top View



Bottom View



Side View

COMMON DIMENSIONS
(Unit of Measure = mm)

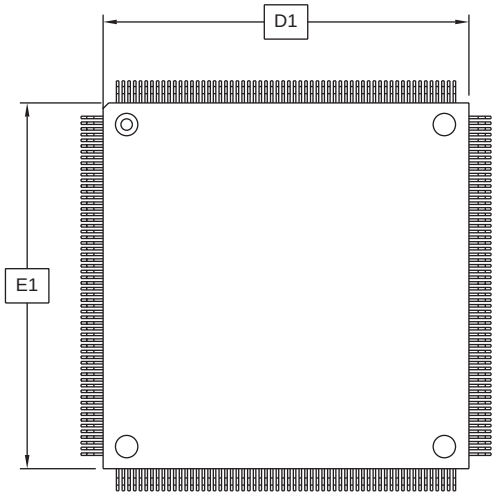
SYMBOL	MIN	NOM	MAX	NOTE
A1	0.05		0.15	6
A2	1.35	1.40	1.45	
D	22.00 BSC			
D1	20.00 BSC			2, 3
E	22.00 BSC			
E1	20.00 BSC			2, 3
e	0.50 BSC			
b	0.17	0.22	0.27	4, 5
L1	1.00 REF			

Notes:
1. This drawing is for general information only; refer to JEDEC Drawing MS-026 for additional information.
2. The top package body size may be smaller than the bottom package size by as much as 0.15 mm.
3. Dimensions D1 and E1 do not include mold protrusions. Allowable protrusion is 0.25 mm per side. D1 and E1 are maximum plastic body size dimensions including mold mismatch.
4. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall not cause the lead width to exceed the maximum b dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 and 0.5 mm pitch packages.
5. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
6. A1 is defined as the distance from the seating place to the lowest point on the package body.

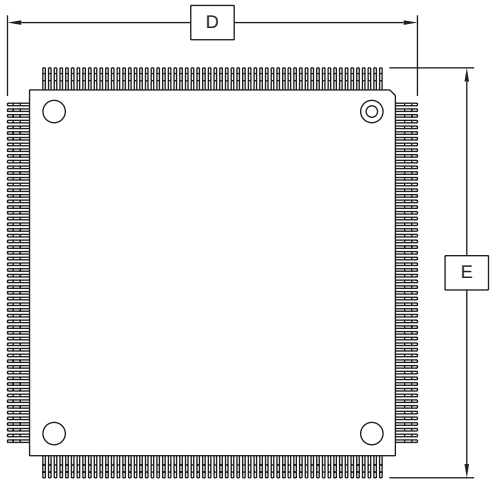
11/30/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**144L1**, 144-lead (20 x 20 x 1.4 mm Body), Low Profile Plastic Quad Flat Pack (LQFP)	144L1	A

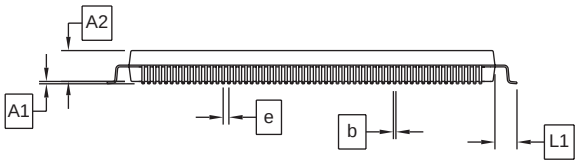
240Q1 – PQFP



Top View



Bottom View



Side View

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A1	0.25	–	0.50	
A2	3.20	3.40	3.60	
D		34.60 BSC		3
D1		32.00 BSC		2, 4
E		34.60 BSC		3
E1		32.00 BSC		2, 4
e		0.50 BSC		
b	0.17	–	0.27	5
L1		1.30 REF		

Notes:
1. This drawing is for general information only. Refer to JEDEC Drawing MS-029, Variation GA, for additional information.
2. All dimensioning and tolerancing conforms to ASME Y14.5M-1994.
3. To be determined at seating plane.
4. Dimensions D1 and E1 do not include mold protrusions. Allowable protrusion is 0.25 mm per side. D1 and E1 are maximum plastic body size dimensions including mold mismatch. Dimensions D1 and E1 shall be determined at datum plane.
5. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall not cause the lead width to exceed the maximum b dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. The minimum space between protrusion and an adjacent lead shall not be less than 0.07 mm.

3/29/02

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**240Q1,** 240-lead, 32 x 32 mm Body, 2.6 Form Opt., Plastic Quad Flat Pack (PQFP)	240Q1	A