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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	1024
Total RAM Bits	8192
Number of I/O	114
Number of Gates	30000
Voltage - Supply	3V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TC)
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at40k20al-1bqu

Table 1. AT40KAL Family[1]

Device	AT40K05AL	AT40K10AL	AT40K20AL	AT40K40AL
Usable Gates	5K - 10K	10K - 20K	20K - 30K	40K - 50K
Rows x Columns	16 x 16	24 x 24	32 x 32	48 x 48
Cells	256	576	1,024	2,304
Registers	496[1]	954[1]	1,520[1]	3,048[1]
RAM Bits	2,048	4,608	8,192	18,432
I/O (Maximum)	128	192	256	384

Note: 1. Packages with FCK will have 8 less registers.

Description

The AT40KAL is a family of fully PCI-compliant, SRAM-based FPGAs with distributed 10 ns programmable synchronous/asynchronous, dual-port/single-port SRAM, 8 global clocks, Cache Logic ability (partially or fully reconfigurable without loss of data), automatic component generators, and range in size from 5,000 to 50,000 usable gates. I/O counts range from 128 to 384 in industry standard packages ranging from 84-pin PLCC to 352-ball Square BGA, and support 3.3V designs.

The AT40KAL is designed to quickly implement high-performance, large gate count designs through the use of synthesis and schematic-based tools used on a PC or Sun platform. Atmel's design tools provide seamless integration with industry standard tools such as Synplicity, ModelSim, Exemplar and Viewlogic. See the "IDS Datasheet" available on the Atmel web site (http://www.atmel.com/atmel/acrobat/doc1421.pdf) for a list of other supported tools.

The AT40KAL can be used as a coprocessor for high-speed (DSP/processor-based) designs by implementing a variety of computation intensive, arithmetic functions. These include adaptive finite impulse response (FIR) filters, fast Fourier transforms (FFT), convolvers, interpolators and discrete-cosine transforms (DCT) that are required for video compression and decompression, encryption, convolution and other multimedia applications.

Fast, Flexible and Efficient SRAM

The AT40KAL FPGA offers a patented distributed 10 ns SRAM capability where the RAM can be used without losing logic resources. Multiple independent, synchronous or asynchronous, dual-port or single-port RAM functions (FIFO, scratch pad, etc.) can be created using Atmel's macro generator tool.

Fast, Efficient Array and Vector Multipliers

The AT40KAL's patented 8-sided core cell with direct horizontal, vertical and diagonal cell-to-cell connections implements ultra fast array multipliers without using any busing resources. The AT40KAL's Cache Logic capability enables a large number of design coefficients and variables to be implemented in a very small amount of silicon, enabling vast improvement in system speed at much lower cost than conventional FPGAs.

Cache Logic Design

The AT40KAL, AT6000 and FPSLIC families are capable of implementing Cache Logic (dynamic full/partial logic reconfiguration, without loss of data, on-the-fly) for building adaptive logic and systems. As new logic functions are required, they can be loaded into the logic cache without losing the data already there or disrupting the operation of the rest of the chip; replacing or complementing the active logic. The AT40KAL can act as a reconfigurable coprocessor.

Automatic Component Generators

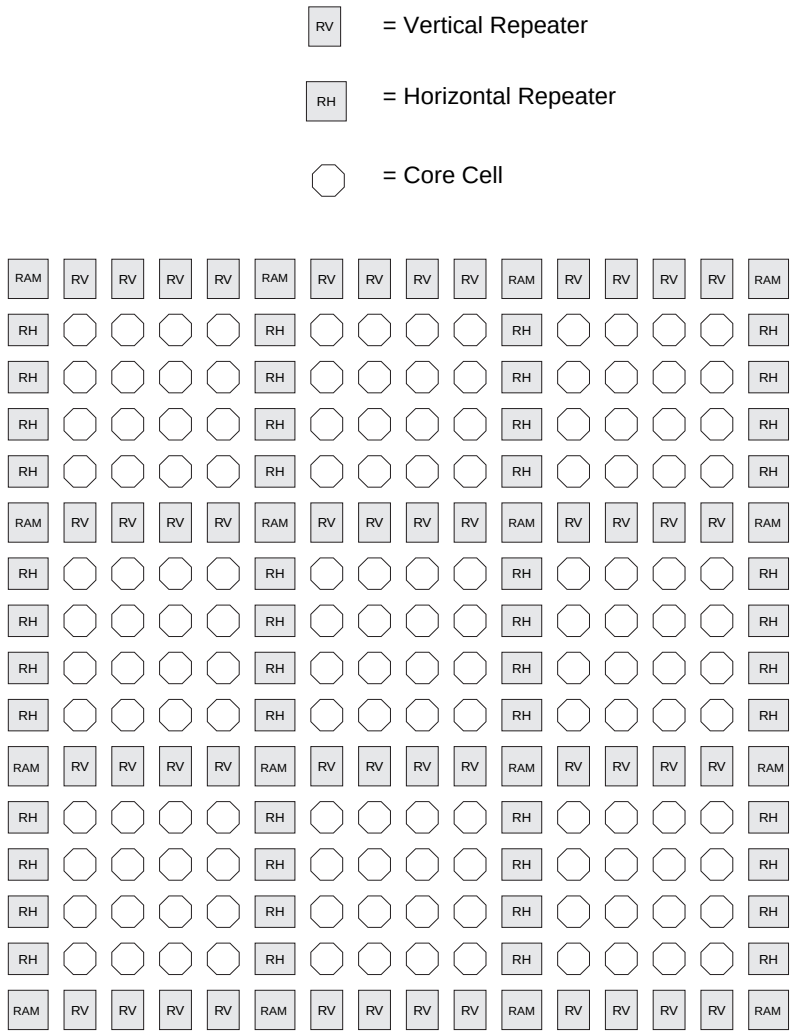
The AT40KAL FPGA family is capable of implementing user-defined, automatically generated, macros in multiple designs; speed and functionality are unaffected by the macro orientation or density of the target device. This enables the fastest, most predictable and efficient FPGA design approach and minimizes design risk by reusing already proven functions. The Automatic Component Generators work seamlessly with industry standard schematic and synthesis tools to create the fastest, most efficient designs available.

The patented AT40KAL series architecture employs a symmetrical grid of small yet powerful cells connected to a flexible busing network. Independently controlled clocks and resets govern every column of cells. The array is surrounded by programmable I/O.

Devices range in size from 5,000 to 50,000 usable gates in the family, and have 256 to 3,048 registers. Pin locations are consistent throughout the AT40KAL series for easy design migration in the same package footprint. The AT40KAL series FPGAs utilize a reliable 0.35µ triple-metal, CMOS process and are 100% factory-tested. Atmel's PC- and workstation-based integrated development system (IDS) is used to create AT40KAL series designs. Multiple design entry methods are supported.

The Atmel architecture was developed to provide the highest levels of performance, functional density and design flexibility in an FPGA. The cells in the Atmel array are small, efficient and can implement any pair of Boolean functions of (the same) three inputs or any single Boolean function of four inputs. The cell's small size leads to arrays with large numbers of cells, greatly multiplying the functionality in each cell. A simple, high-speed busing network provides fast, efficient communication over medium and long distances.

Figure 2. Floor Plan (Representative Portion)[1]



Note: 1. Repeaters regenerate signals and can connect any bus to any other bus (all pathways are legal) on the same plane. Each repeater has connections to two adjacent local-bus segments and two express-bus segments. This is done automatically using the integrated development system (IDS) tool.

Reading and writing of the 10 ns 32 x 4 dual-port FreeRAM are independent of each other. Reading the 32 x 4 dual-port RAM is completely asynchronous. Latches are transparent; when Load is logic 1, data flows through; when Load is logic 0, data is latched. These latches are used to synchronize Write Address, $\overline{\text{Write Enable Not}}$, and Din signals for a synchronous RAM. Each bit in the 32 x 4 dual-port RAM is also a transparent latch. The front-end latch and the memory latch together form an edge-triggered flip flop. When a nibble (bit = 7) is (Write) addressed and LOAD is logic 1 and $\overline{\text{WE}}$ is logic 0, data flows through the bit. When a nibble is not (Write) addressed or LOAD is logic 0 or $\overline{\text{WE}}$ is logic 1, data is latched in the nibble. The two CLOCK muxes are controlled together; they both select CLOCK (for a synchronous RAM) or they both select "1" (for an asynchronous RAM). CLOCK is obtained from the clock for the sector-column immediately to the left and immediately above the RAM block. Writing any value to the RAM clear byte during configuration clears the RAM (see the "AT40K/40KAL Configuration Series" application note at www.atmel.com).

Figure 8. RAM Logic

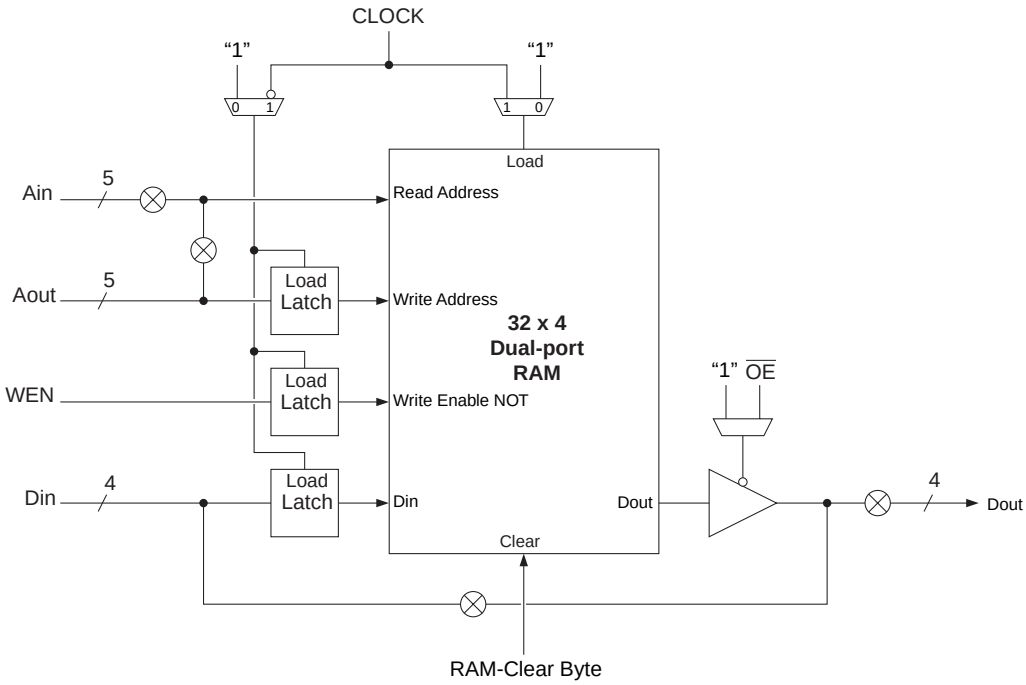


Figure 9 on page 13 shows an example of a RAM macro constructed using the AT40KAL's FreeRAM cells. The macro shown is a 128 x 8 dual-ported asynchronous RAM. Note the very small amount of external logic required to complete the address decoding for the macro. Most of the logic cells (core cells) in the sectors occupied by the RAM will be unused: they can be used for other logic in the design. This logic can be automatically generated using the macro generators.

Primary, Secondary and Corner I/Os

The AT40KAL has three kinds of I/Os: Primary I/O, Secondary I/O and a Corner I/O. Every edge cell except corner cells on the AT40KAL has access to one Primary I/O and two Secondary I/Os.

Primary I/O

Every logic cell at the edge of the FPGA array has a direct orthogonal connection to and from a Primary I/O cell. The Primary I/O interfaces directly to its adjacent core cell. It also connects into the repeaters on the row immediately above and below the adjacent core cell. In addition, each Primary I/O also connects into the busing network of the three nearest edge cells. This is an extremely powerful feature, as it provides logic cells toward the center of the array with fast access to I/Os via local and express buses. It can be seen from the diagram that a given Primary I/O can be accessed from any logic cell on three separate rows or columns of the FPGA. See Figure 12 on page 20.

Secondary I/O

Every logic cell at the edge of the FPGA array has two direct diagonal connections to a Secondary I/O cell. The Secondary I/O is located between core cell locations. This I/O connects on the diagonal inputs to the cell above and the cell below. It also connects to the repeater of the cell above and below. In addition, each Secondary I/O also connects into the busing network of the two nearest edge cells. This is an extremely powerful feature, as it provides logic cells toward the center of the array with fast access to I/Os via local and express buses. It can be seen from the diagram that a given Secondary I/O can be accessed from any logic cell on two rows or columns of the FPGA. See Figure 13 on page 20.

Corner I/O

Logic cells at the corner of the FPGA array have direct-connect access to five separate I/Os: 2 Primary, 2 Secondary and 1 Corner I/O. Corner I/Os are like an extra Secondary I/O at each corner of the array. With the inclusion of Corner I/Os, an AT40KAL FPGA with n x n core cells always has 8n I/Os. As the diagram shows, Corner I/Os can be accessed both from the corner logic cell and the horizontal and vertical busing networks running along the edges of the array. This means that many different edge logic cells can access the Corner I/Os. See Figure 14 on page 21.

Absolute Maximum Ratings – 3.3V Commercial/Industrial*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-0.5V to V_{CC} +7V
Supply Voltage (V_{CC})	-0.5V to +7.0V
Maximum Soldering Temp. (10 sec. @ 1/16 in.)	250°C
ESD (R_{ZAP} = 1.5K, C_{ZAP} = 100 pF)	2000V

*NOTICE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those listed under operating conditions is not implied. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect device reliability.

DC and AC Operating Range – 3.3V Operation

		Commercial	Industrial
Operating Temperature (Case)		0°C - 70°C	-40°C - 85°C
V_{CC} Power Supply		3.3V ± 0.3V	3.3V ± 0.3V
Input Voltage Level (CMOS)	High (V_{IHC})	70% - 100% V_{CC}	70% - 100% V_{CC}
	Low (V_{ILC})	0 - 30% V_{CC}	0 - 30% V_{CC}

DC Characteristics – 3.3V Operation Commercial/Industrial

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{IH}	High-level Input Voltage	CMOS	0.7 V_{CC}		5.5V	V
V_{IL}	Low-level Input Voltage	CMOS	-0.3		30% V_{CC}	V
V_{OH}	High-level Output Voltage	I_{OH} = 4 mA V_{CC} = V_{CC} minimum	2.1			V
		I_{OH} = 12 mA V_{CC} = 3.0V	2.1			V
		I_{OH} = 16 mA V_{CC} = 3.0V	2.1			V
V_{OL}	Low-level Output Voltage	I_{OL} = -4 mA V_{CC} = 3.0V			0.4	V
		I_{OL} = -12 mA V_{CC} = 3.0V			0.4	V
		I_{OL} = -16 mA V_{CC} = 3.0V			0.4	V
I_{IH}	High-level Input Current	V_{IN} = V_{CC} Maximum			10.0	µA
		With pull-down, V_{IN} = V_{CC}	75.0	150.0	300.0	µA
I_{IL}	Low-level Input Current	V_{IN} = V_{SS}	-10.0			µA
		With pull-up, V_{IN} = V_{SS}	-300.0	-150.0	-75.0	µA
I_{OZH}	High-level Tri-state Output Leakage Current	Without pull-down, V_{IN} = V_{CC} Maximum			10.0	µA
		With pull-down, V_{IN} = V_{CC} Maximum	75.0	150.0	300.0	µA
I_{OZL}	Low-level Tri-state Output Leakage Current	Without pull-up, V_{IN} = V_{SS}	-10.0			mA
		With pull-up, V_{IN} = V_{SS}	CON = -500 µA TO -125 µA	-150.0	CON = -500 µA TO -125 µA	µA
I_{CC}	Standby Current Consumption	Standby, unprogrammed		0.6	1.0	mA
C_{IN}	Input Capacitance	All pins			10.0	pF

Note: 1. Parameter based on characterization and simulation; it is not tested in production.

AC Timing Characteristics – 3.3V Operation

Delays are based on fixed loads and are described in the notes.
Maximum times based on worst case: V_{CC} = 3.0V, temperature = 70°C
Minimum times based on best case: V_{CC} = 3.6V, temperature = 0°C
Maximum delays are the average of t_{PDLH} and t_{PDHL}.

All input IO characteristics measured from a V_{IH} of 50% of V_{DD} at the pad (CMOS threshold) to the internal V_{IH} of 50% of V_{DD}. All output IO characteristics are measured as the average of t_{PDLH} and t_{PDHL} to the pad V_{IH} of 50% of V_{DD}.

Cell Function	Parameter	Path	-1	Units	Notes
Repeaters					
Repeater	t_{PD} (Maximum)	L -> E	1.3	ns	1 unit load
Repeater	t_{PD} (Maximum)	E -> E	1.3	ns	1 unit load
Repeater	t_{PD} (Maximum)	L -> L	1.3	ns	1 unit load
Repeater	t_{PD} (Maximum)	E -> L	1.3	ns	1 unit load
Repeater	t_{PD} (Maximum)	E -> IO	0.8	ns	1 unit load
Repeater	t_{PD} (Maximum)	L -> IO	0.8	ns	1 unit load

All input IO characteristics measured from a V_{IH} of 50% of V_{DD} at the pad (CMOS threshold) to the internal V_{IH} of 50% of V_{DD}. All output IO characteristics are measured as the average of t_{PDLH} and t_{PDHL} to the pad V_{IH} of 50% of V_{DD}.

Cell Function	Parameter	Path	-1	Units	Notes
IO					
Input	t_{PD} (Maximum)	pad -> x/y	1.2	ns	No extra delay
Input	t_{PD} (Maximum)	pad -> x/y	3.6	ns	1 extra delay
Input	t_{PD} (Maximum)	pad -> x/y	7.3	ns	2 extra delays
Input	t_{PD} (Maximum)	pad -> x/y	10.8	ns	3 extra delays
Output, Slow	t_{PD} (Maximum)	x/y/E/L -> pad	5.9	ns	50 pf load
Output, Medium	t_{PD} (Maximum)	x/y/E/L -> pad	4.8	ns	50 pf load
Output, Fast	t_{PD} (Maximum)	x/y/E/L -> pad	3.9	ns	50 pf load
Output, Slow	t_{PZX} (Maximum)	oe -> pad	6.2	ns	50 pf load
Output, Slow	t_{PXZ} (Maximum)	oe -> pad	1.3	ns	50 pf load
Output, Medium	t_{PZX} (Maximum)	oe -> pad	4.8	ns	50 pf load
Output, Medium	t_{PXZ} (Maximum)	oe -> pad	1.9	ns	50 pf load
Output, Fast	t_{PZX} (Maximum)	oe -> pad	3.7	ns	50 pf load
Output, Fast	t_{PXZ} (Maximum)	oe -> pad	1.6	ns	50 pf load

AC Timing Characteristics – 3.3V Operation

Delays are based on fixed loads and are described in the notes.
Maximum times based on worst case: V_{CC} = 3.0V, temperature = 70°C
Minimum times based on best case: V_{CC} = 3.6V, temperature = 0°C
Maximum delays are the average of t_{PDLH} and t_{PDHL}.

Clocks and Reset Input buffers are measured from a V_{IH} of 1.5V at the input pad to the internal V_{IH} of 50% of V_{CC}.
Maximum times for clock input buffers and internal drivers are measured for rising edge delays only.

Cell Function	Parameter	Path	Device	-1	Units	Notes
Global Clocks and Set/Reset						
GCLK Input Buffer	t_{PD} (Maximum)	pad -> clock pad -> clock pad -> clock pad -> clock	AT40K05AL AT40K10AL AT40K20AL AT40K40AL	1.1 1.2 1.2 1.4	ns ns ns ns	Rising edge clock
FCLK Input Buffer	t_{PD} (Maximum)	pad -> clock pad -> clock pad -> clock pad -> clock	AT40K05AL AT40K10AL AT40K20AL AT40K40AL	0.7 0.8 0.8 0.8	ns ns ns ns	Rising edge clock
Clock Column Driver	t_{PD} (Maximum)	clock -> colclk clock -> colclk clock -> colclk clock -> colclk	AT40K05AL AT40K10AL AT40K20AL AT40K40AL	0.8 0.9 1.0 1.1	ns ns ns ns	Rising edge clock
Clock Sector Driver	t_{PD} (Maximum)	colclk -> secclk colclk -> secclk colclk -> secclk colclk -> secclk	AT40K05AL AT40K10AL AT40K20AL AT40K40AL	0.5 0.5 0.5 0.5	ns ns ns ns	Rising edge clock
GSRN Input Buffer	t_{PD} (Maximum)	pad -> GSRN pad -> GSRN pad -> GSRN pad -> GSRN	AT40K05AL AT40K10AL AT40K20AL AT40K40AL	3.0 3.7 4.3 5.6	ns ns ns ns	From any pad to Global Set/Reset network
Global Clock to Output	t_{PD} (Maximum)	clock pad -> out clock pad -> out clock pad -> out clock pad -> out	AT40K05AL AT40K10AL AT40K20AL AT40K40AL	8.3 8.4 8.6 8.8	ns ns ns ns	Rising edge clock Fully loaded clock tree Rising edge DFF 20 mA output buffer 50 pf pin load
Fast Clock to Output	t_{PD} (Maximum)	clock pad -> out clock pad -> out clock pad -> out clock pad -> out	AT40K05AL AT40K10AL AT40K20AL AT40K40AL	7.9 8.0 8.1 8.3	ns ns ns ns	Rising edge clock Fully loaded clock tree Rising edge DFF 20 mA output buffer 50 pf pin load

AT40K05AL	AT40K10AL	AT40K20AL	AT40K40AL	Left Side (Top to Bottom)				
128 I/O	192 I/O	256 I/O	384 I/O	84 PLCC	100 TQFP	144 LQFP	208 PQFP	240 PQFP
GND	GND	GND	GND	12	1	1	2	1
I/O1, GCK1 (A16)	I/O1, GCK1 (A16)	I/O1, GCK1 (A16)	I/O1, GCK1 (A16)	13	2	2	4	2
I/O2 (A17)	I/O2 (A17)	I/O2 (A17)	I/O2 (A17)	14	3	3	5	3
I/O3	I/O3	I/O3	I/O3			4	6	4
I/O4	I/O4	I/O4	I/O4			5	7	5
I/O5 (A18)	I/O5 (A18)	I/O5 (A18)	I/O5 (A18)	15	4	6	8	6
I/O6 (A19)	I/O6 (A19)	I/O6 (A19)	I/O6 (A19)	16	5	7	9	7
			GND					
			I/O7					
			I/O8					
			I/O9					
			I/O10					
		I/O7	I/O11					
		I/O8	I/O12					
		VCC	VCC					
		GND	GND					
			I/O13					
			I/O14					
I/O7	I/O7	I/O9	I/O15				10	8
I/O8	I/O8	I/O10	I/O16				11	9
	I/O9	I/O11	I/O17				12	10
	I/O10	I/O12	I/O18				13	11
			GND					
			I/O19					
			I/O20					
	I/O11	I/O13	I/O21					12
	I/O12	I/O14	I/O22					13
		I/O15	I/O23					
		I/O16	I/O24					
GND	GND	GND	GND			8	14	14

Note: 1. On-chip tri-state

AT40K05AL	AT40K10AL	AT40K20AL	AT40K40AL	Left Side (Top to Bottom)				
128 I/O	192 I/O	256 I/O	384 I/O	84 PLCC	100 TQFP	144 LQFP	208 PQFP	240 PQFP
I/O9, FCK1	I/O13, FCK1	I/O17, FCK1	I/O25, FCK1			9	15	15
I/O10	I/O14	I/O18	I/O26			10	16	16
I/O11 (A20)	I/O15 (A20)	I/O19 (A20)	I/O27 (A20)	17	6	11	17	17
I/O12 (A21)	I/O16 (A21)	I/O20 (A21)	I/O28 (A21)	18	7	12	18	18
	VCC	VCC	VCC					19
	I/O17	I/O21	I/O29					20
	I/O18	I/O22	I/O30					21
			GND					
			I/O31					
			I/O32					
			I/O33					
			I/O34					
		I/O23	I/O35					
		I/O24	I/O36					
		GND	GND					22
			VCC					
			I/O37					
			I/O38					
		I/O25	I/O39					
		I/O26	I/O40					
	I/O19	I/O27	I/O41				19	23
	I/O20	I/O28	I/O42				20	24
			GND					
I/O13	I/O21	I/O29	I/O43			13	21	25
I/O14	I/O22	I/O30	I/O44		8	14	22	26
			I/O45					
			I/O46					
I/O15 (A22)	I/O23 (A22)	I/O31 (A22)	I/O47 (A22)	19	9	15	23	27
I/O16 (A23)	I/O24 (A23)	I/O32 (A23)	I/O48 (A23)	20	10	16	24	28
GND	GND	GND	GND	21	11	17	25	29
VCC	VCC	VCC	VCC	22	12	18	26	30

Note: 1. On-chip tri-state

AT40K05AL	AT40K10AL	AT40K20AL	AT40K40AL	Left Side (Top to Bottom)				
128 I/O	192 I/O	256 I/O	384 I/O	84 PLCC	100 TQFP	144 LQFP	208 PQFP	240 PQFP
I/O17	I/O25	I/O33	I/O49	23	13	19	27	31
I/O18	I/O26	I/O34	I/O50	24	14	20	28	32
			I/O51					
			I/O52					
I/O19	I/O27	I/O35	I/O53		15	21	29	33
I/O20	I/O28	I/O36	I/O54			22	30	34
			GND					
	I/O29	I/O37	I/O55				31	35
	I/O30	I/O38	I/O56				32	36
		I/O39	I/O57					
		I/O40	I/O58					
			I/O59					
			I/O60					
			VCC					
		GND	GND					37
		I/O41	I/O61					
		I/O42	I/O62					
			I/O63					
			I/O64					
			I/O65					
			I/O66					
			GND					
	I/O31	I/O43	I/O67					38
	I/O32	I/O44	I/O68					39
	VCC	VCC	VCC					40
I/O21	I/O33	I/O45	I/O69	25	16	23	33	41
I/O22	I/O34	I/O46	I/O70	26	17	24	34	42
I/O23	I/O35	I/O47	I/O71			25	35	43
I/O24, FCK2	I/O36, FCK2	I/O48, FCK2	I/O72, FCK2			26	36	44
GND	GND	GND	GND			27	37	45
		I/O49	I/O73					
		I/O50	I/O74					
	I/O37	I/O51	I/O75					46

Note: 1. On-chip tri-state

AT40K05AL	AT40K10AL	AT40K20AL	AT40K40AL	Left Side (Top to Bottom)				
128 I/O	192 I/O	256 I/O	384 I/O	84 PLCC	100 TQFP	144 LQFP	208 PQFP	240 PQFP
	I/O38	I/O52	I/O76					47
			I/O77					
			I/O78					
			GND					
			I/O79					
			I/O80					
	I/O39	I/O53	I/O81				38	48
	I/O40	I/O54	I/O82				39	49
I/O25	I/O41	I/O55	I/O83				40	50
I/O26	I/O42	I/O56	I/O84				41	51
		GND	GND					
		VCC	VCC					
		I/O57	I/O85					
		I/O58	I/O86					
			I/O87					
			I/O88					
I/O27	I/O43	I/O59	I/O89	27	18	28	42	52
I/O28	I/O44	I/O60	I/O90		19	29	43	53
			GND					
			I/O91					
			I/O92					
I/O29	I/O45	I/O61	I/O93			30	44	54
I/O30	I/O46	I/O62	I/O94			31	45	55
I/O31 ($\overline{OTS}$)[1]	I/O47 ($\overline{OTS}$)[1]	I/O63 ($\overline{OTS}$)[1]	I/O95 ($\overline{OTS}$)[1]	28	20	32	46	56
I/O32, GCK2	I/O48, GCK2	I/O64, GCK2	I/O96, GCK2	29	21	33	47	57
M1	M1	M1	M1	30	22	34	48	58
GND	GND	GND	GND	31	23	35	49	59
M0	M0	M0	M0	32	24	36	50	60

Note: 1. On-chip tri-state

AT40K05AL	AT40K10AL	AT40K20AL	AT40K40AL	Bottom Side (Left to Right)				
128 I/O	192 I/O	256 I/O	384 I/O	84 PLCC	100 TQFP	144 LQFP	208 PQFP	240 PQFP
I/O42	I/O62	I/O82	I/O122			47	69	77
I/O43	I/O63	I/O83	I/O123	38	31	48	70	78
I/O44	I/O64	I/O84	I/O124	39	32	49	71	79
	VCC	VCC	VCC					80
	I/O65	I/O85	I/O125				72	81
	I/O66	I/O86	I/O126				73	82
			GND					
			I/O127					
			I/O128					
			I/O129					
			I/O130					
		I/O87	I/O131					
		I/O88	I/O132					
		GND	GND					83
			VCC					
		I/O89	I/O133					
		I/O90	I/O134					
	I/O67	I/O91	I/O135					84
	I/O68	I/O92	I/O136					85
I/O45	I/O69	I/O93	I/O137		33	50	74	86
I/O46	I/O70	I/O94	I/O138		34	51	75	87
			GND					
			I/O139					
			I/O140					
			I/O141					
			I/O142					
I/O47 (D15)	I/O71 (D15)	I/O95 (D15)	I/O143 (D15)	40	35	52	76	88
I/O48 (INIT)	I/O72 (INIT)	I/O96 (INIT)	I/O144 (INIT)	41	36	53	77	89
VCC	VCC	VCC	VCC	42	37	54	78	90
GND	GND	GND	GND	43	38	55	79	91
I/O49 (D14)	I/O73 (D14)	I/O97 (D14)	I/O145 (D14)	44	39	56	80	92
I/O50 (D13)	I/O74 (D13)	I/O98 (D13)	I/O146 (D13)	45	40	57	81	93

AT40K05AL	AT40K10AL	AT40K20AL	AT40K40AL	Right Side (Bottom to Top)				
128 I/O	192 I/O	256 I/O	384 I/O	84 PLCC	100 TQFP	144 LQFP	208 PQFP	240 PQFP
I/O73, FCK3	I/O111, FCK3	I/O147, FCK3	I/O219, FCK3			82	120	138
I/O74	I/O112	I/O148	I/O220			83	121	139
	VCC	VCC	VCC					140
I/O75 (D5)	I/O113 (D5)	I/O149 (D5)	I/O221 (D5)	59	57	84	122	141
I/O76 (CS0)	I/O114 (CS0)	I/O150 (CS0)	I/O222 (CS0)	60	58	85	123	142
			GND					
			I/O223					
			I/O224					
			I/O225					
			I/O226					
		I/O151	I/O227					
		I/O152	I/O228					
		GND	GND					143
			VCC					
			I/O229					
			I/O230					
		I/O153	I/O231					
		I/O154	I/O232					
	I/O115	I/O155	I/O233				124	144
	I/O116	I/O156	I/O234				125	145
			GND					
I/O77	I/O117	I/O157	I/O235		59	86	126	146
I/O78	I/O118	I/O158	I/O236		60	87	127	147
			I/O237					
			I/O238					
I/O79(D4)	I/O119(D4)	I/O159(D4)	I/O239(D4)	61	61	88	128	148
I/O80	I/O120	I/O160	I/O240	62	62	89	129	149
VCC	VCC	VCC	VCC	63	63	90	130	150
GND	GND	GND	GND	64	64	91	131	151
I/O81 (D3)	I/O121 (D3)	I/O161 (D3)	I/O241 (D3)	65	65	92	132	152
I/O82 ($\overline{\text{CHECK}}$)	I/O122 ($\overline{\text{CHECK}}$)	I/O162 ($\overline{\text{CHECK}}$)	I/O242 ($\overline{\text{CHECK}}$)	66	66	93	133	153

AT40K05AL	AT40K10AL	AT40K20AL	AT40K40AL	Right Side (Bottom to Top)				
128 I/O	192 I/O	256 I/O	384 I/O	84 PLCC	100 TQFP	144 LQFP	208 PQFP	240 PQFP
			I/O243					
			I/O244					
I/O83	I/O123	I/O163	I/O245		67	94	134	154
I/O84	I/O124	I/O164	I/O246			95	135	155
			GND					
	I/O125	I/O165	I/O247				136	156
	I/O126	I/O166	I/O248				137	157
		I/O167	I/O249					
		I/O168	I/O250					
			I/O251					
			I/O252					
			VCC					
		GND	GND					158
		I/O169	I/O253					
		I/O170	I/O254					
			I/O255					
			I/O256					
			I/O257					
			I/O258					
			GND					
I/O85 (D2)	I/O127 (D2)	I/O171 (D2)	I/O259 (D2)	67	68	96	138	159
I/O86	I/O128	I/O172	I/O260	68	69	97	139	160
	VCC	VCC	VCC					161
I/O87	I/O129	I/O173	I/O261			98	140	162
I/O88, FCK4	I/O130, FCK4	I/O174, FCK4	I/O262, FCK4			99	141	163
	I/O131	I/O175	I/O263					164
	I/O132	I/O176	I/O264					165
GND	GND	GND	GND			100	142	166
		I/O177	I/O265					
		I/O178	I/O266					
	I/O133	I/O179	I/O267					167
	I/O134	I/O180	I/O268					168
			I/O269					

AT40K05AL	AT40K10AL	AT40K20AL	AT40K40AL	Top Side (Right to Left)				
128 I/O	192 I/O	256 I/O	384 I/O	84 PLCC	100 TQFP	144 LQFP	208 PQFP	240 PQFP
		I/O242	I/O362					
	I/O181	I/O243	I/O363				195	228
	I/O182	I/O244	I/O364				196	229
			I/O365					
			I/O366					
			GND					
			I/O367					
			I/O368					
I/O121	I/O183	I/O245	I/O369				197	230
I/O122	I/O184	I/O246	I/O370				198	231
I/O123 (A12)	I/O185 (A12)	I/O247 (A12)	I/O371 (A12)	7	96	138	199	232
I/O124 (A13)	I/O186 (A13)	I/O248 (A13)	I/O372 (A13)	8	97	139	200	233
		GND	GND					
		VCC	VCC					
		I/O249	I/O373					
		I/O250	I/O374					
			I/O375					
			I/O376					
			I/O377					
			I/O378					
			GND					
	I/O187	I/O251	I/O379					234
	I/O188	I/O252	I/O380					235
I/O125	I/O189	I/O253	I/O381			140	201	236
I/O126	I/O190	I/O254	I/O382			141	202	237
I/O127 (A14)	I/O191 (A14)	I/O255 (A14)	I/O383 (A14)	9	98	142	203	238
I/O128, GCK8 (A15)	I/O192, GCK8 (A15)	I/O256, GCK8 (A15)	I/O384, GCK8 (A15)	10	99	143	204	239
VCC	VCC	VCC	VCC	11	100	144	205	240

Note: 1. Shared with TSTCLK. No Connect.

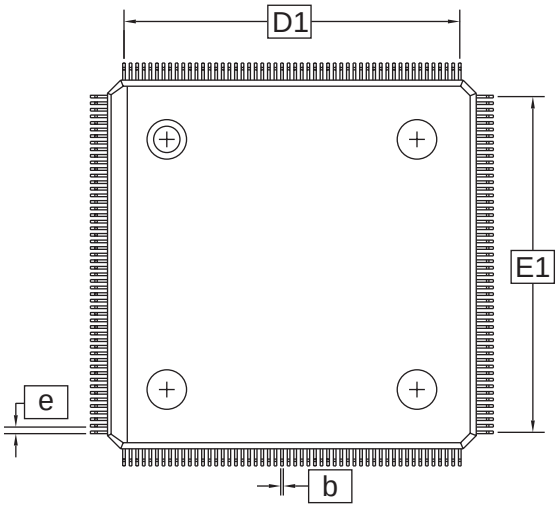
Part/Package Availability and User I/O Counts (including Dual-function Pins)

Package[1]	AT40K05AL	AT40K10AL	AT40K20AL	AT40K40AL
84 PLCC	62	62	–	62
100 TQFP	78	78	78	–
144 LQFP	114	114	114	114
208 PQFP	128	161	161	161
240 PQFP	–	–	–	193

Note: 1. Devices in same package are pin-to-pin compatible.

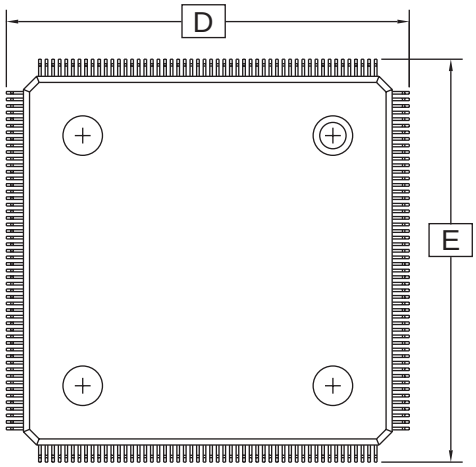
Package Type	
84J	84-lead, Plastic J-leaded Chip Carrier (PLCC)
100T1	100-lead, Thin (1.0 mm) Plastic Quad Flat Package (TQFP)
144L1	144-lead, Low-profile (1.4 mm) Plastic Quad Flat Package (LQFP)
208Q1	208-lead, Plastic Quad Flat Package (PQFP)
240Q1	240-lead, Plastic Quad Flat Package (PQFP)

208Q1 – PQFP



Top View

Side View



Bottom View

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A1	0.25	–	0.50	
A2	3.20	3.40	3.60	
D		30.60 BSC		
D1		28.00 BSC		2, 3
E		30.60 BSC		
E1		28.00 BSC		2, 3
e		0.50 BSC		
b	0.17	–	0.27	4
L1		1.30 REF		

Notes:
1. This drawing is for general information only; refer to JEDEC Drawing MS-129, Variation FA-1, for proper dimensions, tolerances, datums, etc.
2. The top package body size may be smaller than the bottom package size by as much as 0.15 mm.
3. Dimensions D1 and E1 do not include mold protrusions. Allowable protrusion is 0.25 mm per side. D1 and E1 are maximum plastic body size dimensions including mold mismatch.
4. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall not cause the lead width to exceed the maximum b dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm.

07/23/02

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**208Q1**, 208-lead (28 x 28 mm Body, 2.6 Form Opt.), Plastic Quad Flat Pack (PQFP)	208Q1	B

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