Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	2304
Total RAM Bits	18432
Number of I/O	114
Number of Gates	50000
Voltage - Supply	3V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at40k40al-1bqc

Table 1. AT40KAL Family[1]

Device	AT40K05AL	AT40K10AL	AT40K20AL	AT40K40AL
Usable Gates	5K - 10K	10K - 20K	20K - 30K	40K - 50K
Rows x Columns	16 x 16	24 x 24	32 x 32	48 x 48
Cells	256	576	1,024	2,304
Registers	496[1]	954[1]	1,520[1]	3,048[1]
RAM Bits	2,048	4,608	8,192	18,432
I/O (Maximum)	128	192	256	384

Note: 1. Packages with FCK will have 8 less registers.

Description

The AT40KAL is a family of fully PCI-compliant, SRAM-based FPGAs with distributed 10 ns programmable synchronous/asynchronous, dual-port/single-port SRAM, 8 global clocks, Cache Logic ability (partially or fully reconfigurable without loss of data), automatic component generators, and range in size from 5,000 to 50,000 usable gates. I/O counts range from 128 to 384 in industry standard packages ranging from 84-pin PLCC to 352-ball Square BGA, and support 3.3V designs.

The AT40KAL is designed to quickly implement high-performance, large gate count designs through the use of synthesis and schematic-based tools used on a PC or Sun platform. Atmel's design tools provide seamless integration with industry standard tools such as Synplicity, ModelSim, Exemplar and Viewlogic. See the "IDS Datasheet" available on the Atmel web site (http://www.atmel.com/atmel/acrobat/doc1421.pdf) for a list of other supported tools.

The AT40KAL can be used as a coprocessor for high-speed (DSP/processor-based) designs by implementing a variety of computation intensive, arithmetic functions. These include adaptive finite impulse response (FIR) filters, fast Fourier transforms (FFT), convolvers, interpolators and discrete-cosine transforms (DCT) that are required for video compression and decompression, encryption, convolution and other multimedia applications.

Fast, Flexible and Efficient SRAM

The AT40KAL FPGA offers a patented distributed 10 ns SRAM capability where the RAM can be used without losing logic resources. Multiple independent, synchronous or asynchronous, dual-port or single-port RAM functions (FIFO, scratch pad, etc.) can be created using Atmel's macro generator tool.

Fast, Efficient Array and Vector Multipliers

The AT40KAL's patented 8-sided core cell with direct horizontal, vertical and diagonal cell-to-cell connections implements ultra fast array multipliers without using any busing resources. The AT40KAL's Cache Logic capability enables a large number of design coefficients and variables to be implemented in a very small amount of silicon, enabling vast improvement in system speed at much lower cost than conventional FPGAs.

Cache Logic Design

The AT40KAL, AT6000 and FPSLIC families are capable of implementing Cache Logic (dynamic full/partial logic reconfiguration, without loss of data, on-the-fly) for building adaptive logic and systems. As new logic functions are required, they can be loaded into the logic cache without losing the data already there or disrupting the operation of the rest of the chip; replacing or complementing the active logic. The AT40KAL can act as a reconfigurable coprocessor.

Automatic Component Generators

The AT40KAL FPGA family is capable of implementing user-defined, automatically generated, macros in multiple designs; speed and functionality are unaffected by the macro orientation or density of the target device. This enables the fastest, most predictable and efficient FPGA design approach and minimizes design risk by reusing already proven functions. The Automatic Component Generators work seamlessly with industry standard schematic and synthesis tools to create the fastest, most efficient designs available.

The patented AT40KAL series architecture employs a symmetrical grid of small yet powerful cells connected to a flexible busing network. Independently controlled clocks and resets govern every column of cells. The array is surrounded by programmable I/O.

Devices range in size from 5,000 to 50,000 usable gates in the family, and have 256 to 3,048 registers. Pin locations are consistent throughout the AT40KAL series for easy design migration in the same package footprint. The AT40KAL series FPGAs utilize a reliable 0.35µ triple-metal, CMOS process and are 100% factory-tested. Atmel's PC- and workstation-based integrated development system (IDS) is used to create AT40KAL series designs. Multiple design entry methods are supported.

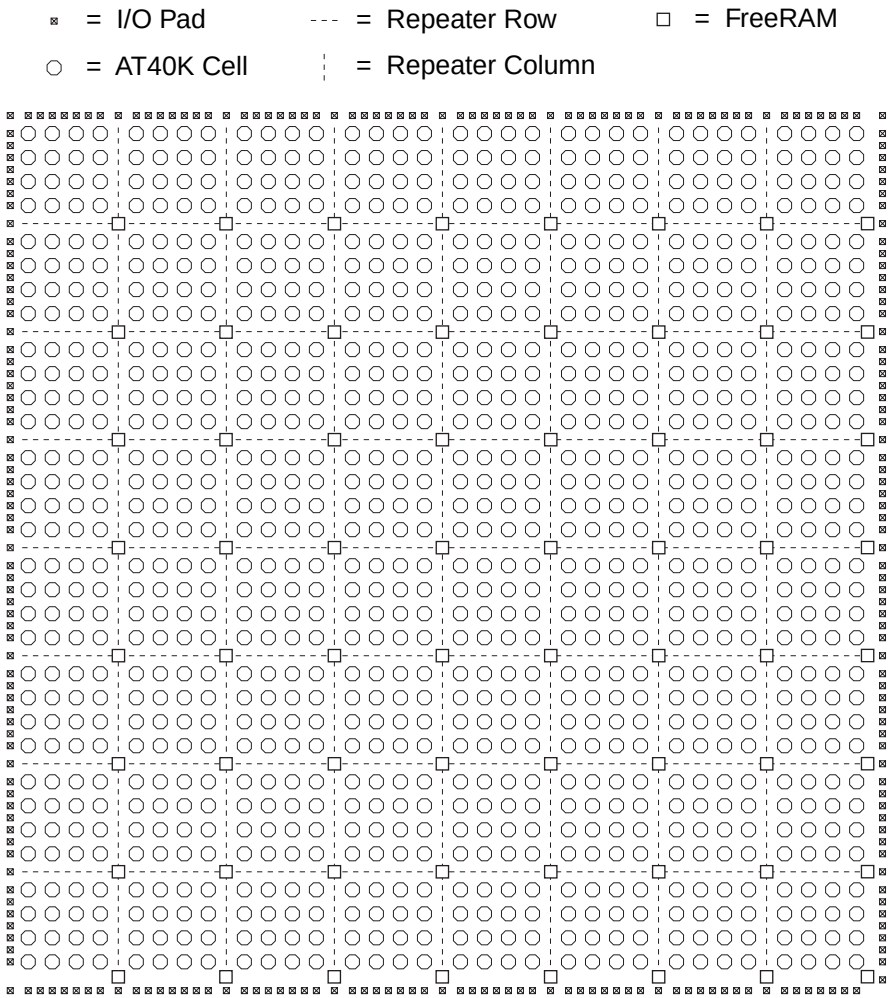
The Atmel architecture was developed to provide the highest levels of performance, functional density and design flexibility in an FPGA. The cells in the Atmel array are small, efficient and can implement any pair of Boolean functions of (the same) three inputs or any single Boolean function of four inputs. The cell's small size leads to arrays with large numbers of cells, greatly multiplying the functionality in each cell. A simple, high-speed busing network provides fast, efficient communication over medium and long distances.

The Symmetrical Array

At the heart of the Atmel architecture is a symmetrical array of identical cells, see Figure 1. The array is continuous from one edge to the other, except for bus repeaters spaced every four cells, see Figure 2 on page 5. At the intersection of each repeater row and column there is a 32 x 4 RAM block accessible by adjacent buses. The RAM can be configured as either a single-ported or dual-ported RAM(1), with either synchronous or asynchronous operation.

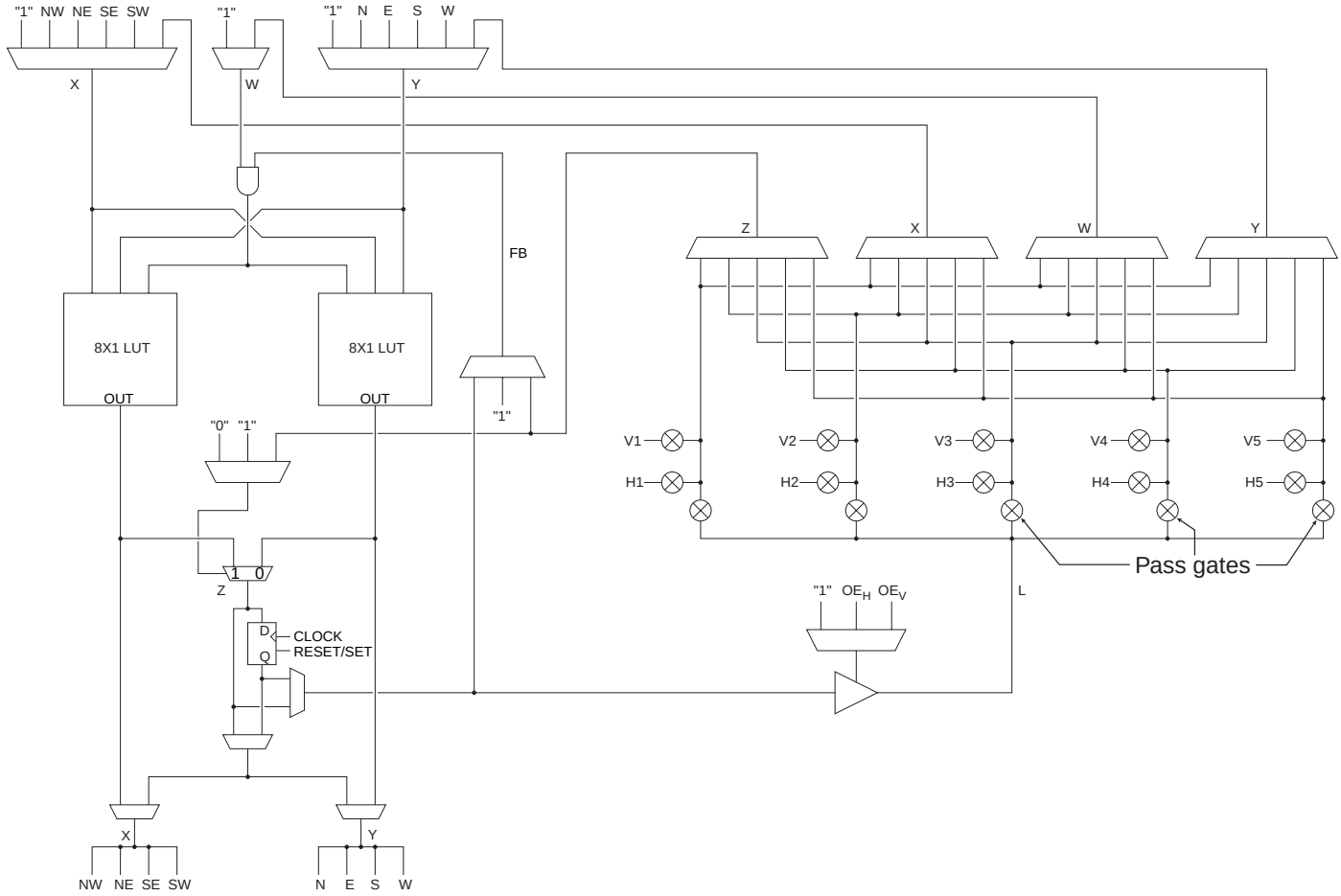
Note: 1. The right-most column can only be used as single-port RAM.

Figure 1. Symmetrical Array Surrounded by I/O (AT40K20AL)(1)



Note: 1. AT40KAL has registered I/Os. Group enable on every sector for tri-states on obufe's.

Figure 5. The Cell



X = Diagonal Direct Connect or Bus
Y = Orthogonal Direct Connect or Bus
W = Bus Connection
Z = Bus Connection
FB = Internal Feedback

Set/Reset Scheme

The AT40KAL family reset scheme is essentially the same as the clock scheme except that there is only one Global Reset. A dedicated Global Set/Reset bus can be driven by any User I/O, except those used for clocking (Global Clocks or Fast Clocks). The automatic placement tool will choose the reset net with the most connections to use the global resources. You can change this by using an RSBUF component in your design to indicate the global reset. Additional resets will use the express bus network.

The Global Set/Reset is distributed to each column of the array. Like Sector Clock mux, there is Sector Set/Reset mux at every four cells. Each sector column of four cells is set/reset by a Plane 5 express bus or Global Set/Reset using the Sector Set/Reset mux, see Figure 11 on page 17. The set/reset provided to each sector column of four cells is either inverted or non-inverted using the Sector Reset mux.

The function of the Set/Reset input of a register is determined by a configuration bit in each cell. The Set/Reset input of a register is active low (logic 0) by default. Setting or Resetting of a register is asynchronous. Before configuration on power-up, a logic 1 (a high) is provided by each register (i.e., all registers are set at power-up).

Primary, Secondary and Corner I/Os

The AT40KAL has three kinds of I/Os: Primary I/O, Secondary I/O and a Corner I/O. Every edge cell except corner cells on the AT40KAL has access to one Primary I/O and two Secondary I/Os.

Primary I/O

Every logic cell at the edge of the FPGA array has a direct orthogonal connection to and from a Primary I/O cell. The Primary I/O interfaces directly to its adjacent core cell. It also connects into the repeaters on the row immediately above and below the adjacent core cell. In addition, each Primary I/O also connects into the busing network of the three nearest edge cells. This is an extremely powerful feature, as it provides logic cells toward the center of the array with fast access to I/Os via local and express buses. It can be seen from the diagram that a given Primary I/O can be accessed from any logic cell on three separate rows or columns of the FPGA. See Figure 12 on page 20.

Secondary I/O

Every logic cell at the edge of the FPGA array has two direct diagonal connections to a Secondary I/O cell. The Secondary I/O is located between core cell locations. This I/O connects on the diagonal inputs to the cell above and the cell below. It also connects to the repeater of the cell above and below. In addition, each Secondary I/O also connects into the busing network of the two nearest edge cells. This is an extremely powerful feature, as it provides logic cells toward the center of the array with fast access to I/Os via local and express buses. It can be seen from the diagram that a given Secondary I/O can be accessed from any logic cell on two rows or columns of the FPGA. See Figure 13 on page 20.

Corner I/O

Logic cells at the corner of the FPGA array have direct-connect access to five separate I/Os: 2 Primary, 2 Secondary and 1 Corner I/O. Corner I/Os are like an extra Secondary I/O at each corner of the array. With the inclusion of Corner I/Os, an AT40KAL FPGA with n x n core cells always has 8n I/Os. As the diagram shows, Corner I/Os can be accessed both from the corner logic cell and the horizontal and vertical busing networks running along the edges of the array. This means that many different edge logic cells can access the Corner I/Os. See Figure 14 on page 21.

Figure 12. West Primary I/O (Mirrored for East I/O)

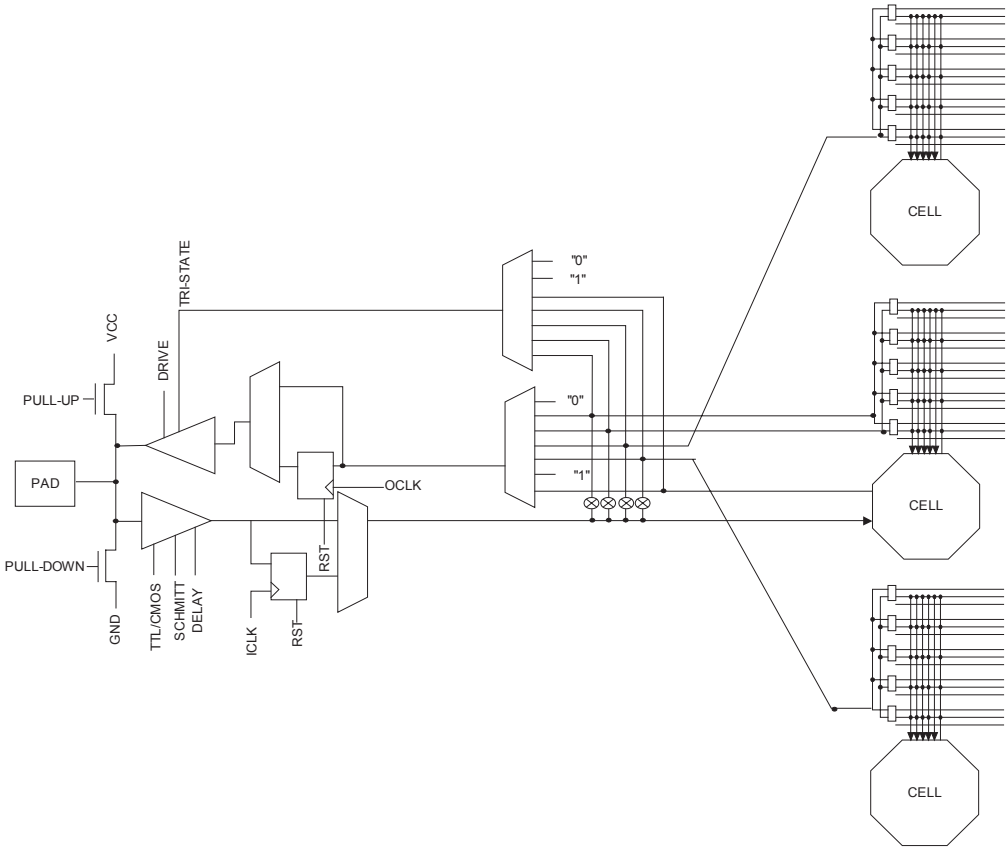
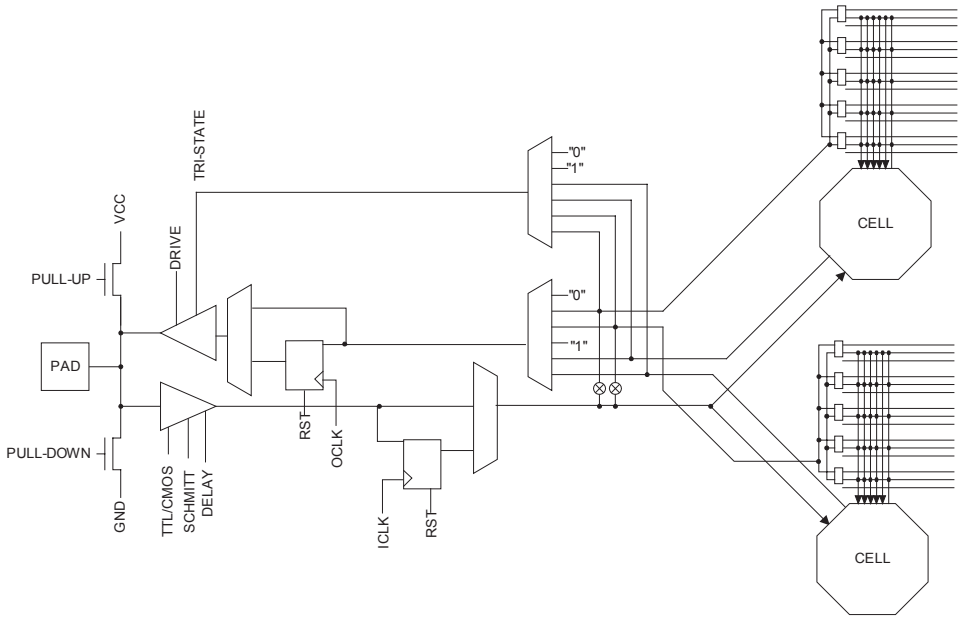


Figure 13. West Secondary I/O (Mirrored for East I/O)



AC Timing Characteristics – 3.3V Operation

Delays are based on fixed loads and are described in the notes.
Maximum times based on worst case: V_{CC} = 3.00V, temperature = 70°C
Minimum times based on best case: V_{CC} = 3.60V, temperature = 0°C
Maximum delays are the average of t_{PDLH} and t_{PDHL}.

Cell Function	Parameter	Path	-1	Units	Notes
Core					
2-input Gate	t_{PD} (Maximum)	x/y -> x/y	1.8	ns	1 unit load
3-input Gate	t_{PD} (Maximum)	x/y/z -> x/y	2.1	ns	1 unit load
3-input Gate	t_{PD} (Maximum)	x/y/w -> x/y	2.2	ns	1 unit load
4-input Gate	t_{PD} (Maximum)	x/y/w/z -> x/y	2.2	ns	1 unit load
Fast Carry	t_{PD} (Maximum)	y -> y	1.4	ns	1 unit load
Fast Carry	t_{PD} (Maximum)	x -> y	1.7	ns	1 unit load
Fast Carry	t_{PD} (Maximum)	y -> x	1.8	ns	1 unit load
Fast Carry	t_{PD} (Maximum)	x -> x	1.5	ns	1 unit load
Fast Carry	t_{PD} (Maximum)	w -> y	2.2	ns	1 unit load
Fast Carry	t_{PD} (Maximum)	w -> x	2.3	ns	1 unit load
Fast Carry	t_{PD} (Maximum)	z -> y	2.3	ns	1 unit load
Fast Carry	t_{PD} (Maximum)	z -> x	1.7	ns	1 unit load
DFF	t_{PD} (Maximum)	q -> x/y	1.8	ns	1 unit load
DFF	t_{PD} (Maximum)	R -> x/y	2.2	ns	1 unit load
DFF	t_{PD} (Maximum)	S -> x/y	2.2	ns	1 unit load
DFF	t_{PD} (Maximum)	q -> w	1.8	ns	
Incremental -> L	t_{PD} (Maximum)	x/y -> L	1.5	ns	1 unit load
Local Output Enable	t_{PZX} (Maximum)	oe -> L	1.4	ns	1 unit load
Local Output Enable	t_{PXZ} (Maximum)	oe -> L	1.8	ns	

AC Timing Characteristics – 3.3V Operation

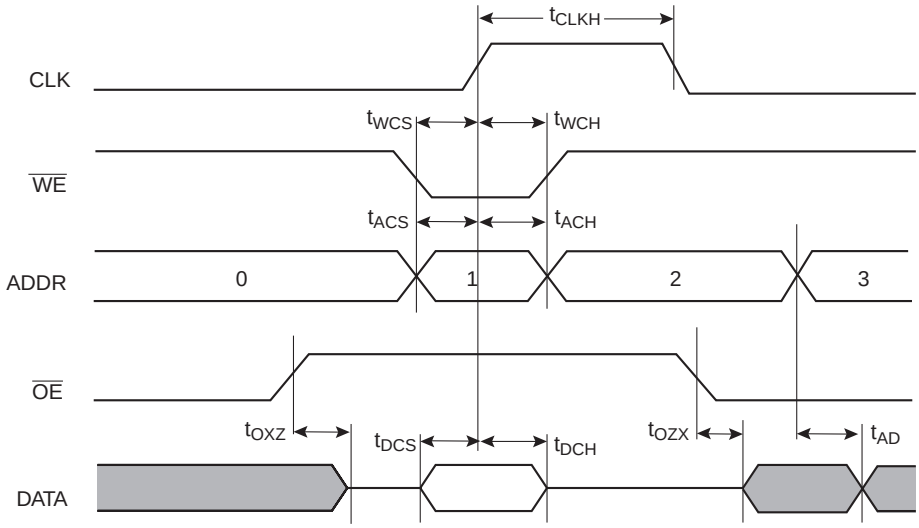
Delays are based on fixed loads and are described in the notes.
Maximum times based on worst case: V_{CC} = 3.0V, temperature = 70°C
Minimum times based on best case: V_{CC} = 3.6V, temperature = 0°C

Cell Function	Parameter	Path	-1	Units	Notes
Async RAM					
Write	t_{WECYC} (Minimum)	cycle time	12.0	ns	
Write	t_{WEL} (Minimum)	we	5.0	ns	Pulse width low
Write	t_{WEH} (Minimum)	we	5.0	ns	Pulse width high
Write	t_{AWS} (Minimum)	wr addr setup -> we	5.3	ns	
Write	t_{AWH} (Minimum)	wr addr hold -> we	0.0	ns	
Write	t_{DS} (Minimum)	din setup -> we	5.0	ns	
Write	t_{DH} (Minimum)	din hold -> we	0.0	ns	
Write/Read	t_{DD} (Maximum)	din -> dout	8.7	ns	rd addr = wr addr
Read	t_{AD} (Maximum)	rd addr -> dout	6.3	ns	
Read	t_{OZX} (Maximum)	oe -> dout	2.9	ns	
Read	t_{OXZ} (Maximum)	oe -> dout	3.5	ns	
Sync RAM					
Write	t_{CYC} (Minimum)	cycle time	12.0	ns	
Write	t_{CLKL} (Minimum)	clk	5.0	ns	Pulse width low
Write	t_{CLKH} (Minimum)	clk	5.0	ns	Pulse width high
Write	t_{WCS} (Minimum)	we setup -> clk	3.2	ns	
Write	t_{WCH} (Minimum)	we hold -> clk	0.0	ns	
Write	t_{ACS} (Minimum)	wr addr setup -> clk	5.0	ns	
Write	t_{ACH} (Minimum)	wr addr hold -> clk	0.0	ns	
Write	t_{DCS} (Minimum)	wr data setup -> clk	3.9	ns	
Write	t_{DCH} (Minimum)	wr data hold -> clk	0.0	ns	
Write/Read	t_{CD} (Maximum)	clk -> dout	5.8	ns	rd addr = wr addr
Read	t_{AD} (Maximum)	rd addr -> dout	6.3	ns	
Read	t_{OZX} (Maximum)	oe -> dout	2.9	ns	
Read	t_{OXZ} (Maximum)	oe -> dout	3.5	ns	

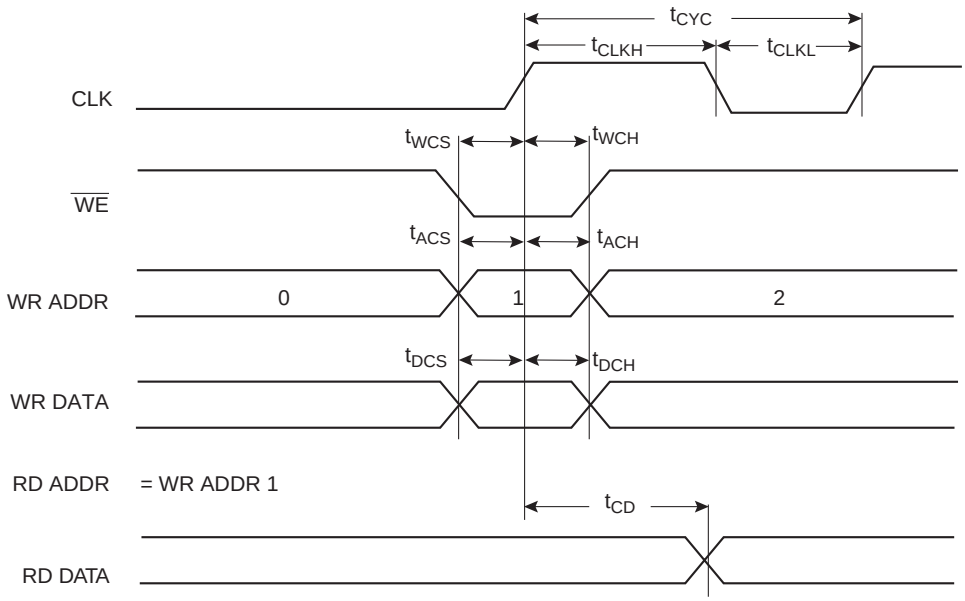
Notes:
1. CMOS buffer delays are measured from a V_{IH} of 1/2 V_{CC} at the pad to the internal V_{IH} at A. The input buffer load is constant.
2. Buffer delay is to a pad voltage of 1.5V with one output switching.
3. Parameter based on characterization and simulation; not tested in production.
4. Exact power calculation is available in Atmel FPGA Designer software.

FreeRAM Synchronous Timing Characteristics

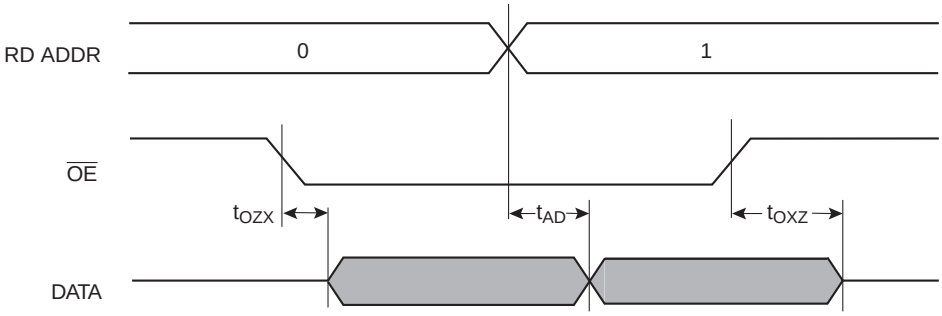
Single-port Write/Read



Dual-port Write with Read



Dual-port Read



AT40K05AL	AT40K10AL	AT40K20AL	AT40K40AL	Left Side (Top to Bottom)				
128 I/O	192 I/O	256 I/O	384 I/O	84 PLCC	100 TQFP	144 LQFP	208 PQFP	240 PQFP
I/O17	I/O25	I/O33	I/O49	23	13	19	27	31
I/O18	I/O26	I/O34	I/O50	24	14	20	28	32
			I/O51					
			I/O52					
I/O19	I/O27	I/O35	I/O53		15	21	29	33
I/O20	I/O28	I/O36	I/O54			22	30	34
			GND					
	I/O29	I/O37	I/O55				31	35
	I/O30	I/O38	I/O56				32	36
		I/O39	I/O57					
		I/O40	I/O58					
			I/O59					
			I/O60					
			VCC					
		GND	GND					37
		I/O41	I/O61					
		I/O42	I/O62					
			I/O63					
			I/O64					
			I/O65					
			I/O66					
			GND					
	I/O31	I/O43	I/O67					38
	I/O32	I/O44	I/O68					39
	VCC	VCC	VCC					40
I/O21	I/O33	I/O45	I/O69	25	16	23	33	41
I/O22	I/O34	I/O46	I/O70	26	17	24	34	42
I/O23	I/O35	I/O47	I/O71			25	35	43
I/O24, FCK2	I/O36, FCK2	I/O48, FCK2	I/O72, FCK2			26	36	44
GND	GND	GND	GND			27	37	45
		I/O49	I/O73					
		I/O50	I/O74					
	I/O37	I/O51	I/O75					46

Note: 1. On-chip tri-state

AT40K05AL	AT40K10AL	AT40K20AL	AT40K40AL	Left Side (Top to Bottom)				
128 I/O	192 I/O	256 I/O	384 I/O	84 PLCC	100 TQFP	144 LQFP	208 PQFP	240 PQFP
	I/O38	I/O52	I/O76					47
			I/O77					
			I/O78					
			GND					
			I/O79					
			I/O80					
	I/O39	I/O53	I/O81				38	48
	I/O40	I/O54	I/O82				39	49
I/O25	I/O41	I/O55	I/O83				40	50
I/O26	I/O42	I/O56	I/O84				41	51
		GND	GND					
		VCC	VCC					
		I/O57	I/O85					
		I/O58	I/O86					
			I/O87					
			I/O88					
I/O27	I/O43	I/O59	I/O89	27	18	28	42	52
I/O28	I/O44	I/O60	I/O90		19	29	43	53
			GND					
			I/O91					
			I/O92					
I/O29	I/O45	I/O61	I/O93			30	44	54
I/O30	I/O46	I/O62	I/O94			31	45	55
I/O31 ($\overline{OTS}$)[1]	I/O47 ($\overline{OTS}$)[1]	I/O63 ($\overline{OTS}$)[1]	I/O95 ($\overline{OTS}$)[1]	28	20	32	46	56
I/O32, GCK2	I/O48, GCK2	I/O64, GCK2	I/O96, GCK2	29	21	33	47	57
M1	M1	M1	M1	30	22	34	48	58
GND	GND	GND	GND	31	23	35	49	59
M0	M0	M0	M0	32	24	36	50	60

Note: 1. On-chip tri-state

AT40K05AL	AT40K10AL	AT40K20AL	AT40K40AL	Bottom Side (Left to Right)				
128 I/O	192 I/O	256 I/O	384 I/O	84 PLCC	100 TQFP	144 LQFP	208 PQFP	240 PQFP
			I/O147					
			I/O148					
			I/O149					
			I/O150					
			GND					
I/O51	I/O75	I/O99	I/O151		41	58	82	94
I/O52	I/O76	I/O100	I/O152		42	59	83	95
	I/O77	I/O101	I/O153				84	96
	I/O78	I/O102	I/O154				85	97
		I/O103	I/O155					
		I/O104	I/O156					
			VCC					
		GND	GND					98
		I/O105	I/O157					
		I/O106	I/O158					
			I/O159					
			I/O160					
			I/O161					
			I/O162					
			GND					
	I/O79	I/O107	I/O163					99
	I/O80	I/O108	I/O164					100
	VCC	VCC	VCC					101
I/O53 (D12)	I/O81 (D12)	I/O109 (D12)	I/O165 (D12)	46	43	60	86	102
I/O54 (D11)	I/O82 (D11)	I/O110 (D11)	I/O166 (D11)	47	44	61	87	103
I/O55	I/O83	I/O111	I/O167			62	88	104
I/O56	I/O84	I/O112	I/O168			63	89	105
GND	GND	GND	GND			64	90	106
		I/O113	I/O169					
		I/O114	I/O170					
	I/O85	I/O115	I/O171					107
	I/O86	I/O116	I/O172					108
			I/O173					

AT40K05AL	AT40K10AL	AT40K20AL	AT40K40AL	Right Side (Bottom to Top)				
128 I/O	192 I/O	256 I/O	384 I/O	84 PLCC	100 TQFP	144 LQFP	208 PQFP	240 PQFP
I/O73, FCK3	I/O111, FCK3	I/O147, FCK3	I/O219, FCK3			82	120	138
I/O74	I/O112	I/O148	I/O220			83	121	139
	VCC	VCC	VCC					140
I/O75 (D5)	I/O113 (D5)	I/O149 (D5)	I/O221 (D5)	59	57	84	122	141
I/O76 (CS0)	I/O114 (CS0)	I/O150 (CS0)	I/O222 (CS0)	60	58	85	123	142
			GND					
			I/O223					
			I/O224					
			I/O225					
			I/O226					
		I/O151	I/O227					
		I/O152	I/O228					
		GND	GND					143
			VCC					
			I/O229					
			I/O230					
		I/O153	I/O231					
		I/O154	I/O232					
	I/O115	I/O155	I/O233				124	144
	I/O116	I/O156	I/O234				125	145
			GND					
I/O77	I/O117	I/O157	I/O235		59	86	126	146
I/O78	I/O118	I/O158	I/O236		60	87	127	147
			I/O237					
			I/O238					
I/O79(D4)	I/O119(D4)	I/O159(D4)	I/O239(D4)	61	61	88	128	148
I/O80	I/O120	I/O160	I/O240	62	62	89	129	149
VCC	VCC	VCC	VCC	63	63	90	130	150
GND	GND	GND	GND	64	64	91	131	151
I/O81 (D3)	I/O121 (D3)	I/O161 (D3)	I/O241 (D3)	65	65	92	132	152
I/O82 ($\overline{\text{CHECK}}$)	I/O122 ($\overline{\text{CHECK}}$)	I/O162 ($\overline{\text{CHECK}}$)	I/O242 ($\overline{\text{CHECK}}$)	66	66	93	133	153

AT40K05AL	AT40K10AL	AT40K20AL	AT40K40AL	Top Side (Right to Left)				
128 I/O	192 I/O	256 I/O	384 I/O	84 PLCC	100 TQFP	144 LQFP	208 PQFP	240 PQFP
GND	GND	GND	GND	76	77	110	160	182
I/O97 (A0)	I/O145 (A0)	I/O193 (A0)	I/O289 (A0)	77	78	111	161	183
I/O98, GCK7 (A1)	I/O146, GCK7 (A1)	I/O194, GCK7 (A1)	I/O290, GCK7 (A1)	78	79	112	162	184
I/O99	I/O147	I/O195	I/O291			113	163	185
I/O100	I/O148	I/O196	I/O292			114	164	186
			I/O293					
			I/O294					
			GND					
			I/O295					
			I/O296					
I/O101 ($\overline{CS1}$,A2)	I/O149 ($\overline{CS1}$,A2)	I/O197 ($\overline{CS1}$,A2)	I/O297 ($\overline{CS1}$,A2)	79	80	115	165	187
I/O102 (A3)	I/O150 (A3)	I/O198 (A3)	I/O298 (A3)	80	81	116	166	188
		I/O199	I/O299					
		I/O200	I/O300					
		VCC	VCC					
		GND	GND					
	I/O151[1]	I/O201[1]	I/O301[1]	75[1] NC	76[1] NC	109[1] NC	159[1] NC	189[1] NC
	I/O152	I/O202	I/O302					190
I/O103	I/O153	I/O203	I/O303			117	167	191
I/O104[1]	I/O154	I/O204	I/O304				168	192
			I/O305					
			I/O306					
			GND					
			I/O307					
			I/O308					
	I/O155	I/O205	I/O309				169	193
	I/O156	I/O206	I/O310				170	194
		I/O207	I/O311					195
		I/O208	I/O312					
GND	GND	GND	GND			118	171	196

Note: 1. Shared with TSTCLK. No Connect.

AT40K05AL	AT40K10AL	AT40K20AL	AT40K40AL	Top Side (Right to Left)				
128 I/O	192 I/O	256 I/O	384 I/O	84 PLCC	100 TQFP	144 LQFP	208 PQFP	240 PQFP
		I/O242	I/O362					
	I/O181	I/O243	I/O363				195	228
	I/O182	I/O244	I/O364				196	229
			I/O365					
			I/O366					
			GND					
			I/O367					
			I/O368					
I/O121	I/O183	I/O245	I/O369				197	230
I/O122	I/O184	I/O246	I/O370				198	231
I/O123 (A12)	I/O185 (A12)	I/O247 (A12)	I/O371 (A12)	7	96	138	199	232
I/O124 (A13)	I/O186 (A13)	I/O248 (A13)	I/O372 (A13)	8	97	139	200	233
		GND	GND					
		VCC	VCC					
		I/O249	I/O373					
		I/O250	I/O374					
			I/O375					
			I/O376					
			I/O377					
			I/O378					
			GND					
	I/O187	I/O251	I/O379					234
	I/O188	I/O252	I/O380					235
I/O125	I/O189	I/O253	I/O381			140	201	236
I/O126	I/O190	I/O254	I/O382			141	202	237
I/O127 (A14)	I/O191 (A14)	I/O255 (A14)	I/O383 (A14)	9	98	142	203	238
I/O128, GCK8 (A15)	I/O192, GCK8 (A15)	I/O256, GCK8 (A15)	I/O384, GCK8 (A15)	10	99	143	204	239
VCC	VCC	VCC	VCC	11	100	144	205	240

Note: 1. Shared with TSTCLK. No Connect.

AT40K05AL Ordering Information

Usable Gates	Operating Voltage	Speed Grade (ns)	Ordering Code	Package	Operation Range[1]
5,000 - 10,000	3.3V	1	AT40K05AL-1AJC AT40K05AL-1AQC AT40K05AL-1BQC AT40K05AL-1DQC	84J 100T1 144L1 208Q1	Commercial (0°C to 70°C)
5,000 - 10,000	3.3V	1	AT40K05AL-1AJI AT40K05AL-1AQI AT40K05AL-1BQI AT40K05AL-1DQI	84J 100T1 144L1 208Q1	Industrial (-40°C to 85°C)

AT40K10AL Ordering Information

Usable Gates	Operating Voltage	Speed Grade (ns)	Ordering Code	Package	Operation Range[1]
10,000 - 20,000	3.3V	1	AT40K10AL-1AJC AT40K10AL-1AQC AT40K10AL-1BQC AT40K10AL-1DQC	84J 100T1 144L1 208Q1	Commercial (0°C to 70°C)
10,000 - 20,000	3.3V	1	AT40K10AL-1AJI AT40K10AL-1AQI AT40K10AL-1BQI AT40K10AL-1DQI	84J 100T1 144L1 208Q1	Industrial (-40°C to 85°C)

AT40K20AL Ordering Information

Usable Gates	Operating Voltage	Speed Grade (ns)	Ordering Code	Package	Operation Range[1]
20,000 - 30,000	3.3V	1	AT40K20AL-1AJC AT40K20AL-1AQC AT40K20AL-1BQC AT40K20AL-1DQC	84J 100T1 144L1 208Q1	Commercial (0°C to 70°C)
20,000 - 30,000	3.3V	1	AT40K20AL-1AJI AT40K20AL-1AQI AT40K20AL-1BQI AT40K20AL-1DQI	84J 100T1 144L1 208Q1	Industrial (-40°C to 85°C)

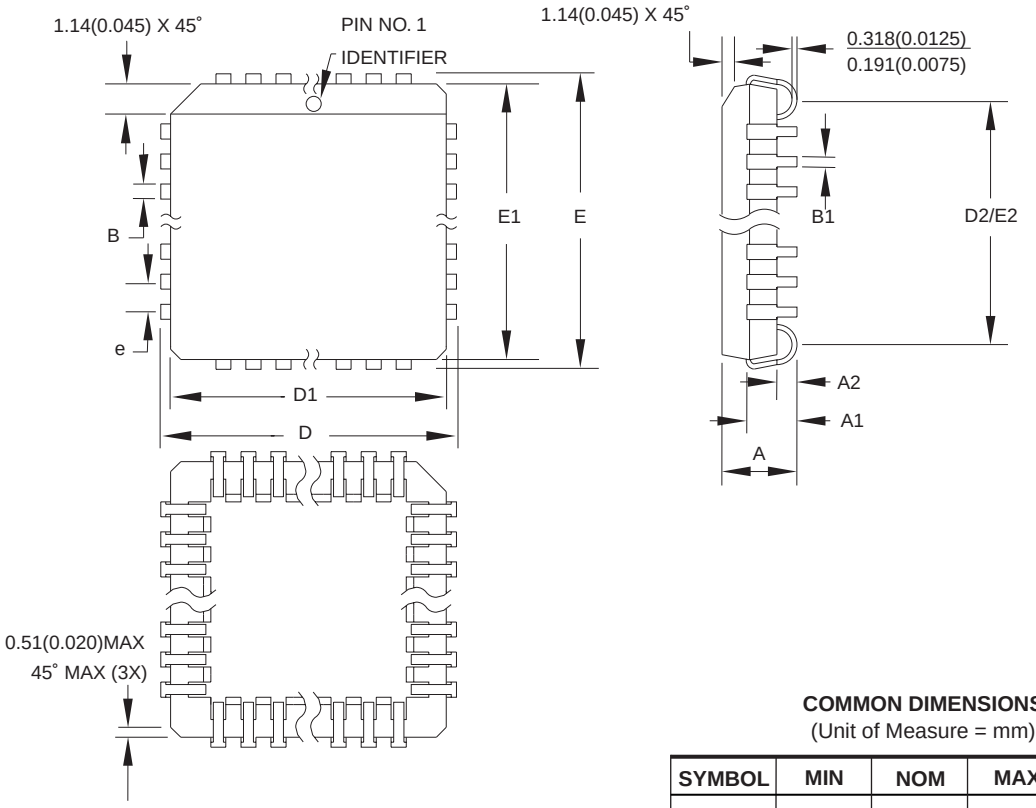
AT40K40AL Ordering Information

Usable Gates	Operating Voltage	Speed Grade (ns)	Ordering Code	Package	Operation Range[1]
40,000 - 50,000	3.3V	1	AT40K40AL-1BQC AT40K40AL-1DQC AT40K40AL-1EQC	144L1 208Q1 240Q1	Commercial (0°C to 70°C)
40,000 - 50,000	3.3V	1	AT40K40AL-1BQI AT40K40AL-1DQI AT40K40AL-1EQI	144L1 208Q1 240Q1	Industrial (-40°C to 85°C)

Note: 1. For military parts, contact Atmel at fpga@atmel.com.

Packaging Information

84J – PLCC



COMMON DIMENSIONS
(Unit of Measure = mm)

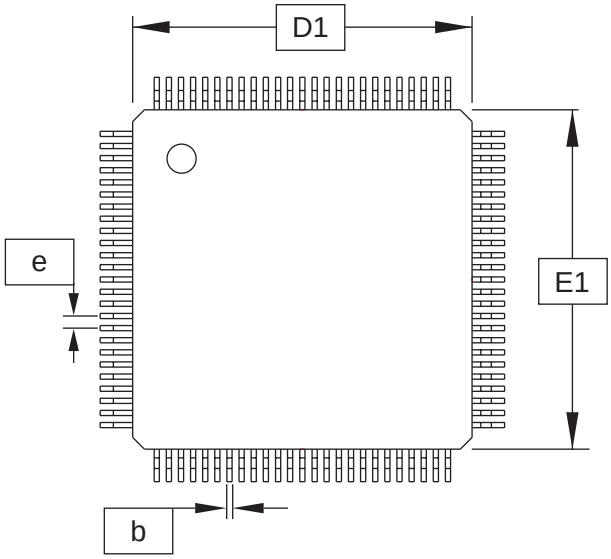
SYMBOL	MIN	NOM	MAX	NOTE
A	4.191	–	4.572	
A1	2.286	–	3.048	
A2	0.508	–	–	
D	30.099	–	30.353	
D1	29.210	–	29.413	Note 2
E	30.099	–	30.353	
E1	29.210	–	29.413	Note 2
D2/E2	27.686	–	28.702	
B	0.660	–	0.813	
B1	0.330	–	0.533	
e	1.270 TYP			

Notes:
1. This package conforms to JEDEC reference MS-018, Variation AF.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010"(0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
3. Lead coplanarity is 0.004" (0.102 mm) maximum.

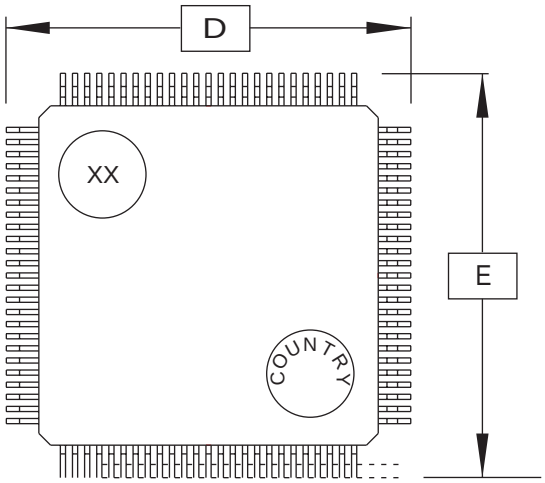
10/04/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**84J**, 84-lead, Plastic J-leaded Chip Carrier (PLCC)	84J	B

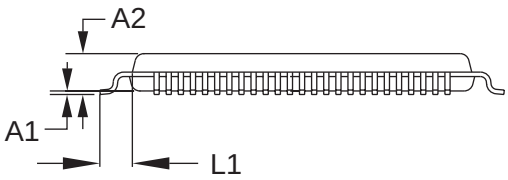
100T1 – TQFP



Top View



Bottom View



Side View

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A1	0.05		0.15	6
A2	0.95	1.00	1.05	
D		16.00 BSC		
D1		14.00 BSC		2, 3
E		16.00 BSC		
E1		14.00 BSC		2, 3
e		0.50 BSC		
b	0.17	0.22	0.27	4, 5
L1		1.00 REF		

Notes:
1. This drawing is for general information only. Refer to JEDEC Drawing MO-153, Variation AA, for proper dimensions, tolerances, datums, etc.
2. The top package body size may be smaller than the bottom package size by as much as 0.15 mm.
3. Dimensions D1 and E1 do not include mold protrusions. Allowable protrusion is 0.25 mm per side. D1 and E1 are maximum plastic body size dimensions, including mold mismatch.
4. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall not cause the lead width to exceed the maximum b dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 and 0.5 mm pitch packages.
5. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
6. A1 is defined as the distance from the seating place to the lowest point on the package body.

11/30/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**100T1**, 100-lead (14 x 14 x 1.0 mm Body), Thin Plastic Quad Flat Pack (TQFP)	100T1	A

Atmel Corporation

2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 487-2600

Regional Headquarters

Europe
Atmel Sarl
Route des Arsenaux 41
Case Postale 80
CH-1705 Fribourg
Switzerland
Tel: (41) 26-426-5555
Fax: (41) 26-426-5500

Asia
Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimshatsui
East Kowloon
Hong Kong
Tel: (852) 2721-9778
Fax: (852) 2722-1369

Japan
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
Tel: (81) 3-3523-3551
Fax: (81) 3-3523-7581

Atmel Operations

Memory
2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

Microcontrollers
2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

La Chantrerie
BP 70602
44306 Nantes Cedex 3, France
Tel: (33) 2-40-18-18-18
Fax: (33) 2-40-18-19-60

ASIC/ASSP/Smart Cards
Zone Industrielle
13106 Rousset Cedex, France
Tel: (33) 4-42-53-60-00
Fax: (33) 4-42-53-60-01

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906, USA
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Scottish Enterprise Technology Park
Maxwell Building
East Kilbride G75 0QR, Scotland
Tel: (44) 1355-803-000
Fax: (44) 1355-242-743

RF/Automotive
Theresienstrasse 2
Postfach 3535
74025 Heilbronn, Germany
Tel: (49) 71-31-67-0
Fax: (49) 71-31-67-2340

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906, USA
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Biometrics/Imaging/Hi-Rel MPU/
High Speed Converters/RF Datacom
Avenue de Rochepleine
BP 123
38521 Saint-Egreve Cedex, France
Tel: (33) 4-76-58-30-00
Fax: (33) 4-76-58-34-80

Literature Requests
www.atmel.com/literature

2818E–FPGA–1/04 xM