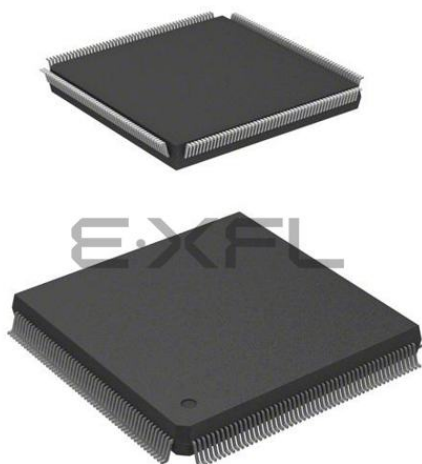




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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	2304
Total RAM Bits	18432
Number of I/O	114
Number of Gates	50000
Voltage - Supply	3V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TC)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at40k40al-1dqu

Cache Logic Design

The AT40KAL, AT6000 and FPSLIC families are capable of implementing Cache Logic (dynamic full/partial logic reconfiguration, without loss of data, on-the-fly) for building adaptive logic and systems. As new logic functions are required, they can be loaded into the logic cache without losing the data already there or disrupting the operation of the rest of the chip; replacing or complementing the active logic. The AT40KAL can act as a reconfigurable coprocessor.

Automatic Component Generators

The AT40KAL FPGA family is capable of implementing user-defined, automatically generated, macros in multiple designs; speed and functionality are unaffected by the macro orientation or density of the target device. This enables the fastest, most predictable and efficient FPGA design approach and minimizes design risk by reusing already proven functions. The Automatic Component Generators work seamlessly with industry standard schematic and synthesis tools to create the fastest, most efficient designs available.

The patented AT40KAL series architecture employs a symmetrical grid of small yet powerful cells connected to a flexible busing network. Independently controlled clocks and resets govern every column of cells. The array is surrounded by programmable I/O.

Devices range in size from 5,000 to 50,000 usable gates in the family, and have 256 to 3,048 registers. Pin locations are consistent throughout the AT40KAL series for easy design migration in the same package footprint. The AT40KAL series FPGAs utilize a reliable 0.35 μ triple-metal, CMOS process and are 100% factory-tested. Atmel's PC- and workstation-based integrated development system (IDS) is used to create AT40KAL series designs. Multiple design entry methods are supported.

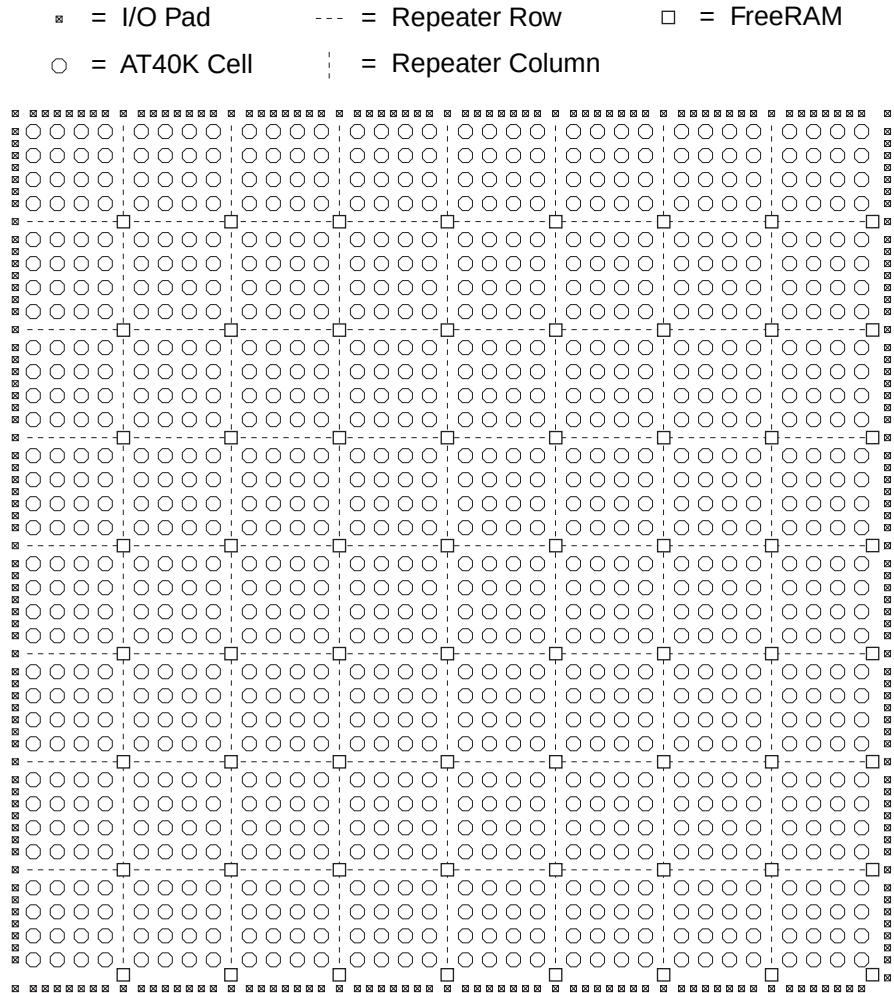
The Atmel architecture was developed to provide the highest levels of performance, functional density and design flexibility in an FPGA. The cells in the Atmel array are small, efficient and can implement any pair of Boolean functions of (the same) three inputs or any single Boolean function of four inputs. The cell's small size leads to arrays with large numbers of cells, greatly multiplying the functionality in each cell. A simple, high-speed busing network provides fast, efficient communication over medium and long distances.

The Symmetrical Array

At the heart of the Atmel architecture is a symmetrical array of identical cells, see Figure 1. The array is continuous from one edge to the other, except for bus repeaters spaced every four cells, see Figure 2 on page 5. At the intersection of each repeater row and column there is a 32 x 4 RAM block accessible by adjacent buses. The RAM can be configured as either a single-ported or dual-ported RAM⁽¹⁾, with either synchronous or asynchronous operation.

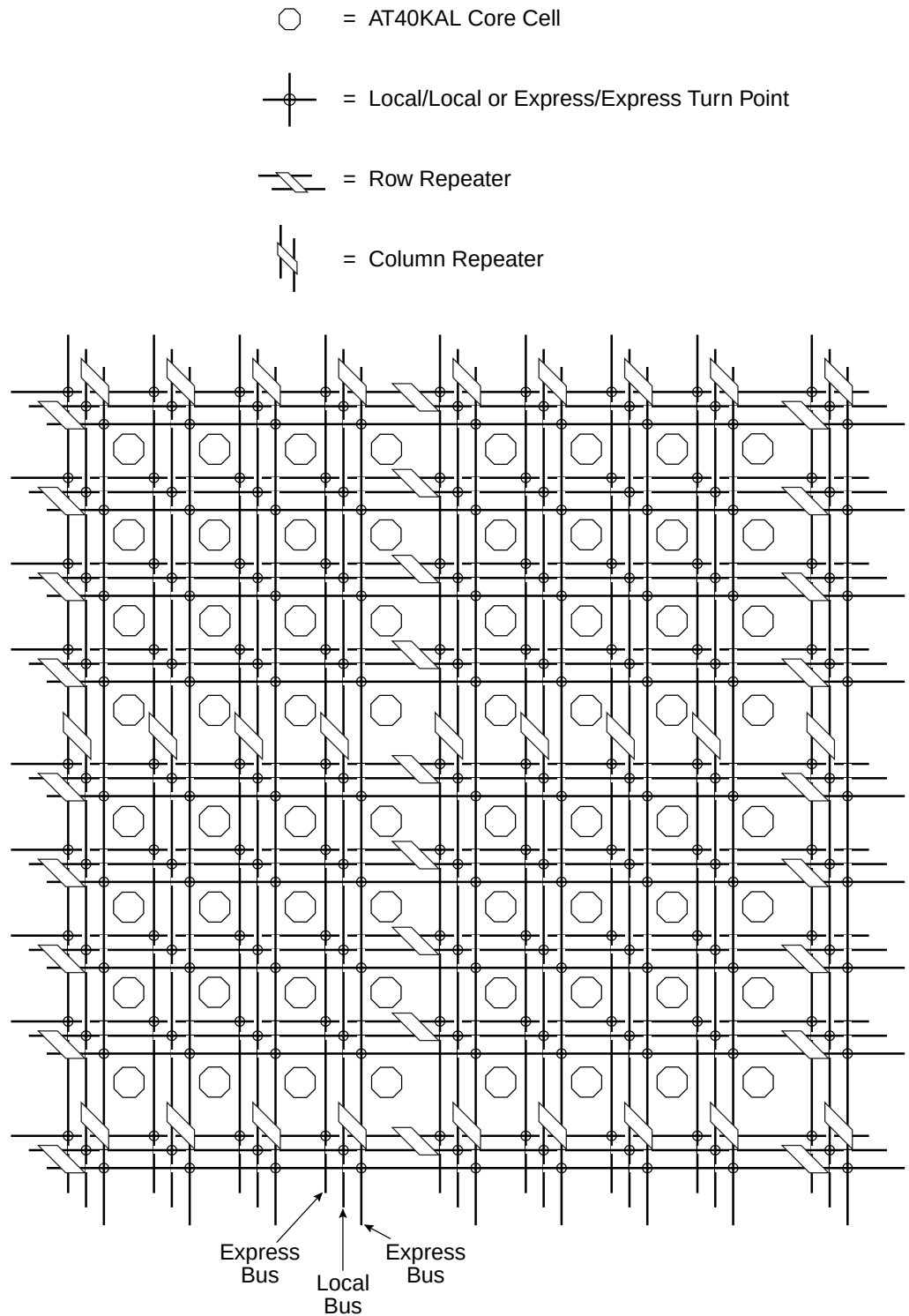
Note: 1. The right-most column can only be used as single-port RAM.

Figure 1. Symmetrical Array Surrounded by I/O (AT40K20AL)⁽¹⁾



Note: 1. AT40KAL has registered I/Os. Group enable on every sector for tri-states on obufe's.

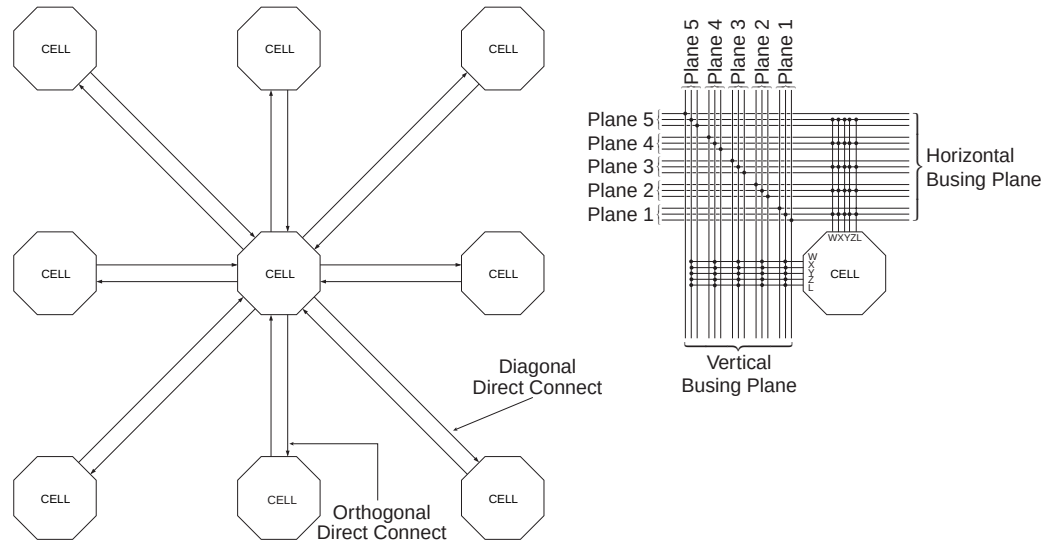
Figure 3. Busing Plane (One of Five)



Cell Connections

Figure 4(a) depicts direct connections between a cell and its eight nearest neighbors. Figure 4(b) shows the connections between a cell and five horizontal local buses (1 per busing plane) and five vertical local buses (1 per busing plane).

Figure 4. Cell Connections



(a) Cell-to-cell Connections

(b) Cell-to-bus Connections

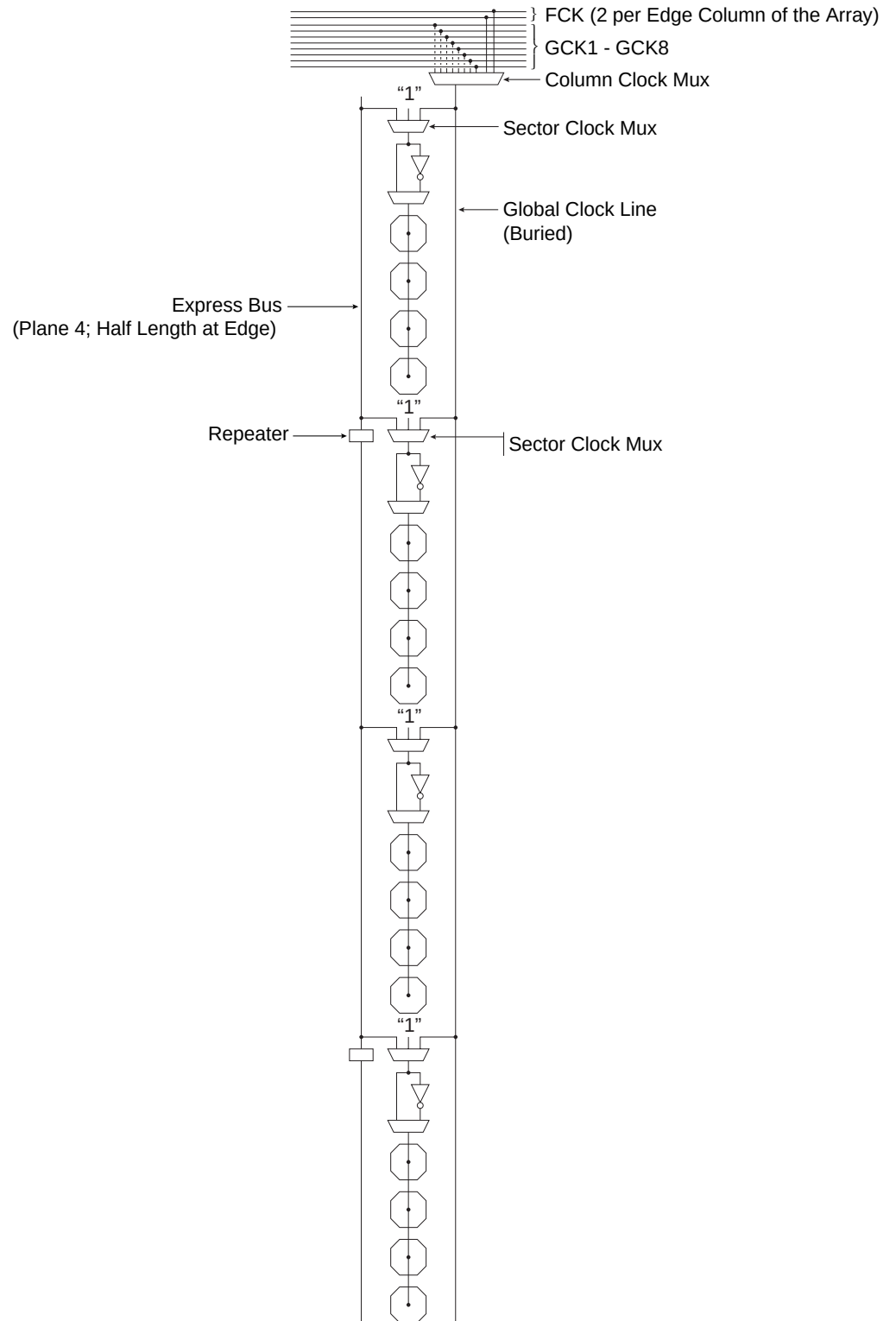
The Cell

Figure 5 depicts the AT40KAL cell. Configuration bits for separate muxes and pass gates are independent. All permutations of programmable muxes and pass gates are legal. V_n ($V_1 - V_5$) is connected to the vertical local bus in plane n . H_n ($H_1 - H_5$) is connected to the horizontal local bus in plane n . A local/local turn in plane n is achieved by turning on the two pass gates connected to V_n and H_n . Pass gates are opened to let signals into the cell from a local bus or to drive a signal out onto a local bus. Signals coming into the logic cell on one local bus plane can be switched onto another plane by opening two of the pass gates. This allows bus signals to switch planes to achieve greater route ability. Up to five simultaneous local/local turns are possible.

The AT40KAL FPGA core cell is a highly configurable logic block based around two 3-input LUTs (8 x 1 ROM), which can be combined to produce one 4-input LUT. This means that any core cell can implement two functions of 3 inputs or one function of 4 inputs. There is a Set/Reset D flip-flop in every cell, the output of which may be tri-stated and fed back internally within the core cell. There is also a 2-to-1 multiplexer in every cell, and an upstream AND gate in the “front end” of the cell. This AND gate is an important feature in the implementation of efficient array multipliers.

With this functionality in each core cell, the core cell can be configured in several “modes”. The core cell flexibility makes the AT40KAL architecture well suited to most digital design application areas, see Figure 6.

Figure 10. Clocking (for One Column of Cells)



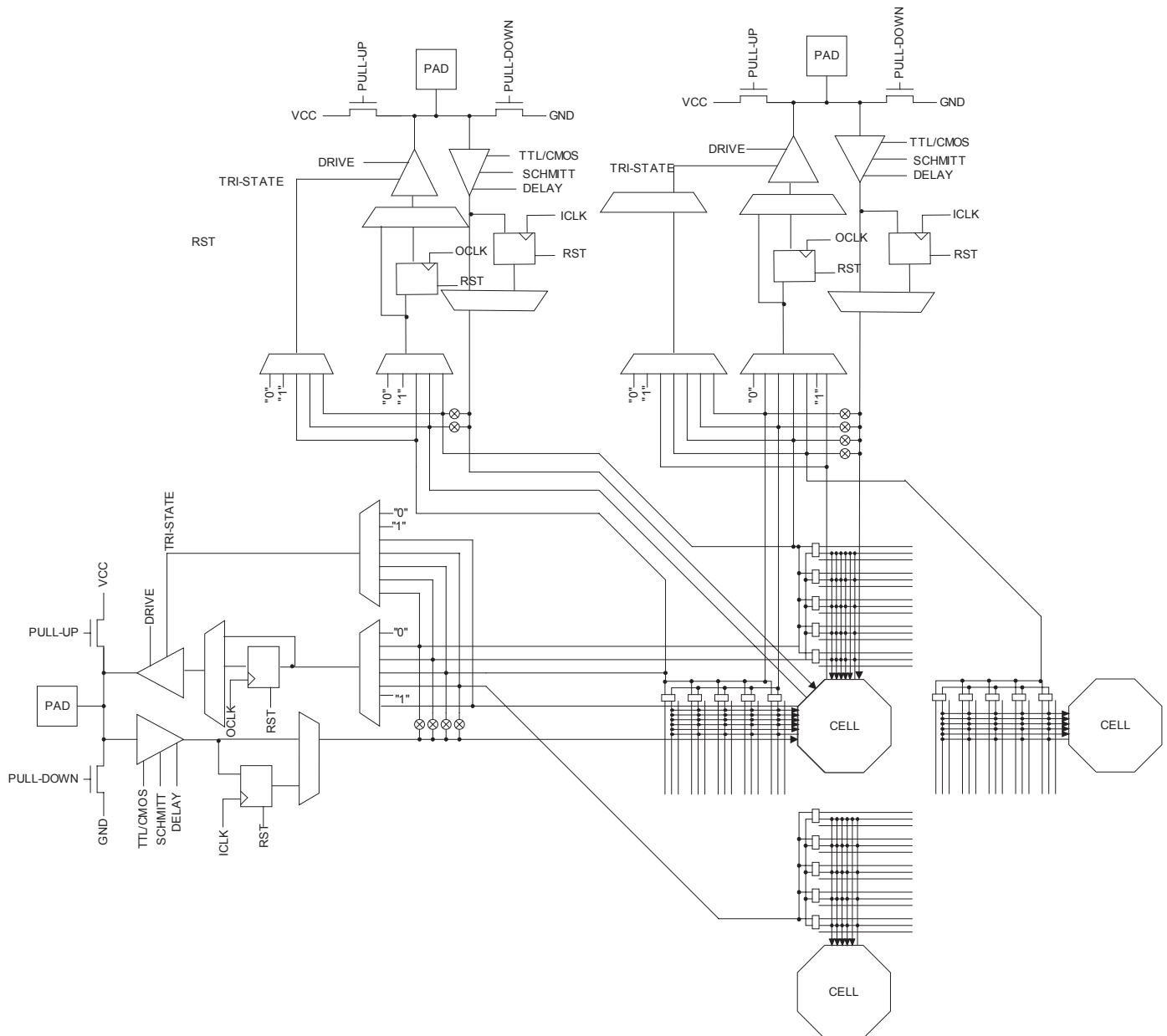
Set/Reset Scheme

The AT40KAL family reset scheme is essentially the same as the clock scheme except that there is only one Global Reset. A dedicated Global Set/Reset bus can be driven by any User I/O, except those used for clocking (Global Clocks or Fast Clocks). The automatic placement tool will choose the reset net with the most connections to use the global resources. You can change this by using an RSBUF component in your design to indicate the global reset. Additional resets will use the express bus network.

The Global Set/Reset is distributed to each column of the array. Like Sector Clock mux, there is Sector Set/Reset mux at every four cells. Each sector column of four cells is set/reset by a Plane 5 express bus or Global Set/Reset using the Sector Set/Reset mux, see Figure 11 on page 17. The set/reset provided to each sector column of four cells is either inverted or non-inverted using the Sector Reset mux.

The function of the Set/Reset input of a register is determined by a configuration bit in each cell. The Set/Reset input of a register is active low (logic 0) by default. Setting or Resetting of a register is asynchronous. Before configuration on power-up, a logic 1 (a high) is provided by each register (i.e., all registers are set at power-up).

Figure 14. Northwest Corner I/O (Similar NE/SE/SW Corners)



DC Characteristics – 3.3V Operation Commercial/Industrial

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{IH}	High-level Input Voltage	CMOS	$0.7 V_{CC}$		5.5V	V
V_{IL}	Low-level Input Voltage	CMOS	-0.3		$30\% V_{CC}$	V
V_{OH}	High-level Output Voltage	$I_{OH} = 4 \text{ mA}$ $V_{CC} = V_{CC} \text{ minimum}$	2.1			V
		$I_{OH} = 12 \text{ mA}$ $V_{CC} = 3.0V$	2.1			V
		$I_{OH} = 16 \text{ mA}$ $V_{CC} = 3.0V$	2.1			V
V_{OL}	Low-level Output Voltage	$I_{OL} = -4 \text{ mA}$ $V_{CC} = 3.0V$			0.4	V
		$I_{OL} = -12 \text{ mA}$ $V_{CC} = 3.0V$			0.4	V
		$I_{OL} = -16 \text{ mA}$ $V_{CC} = 3.0V$			0.4	V
I_{IH}	High-level Input Current	$V_{IN} = V_{CC} \text{ Maximum}$			10.0	μA
		With pull-down, $V_{IN} = V_{CC}$	75.0	150.0	300.0	μA
I_{IL}	Low-level Input Current	$V_{IN} = V_{SS}$	-10.0			μA
		With pull-up, $V_{IN} = V_{SS}$	-300.0	-150.0	-75.0	μA
I_{OZH}	High-level Tri-state Output Leakage Current	Without pull-down, $V_{IN} = V_{CC} \text{ Maximum}$			10.0	μA
		With pull-down, $V_{IN} = V_{CC} \text{ Maximum}$	75.0	150.0	300.0	μA
I_{OZL}	Low-level Tri-state Output Leakage Current	Without pull-up, $V_{IN} = V_{SS}$	-10.0			mA
		With pull-up, $V_{IN} = V_{SS}$	CON = -500 μA TO -125 μA	-150.0	CON = -500 μA TO -125 μA	μA
I_{CC}	Standby Current Consumption	Standby, unprogrammed		0.6	1.0	mA
C_{IN}	Input Capacitance	All pins			10.0	pF

Note: 1. Parameter based on characterization and simulation; it is not tested in production.

Power-On Power Supply Requirements

Atmel FPGAs require a minimum rated power supply current capacity to insure proper initialization, and the power supply ramp-up time does affect the current required. A fast ramp-up time requires more current than a slow ramp-up time.

Table 3. Power-On Power Supply Requirements⁽¹⁾

Device	Description	Maximum Current ⁽²⁾⁽³⁾
AT40K05AL AT40K10AL	Maximum Current Supply	50 mA
AT40K20AL AT40K40AL	Maximum Current Supply	100 mA

- Notes:
1. This specification applies to Commercial and Industrial grade products only.
 2. Devices are guaranteed to initialize properly at 50% of the minimum current listed above. A larger capacity power supply may result in a larger initialization current.
 3. Ramp-up time is measured from 0 V DC to 3.6 V DC. Peak current required lasts less than 2 ms, and occurs near the internal power on reset threshold voltage.

AC Timing Characteristics – 3.3V Operation

Delays are based on fixed loads and are described in the notes.

Maximum times based on worst case: $V_{CC} = 3.0V$, temperature = $70^{\circ}C$

Minimum times based on best case: $V_{CC} = 3.6V$, temperature = $0^{\circ}C$

Maximum delays are the average of t_{PDLH} and t_{PDHL} .

Clocks and Reset Input buffers are measured from a V_{IH} of 1.5V at the input pad to the internal V_{IH} of 50% of V_{CC} .

Maximum times for clock input buffers and internal drivers are measured for rising edge delays only.

Cell Function	Parameter	Path	Device	-1	Units	Notes
Global Clocks and Set/Reset						
GCLK Input Buffer	t_{PD} (Maximum)	pad -> clock	AT40K05AL	1.1	ns	Rising edge clock
		pad -> clock	AT40K10AL	1.2	ns	
		pad -> clock	AT40K20AL	1.2	ns	
		pad -> clock	AT40K40AL	1.4	ns	
FCLK Input Buffer	t_{PD} (Maximum)	pad -> clock	AT40K05AL	0.7	ns	Rising edge clock
		pad -> clock	AT40K10AL	0.8	ns	
		pad -> clock	AT40K20AL	0.8	ns	
		pad -> clock	AT40K40AL	0.8	ns	
Clock Column Driver	t_{PD} (Maximum)	clock -> colclk	AT40K05AL	0.8	ns	Rising edge clock
		clock -> colclk	AT40K10AL	0.9	ns	
		clock -> colclk	AT40K20AL	1.0	ns	
		clock -> colclk	AT40K40AL	1.1	ns	
Clock Sector Driver	t_{PD} (Maximum)	colclk -> secclk	AT40K05AL	0.5	ns	Rising edge clock
		colclk -> secclk	AT40K10AL	0.5	ns	
		colclk -> secclk	AT40K20AL	0.5	ns	
		colclk -> secclk	AT40K40AL	0.5	ns	
GSRN Input Buffer	t_{PD} (Maximum)	pad -> GSRN	AT40K05AL	3.0	ns	From any pad to Global Set/Reset network
		pad -> GSRN	AT40K10AL	3.7	ns	
		pad -> GSRN	AT40K20AL	4.3	ns	
		pad -> GSRN	AT40K40AL	5.6	ns	
Global Clock to Output	t_{PD} (Maximum)	clock pad -> out	AT40K05AL	8.3	ns	Rising edge clock Fully loaded clock tree Rising edge DFF 20 mA output buffer 50 pf pin load
		clock pad -> out	AT40K10AL	8.4	ns	
		clock pad -> out	AT40K20AL	8.6	ns	
		clock pad -> out	AT40K40AL	8.8	ns	
Fast Clock to Output	t_{PD} (Maximum)	clock pad -> out	AT40K05AL	7.9	ns	Rising edge clock Fully loaded clock tree Rising edge DFF 20 mA output buffer 50 pf pin load
		clock pad -> out	AT40K10AL	8.0	ns	
		clock pad -> out	AT40K20AL	8.1	ns	
		clock pad -> out	AT40K40AL	8.3	ns	

AT40K05AL	AT40K10AL	AT40K20AL	AT40K40AL	Left Side (Top to Bottom)				
128 I/O	192 I/O	256 I/O	384 I/O	84 PLCC	100 TQFP	144 LQFP	208 PQFP	240 PQFP
I/O17	I/O25	I/O33	I/O49	23	13	19	27	31
I/O18	I/O26	I/O34	I/O50	24	14	20	28	32
			I/O51					
			I/O52					
I/O19	I/O27	I/O35	I/O53		15	21	29	33
I/O20	I/O28	I/O36	I/O54			22	30	34
			GND					
	I/O29	I/O37	I/O55				31	35
	I/O30	I/O38	I/O56				32	36
		I/O39	I/O57					
		I/O40	I/O58					
			I/O59					
			I/O60					
			VCC					
		GND	GND					37
		I/O41	I/O61					
		I/O42	I/O62					
			I/O63					
			I/O64					
			I/O65					
			I/O66					
			GND					
	I/O31	I/O43	I/O67					38
	I/O32	I/O44	I/O68					39
	VCC	VCC	VCC					40
I/O21	I/O33	I/O45	I/O69	25	16	23	33	41
I/O22	I/O34	I/O46	I/O70	26	17	24	34	42
I/O23	I/O35	I/O47	I/O71			25	35	43
I/O24, FCK2	I/O36, FCK2	I/O48, FCK2	I/O72, FCK2			26	36	44
GND	GND	GND	GND			27	37	45
		I/O49	I/O73					
		I/O50	I/O74					
	I/O37	I/O51	I/O75					46

Note: 1. On-chip tri-state

AT40K05AL	AT40K10AL	AT40K20AL	AT40K40AL	Left Side (Top to Bottom)				
128 I/O	192 I/O	256 I/O	384 I/O	84 PLCC	100 TQFP	144 LQFP	208 PQFP	240 PQFP
	I/O38	I/O52	I/O76					47
			I/O77					
			I/O78					
			GND					
			I/O79					
			I/O80					
	I/O39	I/O53	I/O81				38	48
	I/O40	I/O54	I/O82				39	49
I/O25	I/O41	I/O55	I/O83				40	50
I/O26	I/O42	I/O56	I/O84				41	51
		GND	GND					
		VCC	VCC					
		I/O57	I/O85					
		I/O58	I/O86					
			I/O87					
			I/O88					
I/O27	I/O43	I/O59	I/O89	27	18	28	42	52
I/O28	I/O44	I/O60	I/O90		19	29	43	53
			GND					
			I/O91					
			I/O92					
I/O29	I/O45	I/O61	I/O93			30	44	54
I/O30	I/O46	I/O62	I/O94			31	45	55
I/O31 ($\overline{\text{OTS}}$) ⁽¹⁾	I/O47 ($\overline{\text{OTS}}$) ⁽¹⁾	I/O63 ($\overline{\text{OTS}}$) ⁽¹⁾	I/O95 ($\overline{\text{OTS}}$) ⁽¹⁾	28	20	32	46	56
I/O32, GCK2	I/O48, GCK2	I/O64, GCK2	I/O96, GCK2	29	21	33	47	57
M1	M1	M1	M1	30	22	34	48	58
GND	GND	GND	GND	31	23	35	49	59
M0	M0	M0	M0	32	24	36	50	60

Note: 1. On-chip tri-state

AT40K05AL	AT40K10AL	AT40K20AL	AT40K40AL	Right Side (Bottom to Top)				
128 I/O	192 I/O	256 I/O	384 I/O	84 PLCC	100 TQFP	144 LQFP	208 PQFP	240 PQFP
			I/O243					
			I/O244					
I/O83	I/O123	I/O163	I/O245		67	94	134	154
I/O84	I/O124	I/O164	I/O246			95	135	155
			GND					
	I/O125	I/O165	I/O247				136	156
	I/O126	I/O166	I/O248				137	157
		I/O167	I/O249					
		I/O168	I/O250					
			I/O251					
			I/O252					
			VCC					
		GND	GND					158
		I/O169	I/O253					
		I/O170	I/O254					
			I/O255					
			I/O256					
			I/O257					
			I/O258					
			GND					
I/O85 (D2)	I/O127 (D2)	I/O171 (D2)	I/O259 (D2)	67	68	96	138	159
I/O86	I/O128	I/O172	I/O260	68	69	97	139	160
	VCC	VCC	VCC					161
I/O87	I/O129	I/O173	I/O261			98	140	162
I/O88, FCK4	I/O130, FCK4	I/O174, FCK4	I/O262, FCK4			99	141	163
	I/O131	I/O175	I/O263					164
	I/O132	I/O176	I/O264					165
GND	GND	GND	GND			100	142	166
		I/O177	I/O265					
		I/O178	I/O266					
	I/O133	I/O179	I/O267					167
	I/O134	I/O180	I/O268					168
			I/O269					

AT40K05AL	AT40K10AL	AT40K20AL	AT40K40AL	Top Side (Right to Left)				
128 I/O	192 I/O	256 I/O	384 I/O	84 PLCC	100 TQFP	144 LQFP	208 PQFP	240 PQFP
GND	GND	GND	GND	76	77	110	160	182
I/O97 (A0)	I/O145 (A0)	I/O193 (A0)	I/O289 (A0)	77	78	111	161	183
I/O98, GCK7 (A1)	I/O146, GCK7 (A1)	I/O194, GCK7 (A1)	I/O290, GCK7 (A1)	78	79	112	162	184
I/O99	I/O147	I/O195	I/O291			113	163	185
I/O100	I/O148	I/O196	I/O292			114	164	186
			I/O293					
			I/O294					
			GND					
			I/O295					
			I/O296					
I/O101 ($\overline{\text{CS1}}, \text{A2}$)	I/O149 ($\overline{\text{CS1}}, \text{A2}$)	I/O197 ($\overline{\text{CS1}}, \text{A2}$)	I/O297 ($\overline{\text{CS1}}, \text{A2}$)	79	80	115	165	187
I/O102 (A3)	I/O150 (A3)	I/O198 (A3)	I/O298 (A3)	80	81	116	166	188
		I/O199	I/O299					
		I/O200	I/O300					
		VCC	VCC					
		GND	GND					
	I/O151 ⁽¹⁾	I/O201 ⁽¹⁾	I/O301 ⁽¹⁾	75 ⁽¹⁾ NC	76 ⁽¹⁾ NC	109 ⁽¹⁾ NC	159 ⁽¹⁾ NC	189 ⁽¹⁾ NC
	I/O152	I/O202	I/O302					190
I/O103	I/O153	I/O203	I/O303			117	167	191
I/O104 ⁽¹⁾	I/O154	I/O204	I/O304				168	192
			I/O305					
			I/O306					
			GND					
			I/O307					
			I/O308					
	I/O155	I/O205	I/O309				169	193
	I/O156	I/O206	I/O310				170	194
		I/O207	I/O311					195
		I/O208	I/O312					
GND	GND	GND	GND			118	171	196

Note: 1. Shared with TSTCLK. No Connect.

AT40K05AL	AT40K10AL	AT40K20AL	AT40K40AL	Top Side (Right to Left)				
128 I/O	192 I/O	256 I/O	384 I/O	84 PLCC	100 TQFP	144 LQFP	208 PQFP	240 PQFP
I/O105	I/O157	I/O209	I/O313			119	172	197
I/O106	I/O158	I/O210	I/O314			120	173	198
	I/O159	I/O211	I/O315					199
	I/O160	I/O212	I/O316					200
	VCC	VCC	VCC					201
		I/O213	I/O317					
		I/O214	I/O318					
			GND					
			I/O319					
			I/O320					
			I/O321					
			I/O322					
		I/O215	I/O323					
		I/O216	I/O324					
		GND	GND					
			VCC					
I/O107 (A4)	I/O161 (A4)	I/O217 (A4)	I/O325 (A4)	81	82	121	174	202
I/O108 (A5)	I/O162 (A5)	I/O218 (A5)	I/O326 (A5)	82	83	122	175	203
	I/O163	I/O219	I/O327				176	205
	I/O164	I/O220	I/O328				177	206
I/O109	I/O165	I/O221	I/O329		84	123	178	207
I/O110	I/O166	I/O222	I/O330		85	124	179	208
			GND					
			I/O331					
			I/O332					
			I/O333					
			I/O334					
I/O111 (A6)	I/O167 (A6)	I/O223 (A6)	I/O335 (A6)	83	86	125	180	209
I/O112 (A7)	I/O168 (A7)	I/O224 (A7)	I/O336 (A7)	84	87	126	181	210
GND	GND	GND	GND	1	88	127	182	211
VCC	VCC	VCC	VCC	2	89	128	183	212

Note: 1. Shared with TSTCLK. No Connect.

AT40K05AL	AT40K10AL	AT40K20AL	AT40K40AL	Top Side (Right to Left)				
128 I/O	192 I/O	256 I/O	384 I/O	84 PLCC	100 TQFP	144 LQFP	208 PQFP	240 PQFP
I/O113 (A8)	I/O169 (A8)	I/O225 (A8)	I/O337 (A8)	3	90	129	184	213
I/O114 (A9)	I/O170 (A9)	I/O226 (A9)	I/O338 (A9)	4	91	130	185	214
			I/O339					
			I/O340					
			I/O341					
			I/O342					
			GND					
I/O115	I/O171	I/O227	I/O343		92	131	186	215
I/O116	I/O172	I/O228	I/O344		93	132	187	216
	I/O173	I/O229	I/O345				188	217
	I/O174	I/O230	I/O346				189	218
I/O117 (A10)	I/O175 (A10)	I/O231 (A10)	I/O347 (A10)	5	94	133	190	220
I/O118 (A11)	I/O176 (A11)	I/O232 (A11)	I/O348 (A11)	6	95	134	191	221
			VCC					
		GND	GND					
		I/O233	I/O349					
		I/O234	I/O350					
			I/O351					
			I/O352					
			I/O353					
			I/O354					
			GND					
		I/O235	I/O355					
		I/O236	I/O356					
	VCC	VCC	VCC					222
	I/O177	I/O237	I/O357					223
	I/O178	I/O238	I/O358					224
I/O119	I/O179	I/O239	I/O359			135	192	225
I/O120	I/O180	I/O240	I/O360			136	193	226
GND	GND	GND	GND			137	194	227
		I/O241	I/O361					

Note: 1. Shared with TSTCLK. No Connect.



Part/Package Availability and User I/O Counts (including Dual-function Pins)

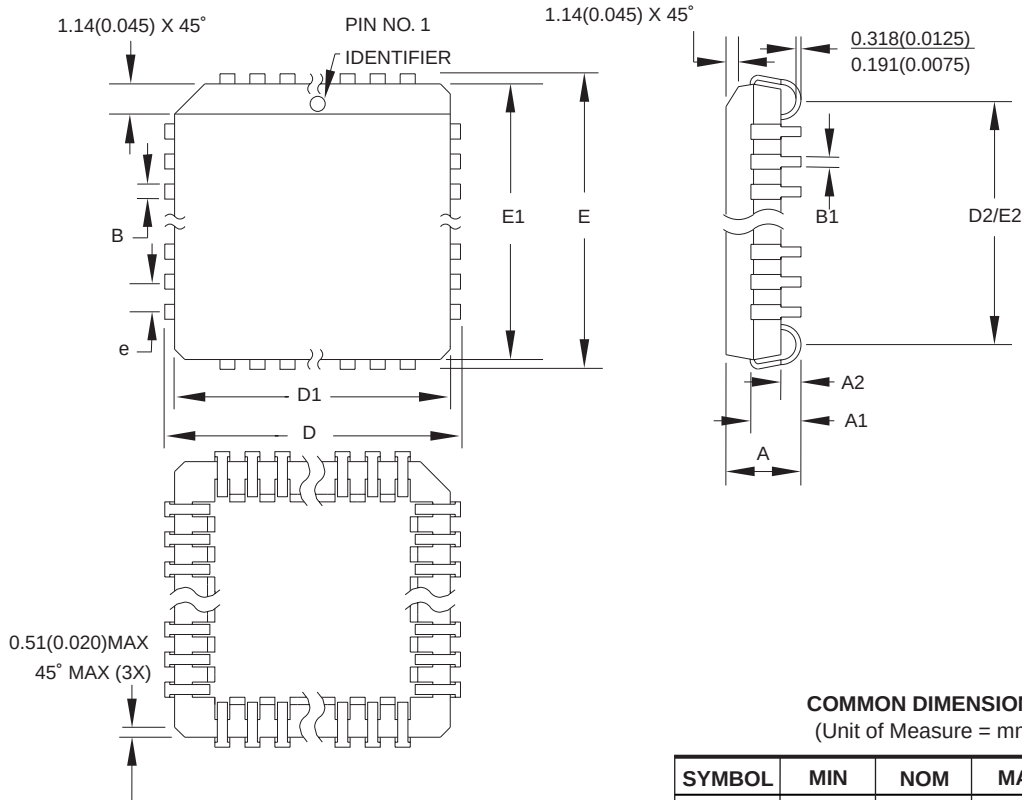
Package ⁽¹⁾	AT40K05AL	AT40K10AL	AT40K20AL	AT40K40AL
84 PLCC	62	62	–	62
100 TQFP	78	78	78	–
144 LQFP	114	114	114	114
208 PQFP	128	161	161	161
240 PQFP	–	–	–	193

Note: 1. Devices in same package are pin-to-pin compatible.

Package Type	
84J	84-lead, Plastic J-leaded Chip Carrier (PLCC)
100T1	100-lead, Thin (1.0 mm) Plastic Quad Flat Package (TQFP)
144L1	144-lead, Low-profile (1.4 mm) Plastic Quad Flat Package (LQFP)
208Q1	208-lead, Plastic Quad Flat Package (PQFP)
240Q1	240-lead, Plastic Quad Flat Package (PQFP)

Packaging Information

84J – PLCC



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	4.191	—	4.572	
A1	2.286	—	3.048	
A2	0.508	—	—	
D	30.099	—	30.353	
D1	29.210	—	29.413	Note 2
E	30.099	—	30.353	
E1	29.210	—	29.413	Note 2
D2/E2	27.686	—	28.702	
B	0.660	—	0.813	
B1	0.330	—	0.533	
e	1.270 TYP			

- Notes:
1. This package conforms to JEDEC reference MS-018, Variation AF.
 2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010" (0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
 3. Lead coplanarity is 0.004" (0.102 mm) maximum.

10/04/01



2325 Orchard Parkway
San Jose, CA 95131

TITLE

84J, 84-lead, Plastic J-leaded Chip Carrier (PLCC)

DRAWING NO.

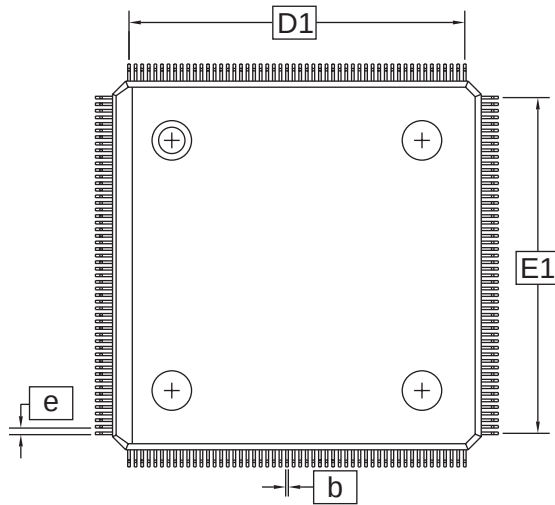
84J

REV.

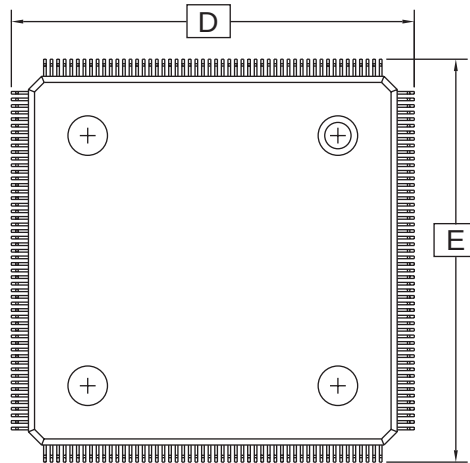
B



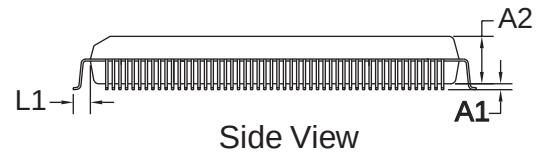
208Q1 – PQFP



Top View



Bottom View



Side View

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A1	0.25	–	0.50	
A2	3.20	3.40	3.60	
D	30.60 BSC			
D1	28.00 BSC			2, 3
E	30.60 BSC			
E1	28.00 BSC			2, 3
e	0.50 BSC			
b	0.17	–	0.27	4
L1	1.30 REF			

- Notes:
1. This drawing is for general information only; refer to JEDEC Drawing MS-129, Variation FA-1, for proper dimensions, tolerances, datums, etc.
 2. The top package body size may be smaller than the bottom package size by as much as 0.15 mm.
 3. Dimensions D1 and E1 do not include mold protrusions. Allowable protrusion is 0.25 mm per side. D1 and E1 are maximum plastic body size dimensions including mold mismatch.
 4. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall not cause the lead width to exceed the maximum b dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm.

07/23/02



2325 Orchard Parkway
San Jose, CA 95131

TITLE

208Q1, 208-lead (28 x 28 mm Body, 2.6 Form Opt.),
Plastic Quad Flat Pack (PQFP)

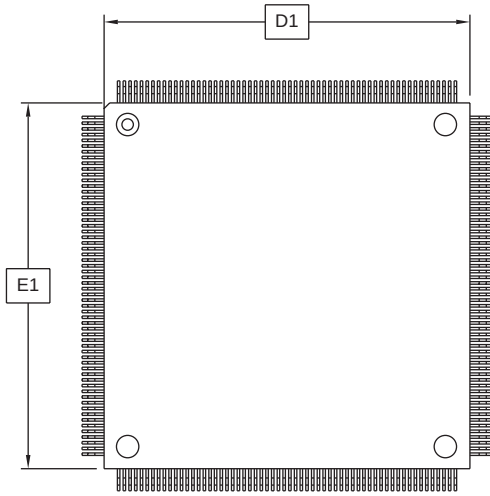
DRAWING NO.

208Q1

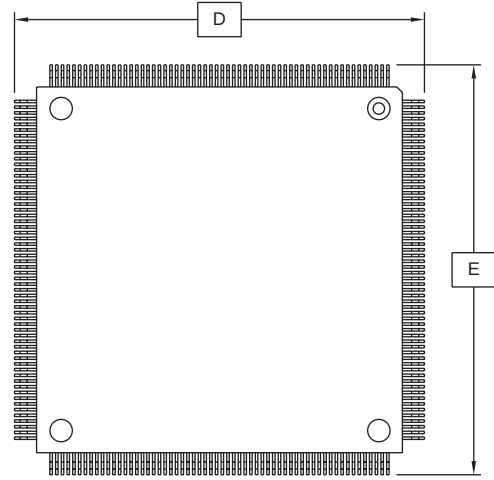
REV.

B

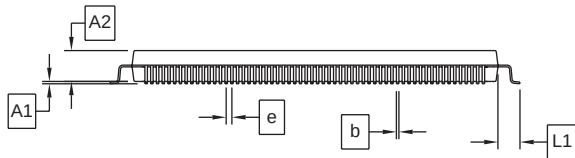
240Q1 – PQFP



Top View



Bottom View



Side View

COMMON DIMENSIONS (Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A1	0.25	–	0.50	
A2	3.20	3.40	3.60	
D	34.60 BSC			3
D1	32.00 BSC			2, 4
E	34.60 BSC			3
E1	32.00 BSC			2, 4
e	0.50 BSC			
b	0.17	–	0.27	5
L1	1.30 REF			

- Notes:
1. This drawing is for general information only. Refer to JEDEC Drawing MS-029, Variation GA, for additional information.
 2. All dimensioning and tolerancing conforms to ASME Y14.5M-1994.
 3. To be determined at seating plane.
 4. Dimensions D1 and E1 do not include mold protrusions. Allowable protrusion is 0.25 mm per side. D1 and E1 are maximum plastic body size dimensions including mold mismatch. Dimensions D1 and E1 shall be determined at datum plane.
 5. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall not cause the lead width to exceed the maximum b dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. The minimum space between protrusion and an adjacent lead shall not be less than 0.07 mm.

3/29/02



2325 Orchard Parkway
San Jose, CA 95131

TITLE

240Q1, 240-lead, 32 x 32 mm Body, 2.6 Form Opt.,
Plastic Quad Flat Pack (PQFP)

DRAWING NO.

240Q1

REV.

A