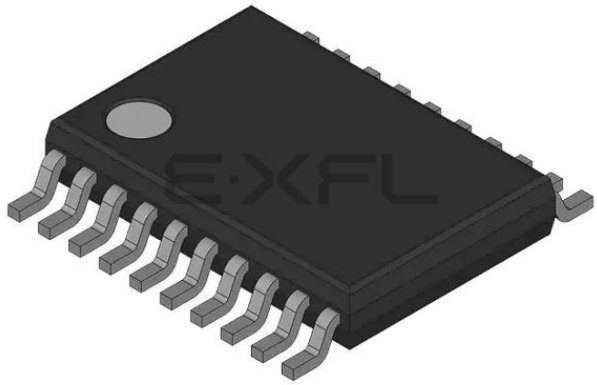


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	20MHz
Connectivity	SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	15
Program Memory Size	2KB (2K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/atmel/at89lp2052-20xu

7. Comparison to Standard 8051

The AT89LP2052/LP4052 is part of a family of devices with enhanced features that are fully binary compatible with the MCS-51 instruction set. In addition, most SFR addresses, bit assignments, and pin alternate functions are identical to Atmel's existing standard 8051 products. However, due to the high performance nature of the device, some system behaviors are different from those of Atmel's standard 8051 products such as AT89S52 or AT89S2051. The differences from the standard 8051 are outlined in the following paragraphs.

7.1 System Clock

The CPU clock frequency equals the external XTAL1 frequency. The oscillator is no longer divided by 2 to provide the internal clock, and x2 mode is not supported.

7.2 Instruction Execution with Single-cycle Fetch

The CPU fetches one code byte from memory every clock cycle instead of every six clock cycles. This greatly increases the throughput of the CPU. As a consequence, the CPU no longer executes instructions in 12 to 48 clock cycles. Each instruction executes in only 1 to 4 clock cycles. See Section 22. “Instruction Set Summary” on page 52 for more details.

7.3 Interrupt Handling

The interrupt controller polls the interrupt flags during the last clock cycle of any instruction. In order for an interrupt to be serviced at the end of an instruction, its flag needs to have been latched as active during the next to last clock cycle of the instruction, or in the last clock cycle of the previous instruction if the current instruction executes in only a single clock cycle.

7.4 Timer/Counters

The Timer/Counters increment at a rate of once per clock cycle. This compares to once every 12 clocks in the standard 8051.

7.5 Serial Port

The baud rate of the UART in Mode 0 is 1/2 the clock frequency, compared to 1/12 the clock frequency in the standard 8051. In should also be noted that when using Timer 1 to generate the baud rate in Mode 1 or Mode 3, the timer counts at the clock frequency and not at 1/12 the clock frequency. To maintain the same baud rate in the AT89LP2052/LP4052 while running at the same frequency as a standard 8051, the time-out period must be 12 times longer. Mode 1 of Timer 1 supports 16-bit auto-reload to facilitate longer time-out periods for generating low baud rates.

7.6 Watchdog Timer

The Watchdog Timer in AT89LP2052/LP4052 counts at a rate of once per clock cycle. This compares to once every 12 clocks in the standard 8051.

Figure 8-2. Single-cycle ALU Operation (Example: INC R0)

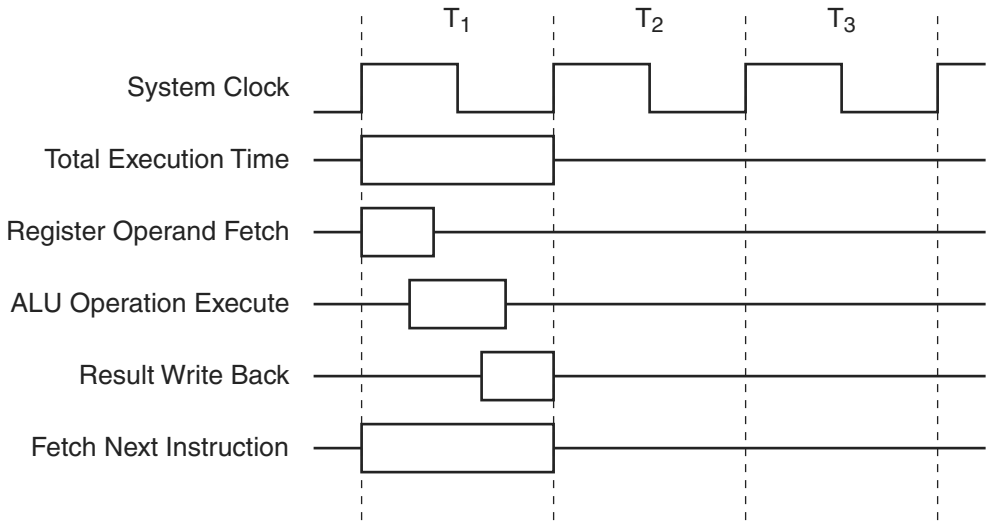


Figure 8-3. Two-Cycle ALU Operation (Example: ADD A, #data)

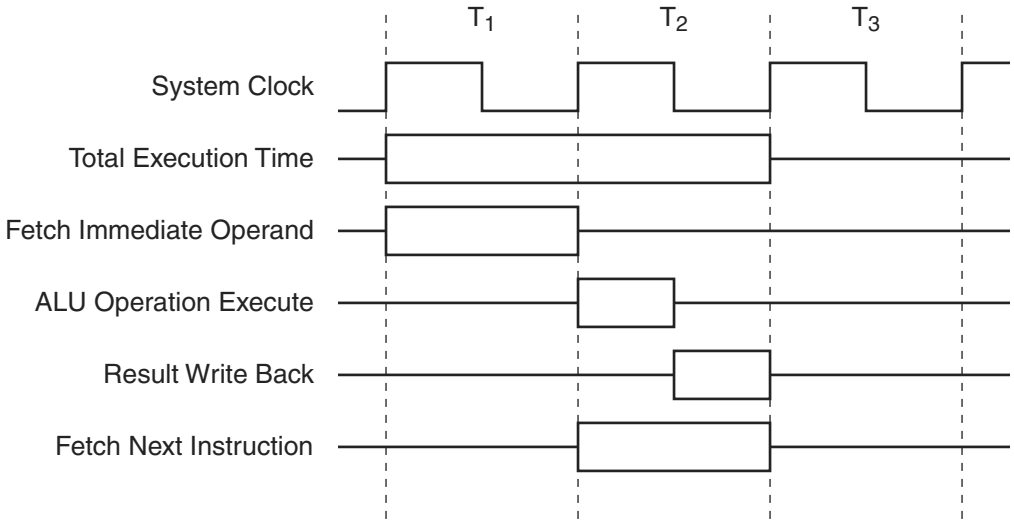


Table 13-1. PCON – Power Control Register

PCON = 87H — Reset Value = 000X 0000B

Not Bit Addressable

	SMOD1	SMOD0	PWDEX	POF	GF1	GF0	PD	IDL
Bit	7	6	5	4	3	2	1	0

Symbol	Function
SMOD1	Double Baud Rate bit. Doubles the baud rate of the UART in Modes 1, 2, or 3.
SMOD0	Frame Error Select. When SMOD0 = 1, SCON.7 is SM0. When SMOD0 = 1, SCON.7 is FE. Note that FE will be set after a frame error regardless of the state of SMOD0.
PWDEX	Power-down Exit Mode. When PWDEX = 1, wake up from Power-down is externally controlled. When PWDEX = 0, wake up from Power-down is internally timed.
POF	Power Off Flag. POF is set to “1” during power up (i.e. cold reset). It can be set or reset under software control and is not affected by RST or BOD (i.e. warm resets).
GF1, GF0	General-purpose Flags
PD	Power-down bit. Setting this bit activates power-down operation.
IDL	Idle Mode bit. Setting this bit activates Idle mode operation

14. Interrupts

The AT89LP2052/LP4052 provides 6 interrupt sources: two external interrupts, two timer interrupts, a serial port interrupt, and an analog comparator interrupt. These interrupts and the system reset each have a separate program vector at the start of the program memory space. Each interrupt source can be individually enabled or disabled by setting or clearing a bit in the interrupt enable register IE. The IE register also contains a global disable bit, EA, which disables all interrupts.

Each interrupt source can be individually programmed to one of four priority levels by setting or clearing bits in the interrupt priority registers IP and IPH. An interrupt service routine in progress can be interrupted by a higher priority interrupt, but not by another interrupt of the same or lower priority. The highest priority interrupt cannot be interrupted by any other interrupt source. If two requests of different priority levels are pending at the end of an instruction, the request of higher priority level is serviced. If requests of the same priority level are pending at the end of an instruction, an internal polling sequence determines which request is serviced. The polling sequence is based on the vector address; an interrupt with a lower vector address has higher priority than an interrupt with a higher vector address. Note that the polling sequence is only used to resolve pending requests of the same priority level.

The External Interrupts $\overline{\text{INT0}}$ and $\overline{\text{INT1}}$ can each be either level-activated or edge-activated, depending on bits IT0 and IT1 in Register TCON. The flags that actually generate these interrupts are the IE0 and IE1 bits in TCON. When the service routine is vectored to, hardware clears the flag that generated an external interrupt only if the interrupt was edge-activated. If the interrupt was level activated, then the external requesting source (rather than the on-chip hardware) controls the request flag.

Table 14-4. IPH – Interrupt Priority High Register

IPH = B7H — Reset Value = X0X0 0000B

Not Bit Addressable

	–	PCH	–	PSH	PT1H	PX1H	PT0H	PX0H
Bit	7	6	5	4	3	2	1	0

Symbol	Function
PCH	Comparator Interrupt Priority High
PSH	Serial Port Interrupt Priority High
PT1H	Timer 1 Interrupt Priority High
PX1H	External Interrupt 1 Priority High
PT0H	Timer 0 Interrupt Priority High
PX0H	External Interrupt 0 Priority High

15. I/O Ports

All 15 port pins on the AT89LP2052/LP4052 may be configured to one of four modes: quasi-bidirectional (standard 8051 port outputs), push-pull output, open-drain output, or input-only. Port modes may be assigned in software on a pin-by-pin basis as shown in Table 15-1. All port pins default to input-only mode after reset. Each port pin also has a Schmitt-triggered input for improved input noise rejection. During Power-down all the Schmitt-triggered inputs are disabled with the exception of P3.2 and P3.3, which may be used to wake-up the device. Therefore P3.2 and P3.3 should not be left floating during Power-down.

Table 15-1. Configuration Modes for Port x, Bit y

PxM0.y	PxM1.y	Port Mode
0	0	Quasi-bidirectional
0	1	Push-pull Output
1	0	Input Only (High Impedance)
1	1	Open-Drain Output

15.1 Quasi-bidirectional Output

Port pins in quasi-bidirectional output mode function similar to standard 8051 port pins. A Quasi-bidirectional port can be used both as an input and output without the need to reconfigure the port. This is possible because when the port outputs a logic high, it is weakly driven, allowing an external device to pull the pin low. When the pin is driven low, it is driven strongly and able to sink a large current. There are three pull-up transistors in the quasi-bidirectional output that serve different purposes.

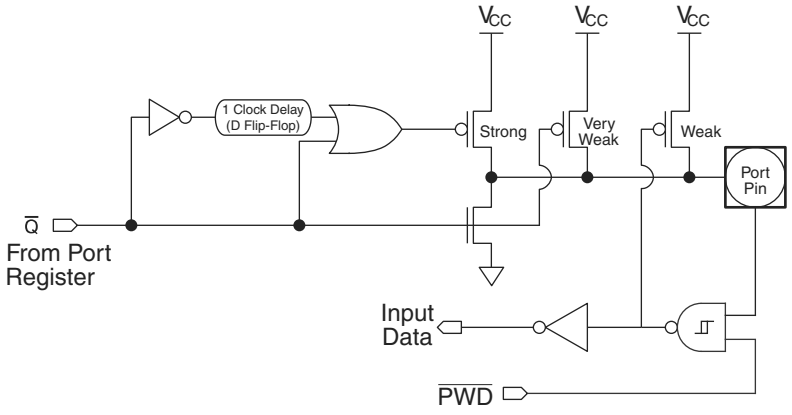
One of these pull-ups, called the “very weak” pull-up, is turned on whenever the port register for the pin contains a logic “1”. This very weak pull-up sources a very small current that will pull the pin high if it is left floating.

A second pull-up, called the “weak” pull-up, is turned on when the port register for the pin contains a logic “1” and the pin itself is also at a logic “1” level. This pull-up provides the primary source current for a quasi-bidirectional pin that is outputting a 1. If this pin is pulled low by an external device, this weak pull-up turns off, and only the very weak pull-up remains on. In order to pull the pin low under these conditions, the external device has to sink enough current to overpower the weak pull-up and pull the port pin below its input threshold voltage.

The third pull-up is referred to as the “strong” pull-up. This pull-up is used to speed up low-to-high transitions on a quasi-bidirectional port pin when the port register changes from a logic “0” to a logic “1”. When this occurs, the strong pull-up turns on for one CPU clock, quickly pulling the port pin high.

When in quasi-bidirectional mode the port pin will always output a “0” when corresponding bit in the port register is also “0”. When the port register is “1” the pin may be used either as an input or an output of “1”. The quasi-bidirectional port configuration is shown in Figure 15-1. The input circuitry of P3.2 and P3.3 is not disabled during Power-down (see Figure 15-3).

Figure 15-1. Quasi-bidirectional Output



15.2 Input-only Mode

The input port configuration is shown in Figure 15-2. It is a Schmitt-triggered input for improved input noise rejection.

Figure 15-2. Input Only

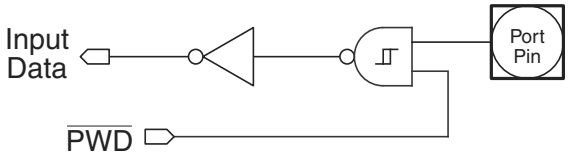
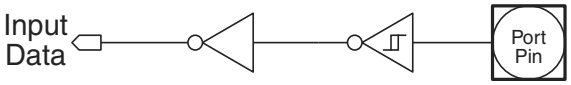


Figure 15-3. Input Only for P3.2 and P3.3



out an address byte that identifies the target slave. An address byte differs from a data byte in that the 9th bit is “1” in an address byte and “0” in a data byte. With SM2 = 1, no slave is interrupted by a data byte. An address byte, however, interrupts all slaves, so that each slave can examine the received byte and see if it is being addressed. The addressed slave clears its SM2 bit and prepares to receive the data bytes that follows. The slaves that are not addressed set their SM2 bits and ignore the data bytes.

The SM2 bit has no effect in Mode 0 but can be used to check the validity of the stop bit in Mode 1. In a Mode 1 reception, if SM2 = 1, the receive interrupt is not activated unless a valid stop bit is received.

Table 18-1. SCON – Serial Port Control Register

SCON Address = 98H — Reset Value = 0000 0000B

Bit Addressable

Bit	7	6	5	4	3	2	1	0
	SM0/FE	SM1	SM2	REN	TB8	RB8	T1	RI

(SMOD0 = 0/1)[1]

Symbol	Function
FE	Framing error bit. This bit is set by the receiver when an invalid stop bit is detected. The FE bit is not cleared by valid frames but should be cleared by software. The SMOD0 bit must be set to enable access to the FE bit. FE will be set regardless of the state of SMOD0.
SM0	Serial Port Mode Bit 0, (SMOD0 must = 0 to access bit SM0)
SM1	Serial Port Mode Bit 1 **SM0** **SM1** **Mode** **Description** **Baud Rate**[2] 0 0 0 shift register $f_{osc}/2$ 0 1 1 8-bit UART variable 1 0 2 9-bit UART $f_{osc}/32$ or $f_{osc}/16$ 1 1 3 9-bit UART variable
SM2	Enables the Automatic Address Recognition feature in Modes 2 or 3. If SM2 = 1 then RI will not be set unless the received 9th data bit (RB8) is 1, indicating an address, and the received byte is a Given or Broadcast Address. In Mode 1, if SM2 = 1 then RI will not be activated unless a valid stop bit was received, and the received byte is a Given or Broadcast Address. In Mode 0, SM2 should be 0.
REN	Enables serial reception. Set by software to enable reception. Clear by software to disable reception.
TB8	The 9th data bit that will be transmitted in Modes 2 and 3. Set or clear by software as desired.
RB8	In Modes 2 and 3, the 9th data bit that was received. In Mode 1, if SM2 = 0, RB8 is the stop bit that was received. In Mode 0, RB8 is not used.
TI	Transmit interrupt flag. Set by hardware at the end of the 8th bit time in Mode 0, or at the beginning of the stop bit in the other modes, in any serial transmission. Must be cleared by software.
RI	Receive interrupt flag. Set by hardware at the end of the 8th bit time in Mode 0, or halfway through the stop bit time in the other modes, in any serial reception (except see SM2). Must be cleared by software.

Notes: 1. SMOD0 is located at PCON.6.
2. f_{osc} = oscillator frequency.

In a more complex system the following could be used to select slaves 1 and 2 while excluding slave 0:

Slave 0 SADDR = 1100 0000

SADEN = 1111 1001

Given = 1100 0XX0

Slave 1 SADDR = 1110 0000

SADEN = 1111 1010

Given = 1110 0X0X

Slave 2 SADDR = 1110 0000

SADEN = 1111 1100

Given = 1110 00XX

In the above example the differentiation among the 3 slaves is in the lower 3 address bits. Slave 0 requires that bit 0 = 0 and it can be uniquely addressed by 1110 0110. Slave 1 requires that bit 1 = 0 and it can be uniquely addressed by 1110 and 0101. Slave 2 requires that bit 2 = 0 and its unique address is 1110 0011. To select Slaves 0 and 1 and exclude Slave 2, use address 1110 0100, since it is necessary to make bit 2 = 1 to exclude slave 2.

The Broadcast Address for each slave is created by taking the logic OR of SADDR and SADEN. Zeros in this result are treated as don't cares. In most cases, interpreting the don't cares as ones, the broadcast address will be FF hexadecimal.

Upon reset SADDR (SFR address 0A9H) and SADEN (SFR address 0B9H) are loaded with "0"s. This produces a given address of all "don't cares" as well as a Broadcast address of all "don't cares". This effectively disables the Automatic Addressing mode and allows the microcontroller to use standard 80C51-type UART drivers which do not make use of this feature.

19. Serial Peripheral Interface

The serial peripheral interface (SPI) allows high-speed synchronous data transfer between the AT89LP2052/LP4052 and peripheral devices or between multiple AT89LP2052/LP4052 devices. The AT89LP2052/LP4052 SPI features include the following:

- Full-duplex, 3-wire Synchronous Data Transfer
- Master or Slave Operation
- Maximum Bit Frequency = f/4
- LSB First or MSB First Data Transfer
- Four Programmable Bit Rates in Master Mode
- End of Transmission Interrupt Flag
- Write Collision Flag Protection
- Double-buffered Receive
- Double-buffered Transmit (Enhanced Mode Only)
- Wake up from Idle Mode (Slave Mode Only)

19.1 Normal Mode

The SPI has two modes of operation: normal (non-buffered write) and enhanced (buffered write). In normal mode, writing to the SPI data register (SPDR) of the master CPU starts the SPI clock generator and the data written shifts out of the MOSI pin and into the MOSI pin of the slave CPU. Transmission may start after an initial delay while the clock generator waits for the next full bit slot of the specified baud rate. After shifting one byte, the SPI clock generator stops, setting the end of transmission flag (SPIF) and transferring the received byte to the read buffer (SPDR). If both the SPI interrupt enable bit (SPIE) and the serial port interrupt enable bit (ES) are set, an interrupt is requested. Note that SPDR refers to either the write data buffer or the read data buffer, depending on whether the access is a write or read. In normal mode, because the write buffer is transparent (and a write access to SPDR will be directed to the shift buffer), any attempt to write to SPDR while a transmission is in progress will result in a write collision with WCOL set. However, the transmission will still complete normally, but the new byte will be ignored and a new write access to SPDR will be necessary.

19.2 Enhanced Mode

Enhanced mode is similar to normal mode except that the write buffer holds the next byte to be transmitted. Writing to SPDR loads the write buffer and sets WCOL to signify that the buffer is full and any further writes will overwrite the buffer. WCOL is cleared by hardware when the buffered byte is loaded into the shift register and transmission begins. If the master SPI is currently idle, i.e. if this is the first byte, then after loading SPDR, transmission of the byte starts and WCOL is cleared immediately. While this byte is transmitting, the next byte may be written to SPDR. The Load Enable flag (LDEN) in SPSR can be used to determine when transmission has started. LDEN is asserted during the first four bit slots of a SPI transfer. The master CPU should first check that LDEN is set and that WCOL is cleared before loading the next byte. In enhanced mode, if WCOL is set when a transfer completes, i.e. the next byte is available, then the SPI immediately loads the buffered byte into the shift register, resets WCOL, and continues transmission without stopping and restarting the clock generator. As long as the CPU can keep the write buffer full in this manner, multiple bytes may be transferred with minimal latency between bytes.

20. Analog Comparator

A single analog comparator is provided on the AT89LP2052/LP4052. Comparator operation is such that the output is a logic “1” when the positive input AIN0 (P1.0) is greater than the negative input AIN1 (P1.1). Otherwise, the output is a zero. Setting the CEN bit in ACSR enables the comparator. When the comparator is first enabled, the comparator output and interrupt flag are guaranteed to be stable only after 10 µs. The corresponding comparator interrupt should not be enabled during that time, and the comparator interrupt flag must be cleared before the interrupt is enabled in order to prevent an immediate interrupt service. Before enabling the comparator the analog inputs should be tri-stated by putting P1.0 and P1.1 into input-only mode. See Section 15.5 “Port 1 Analog Functions” on page 22.

The comparator output is internally tied to the P3.6 pin. Instructions which read the pins of P3 will also read the comparator output directly. Read-Modify-Write instructions or Write instructions to P3.6 will access bit 6 of the Port 3 register without affecting the comparator.

The comparator may be configured to cause an interrupt under a variety of output value conditions by setting the CM bits in ACSR. The comparator interrupt flag CF in ACSR is set whenever the comparator output matches the condition specified by CM. The flag may be polled by software or may be used to generate an interrupt and must be cleared by software. The EC bit in IE must be set before CF will generate an interrupt.

20.1 Comparator Interrupt with Debouncing

The comparator output is sampled every clock cycle. The conditions on the analog inputs may be such that the comparator output will toggle excessively. This is especially true if applying slow moving analog inputs. Three debouncing modes are provided to filter out this noise. In debouncing mode, the comparator uses Timer 1 to modulate its sampling time. When a relevant transition occurs, the comparator waits until two Timer 1 overflows have occurred before resampling the output. If the new sample agrees with the expected value, CF is set. Otherwise the event is ignored. The filter may be tuned by adjusting the time-out period of Timer 1. Because Timer 1 is free running, the debouncer must wait for two overflows to guarantee that the sampling delay is at least 1 time-out period. Therefore after the initial edge event, the interrupt may occur between 1 and 2 time-out periods later. See Figure 20-1.

By default the comparator is disabled during Idle mode. To allow the comparator to function during Idle, the CIDL bit in ACSR must be set. When CIDL is set, the comparator can be used to wake-up the CPU from Idle if the comparator interrupt is enabled. The comparator is always disabled during Power-down mode.

Figure 20-1. Negative Edge with Debouncing Example

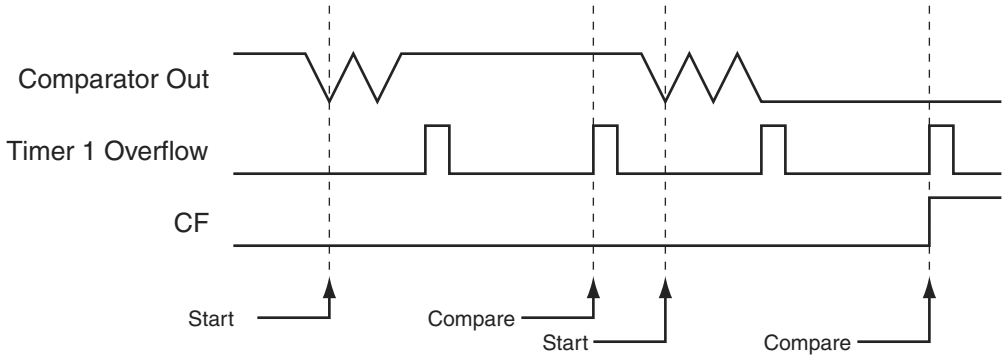


Table 20-1. ACSR – Analog Comparator Control & Status Register

ACSR = 97H — Reset Value = XXX0 0000B

Not Bit Addressable

	–	–	CIDL	CF	CEN	CM2	CM1	CM0
Bit	7	6	5	4	3	2	1	0

Symbol	Function
CIDL	Comparator Idle Enable. If CIDL = 1 the comparator will continue to operate during Idle mode. If CIDL = 0 the comparator is powered down during Idle mode. The comparator is always shut down during Power-down mode.
CF	Comparator Interrupt Flag. Set when the comparator output meets the conditions specified by the CM [2:0] bits and CEN is set. The flag must be cleared by software. The interrupt may be enabled/disabled by setting/clearing bit 6 of IE.
CEN	Comparator Enable. Set this bit to enable the comparator. Clearing this bit will force the comparator output low and prevent further events from setting CF.
CM [2:0]	Comparator Interrupt Mode **2 1 0 Interrupt Mode** 0 0 0 Negative (Low) level 0 0 1 Positive edge 0 1 0 Toggle with debounce 0 1 1 Positive edge with debounce 1 0 0 Negative edge 1 0 1 Toggle 1 1 0 Negative edge with debounce 1 1 1 Positive (High) level

21. Programmable Watchdog Timer

The programmable Watchdog Timer (WDT) protects the system from incorrect execution by triggering a system reset when it times out after the software has failed to feed the timer prior to the timer overflow. The WDT counts CPU clock cycles. The prescaler bits, PS0, PS1 and PS2 in SFR WDTCON are used to set the period of the Watchdog Timer from 16K to 2048K clock cycles. The WDT is disabled by Reset and during Power-down mode. When the WDT times out without being serviced, an internal RST pulse is generated to reset the CPU. See Table 21-1 for the available WDT period selections.

Table 21-1. Watchdog Timer Time-out Period Selection

WDT Prescaler Bits			Period* (Clock Cycles)
PS2	PS1	PS0	
0	0	0	16K
0	0	1	32K
0	1	0	64K
0	1	1	128K
1	0	0	256K
1	0	1	512K
1	1	0	1024K
1	1	1	2048K

Note: *The WDT time-out period is dependent on the system clock frequency.

The Watchdog Timer consists of a 14-bit timer with 7-bit programmable prescaler. Writing the sequence 1EH/E1H to the WDTRST register enables the timer. When the WDT is enabled, the WDTEN bit in WDTCON will be set to “1”. To prevent the WDT from generating a reset when if overflows, the watchdog feed sequence must be written to WDTRST before the end of the time-out period. To feed the watchdog, two write instructions must be sequentially executed successfully. Between the two write instructions, SFR reads are allowed, but writes are not allowed. The instructions should move 1EH to the WDTRST register and then 1EH to the WDTRST register. An incorrect feed or enable sequence will cause an immediate watchdog reset. The program sequence to feed or enable the watchdog timer is as follows:

```
MOV WDTRST, #01Eh
MOV WDTRST, #0E1h
```

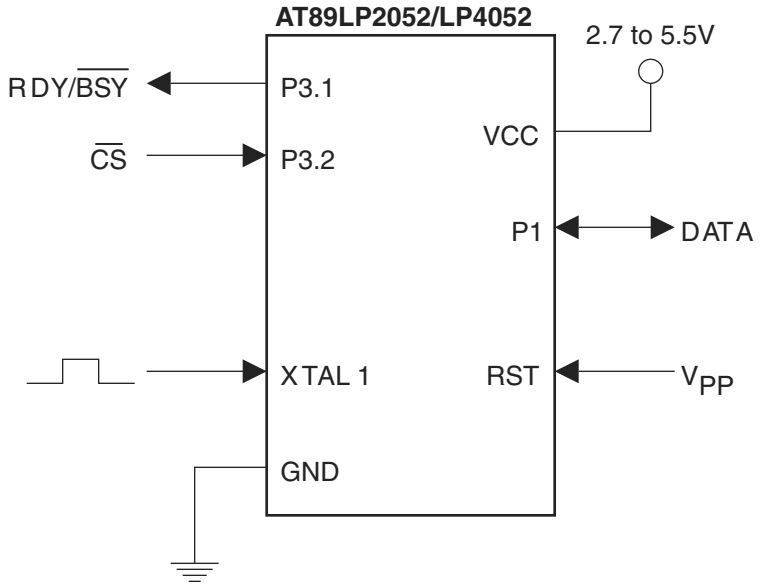
Table 22-1. Generic Instruction Execution Times and Exceptions

Instruction Type	Cycle Count
Most arithmetic, logical, bit and transfer instructions	# bytes
Branches and Calls	# bytes + 1
Single Byte Indirect (i.e. ADD A, @Ri, etc.)	2
RET, RETI	4
MOVC	3
MUL	2
DIV	4
INC DPTR	2

Table 22-2. Detailed Arithmetic Instruction Summary

		Clock Cycles		
Arithmetic Instruction	**Bytes**	**8051**	**LP2052**	**Hex Code**
ADD A, Rn	1	12	1	28-2F
ADD A, direct	2	12	2	25
ADD A, @Ri	1	12	2	26-27
ADD A, #data	2	12	2	24
ADDC A, Rn	1	12	1	38-3F
ADDC A, direct	2	12	2	35
ADDC A, @Ri	1	12	2	36-37
ADDC A, #data	2	12	2	34
SUBB A, Rn	1	12	1	98-9F
SUBB A, direct	2	12	2	95
SUBB A, @Ri	1	12	2	96-97
SUBB A, #data	2	12	2	94
INC Rn	1	12	1	08-0F
INC direct	2	12	2	05
INC @Ri	1	12	2	06-07
INC A	1	12	1	04
DEC Rn	1	12	1	18-1F
DEC direct	2	12	2	15
DEC @Ri	1	12	2	16-17
DEC A	1	12	1	14
INC DPTR	1	24	2	A3
MUL AB	1	48	2	A4
DIV AB	1	48	4	84
DA A	1	12	1	D4

Figure 23-2. Flash Parallel Programming Device Connections



Note: Sampling of pin P3.1 (RDY/$\overline{BSY}$) is optional. During Parallel Programming, P3.1 will be pulled low while the device is busy. Note that it does not require an external passive pull-up to V_{CC}.

While $\overline{CS}$ is high, the interface is reset to its default state and P1 is tri-stated. $\overline{CS}$ should be brought low before the first byte of a command is issued, and should return high only after the last byte of the command has been strobed. Figure 23-3 shows a generic parallel write command sequence. Command, address, and data bytes are sampled from P1 on the rising edge of the XTAL1 pulse. Figure 23-4 shows a generic parallel read command sequence. Command and address bytes are sampled from P1 on the rising edge of the XTAL1 pulse. At the falling edge of the fourth XTAL1 pulse the device enables P1 to output data. The data remains on P1 until $\overline{CS}$ is brought high. During reads the parallel programmer should tri-state P1 before the negative edge of the fourth XTAL1 pulse to avoid bus contention.

Figure 23-3. Parallel Write Command Sequence

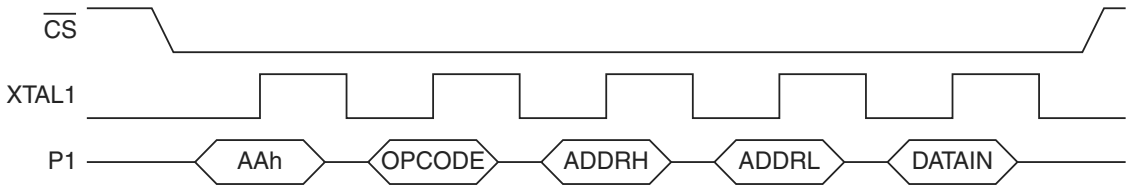
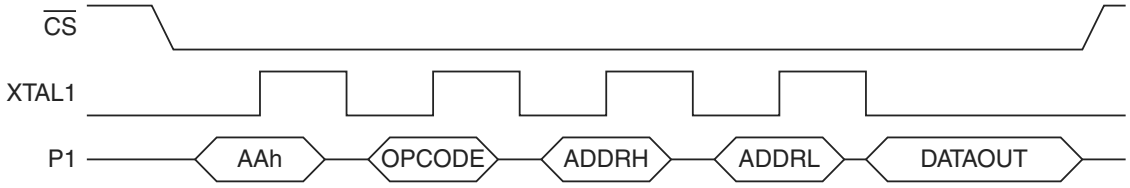


Figure 23-4. Parallel Read Command Sequence

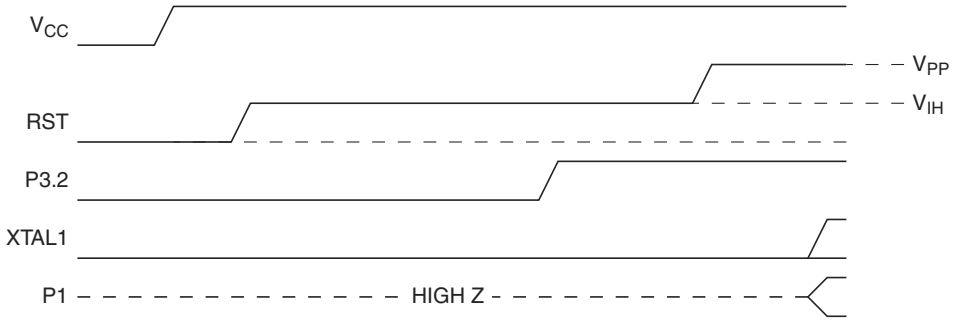


23.4.1 Power-up Sequence

Execute the following sequence to power-up the device **before** parallel programming.

1. Apply power between VCC and GND pins.
2. After V_{CC} has settled, wait 10 µs and bring RST to “H”.
3. Wait 2 ms for the internal Power-on Reset to time out.
4. Bring P3.2 to “H” and then wait 10 µs.
5. Raise RST/V_{PP} to 12V to enable the parallel programming modes.
6. After V_{PP} has settled, wait an additional 10 µs before programming.

Figure 23-5. Parallel Mode Power-up Operation

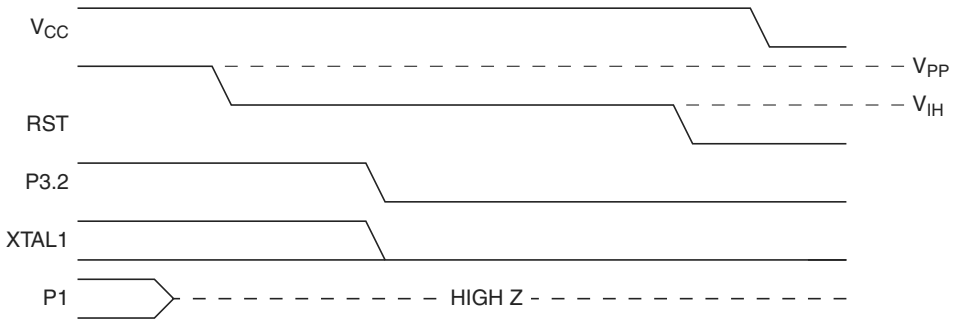


23.4.2 Power-down Sequence

Execute the following sequence to power-down the device **after** parallel programming.

1. Tri-state P1.
2. Bring RST/V_{PP} down from 12V to V_{CC} and wait 10 µs.
3. Bring XTAL and P3.2 to “L”.
4. Bring RST to “L” and wait 10 µs.
5. Power off V_{CC}.

Figure 23-6. Parallel Mode Power-down Operation



Note: The waveforms on this page are not to scale.

23.4.10 Read Atmel Signature Page

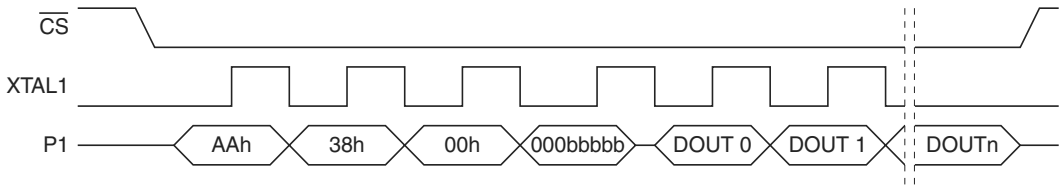
Function:

- Read 1 to 32 bytes of data from the Atmel Signature Row.
- The byte address (offset in page) is initialized to bits [4:0] of the low address byte. The internal address is incremented by one on the negative edge of the XTAL1 pulse. The address will wrap around to the 1st byte of the page when incremented past 31.
- Read data will be output on P1 after the falling edge of fourth XTAL1 pulse (address low byte strobe). The programmer should tri-state P1 prior to this edge to avoid bus contention on P1.

Usage:

1. Bring $\overline{CS}$ (P3.2) low.
2. Drive P1 to AAh and pulse XTAL1 high.
3. Drive P1 to 38h and pulse XTAL1 high.
4. Drive P1 to 00h and pulse XTAL1 high.
5. Drive P1 with bits [4:0] of address and bring XTAL1 high.
6. Tri-state P1.
7. Bring XTAL1 low.
8. Read data from P1.
9. To read additional data bytes in the page, pulse XTAL1 high to increment to the next address.
10. Drive $\overline{CS}$ high.

Figure 23-14. Read Atmel Signature Page Sequence



Note: The waveform on this page is not to scale.

23.4.13 Write User Fuses

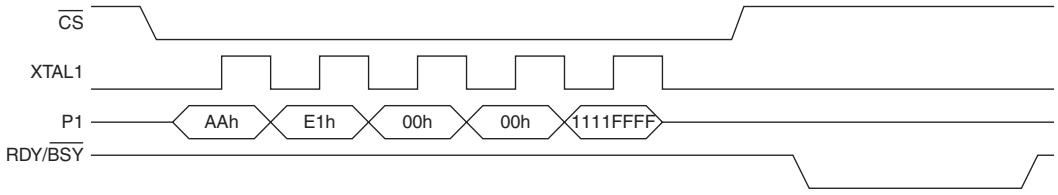
Function:

- Program User Fuses.
- Unimplemented bits should always be written with 1s.

Usage:

1. Bring $\overline{CS}$ (P3.2) low.
2. Drive P1 to AAh and pulse XTAL1 high.
3. Drive P1 to E1h and pulse XTAL1 high.
4. Drive P1 to 00h and pulse XTAL1 high.
5. Drive P1 to 00h and pulse XTAL1 high.
6. Drive data on P1 and pulse XTAL1 high.
7. Drive $\overline{CS}$ high.
8. Wait 4 ms, monitor P3.1, or poll data/status.

Figure 23-17. Write User Fuses Sequence



23.4.14 Read User Fuses

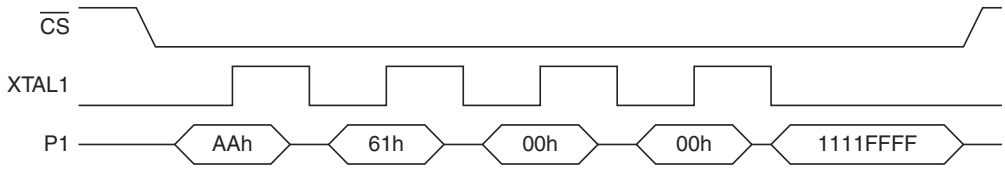
Function:

- Read status of User Fuses

Usage:

1. Bring $\overline{CS}$ (P3.2) low.
2. Drive P1 to 0xAA and pulse XTAL1 high.
3. Drive P1 to 0x61 and pulse XTAL1 high.
4. Drive P1 to 0x00 and pulse XTAL1 high.
5. Drive P1 to 0x00 and bring XTAL1 high.
6. Tri-state P1.
7. Bring XTAL1 low.
8. Read data from P1.
9. Drive $\overline{CS}$ high.

Figure 23-18. Read User Fuses Sequence



Note: The waveforms on this page are not to scale.

24.2 DC Characteristics

T_A = -40°C to 85°C, V_{CC} = 2.4V to 5.5V (unless otherwise noted)

Symbol	Parameter	Condition	Min	Max	Units
V_{IL}	Input Low-voltage	(Except RST)	-0.5	0.25 V_{CC}	V
V_{IL1}	Input Low-voltage	(RST)	-0.5	0.3 V_{CC}	V
V_{IH}	Input High-voltage	(Except RST)	0.65 V_{CC}	V_{CC} + 0.5	V
V_{IH1}	Input High-voltage	(RST)	0.6 V_{CC}	V_{CC} + 0.5	V
V_{OL}	Output Low-voltage (Ports 1, 3)(1)	I_{OL} = 10 mA, V_{CC} = 2.7V, T_A = 85°C		0.5	V
V_{OH}	Output High-voltage (Ports 1, 3) using Weak Pull-up(2)	I_{OH} = -80 µA, V_{CC} = 5V ±10%	2.4		V
		I_{OH} = -30 µA	0.75 V_{CC}		V
		I_{OH} = -12 µA	0.9 V_{CC}		V
V_{OH1}	Output High-voltage (Ports 1, 3) using Strong Pull-up(3)	I_{OH} = -10 mA, T_A = 85°C	0.9 V_{CC}		
I_{IL}	Logic 0 Input Current(2) (Ports 1, 3)	V_{IN} = 0.45V		-50	µA
I_{TL}	Logic 1 to 0 Transition Current(2) (Ports 1, 3)	V_{IN} = 2V, V_{CC} = 5V ±10%		-300	µA
I_{LI}	Input-Only Leakage Current	0 < V_{IN} < V_{CC}		±10	µA
V_{OS}	Comparator Input Offset Voltage	V_{CC} = 5V		20	mV
V_{CM}	Comparator Input Common Mode Voltage		0	V_{CC}	V
RRST	Reset Pull-down Resistor		50	150	kΩ
C_{IO}	Pin Capacitance	Test Freq. = 1 MHz, T_A = 25°C		10	pF
I_{CC}	Power Supply Current	Active Mode, 12 MHz, V_{CC} = 5.5V/3V		5.5/3.5	mA
		Idle Mode, 12 MHz, V_{CC} = 5.5V/3V		3/2	mA
	Power-down Mode(4)	V_{CC} = 5.5V		5	µA
		V_{CC} = 3V		2	µA

Notes:
1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per port pin: 10 mA
   Maximum total I_{OL} for all output pins: 15 mA
   If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
2. Port in Quasi-Bidirectional Mode
3. Port in Push-Pull Output Mode
4. Minimum V_{CC} for Power-down is 2V.

Figure 24-1. SPI Master Timing (CPHA = 0)

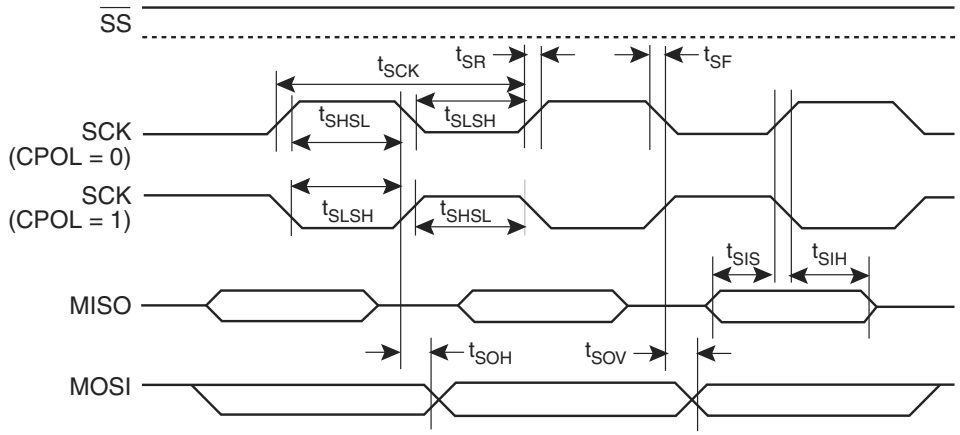


Figure 24-2. SPI Slave Timing (CPHA = 0)

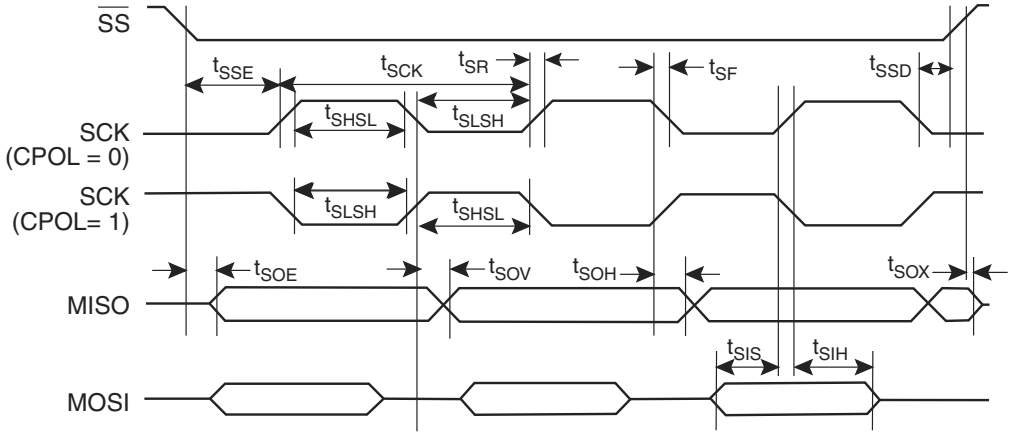


Figure 24-3. SPI Master Timing (CPHA = 1)

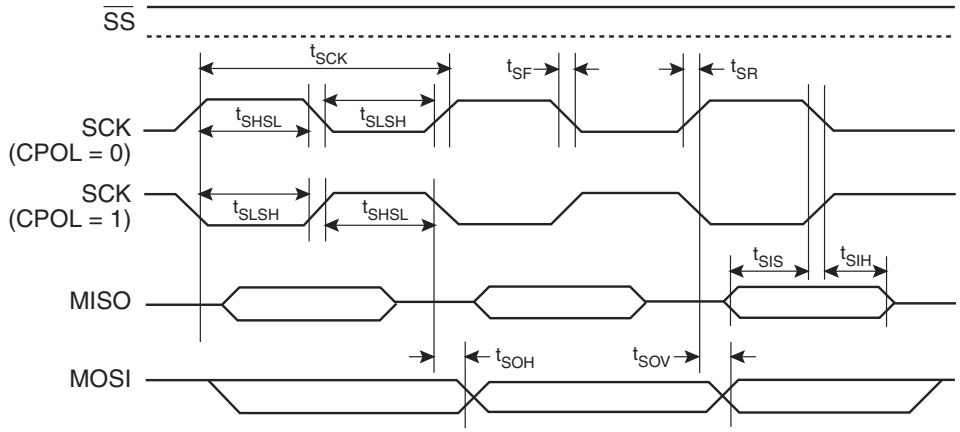
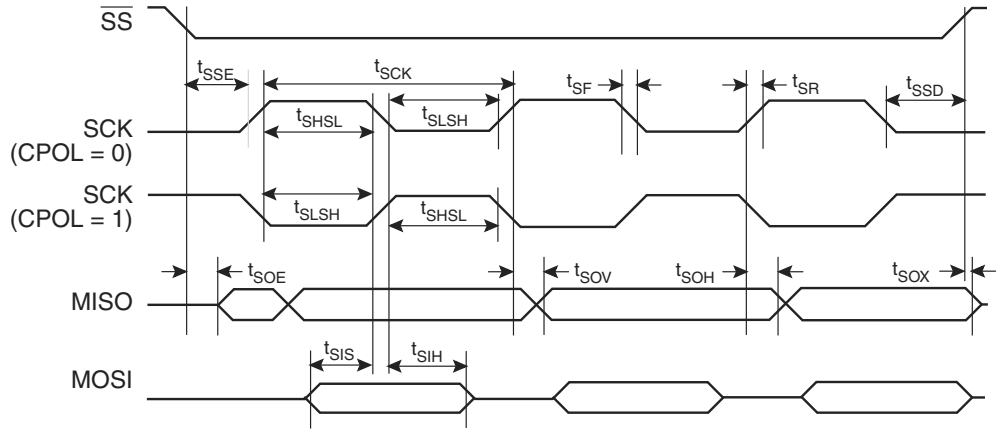


Figure 24-4. SPI Slave Timing (CPHA = 1)



24.4 External Clock Drive

Figure 24-5. External Clock Drive Waveform

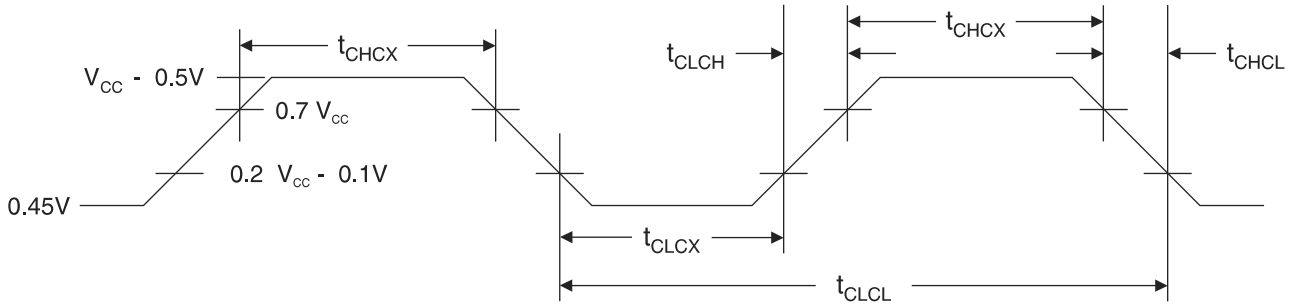
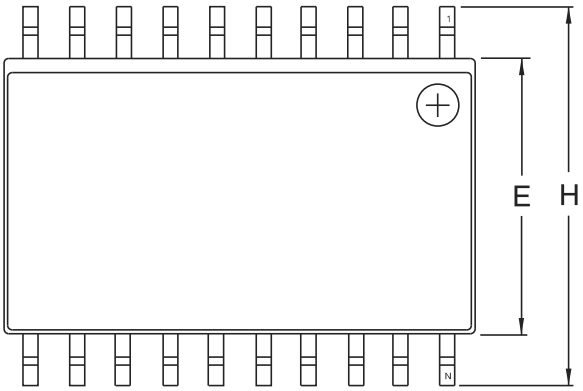


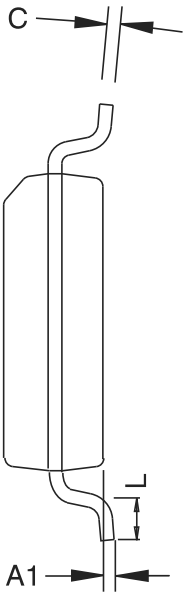
Table 24-3. External Clock Drive Parameters

Symbol	Parameter	V_{CC} = 2.4V to 5.5V		Units
		Min	Max	
$1/t_{CLCL}$	Oscillator Frequency	0	20	MHz
t_{CLCL}	Clock Period	50		ns
t_{CHCX}	High Time	12		ns
t_{CLCX}	Low Time	12		ns
t_{CLCH}	Rise Time		5	ns
t_{CHCL}	Fall Time		5	ns

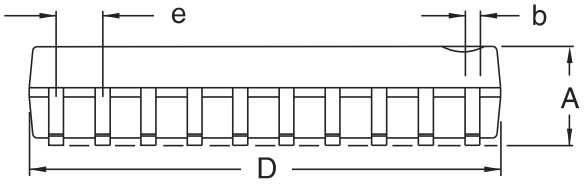
26.2 20S2 – SOIC



Top View



End View



Side View

COMMON DIMENSIONS
(Unit of Measure – mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	2.35		2.65	
A1	0.10		0.30	
b	0.33		0.51	4
C	0.23		0.32	
D	12.60		13.00	1
E	7.40		7.60	2
H	10.00		10.65	
L	0.40		1.27	3
e	1.27 BSC			

Notes.
1. This drawing is for general information only; refer to JEDEC Drawing MS-013, Variation AC for additional information.
2. Dimension 'D' does not include mold Flash, protrusions or gate burrs. Mold Flash, protrusions and gate burrs shall not exceed 0.15 mm (0.006') per side.
3. Dimension 'E' does not include inter-lead Flash or protrusion. Inter-lead Flash and protrusions shall not exceed 0.25 mm (0.010') per side.
4. 'L' is the length of the terminal for soldering to a substrate.
5. The lead width 'b', as measured 0.36 mm (0.014') or greater above the seating plane, shall not exceed a maximum value of 0.61 mm (0.024') per side.

11/6/06

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**20S2**, 20-lead, 0.300' Wide Body, Plastic Gull Wing Small Outline Package (SOIC)	20S2	B