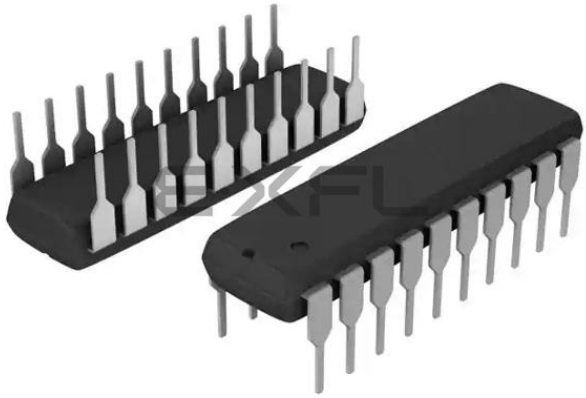


Welcome to E-XFL.COM

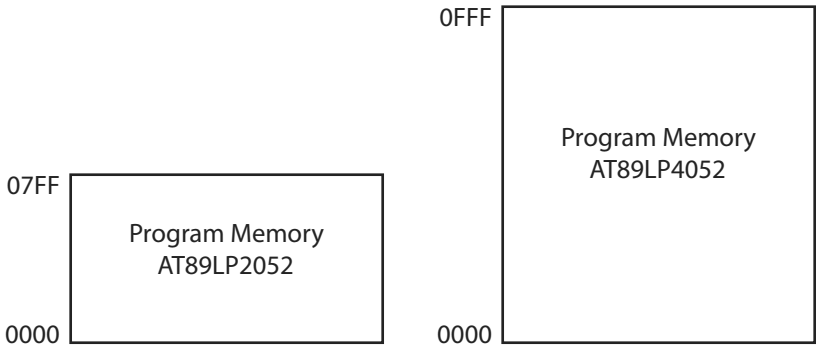
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	16MHz
Connectivity	SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	15
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	20-DIP (0.300", 7.62mm)
Supplier Device Package	20-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at89lp4052-16pi

Figure 5-1. Program Memory Map



5.2 Data Memory

The AT89LP2052/LP4052 contains 256 bytes of general SRAM data memory plus 128 bytes of I/O memory. The lower 128 bytes of data memory may be accessed through both direct and indirect addressing. The upper 128 bytes of data memory and the 128 bytes of I/O memory share the same address space (see Figure 5-2). The upper 128 bytes of data memory may only be accessed using indirect addressing. The I/O memory can only be accessed through direct addressing and contains the Special Function Registers (SFRs). The lowest 32 bytes of data memory are grouped into 4 banks of 8 registers each. The RS0 and RS1 bits (PSW.3 and PSW.4) select which register bank is in use. Instructions using register addressing will only access the currently specified bank. The AT89LP2052/LP4052 does not support external data memory.

Figure 5-2. Data Memory Map

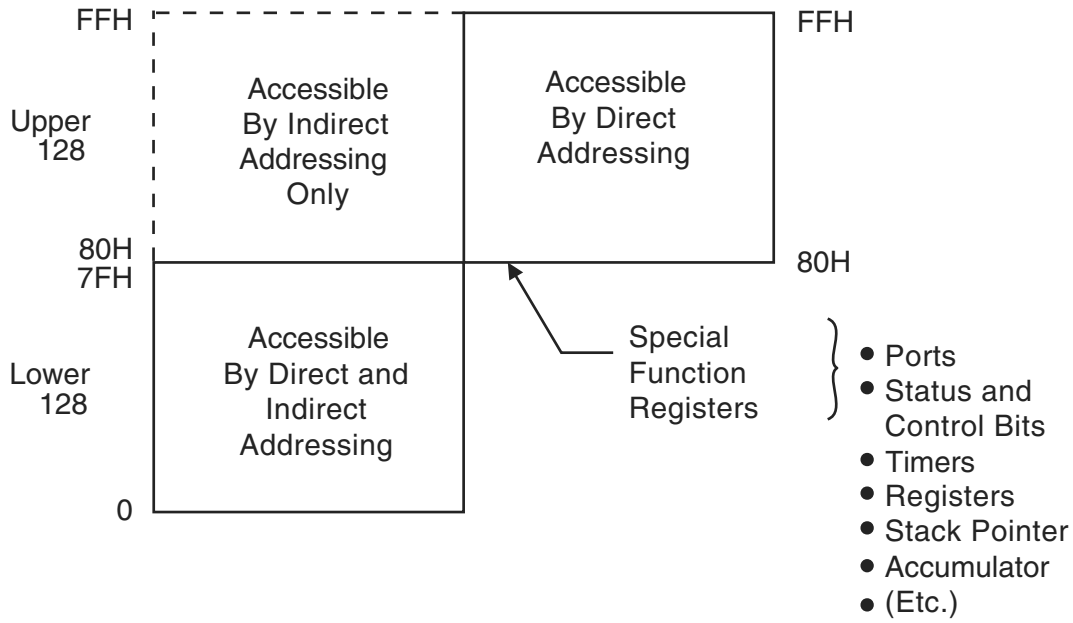


Figure 8-2. Single-cycle ALU Operation (Example: INC R0)

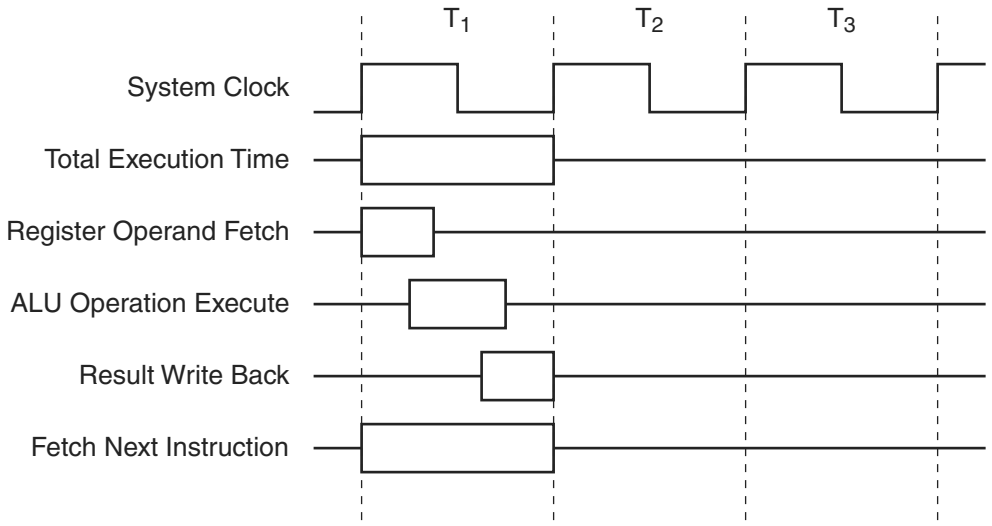


Figure 8-3. Two-Cycle ALU Operation (Example: ADD A, #data)

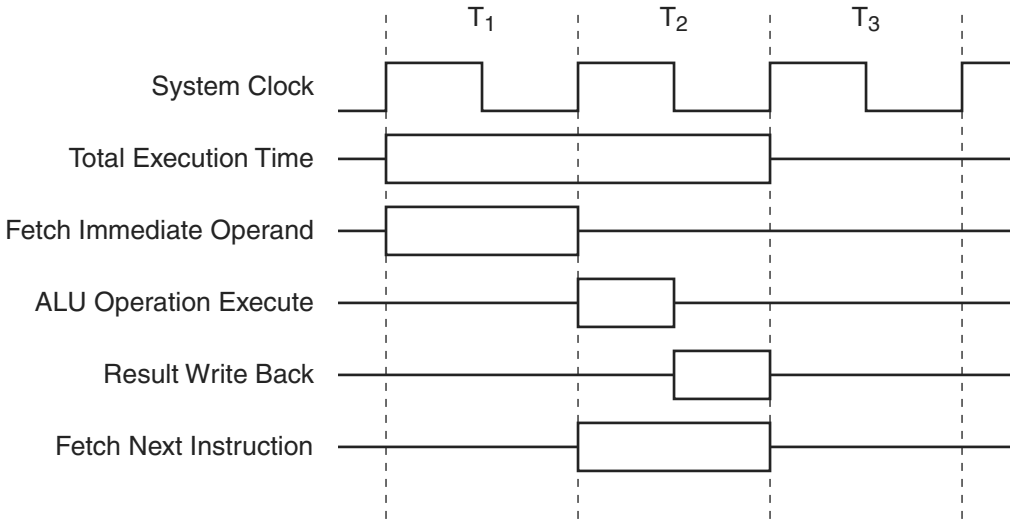


Table 13-1. PCON – Power Control Register

PCON = 87H — Reset Value = 000X 0000B

Not Bit Addressable

	SMOD1	SMOD0	PWDEX	POF	GF1	GF0	PD	IDL
Bit	7	6	5	4	3	2	1	0

Symbol	Function
SMOD1	Double Baud Rate bit. Doubles the baud rate of the UART in Modes 1, 2, or 3.
SMOD0	Frame Error Select. When SMOD0 = 1, SCON.7 is SM0. When SMOD0 = 1, SCON.7 is FE. Note that FE will be set after a frame error regardless of the state of SMOD0.
PWDEX	Power-down Exit Mode. When PWDEX = 1, wake up from Power-down is externally controlled. When PWDEX = 0, wake up from Power-down is internally timed.
POF	Power Off Flag. POF is set to “1” during power up (i.e. cold reset). It can be set or reset under software control and is not affected by RST or BOD (i.e. warm resets).
GF1, GF0	General-purpose Flags
PD	Power-down bit. Setting this bit activates power-down operation.
IDL	Idle Mode bit. Setting this bit activates Idle mode operation

14. Interrupts

The AT89LP2052/LP4052 provides 6 interrupt sources: two external interrupts, two timer interrupts, a serial port interrupt, and an analog comparator interrupt. These interrupts and the system reset each have a separate program vector at the start of the program memory space. Each interrupt source can be individually enabled or disabled by setting or clearing a bit in the interrupt enable register IE. The IE register also contains a global disable bit, EA, which disables all interrupts.

Each interrupt source can be individually programmed to one of four priority levels by setting or clearing bits in the interrupt priority registers IP and IPH. An interrupt service routine in progress can be interrupted by a higher priority interrupt, but not by another interrupt of the same or lower priority. The highest priority interrupt cannot be interrupted by any other interrupt source. If two requests of different priority levels are pending at the end of an instruction, the request of higher priority level is serviced. If requests of the same priority level are pending at the end of an instruction, an internal polling sequence determines which request is serviced. The polling sequence is based on the vector address; an interrupt with a lower vector address has higher priority than an interrupt with a higher vector address. Note that the polling sequence is only used to resolve pending requests of the same priority level.

The External Interrupts $\overline{\text{INT0}}$ and $\overline{\text{INT1}}$ can each be either level-activated or edge-activated, depending on bits IT0 and IT1 in Register TCON. The flags that actually generate these interrupts are the IE0 and IE1 bits in TCON. When the service routine is vectored to, hardware clears the flag that generated an external interrupt only if the interrupt was edge-activated. If the interrupt was level activated, then the external requesting source (rather than the on-chip hardware) controls the request flag.

If a request is active and conditions are met for it to be acknowledged, a hardware subroutine call to the requested service routine will be the next instruction executed. The call itself takes four cycles. Thus, a minimum of five complete clock cycles elapsed between activation of an interrupt request and the beginning of execution of the first instruction of the service routine. A longer response time results if the request is blocked by one of the previously listed conditions. If an interrupt of equal or higher priority level is already in progress, the additional wait time depends on the nature of the other interrupt's service routine. If the instruction in progress is not in its final clock cycle, the additional wait time cannot be more than 3 cycles, since the longest are only 4 cycles long. If the instruction in progress is RETI or an access to IE or IP, the additional wait time cannot be more than 7 cycles (a maximum of three more cycles to complete the instruction in progress, plus a maximum of 4 cycles to complete the next instruction). Thus, in a single-interrupt system, the response time is always more than 5 clock cycles and less than 13 clock cycles. See Figures 14-1 and 14-2.

Figure 14-1. Minimum Interrupt Response Time

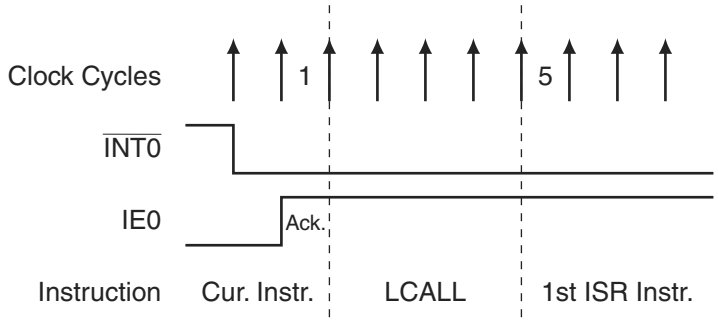


Figure 14-2. Maximum Interrupt Response Time

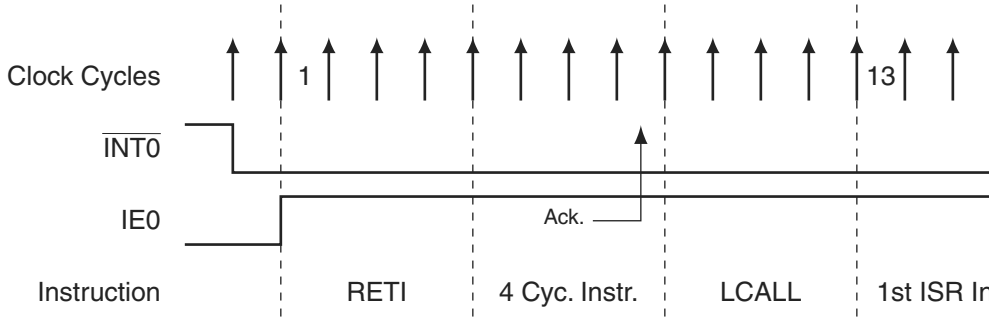


Table 14-2. IE – Interrupt Enable Register

IE = A8H — Reset Value = 00X0 0000B

Bit Addressable

	EA	EC	–	ES	ET1	EX1	ET0	EX0
Bit	7	6	5	4	3	2	1	0

Symbol	Function
EA	Global enable/disable. All interrupts are disabled when EA = 0. When EA = 1, each interrupt source is enabled/disabled by setting /clearing its own enable bit.
EC	Comparator Interrupt Enable
ES	Serial Port Interrupt Enable
ET1	Timer 1 Interrupt Enable
EX1	External Interrupt 1 Enable
ET0	Timer 0 Interrupt Enable
EX0	External Interrupt 0 Enable

Table 14-3. IP – Interrupt Priority Register

IP = B8H — Reset Value = X0X0 0000B

Bit Addressable

	–	PC	–	PS	PT1	PX1	PT0	PX0
Bit	7	6	5	4	3	2	1	0

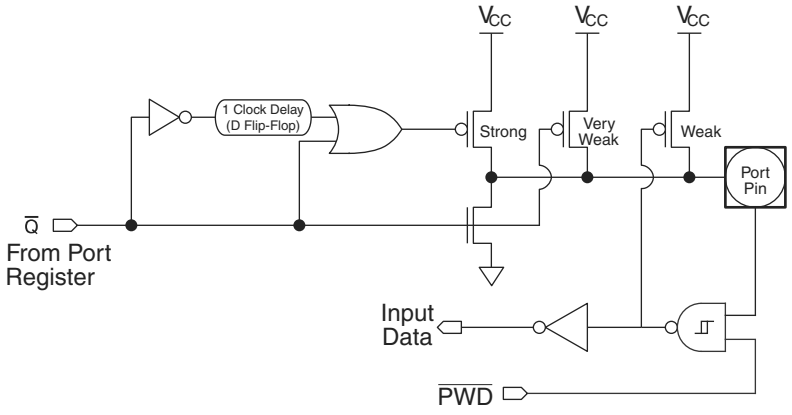
Symbol	Function
PC	Comparator Interrupt Priority Low
PS	Serial Port Interrupt Priority Low
PT1	Timer 1 Interrupt Priority Low
PX1	External Interrupt 1 Priority Low
PT0	Timer 0 Interrupt Priority Low
PX0	External Interrupt 0 Priority Low

A second pull-up, called the “weak” pull-up, is turned on when the port register for the pin contains a logic “1” and the pin itself is also at a logic “1” level. This pull-up provides the primary source current for a quasi-bidirectional pin that is outputting a 1. If this pin is pulled low by an external device, this weak pull-up turns off, and only the very weak pull-up remains on. In order to pull the pin low under these conditions, the external device has to sink enough current to overpower the weak pull-up and pull the port pin below its input threshold voltage.

The third pull-up is referred to as the “strong” pull-up. This pull-up is used to speed up low-to-high transitions on a quasi-bidirectional port pin when the port register changes from a logic “0” to a logic “1”. When this occurs, the strong pull-up turns on for one CPU clock, quickly pulling the port pin high.

When in quasi-bidirectional mode the port pin will always output a “0” when corresponding bit in the port register is also “0”. When the port register is “1” the pin may be used either as an input or an output of “1”. The quasi-bidirectional port configuration is shown in Figure 15-1. The input circuitry of P3.2 and P3.3 is not disabled during Power-down (see Figure 15-3).

Figure 15-1. Quasi-bidirectional Output



15.2 Input-only Mode

The input port configuration is shown in Figure 15-2. It is a Schmitt-triggered input for improved input noise rejection.

Figure 15-2. Input Only

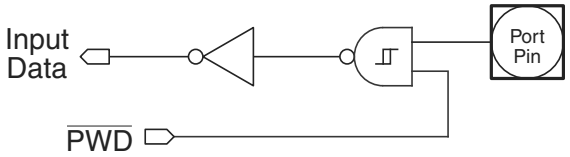


Figure 15-3. Input Only for P3.2 and P3.3

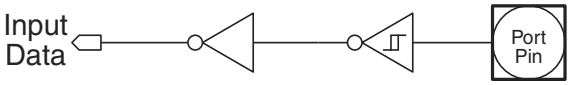


Table 15-4. Port Pin Alternate Functions

Port Pin	Configuration Bits		Alternate Function	Notes
	PxM0.y	PxM1.y		
P1.0	P1M0.0	P1M1.0	AIN0	Input-only
P1.1	P1M0.1	P1M1.1	AIN1	Input-only
P1.4	P1M0.4	P1M1.4	$\overline{SS}$	Refer to Section 19.4 “SPI Pin Configuration” on page 48
P1.5	P1M0.5	P1M1.5	MOSI	
P1.6	P1M0.6	P1M1.6	MISO	
P1.7	P1M0.7	P1M1.7	SCK	
P3.0	P3M0.0	P3M1.0	RXD	
P3.1	P3M0.1	P3M1.1	TXD	
P3.2	P3M0.2	P3M1.2	INT0	
P3.3	P3M0.3	P3M1.3	INT1	
P3.4	P3M0.4	P3M1.4	T0	Refer to Section 16.6 “Timer/Counter Pin Configuration” on page 30
P3.5	P3M0.5	P3M1.5	T1	
P3.6	Not configurable		CMPOUT	Pin is tied to comparator output

16. Enhanced Timer/Counters

The AT89LP2052/LP4052 has two 16-bit Timer/Counter registers: Timer 0 and Timer 1. As a Timer, the register is incremented every clock cycle. Thus, the register counts clock cycles. Since a clock cycle consists of one oscillator period, the count rate is equal to the oscillator frequency.

As a Counter, the register is incremented in response to a 1-to-0 transition at its corresponding input pin, T0 or T1. The external input is sampled every clock cycle. When the samples show a high in one cycle and a low in the next cycle, the count is incremented. The new count value appears in the register during the cycle following the one in which the transition was detected. Since 2 clock cycles are required to recognize a 1-to-0 transition, the maximum count rate is 1/2 of the oscillator frequency. There are no restrictions on the duty cycle of the input signal, but it should be held for at least one full clock cycle to ensure that a given level is sampled at least once before it changes.

Furthermore, the Timer or Counter functions for Timer 0 and Timer 1 have four operating modes: variable width timer/counter, 16 bit auto-reload timer/counter, 8 bit auto-reload timer/counter, and split timer/counter. The control bits C/$\overline{T}$ in the Special Function Register TMOD select the Timer or Counter function. The bit pairs (M1, M0) in TMOD select the operating modes.

16.1 Mode 0

Both Timers in Mode 0 are 8-bit Counters with a variable prescaler. The prescaler may vary from 1 to 8 bits depending on the PSC bits in TCONB, giving the timer a range of 9 to 16 bits. By default the timer is configured as a 13-bit timer compatible to Mode 0 in the standard 8051. Figure 16-1 shows the Mode 0 operation as it applies to Timer 1 in 13-bit mode. As the count rolls over from all “1”s to all “0”s, it sets the Timer interrupt flag TF1. The counted input is enabled to the Timer when TR1 = 1 and either GATE = 0 or $\overline{INT1}$ = 1. Setting GATE = 1 allows the Timer to be controlled by external input $\overline{INT1}$, to facilitate pulse width measurements. TR1 is

Figure 16-6. Timer/Counter 1 PWM Mode 0

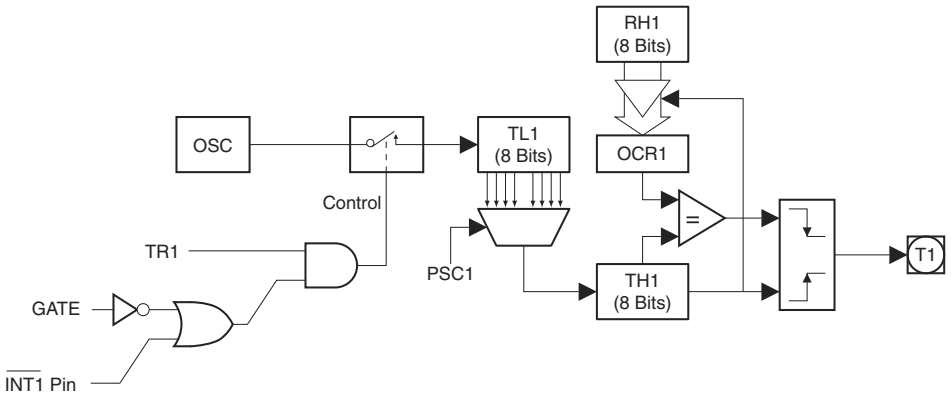
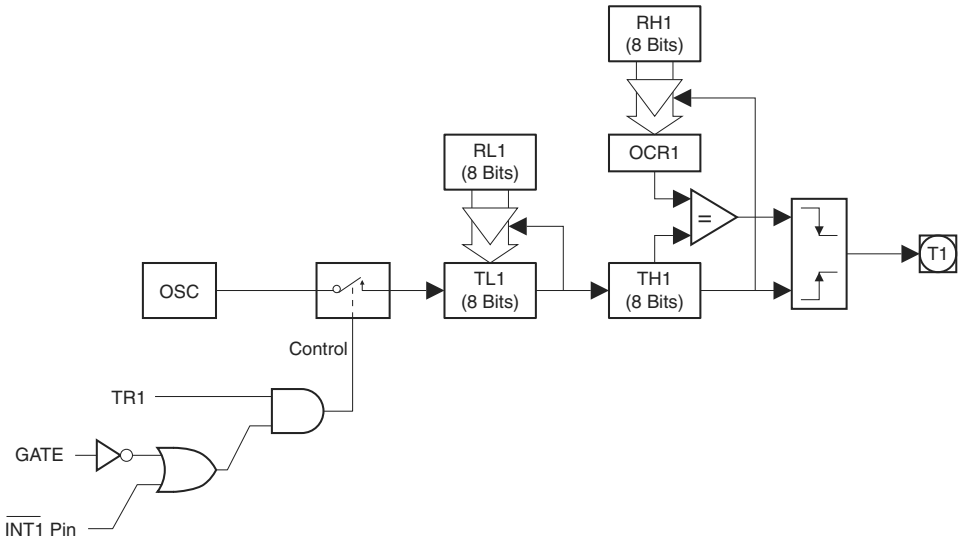


Figure 16-7. Timer/Counter 1 PWM Mode 1



16.6 Timer/Counter Pin Configuration

In order to use the counter input function or pulse width modulation output feature of Timer 0 or Timer 1, the Timer pins T0 (P3.4) and T1 (P3.5) must be configured appropriately. See Section 15.7 “Port Alternate Functions” on page 23. For the external counter input function, T0 or T1 should be configured as input-only, or as bidirectional with P3.4 or P3.5 set to “1”. The counter function may also be triggered by an internal event if T0 or T1 is configured in a bidirectional or output mode and the port bit is toggled accordingly. To enable a PWM output on T0 or T1, the pin must be configured in a bidirectional or output mode with P3.4 or P3.5 set to “1”. Setting the PWM0EN or PWM1En bits in TCONB will **not** automatically configure the pins as outputs. The PWM outputs will use a full CMOS push-pull driver if they are in the quasi-bidirectional or output configurations.

17. External Interrupts

The $\overline{\text{INT0}}$ and $\overline{\text{INT1}}$ external interrupt sources can be programmed to be level-activated or transition-activated by setting or clearing bit IT1 or IT0 in Register TCON. If ITx = 0, external interrupt x is triggered by a detected low at the $\overline{\text{INTx}}$ pin. If ITx = 1, external interrupt x is negative edge-triggered. In this mode if successive samples of the $\overline{\text{INTx}}$ pin show a high in one cycle

Figure 18-1. Serial Port Mode 0

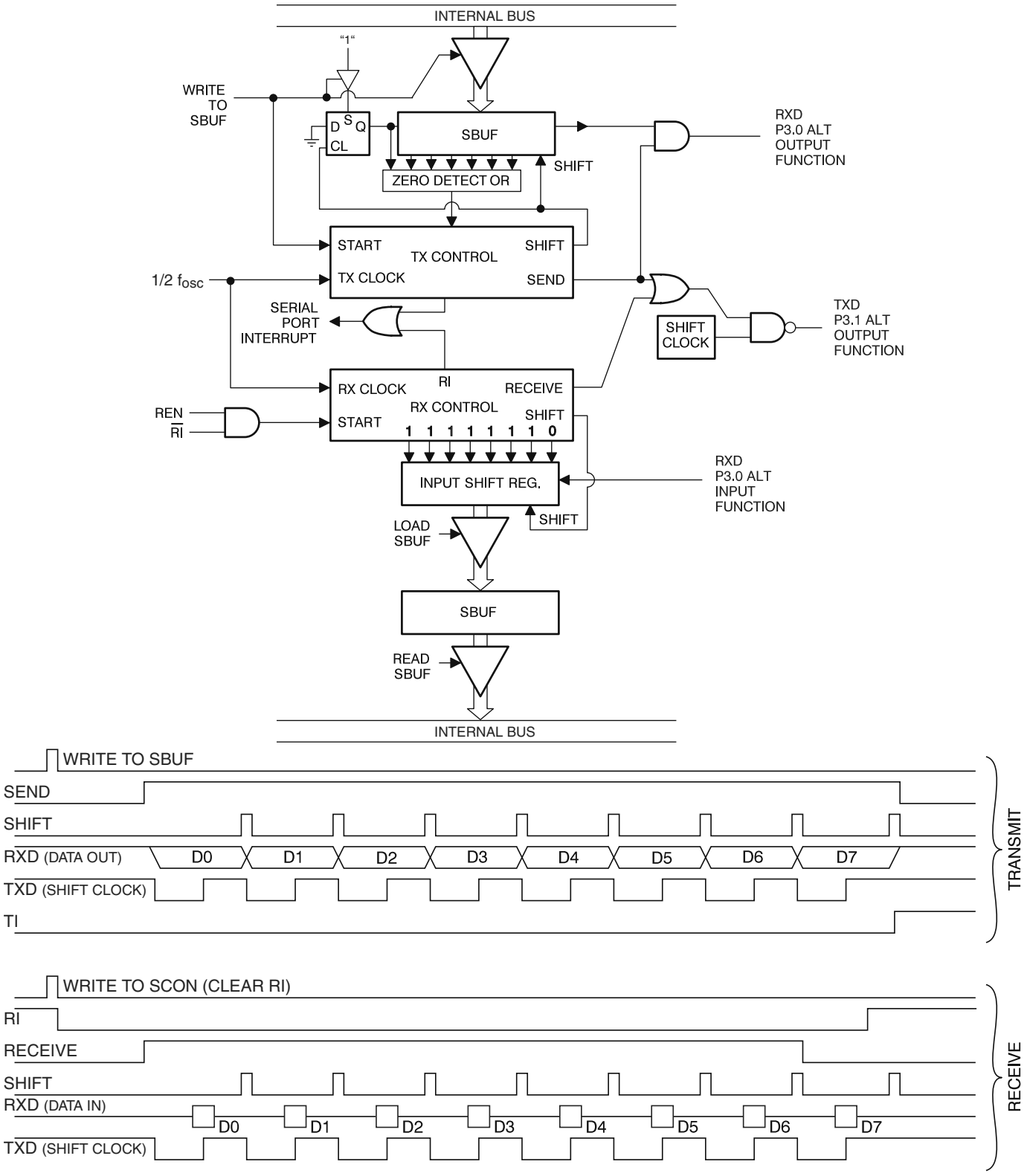


Figure 18-2. Serial Port Mode 1

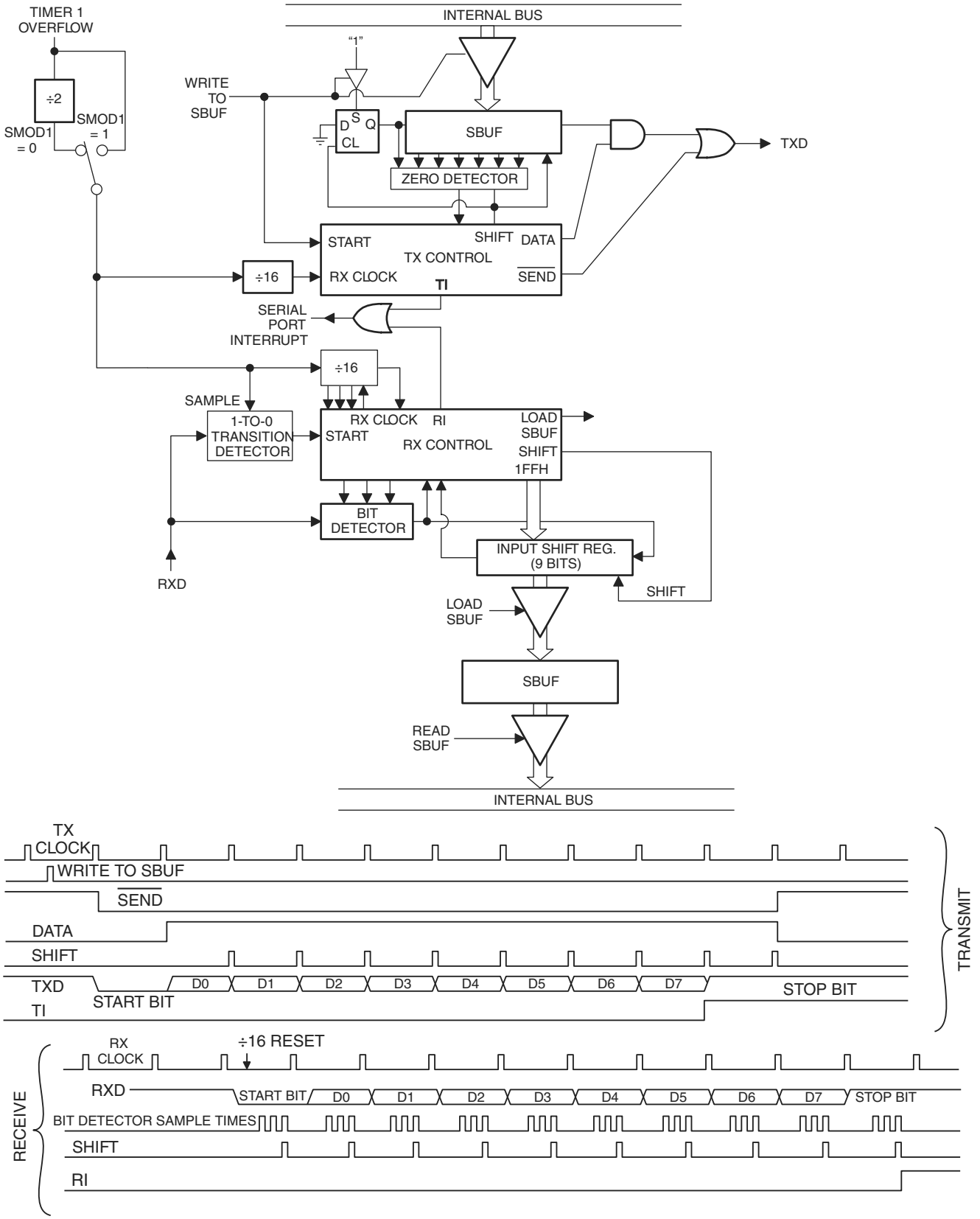
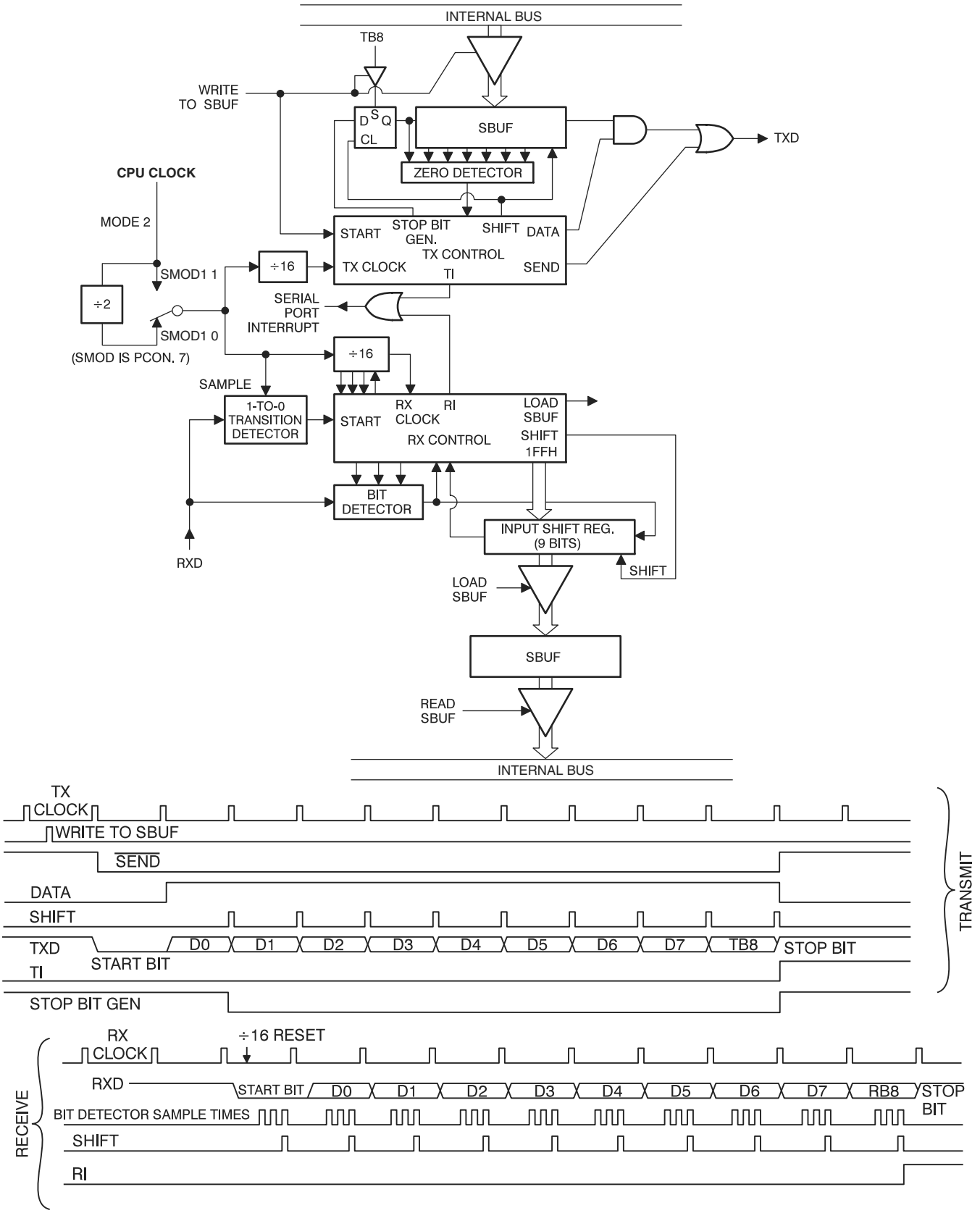


Figure 18-3. Serial Port Mode 2



In a more complex system the following could be used to select slaves 1 and 2 while excluding slave 0:

Slave 0 SADDR = 1100 0000

SADEN = 1111 1001

Given = 1100 0XX0

Slave 1 SADDR = 1110 0000

SADEN = 1111 1010

Given = 1110 0X0X

Slave 2 SADDR = 1110 0000

SADEN = 1111 1100

Given = 1110 00XX

In the above example the differentiation among the 3 slaves is in the lower 3 address bits. Slave 0 requires that bit 0 = 0 and it can be uniquely addressed by 1110 0110. Slave 1 requires that bit 1 = 0 and it can be uniquely addressed by 1110 and 0101. Slave 2 requires that bit 2 = 0 and its unique address is 1110 0011. To select Slaves 0 and 1 and exclude Slave 2, use address 1110 0100, since it is necessary to make bit 2 = 1 to exclude slave 2.

The Broadcast Address for each slave is created by taking the logic OR of SADDR and SADEN. Zeros in this result are treated as don't cares. In most cases, interpreting the don't cares as ones, the broadcast address will be FF hexadecimal.

Upon reset SADDR (SFR address 0A9H) and SADEN (SFR address 0B9H) are loaded with "0"s. This produces a given address of all "don't cares" as well as a Broadcast address of all "don't cares". This effectively disables the Automatic Addressing mode and allows the microcontroller to use standard 80C51-type UART drivers which do not make use of this feature.

19. Serial Peripheral Interface

The serial peripheral interface (SPI) allows high-speed synchronous data transfer between the AT89LP2052/LP4052 and peripheral devices or between multiple AT89LP2052/LP4052 devices. The AT89LP2052/LP4052 SPI features include the following:

- Full-duplex, 3-wire Synchronous Data Transfer
- Master or Slave Operation
- Maximum Bit Frequency = f/4
- LSB First or MSB First Data Transfer
- Four Programmable Bit Rates in Master Mode
- End of Transmission Interrupt Flag
- Write Collision Flag Protection
- Double-buffered Receive
- Double-buffered Transmit (Enhanced Mode Only)
- Wake up from Idle Mode (Slave Mode Only)

Table 19-2. SPSR – SPI Status Register

SPSR Address = AAH — Reset Value = 000X X000B

Not Bit Addressable

	SPIF	WCOL	LDEN	–	–	–	DISSO	ENH
Bit	7	6	5	4	3	2	1	0

Symbol	Function
SPIF	SP interrupt flag. When a serial transfer is complete, the SPIF bit is set and an interrupt is generated if SPIE = 1 and ES = 1. The SPIF bit is cleared by reading the SPI status register followed by reading/writing the SPI data register.
WCOL	When ENH = 0: Write collision flag. The WCOL bit is set if the SPI data register is written during a data transfer. During data transfer, the result of reading the SPDR register may be incorrect, and writing to it has no effect. The WCOL bit (and the SPIF bit) are cleared by reading the SPI status register followed by reading/writing the SPI data register. When ENH = 1: WCOL works in Enhanced mode as Tx Buffer Full. Writing during WCOL = 1 in enhanced mode will overwrite the waiting data already present in the Tx Buffer. In this mode, WCOL is no longer reset by the SPIF reset but is reset when the write buffer has been unloaded into the serial shift register.
LDEN	Load enable for the Tx buffer in enhanced SPI mode. When ENH is set, it is safe to load the Tx Buffer while LDEN = 1 and WCOL = 0. LDEN is high during bits 0 - 3 and is low during bits 4 - 7 of the SPI serial byte transmission time frame.
DISSO	Disable slave output bit. When set, this bit causes the MISO pin to be tri-stated so more than one slave device can share the same interface with a single master. Normally, the first byte in a transmission could be the slave address and only the selected slave should clear its DISSO bit.
ENH	Enhanced SPI mode select bit. When ENH = 0, SPI is in normal mode, i.e. without write double buffering. When ENH = 1, SPI is in enhanced mode with write double buffering. The Tx buffer shares the same address with the SPDR register.

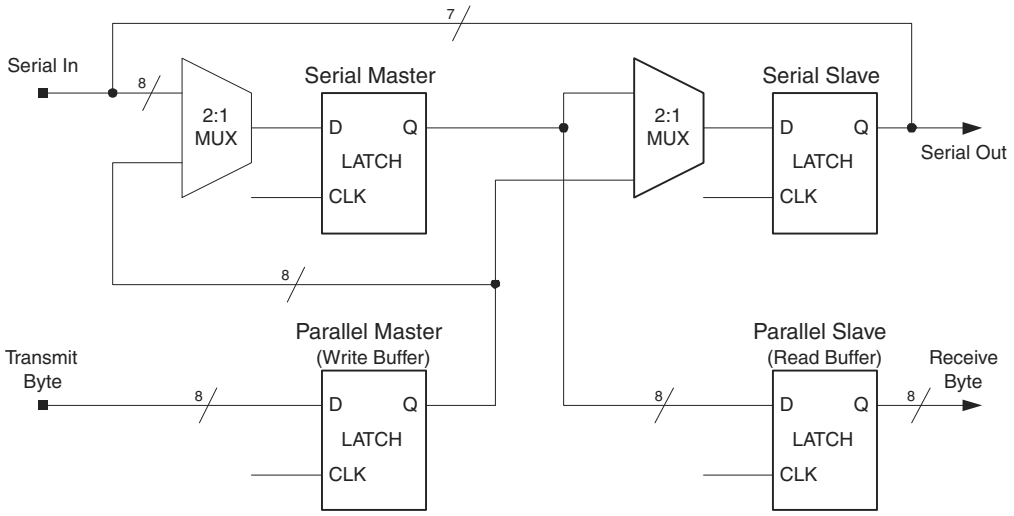
Table 19-3. SPDR – SPI Data Register

SPDR Address = 86H — Reset Value = 00H (after cold reset), unchanged (after warm reset)

Not Bit Addressable

	SPD7	SPD6	SPD5	SPD4	SPD3	SPD2	SPD1	SPD0
Bit	7	6	5	4	3	2	1	0

Figure 19-3. SPI Shift Register Diagram



19.3 Serial Clock Generator

The CPHA (Clock PHAse), CPOL (Clock POLarity), and SPR (Serial Peripheral clock Rate = baud rate) bits in SPCR control the shape and rate of SCK. The two SPR bits provide four possible clock rates when the SPI is in master mode. In slave mode, the SPI will operate at the rate of the incoming SCK as long as it does not exceed the maximum bit rate. There are also four possible combinations of SCK phase and polarity with respect to the serial data. CPHA and CPOL determine which format is used for transmission. The SPI data transfer formats are shown in Figures 19-4 and and 19-5. To prevent glitches on SCK from disrupting the interface, CPHA, CPOL, and SPR should be set up before the interface is enabled, and the master device should be enabled before the slave device(s).

Table 22-3. Detailed Logical Instruction Summary

Logical Instruction	Bytes	Clock Cycles		Hex Code
		8051	LP2052	
CLR A	1	12	1	E4
CPL A	1	12	1	F4
ANL A, Rn	1	12	1	58-5F
ANL A, direct	2	12	2	55
ANL A, @Ri	1	12	2	56-57
ANL A, #data	2	12	2	54
ANL direct, A	2	12	2	52
ANL direct, #data	3	24	3	53
ORL A, Rn	1	12	1	48-4F
ORL A, direct	2	12	2	45
ORL A, @Ri	1	12	2	46-47
ORL A, #data	2	12	2	44
ORL direct, A	2	12	2	42
ORL direct, #data	3	24	3	43
XRL A, Rn	1	12	1	68-6F
XRL A, direct	2	12	2	65
XRL A, @Ri	1	12	2	66-67
XRL A, #data	2	12	2	64
XRL direct, A	2	12	2	62
XRL direct, #data	3	24	3	63
RL A	1	12	1	23
RLC A	1	12	1	33
RR A	1	12	1	03
RRC A	1	12	1	13
SWAP A	1	12	1	C4

23. Programming the Flash Memory

The AT89LP2052/LP4052 offers 2/4K bytes of In-System Programmable (ISP) non-volatile Flash code memory. In addition, the device contains a 32-byte User Signature Row and a 32-byte read-only Atmel Signature Row. The memory organization is shown in Table 23-1. The Memory is divided into pages of 32 bytes each. A single read or write command may only access a single page in the memory.

Table 23-1. Memory Organization

Device #	Code Size	Page Size	# Pages	Address Range
AT89LP2052	2K bytes	32 bytes	64	0000H - 07FFH
AT89LP4052	4K bytes	32 bytes	128	0000H - 0FFFH

The AT89LP2052/LP4052 provides two flexible interfaces for programming the Flash memory: a parallel interface which uses 10 pins; and a serial interface which uses the 4 SPI pins. The parallel and serial programming algorithms are identical. Both interfaces support the same command format where each command is issued to the device one byte at a time. Commands consist of a preamble byte for noise immunity, an opcode byte, two address bytes, and from 1 to 32 data bytes. Figure 23-1 shows a simplified flow chart of a command sequence.

Figure 23-1. Command Sequence Flow Chart

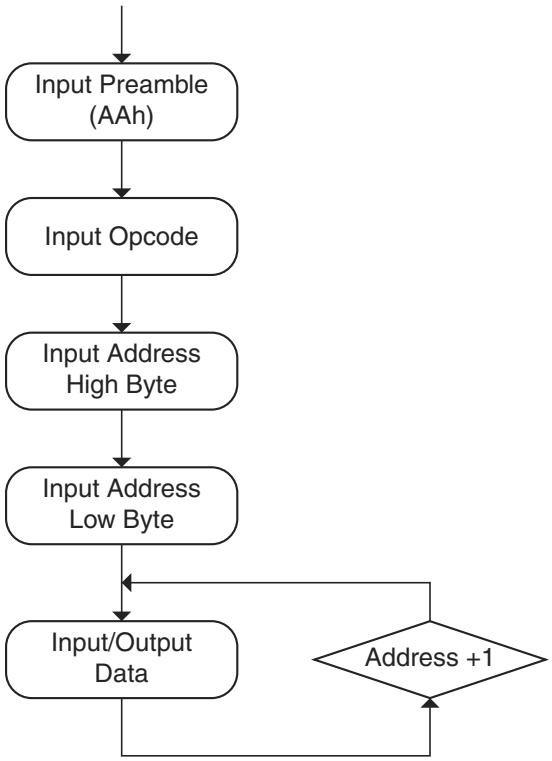
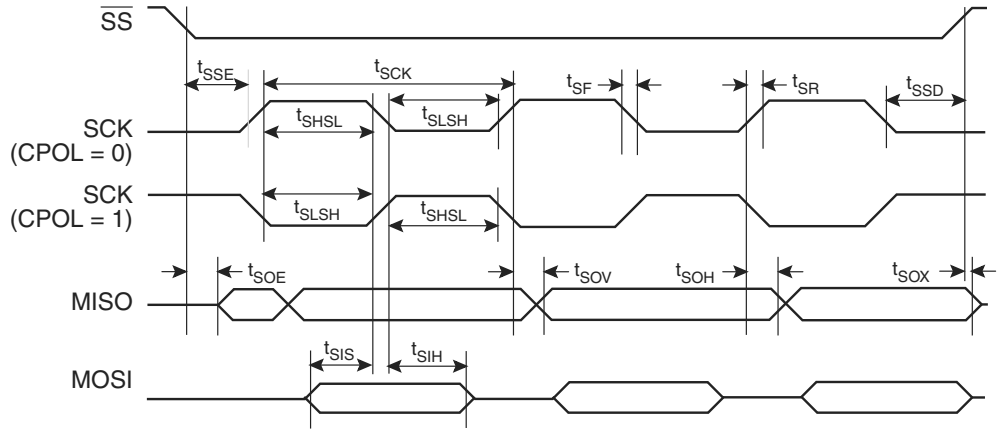


Figure 24-4. SPI Slave Timing (CPHA = 1)



24.4 External Clock Drive

Figure 24-5. External Clock Drive Waveform

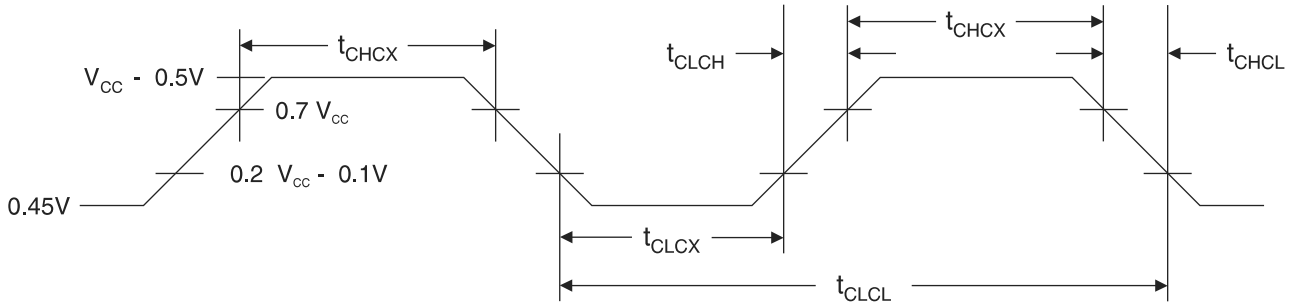
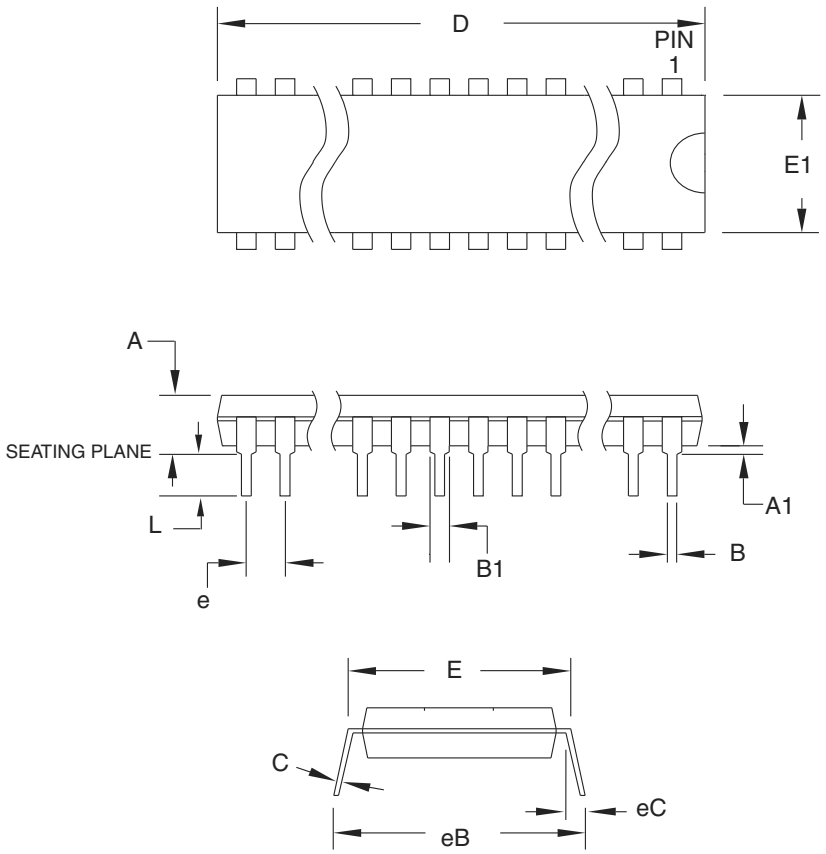


Table 24-3. External Clock Drive Parameters

Symbol	Parameter	V_{CC} = 2.4V to 5.5V		Units
		Min	Max	
$1/t_{CLCL}$	Oscillator Frequency	0	20	MHz
t_{CLCL}	Clock Period	50		ns
t_{CHCX}	High Time	12		ns
t_{CLCX}	Low Time	12		ns
t_{CLCH}	Rise Time		5	ns
t_{CHCL}	Fall Time		5	ns

26. Packaging Information

26.1 20P3 – PDIP



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	5.334	
A1	0.381	–	–	
D	24.892	–	26.924	Note 2
E	7.620	–	8.255	
E1	6.096	–	7.112	Note 2
B	0.356	–	0.559	
B1	1.270	–	1.551	
L	2.921	–	3.810	
C	0.203	–	0.356	
eB	–	–	10.922	
eC	0.000	–	1.524	
e	2.540 TYP			

Notes: 1. This package conforms to JEDEC reference MS-001, Variation AD.
2. Dimensions D and E1 do not include mold Flash or Protrusion. Mold Flash or Protrusion shall not exceed 0.25 mm (0.010").

1/23/04

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**20P3**, 20-lead (0.300"/7.62 mm Wide) Plastic Dual Inline Package (PDIP)	20P3	D

Table of Contents

Headquarters

Atmel Corporation
2325 Orchard Parkway
San Jose, CA 95131
USA
Tel: 1(408) 441-0311
Fax: 1(408) 487-2600

International

Atmel Asia
Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimshatsui
East Kowloon
Hong Kong
Tel: (852) 2721-9778
Fax: (852) 2722-1369

Atmel Europe
Le Krebs
8, Rue Jean-Pierre Timbaud
BP 309
78054 Saint-Quentin-en-
Yvelines Cedex
France
Tel: (33) 1-30-60-70-00
Fax: (33) 1-30-60-71-11

Atmel Japan
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
Tel: (81) 3-3523-3551
Fax: (81) 3-3523-7581

Product Contact

Web Site
www.atmel.com

Technical Support
mcu@atmel.com

Sales Contact
www.atmel.com/contacts

Literature Requests
www.atmel.com/literature