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Applications of "Embedded - Microcontrollers"

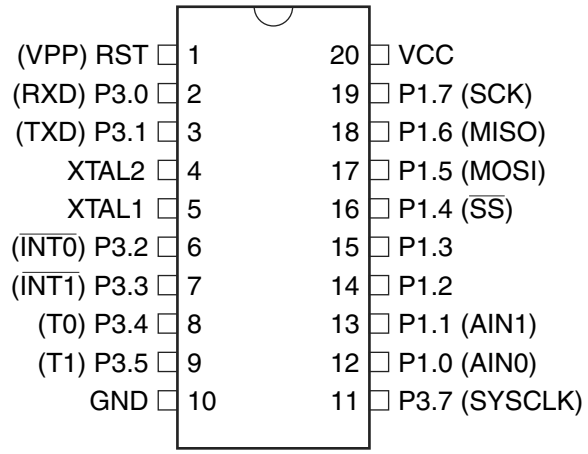
Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	16MHz
Connectivity	SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	15
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at89lp4052-16xi

The two timer/counters in the AT89LP2052/LP4052 are enhanced with two new modes. Mode 0 can be configured as a variable 9- to 16-bit timer/counter and Mode 1 can be configured as a 16-bit auto-reload timer/counter. In addition both timer/counters may be configured as 8-bit Pulse Width Modulators with 8-bit prescalers.

The I/O ports of the AT89LP2052/LP4052 can be independently configured in one of four operating modes. In quasi-bidirectional mode, the ports operate as in the classic 8051. In input mode, the ports are tri-stated. Push-pull output mode provides full CMOS drivers and open-drain mode provides just a pull-down.

2. Pin Configuration

2.1 20-lead PDIP/SOIC/TSSOP



7.7 I/O Ports

The I/O ports of the AT89LP2052/LP4052 may be configured in four different modes. On the AT89LP2052/LP4052, all the I/O ports revert to input-only (tri-stated) mode at power-up or reset. In the standard 8051, all ports are weakly pulled high during power-up or reset. To enable 8051-like ports, the ports must be put into quasi-bidirectional mode by clearing the P1M0 and P3M0 SFRs.

7.8 Reset

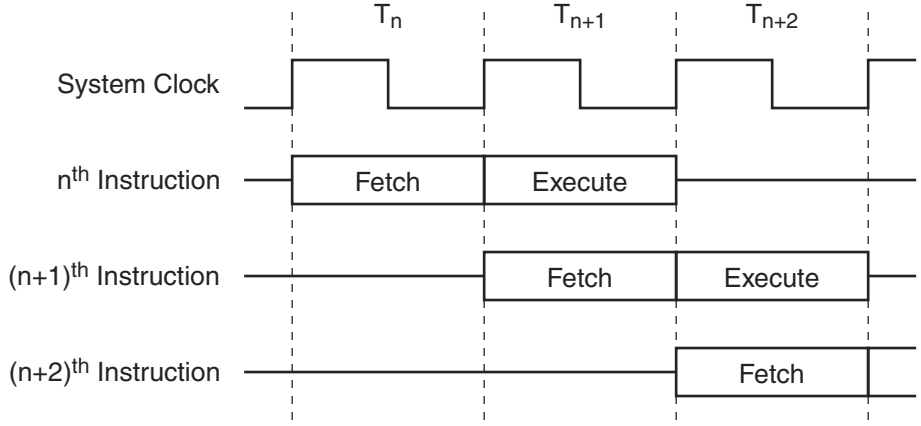
The RST pin in the AT89LP2052/LP4052 has different pulse width requirements than the standard 8051. The RST pin is sampled every clock cycle and must be held **high** for a minimum of two clock cycles, instead of 24 clock cycles, to be recognized as a valid reset pulse

8. Enhanced CPU

The AT89LP2052/LP4052 uses an enhanced 8051 CPU that runs at 6 to 12 times the speed of standard 8051 devices (or 3 to 6 times the speed of X2-mode 8051 devices). The increase in performance is due to two factors. First, the CPU fetches one instruction byte from the code memory every clock cycle. Second, the CPU uses a simple two-stage pipeline to fetch and execute instructions in parallel. This basic pipelining concept allows the CPU to obtain up to 1 MIPS per MHz. A simple example is shown in Figure 8-1.

The MCS-51 instruction set allows for instructions of variable length from 1 to 3 bytes. In a single-clock-per-byte-fetch system this means each instruction takes at least as many clocks as it has bytes to execute. A majority of the instructions in the AT89LP2052/LP4052 follow this rule: the instruction execution time in clock cycles equals the number of bytes per instruction with a few exceptions. Branches and Calls require an additional cycle to compute the target address and some other complex instructions require multiple cycles. See Section 22. “Instruction Set Summary” on page 52 for more detailed information on individual instructions. Figures 8-2 and 8-3 show examples of one- and two-byte instructions.

Figure 8-1. Parallel Instruction Fetches and Executions



9. Restrictions on Certain Instructions

The AT89LP2052/LP4052 is an economical and cost-effective member of Atmel's growing family of microcontrollers. It contains 2/4K bytes of Flash program memory. It is fully compatible with the MCS-51 architecture, and can be programmed using the MCS-51 instruction set. However, there are a few considerations one must keep in mind when utilizing certain instructions to program this device. All the instructions related to jumping or branching should be restricted such that the destination address falls within the physical program memory space of the device, which is 2K bytes for the AT89LP2052 and 4K bytes for the AT89LP4052. This should be the responsibility of the software programmer. For example, LJMP 7E0H would be a valid instruction for the AT89LP2052 (with 2K bytes of memory), whereas LJMP 900H would not.

9.1 Branching Instructions

The LCALL, LJMP, ACALL, AJMP, SJMP, and JMP @A+DPTR unconditional branching instructions will execute correctly as long as the programmer keeps in mind that the destination branching address must fall within the physical boundaries of the program memory size (locations 000H to 7FFH for the AT89LP2052, 000H to FFFH for the AT89LP4052). Violating the physical space limits may cause unknown program behavior. With the CJNE [...], DJNZ [...], JB, JNB, JC, JNC, JBC, JZ, and JNZ conditional branching instructions, the same previous rule applies. Again, violating the memory boundaries may cause erratic execution. For applications involving interrupts, the normal interrupt service routine address locations of the 8051 family architecture have been preserved.

9.2 MOVX-related Instructions, Data Memory

External DATA memory access is not supported in this device, nor is external PROGRAM memory execution. Therefore, no MOVX [...] instructions should be included in the program. A typical 8051 assembler will still assemble instructions, even if they are written in violation of the restrictions mentioned above. It is the responsibility of the user to know the physical features and limitations of the device being used and to adjust the instructions used accordingly.

10. System Clock

The system clock is generated directly from one of two selectable clock sources. The two sources are the on-chip crystal oscillator and external clock source. No internal clock division is used to generate the CPU clock from the system clock.

10.1 Crystal Oscillator

When enabled, the internal inverting oscillator amplifier is connected between XTAL1 and XTAL2 for connection to an external quartz crystal or ceramic resonator. When using the crystal oscillator, XTAL2 should not be used to drive a board-level clock.

10.2 External Clock Source

The external clock option is selected by setting the Oscillator Bypass fuse. This disables the amplifier and allows XTAL1 to be driven directly by the clock source. XTAL2 may be left unconnected.

10.3 System Clock Out

When the System Clock Out fuse is enabled, P3.7 will output the system clock with no division using the push-pull output mode. During Power-down the system clock will output as “1”.

13.1 Idle Mode

Setting the IDL bit in PCON enters Idle mode. Idle mode halts the internal CPU clock. The CPU state is preserved in its entirety, including the RAM, stack pointer, program counter, program status word, and accumulator. The Port pins hold the logic states they had at the time that Idle was activated. Idle mode leaves the peripherals running in order to allow them to wake up the CPU when an interrupt is generated. The Timer, UART and SPI blocks continue to function during Idle. The comparator and watchdog may be selectively enabled or disabled during Idle. Any enabled interrupt source or reset may terminate Idle mode. When exiting Idle mode with an interrupt, the interrupt will immediately be serviced, and following RETI the next instruction to be executed will be the one following the instruction that put the device into Idle.

13.2 Power-down Mode

Setting the Power-down (PD) bit in PCON enters Power-down mode. Power-down mode stops the oscillator and powers down the Flash memory in order to minimize power consumption. Only the power-on circuitry will continue to draw power during Power-down. During Power-down, the power supply voltage may be reduced to the RAM keep-alive voltage. The RAM contents will be retained, but the SFR contents are not guaranteed once V_{CC} has been reduced. Power-down may be exited by external reset, power-on reset, or certain interrupts.

The user should not attempt to enter (or re-enter) the power-down mode for a minimum of 4 µs until after one of the following conditions has occurred: Start of code execution (after any type of reset), or Exit from power-down mode.

13.2.1 Interrupt Recovery from Power-down

Two external interrupts may be configured to terminate Power-down mode. Pins P3.2 and P3.3 may be used to exit Power-down through external interrupts $\overline{INT0}$ and $\overline{INT1}$. To wake up by external interrupts $\overline{INT0}$ or $\overline{INT1}$, that interrupt must be enabled and configured for level-sensitive operation. If configured as inputs, $\overline{INT0}$ and $\overline{INT1}$ should not be left floating during Power-down even if interrupt recovery is not used.

When terminating Power-down by an interrupt, two different wake-up modes are available. When PWDEX in PCON is zero, the wake-up period is internally timed. At the falling edge on the interrupt pin, Power-down is exited, the oscillator is restarted, and an internal timer begins counting. The internal clock will not be allowed to propagate to the CPU until after the timer has counted for nominally 2 ms. After the time-out period the interrupt service routine will begin. The interrupt pin may be held low until the device has timed out and begun executing, or it may return high before the end of the time-out period. If the pin remains low, the service routine should disable the interrupt before returning to avoid re-triggering the interrupt.

When PWDEX = “1”, the wake-up period is controlled externally by the interrupt. Again, at the falling edge on the interrupt pin, Power-down is exited and the oscillator is restarted. However, the internal clock will not propagate until the rising edge of the interrupt pin. The interrupt should be held low long enough for the selected clock source to stabilize.

13.2.2 Reset Exit from Power-down

The wake-up from Power-down through an external reset is similar to the interrupt with PWDEX = “0”. At the rising edge of RST, Power-down is exited, the oscillator is restarted, and an internal timer begins counting. The internal clock will not be allowed to propagate to the CPU until after the timer has counted for nominally 2 ms. The RST pin must be held high for longer than the time-out period to ensure that the device is reset properly. The device will begin executing once RST is brought back low.

Table 14-4. IPH – Interrupt Priority High Register

IPH = B7H — Reset Value = X0X0 0000B

Not Bit Addressable

	–	PCH	–	PSH	PT1H	PX1H	PT0H	PX0H
Bit	7	6	5	4	3	2	1	0

Symbol	Function
PCH	Comparator Interrupt Priority High
PSH	Serial Port Interrupt Priority High
PT1H	Timer 1 Interrupt Priority High
PX1H	External Interrupt 1 Priority High
PT0H	Timer 0 Interrupt Priority High
PX0H	External Interrupt 0 Priority High

15. I/O Ports

All 15 port pins on the AT89LP2052/LP4052 may be configured to one of four modes: quasi-bidirectional (standard 8051 port outputs), push-pull output, open-drain output, or input-only. Port modes may be assigned in software on a pin-by-pin basis as shown in Table 15-1. All port pins default to input-only mode after reset. Each port pin also has a Schmitt-triggered input for improved input noise rejection. During Power-down all the Schmitt-triggered inputs are disabled with the exception of P3.2 and P3.3, which may be used to wake-up the device. Therefore P3.2 and P3.3 should not be left floating during Power-down.

Table 15-1. Configuration Modes for Port x, Bit y

PxM0.y	PxM1.y	Port Mode
0	0	Quasi-bidirectional
0	1	Push-pull Output
1	0	Input Only (High Impedance)
1	1	Open-Drain Output

15.1 Quasi-bidirectional Output

Port pins in quasi-bidirectional output mode function similar to standard 8051 port pins. A Quasi-bidirectional port can be used both as an input and output without the need to reconfigure the port. This is possible because when the port outputs a logic high, it is weakly driven, allowing an external device to pull the pin low. When the pin is driven low, it is driven strongly and able to sink a large current. There are three pull-up transistors in the quasi-bidirectional output that serve different purposes.

One of these pull-ups, called the “very weak” pull-up, is turned on whenever the port register for the pin contains a logic “1”. This very weak pull-up sources a very small current that will pull the pin high if it is left floating.

Table 16-2. TMOD: Timer/Counter Mode Control Register

TMOD = 89H — Reset Value = 0000 0000B

Not Bit Addressable

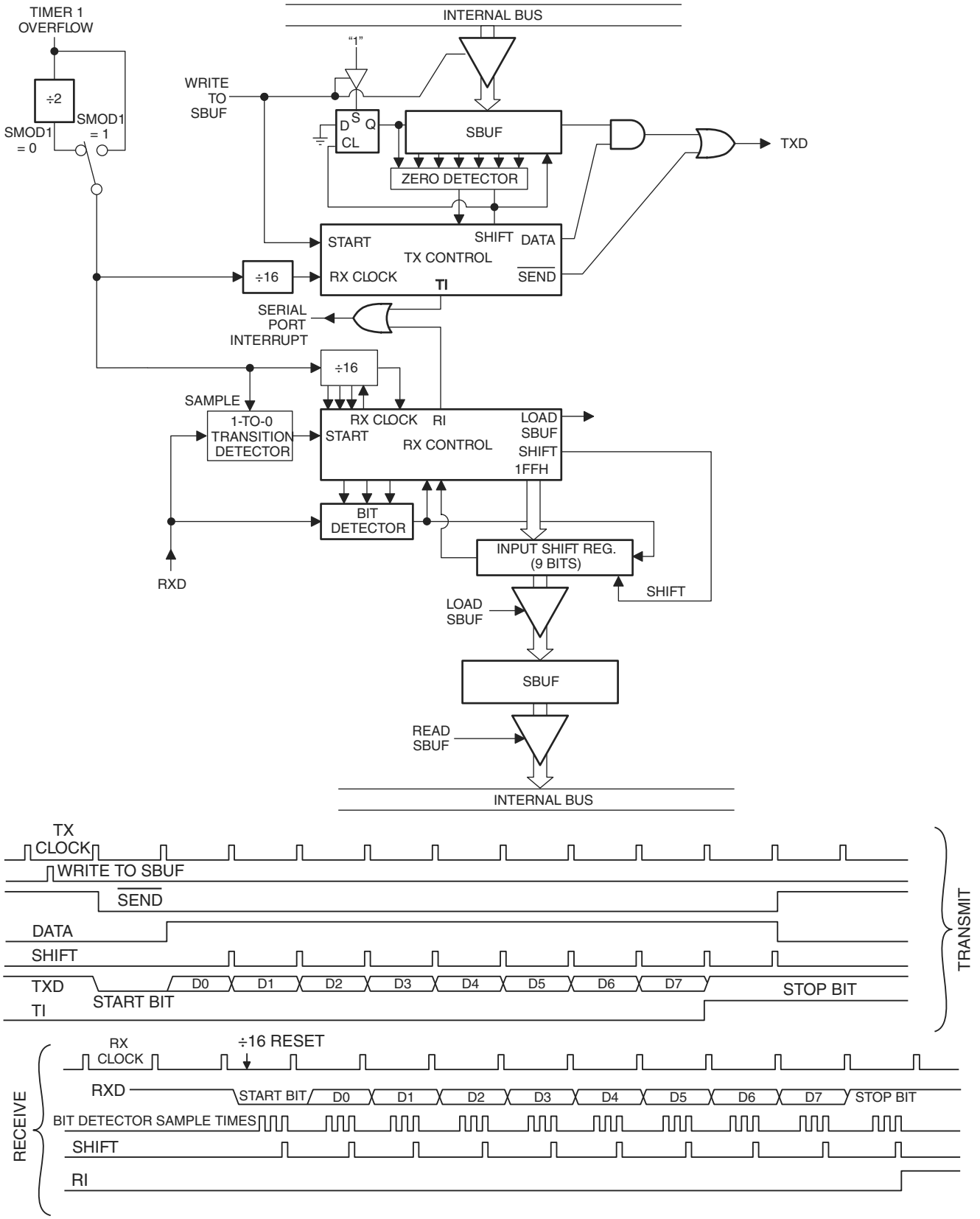
GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0
7	$\overline{6}$	5	4	3	$\overline{2}$	1	0
Timer1				**Timer0**			

Gate	Gating control: when set Timer/Counter x is enabled only while $\overline{INTx}$ pin is high and TRx control pin is set. When cleared, Timer x is enabled whenever TRx control bit is set.	Timer 0 gate bit
C/$\overline{T}$	Timer or Counter Selector: cleared for Timer operation (input from internal system clock). Set for Counter operation (input from Tx input pin).	Timer 0 counter/timer select bit
M1	Mode bit 1	Timer 0 M1 bit
M0	Mode bit 0	Timer 0 M0 bit

M1	M0	Mode	Operating Mode
0	0	0	Variable 9 - 16-bit Timer/Counter. 8-bit Timer/Counter THz with TLx as 1 - 8-bit prescaler.
0	1	1	16-bit Auto Reload Timer/Counter. 8-bit Timer/Counters THx and TLx are cascaded; there is no prescaler.
1	0	2	8-bit Auto Reload Timer/Counter. 8-bit auto-reload Timer/Counter THx holds a value which is to be reloaded into TLx each time it overflows.
1	1	3	Split Timer/Counter. (Timer 0) TL0 is an 8-bit Timer/Counter controlled by the standard Timer 0 control bits. TH0 is an 8-bit timer only controlled by Timer 1 control bits.
1	1	3	(Timer 1) Timer/Counter 1 stopped.

Timer SFR	Purpose	Address	Bit-Addressable
TCON	Control	88H	Yes
TMOD	Mode	89H	No
TL0	Timer 0 low-byte	8AH	No
TL1	Timer 1 low-byte	8BH	No
TH0	Timer 0 high-byte	8CH	No
TH1	Timer 1 high-byte	8DH	No
TCONB	Mode	91H	No
RL0	Timer 0 reload low-byte	92H	No
RL1	Timer 1 reload low-byte	93H	No
RH0	Timer 0 reload high-byte	94H	No
RH1	Timer 1 reload high-byte	95H	No

Figure 18-2. Serial Port Mode 1



18.5 More About Modes 2 and 3

Eleven bits are transmitted (through TXD), or received (through RXD): a start bit (0), 8 data bits (LSB first), a programmable ninth data bit, and a stop bit (1). On transmit, the ninth data bit (TB8) can be assigned the value of “0” or “1”. On receive, the ninth data bit goes into RB8 in SCON. The baud rate is programmable to either 1/16 or 1/32 of the oscillator frequency in Mode 2. Mode 3 may have a variable baud rate generated from Timer 1.

Figures 18-3 and 18-4 show a functional diagram of the serial port in Modes 2 and 3. The receive portion is exactly the same as in Mode 1. The transmit portion differs from Mode 1 only in the ninth bit of the transmit shift register.

Transmission is initiated by any instruction that uses SBUF as a destination register. The “write to SBUF” signal also loads TB8 into the ninth bit position of the transmit shift register and flags the TX Control unit that a transmission is requested. Transmission commences at S1P1 of the machine cycle following the next rollover in the divide-by-16 counter. Thus, the bit times are synchronized to the divide-by-16 counter, not to the “write to SBUF” signal.

The transmission begins when $\overline{\text{SEND}}$ is activated, which puts the start bit at TXD. One bit time later, DATA is activated, which enables the output bit of the transmit shift register to TXD. The first shift pulse occurs one bit time after that. The first shift clocks a “1” (the stop bit) into the ninth bit position of the shift register. Thereafter, only “0”s are clocked in. Thus, as data bits shift out to the right, “0”s are clocked in from the left. When TB8 is at the output position of the shift register, then the stop bit is just to the left of TB8, and all positions to the left of that contain “0”s. This condition flags the TX Control unit to do one last shift, then deactivate SEND and set TI. This occurs at the 11th divide-by-16 rollover after “write to SBUF.”

Reception is initiated by a 1-to-0 transition detected at RXD. For this purpose, RXD is sampled at a rate of 16 times the established baud rate. When a transition is detected, the divide-by-16 counter is immediately reset, and 1FFH is written to the input shift register.

At the seventh, eighth and ninth counter states of each bit time, the bit detector samples the value of RXD. The value accepted is the value that was seen in at least 2 of the 3 samples. If the value accepted during the first bit time is not 0, the receive circuits are reset and the unit continues looking for another 1-to-0 transition. If the start bit proves valid, it is shifted into the input shift register, and reception of the rest of the frame proceeds.

As data bits come in from the right, “1”s shift out to the left. When the start bit arrives at the left most position in the shift register (which in Modes 2 and 3 is a 9-bit register), it flags the RX Control block to do one last shift, load SBUF and RB8, and set RI. The signal to load SBUF and RB8 and to set RI is generated if, and only if, the following conditions are met at the time the final shift pulse is generated:

RI = 0, and

Either SM2 = 0 or the received 9th data bit = 1

If either of these conditions is not met, the received frame is irretrievably lost, and RI is not set. If both conditions are met, the received ninth data bit goes into RB8, and the first 8 data bits go into SBUF. One bit time later, whether the above conditions were met or not, the unit continues looking for a 1-to-0 transition at the RXD input.

Note that the value of the received stop bit is irrelevant to SBUF, RB8, or RI.

The interconnection between master and slave CPUs with SPI is shown in Figure 19-1. The four pins in the interface are Master-In/Slave-Out (MISO), Master-Out/Slave-In (MOSI), Shift Clock (SCK), and Slave Select ($\overline{SS}$). The SCK pin is the clock output in master mode, but is the clock input in slave mode. The MSTR bit in SPCR determines the directions of MISO and MOSI. Also notice that MOSI connects to MOSI and MISO to MISO. In master mode, $\overline{SS}$/P1.4 is ignored and may be used as a general-purpose input or output. In slave mode, $\overline{SS}$ must be driven low to select an individual device as a slave. When $\overline{SS}$ is driven high, the slave's SPI port is deactivated and the MOSI/P1.5 pin can be used as a general-purpose input.

Figure 19-1. SPI Master-Slave Interconnection

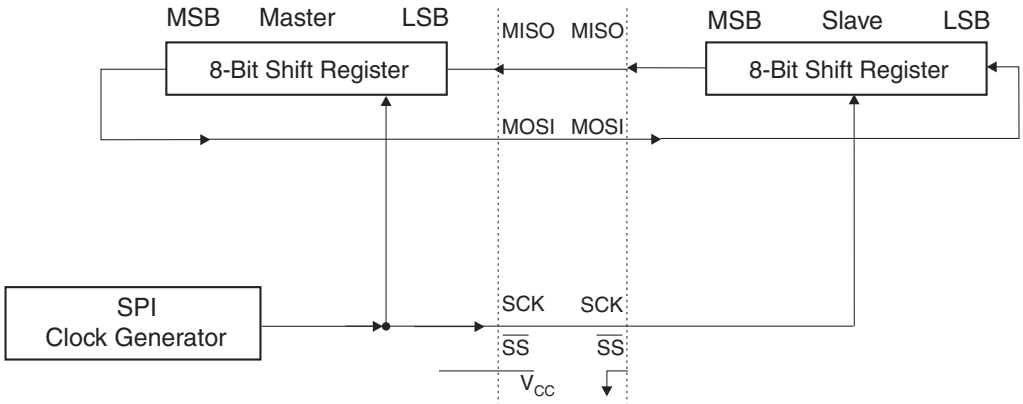


Figure 19-2. SPI Block Diagram

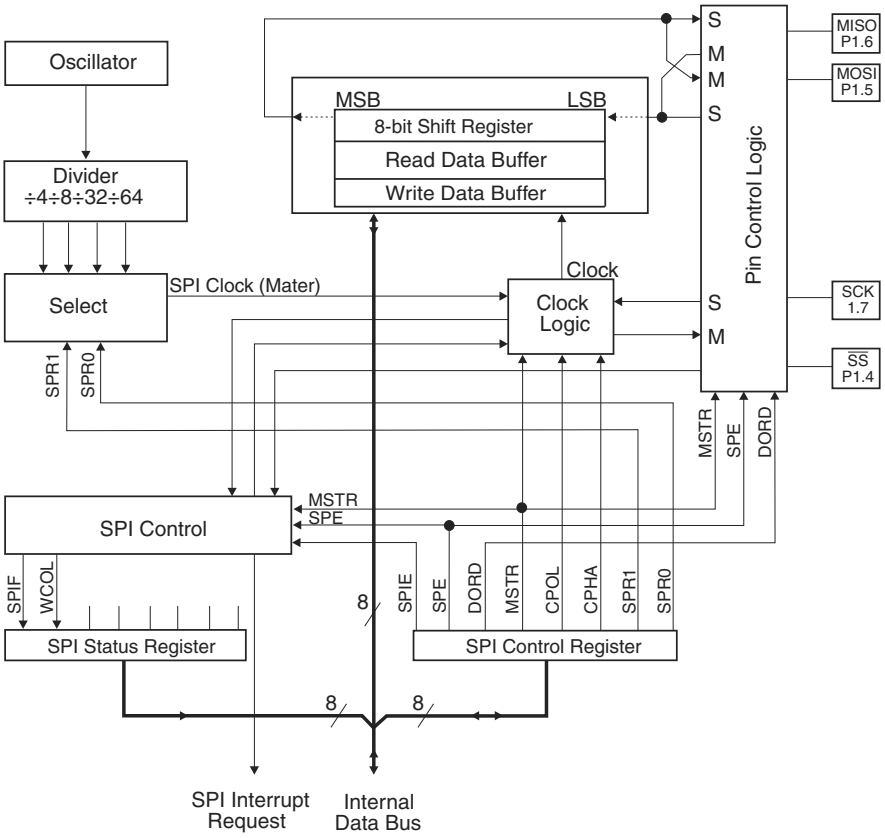


Table 19-1. SPCR – SPI Control Register

SPCR Address = D5H — Reset Value = 0000 0000B

Not Bit Addressable

	SPIE	SPE	DORD	MSTR	CPOL	CPHA	SPR1	SPR0
Bit	7	6	5	4	3	2	1	0

Symbol	Function
SPIE	SPI interrupt enable. This bit, in conjunction with the ES bit in the IE register, enables SPI interrupts: SPIE = 1 and ES = 1 enable SPI interrupts. SPIE = 0 disables SPI interrupts.
SPE	SPI enable. SPE = 1 enables the SPI channel and connects $\overline{SS}$, MOSI, MISO and SCK to pins P1.4, P1.5, P1.6, and P1.7. SPE = 0 disables the SPI channel.
DORD	Data order. DORD = 1 selects LSB first data transmission. DORD = 0 selects MSB first data transmission.
MSTR	Master/slave select. MSTR = 1 selects Master SPI mode. MSTR = 0 selects slave SPI mode.
CPOL	Clock polarity. When CPOL = 1, SCK is high when idle. When CPOL = 0, SCK of the master device is low when not transmitting. Please refer to figure on SPI clock phase and polarity control.
CPHA	Clock phase. The CPHA bit together with the CPOL bit controls the clock and data relationship between master and slave. Please refer to figure on SPI clock phase and polarity control.
SPR0 SPR1	SPI clock rate select. These two bits control the SCK rate of the device configured as master. SPR1 and SPR0 have no effect on the slave. The relationship between SCK and the oscillator frequency, $F_{OSC.}$, is as follows: **SPR1 SPR0 SCK** 0 0 f/4 0 1 f/8 1 0 f/32 1 1 f/64

Notes:
1. Set up the clock mode before enabling the SPI: set all bits needed in SPCR except the SPE bit, then set SPE.
2. Enable the master SPI prior to the slave device.
3. Slave echoes master on the next Tx if not loaded with new data.

Table 19-2. SPSR – SPI Status Register

SPSR Address = AAH — Reset Value = 000X X000B

Not Bit Addressable

	SPIF	WCOL	LDEN	–	–	–	DISSO	ENH
Bit	7	6	5	4	3	2	1	0

Symbol	Function
SPIF	SP interrupt flag. When a serial transfer is complete, the SPIF bit is set and an interrupt is generated if SPIE = 1 and ES = 1. The SPIF bit is cleared by reading the SPI status register followed by reading/writing the SPI data register.
WCOL	When ENH = 0: Write collision flag. The WCOL bit is set if the SPI data register is written during a data transfer. During data transfer, the result of reading the SPDR register may be incorrect, and writing to it has no effect. The WCOL bit (and the SPIF bit) are cleared by reading the SPI status register followed by reading/writing the SPI data register. When ENH = 1: WCOL works in Enhanced mode as Tx Buffer Full. Writing during WCOL = 1 in enhanced mode will overwrite the waiting data already present in the Tx Buffer. In this mode, WCOL is no longer reset by the SPIF reset but is reset when the write buffer has been unloaded into the serial shift register.
LDEN	Load enable for the Tx buffer in enhanced SPI mode. When ENH is set, it is safe to load the Tx Buffer while LDEN = 1 and WCOL = 0. LDEN is high during bits 0 - 3 and is low during bits 4 - 7 of the SPI serial byte transmission time frame.
DISSO	Disable slave output bit. When set, this bit causes the MISO pin to be tri-stated so more than one slave device can share the same interface with a single master. Normally, the first byte in a transmission could be the slave address and only the selected slave should clear its DISSO bit.
ENH	Enhanced SPI mode select bit. When ENH = 0, SPI is in normal mode, i.e. without write double buffering. When ENH = 1, SPI is in enhanced mode with write double buffering. The Tx buffer shares the same address with the SPDR register.

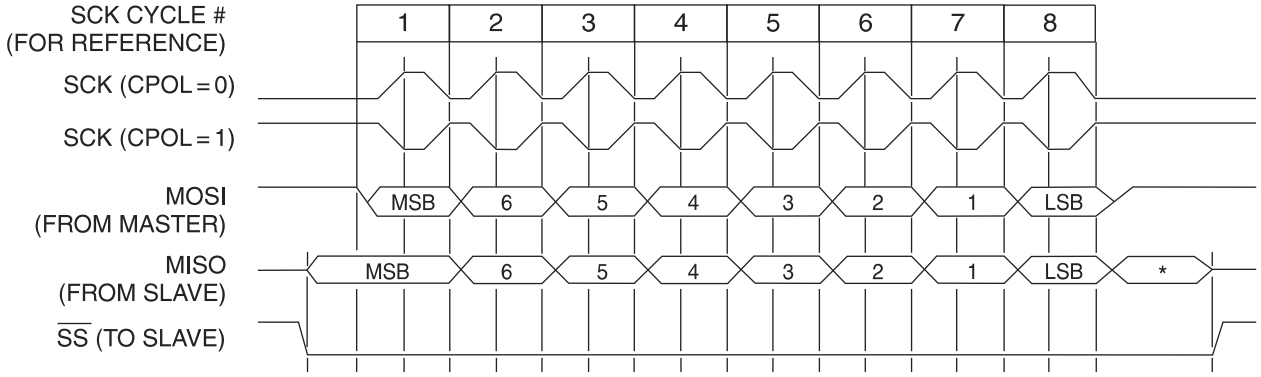
Table 19-3. SPDR – SPI Data Register

SPDR Address = 86H — Reset Value = 00H (after cold reset), unchanged (after warm reset)

Not Bit Addressable

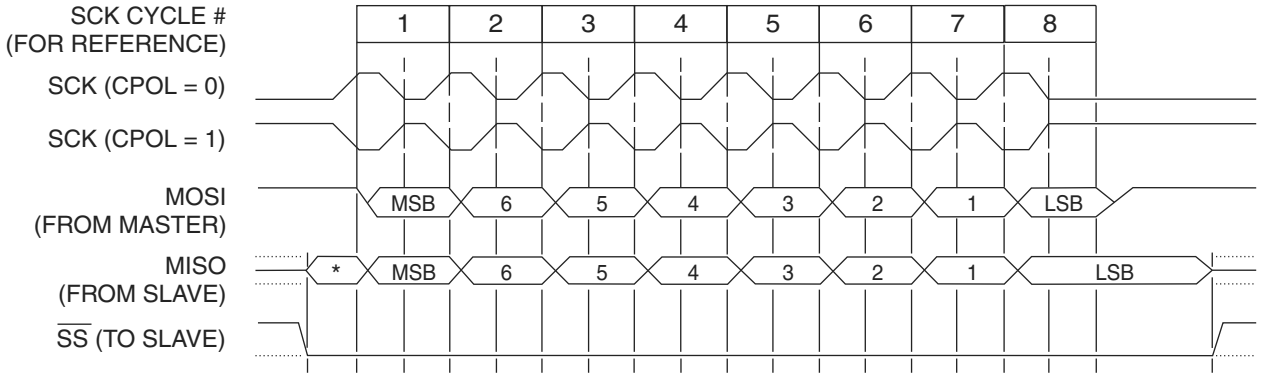
	SPD7	SPD6	SPD5	SPD4	SPD3	SPD2	SPD1	SPD0
Bit	7	6	5	4	3	2	1	0

Figure 19-4. SPI Transfer Format with CPHA = 0



Note: *Not defined but normally MSB of character just received

Figure 19-5. SPI Transfer Format with CPHA = 1



Note: *Not defined but normally LSB of previously transmitted character

19.4 SPI Pin Configuration

Before using the Serial Peripheral Interface the four SPI pins – SCK, MISO, MOSI and $\overline{SS}$ – must be properly configured for the desired functionality. See Section 15.7 “Port Alternate Functions” on page 23. When the SPI is in Master mode, SCK and MOSI must be configured as bidirectional or output, with P1.7 and P1.5 set to “1”. MISO should be input-only, or bidirectional with P1.6 set to “1”. When the SPI is in Slave mode, SCK, MOSI and SS must be configured as input-only, or as bidirectional with P1.7, P1.6 and P1.4 set to “1”. MISO should be set as bidirectional or output, with P1.6 set to “1”. If all four pins are set as bidirectional and their respectively port bits are all “1”, it is possible to switch between Master and Slave mode without reconfiguring the pins.

Table 22-4. Detailed Data Transfer Instruction Summary

Data Transfer Instruction	Bytes	Clock Cycles		Hex Code
		8051	LP2052	
MOV A, Rn	1	12	1	E8-EF
MOV A, direct	2	12	2	E5
MOV A, @Ri	1	12	2	E6-E7
MOV A, #data	2	12	2	74
MOV Rn, A	1	12	1	F8-FF
MOV Rn, direct	2	24	2	A8-AF
MOV Rn, #data	2	12	2	78-7F
MOV direct, A	2	12	2	F5
MOV direct, Rn	2	24	2	88-8F
MOV direct, direct	3	24	3	85
MOV direct, @Ri	2	24	2	86-87
MOV direct, #data	3	24	3	75
MOV @Ri, A	1	12	1	F6-F7
MOV @Ri, direct	2	24	2	A6-A7
MOV @Ri, #data	2	12	2	76-77
MOV DPTR, #data16	3	24	3	90
MOVC A, @A+DPTR	1	24	3	93
MOVC A, @A+PC	1	24	3	83
PUSH direct	2	24	2	C0
POP direct	2	24	2	D0
XCH A, Rn	1	12	1	C8-CF
XCH A, direct	2	12	2	C5
XCH A, @Ri	1	12	2	C6-C7
XCHD A, @Ri	1	12	2	D6-D7

Table 22-5. Detailed Bit Instruction Summary

Bit Instruction	Bytes	Clock Cycles		Hex Code
		8051	LP2052	
CLR C	1	12	1	C3
CLR bit	2	12	2	C2
SETB C	1	12	1	D3

23.2 Status Register

The current state of the memory may be accessed by reading the status register. The status register is shown in Table 23-2.

Table 23-2. Status Register

	–	–	–	–	$\overline{\text{LOAD}}$	SUCCESS	$\overline{\text{WRTINH}}$	$\overline{\text{BUSY}}$
Bit	7	6	5	4	3	2	1	0

Symbol	Function
$\overline{\text{LOAD}}$	Load flag. Cleared low by the load page buffer command and set high by the next memory write. This flag signals that the page buffer was previously loaded with data by the load page buffer command.
SUCCESS	Success flag. Cleared low at the start of a programming cycle and will only be set high if the programming cycle completes without interruption from the brownout detector.
$\overline{\text{WRTINH}}$	Write Inhibit flag. Cleared low by the brownout detector (BOD) whenever programming is inhibited due to V_{CC} falling below the minimum required programming voltage. If a BOD episode occurs during programming, the SUCCESS flag will remain low after the cycle is complete. $\overline{\text{WRTINH}}$ low also forces $\overline{\text{BUSY}}$ low.
$\overline{\text{BUSY}}$	Busy flag. Cleared low whenever the memory is busy programming or if write is currently inhibited.

23.3 $\overline{\text{DATA}}$ Polling

The AT89LP2052/LP4052 implements $\overline{\text{DATA}}$ polling to indicate the end of a programming cycle. While the device is busy, any attempted read of the last byte written will return the data byte with the MSB complemented. Once the programming cycle has completed, the true value will be accessible. During Erase the data is assumed to be FFH and $\overline{\text{DATA}}$ polling will return 7FH. When writing multiple bytes in a page, the $\overline{\text{DATA}}$ value will be the last data byte loaded before programming begins, not the written byte with the highest physical address within the page.

23.4 Parallel Programming

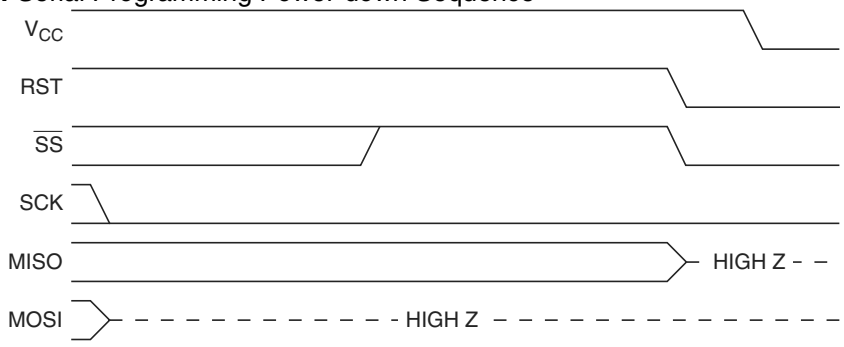
Parallel Programming Mode is enabled by applying V_{PP} to the RST pin. The connections required during parallel mode are shown in Figure 23-2. During parallel programming, Port 1 is configured as an 8-bit wide bidirectional command bus. Data on P1 is strobed by a positive pulse on the XTAL1 pin. No other clock is required. The interface is enabled by pulling $\overline{\text{CS}}$ (P3.2) low. P3.1 acts as RDY/$\overline{\text{BSY}}$, and will be pulled low to indicate that the device is busy regardless of the state of $\overline{\text{CS}}$.

23.5.2 Power-down Sequence

Execute this sequence to power-down the device **after** serial programming.

1. Tri-state MOSI (P1.5).
2. Bring SCK (P1.7) to “L”.
3. Bring RST to “L”.
4. Bring $\overline{SS}$ (P1.4) to “L”
5. Power off Vcc.

Figure 23-23. Serial Programming Power-down Sequence



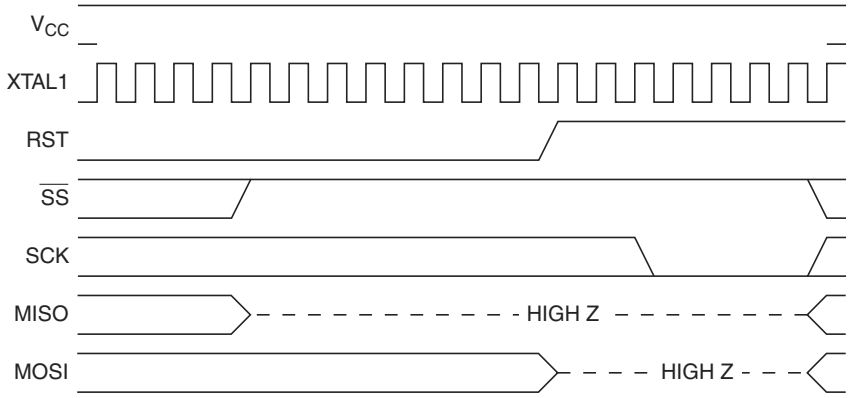
Note: The waveforms on this page are not to scale.

23.5.3 ISP Start Sequence

Execute this sequence to enter ISP when the device is **already** operational.

1. Bring $\overline{SS}$ (P1.4) to “H”.
2. Tri-state MISO (P1.6).
3. Bring RST to “H”.
4. Bring SCK (P1.7) to “L”.

Figure 23-24. In-System Programming (ISP) Start Sequence

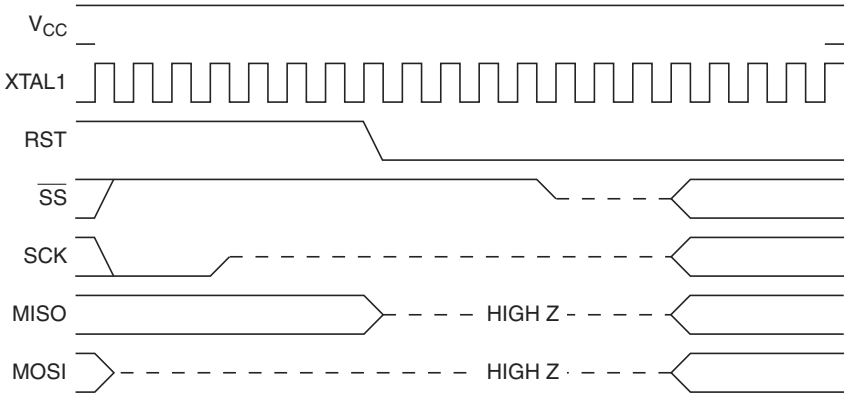


23.5.4 ISP Exit Sequence

Execute this sequence to exit ISP and resume execution.

1. Bring $\overline{SS}$ (P1.4) to “H”.
2. Tri-state MOSI (P1.5).
3. Tri-state SCK (P1.7).
4. Bring RST to “L”.
5. Tri-state $\overline{SS}$.

Figure 23-25. In-System Programming (ISP) Exit Sequence



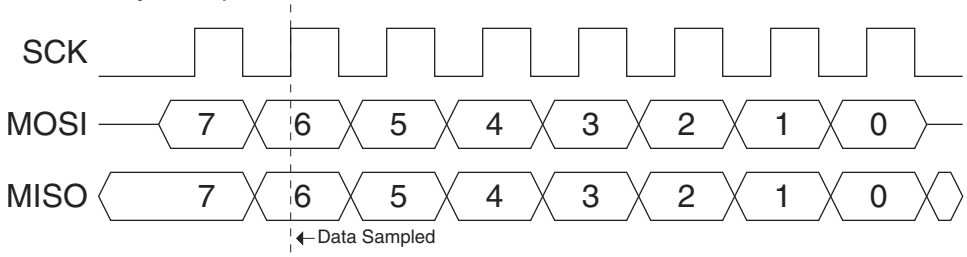
Note: The waveforms on this page are not to scale.

23.5.5 ISP Byte Sequence

The ISP byte sequence is shown in Figure 23-26.

- Data shifts in/out MSB first.
- MISO changes at **falling** edge of SCK.
- MOSI is sampled at **rising** edge of SCK.

Figure 23-26. ISP Byte Sequence



23.5.6 ISP Command Sequence

The ISP multi-byte command sequence is shown in Figure 23-27.

- $\overline{SS}$ should be brought low before the first byte in a command is sent and brought back high after the final byte in the command has been sent. The command is not complete until $\overline{SS}$ returns high.
- Command bytes are issued serially on MOSI (P1.5).
- Data bytes are output serially on MISO (P1.6).

Figure 23-27. ISP Command Sequence

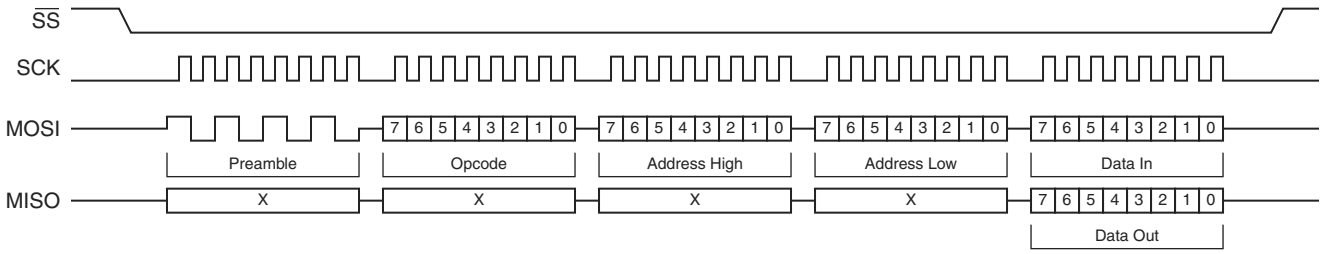
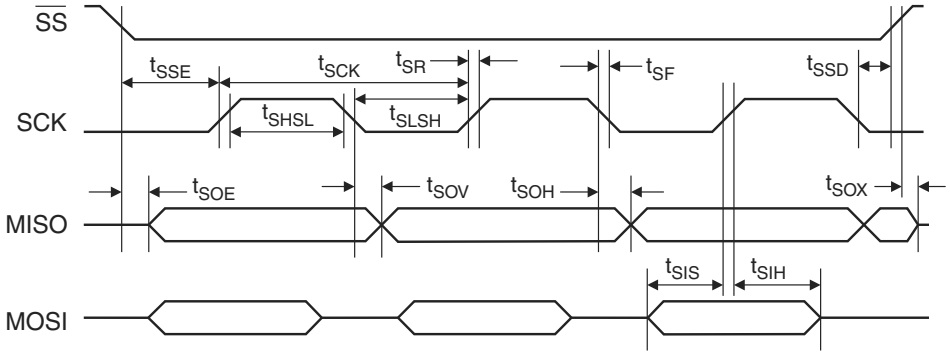


Table 23-4. Serial Programming Interface Parameters

Symbol	Parameter	Min	Max	Units
t_{SCK}	Serial Clock Cycle Time	200		ns
t_{SHSL}	Clock High Time	100		ns
t_{SLSH}	Clock Low Time	50		ns
t_{SR}	Rise Time		25	ns
t_{SF}	Fall Time		25	ns
t_{SIS}	Serial Input Setup Time	10		ns
t_{SIH}	Serial Input Hold Time	10		ns
t_{SOH}	Serial Output Hold Time		10	ns
t_{SOV}	Serial Output Valid Time		35	ns
t_{SOE}	Output Enable Time		10	ns
t_{SOX}	Output Disable Time		25	ns
t_{SSE}	$\overline{SS}$ Enable Lead Time	100		ns
t_{SSD}	$\overline{SS}$ Disable Lag Time	100		ns
t_{WRC}	Wire Cycle Time		4.5	ms
t_{ERS}	Erase Cycle Time		9	ms

Figure 23-28. Serial Programming Interface Timing



24. Electrical Characteristics

24.1 Absolute Maximum Ratings*

Operating Temperature	-40°C to +85°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-0.7V to +6.2V
Maximum Operating Voltage	5.5V
DC Output Current	15.0 mA

Note: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

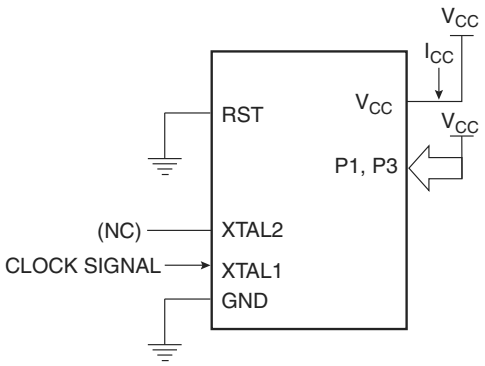
24.2 DC Characteristics

T_A = -40°C to 85°C, V_{CC} = 2.4V to 5.5V (unless otherwise noted)

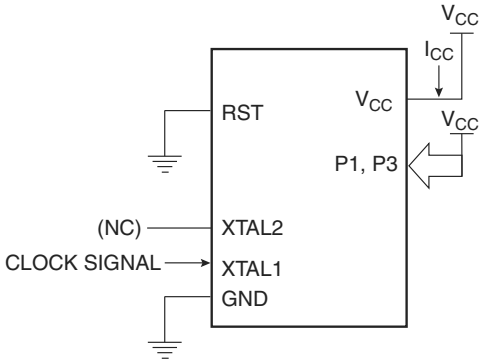
Symbol	Parameter	Condition	Min	Max	Units
V_{IL}	Input Low-voltage	(Except RST)	-0.5	0.25 V_{CC}	V
V_{IL1}	Input Low-voltage	(RST)	-0.5	0.3 V_{CC}	V
V_{IH}	Input High-voltage	(Except RST)	0.65 V_{CC}	V_{CC} + 0.5	V
V_{IH1}	Input High-voltage	(RST)	0.6 V_{CC}	V_{CC} + 0.5	V
V_{OL}	Output Low-voltage (Ports 1, 3)(1)	I_{OL} = 10 mA, V_{CC} = 2.7V, T_A = 85°C		0.5	V
V_{OH}	Output High-voltage (Ports 1, 3) using Weak Pull-up(2)	I_{OH} = -80 µA, V_{CC} = 5V ±10%	2.4		V
		I_{OH} = -30 µA	0.75 V_{CC}		V
		I_{OH} = -12 µA	0.9 V_{CC}		V
V_{OH1}	Output High-voltage (Ports 1, 3) using Strong Pull-up(3)	I_{OH} = -10 mA, T_A = 85°C	0.9 V_{CC}		
I_{IL}	Logic 0 Input Current(2) (Ports 1, 3)	V_{IN} = 0.45V		-50	µA
I_{TL}	Logic 1 to 0 Transition Current(2) (Ports 1, 3)	V_{IN} = 2V, V_{CC} = 5V ±10%		-300	µA
I_{LI}	Input-Only Leakage Current	0 < V_{IN} < V_{CC}		±10	µA
V_{OS}	Comparator Input Offset Voltage	V_{CC} = 5V		20	mV
V_{CM}	Comparator Input Common Mode Voltage		0	V_{CC}	V
RRST	Reset Pull-down Resistor		50	150	kΩ
C_{IO}	Pin Capacitance	Test Freq. = 1 MHz, T_A = 25°C		10	pF
I_{CC}	Power Supply Current	Active Mode, 12 MHz, V_{CC} = 5.5V/3V		5.5/3.5	mA
		Idle Mode, 12 MHz, V_{CC} = 5.5V/3V		3/2	mA
	Power-down Mode(4)	V_{CC} = 5.5V		5	µA
		V_{CC} = 3V		2	µA

Notes:
1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per port pin: 10 mA
   Maximum total I_{OL} for all output pins: 15 mA
   If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
2. Port in Quasi-Bidirectional Mode
3. Port in Push-Pull Output Mode
4. Minimum V_{CC} for Power-down is 2V.

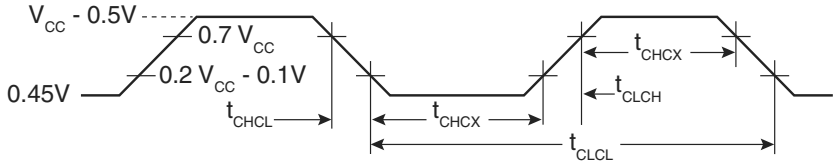
24.6.3 I_{CC} Test Condition, Active Mode, All Other Pins are Disconnected



24.6.4 I_{CC} Test Condition, Idle Mode, All Other Pins are Disconnected



24.6.5 Clock Signal Waveform for I_{CC} Tests in Active and Idle Modes, $t_{CLCH} = t_{CHCL} = 5$ ns



24.6.6 I_{CC} Test Condition, Power-down Mode, All Other Pins are Disconnected, V_{CC} = 2V to 5.5V