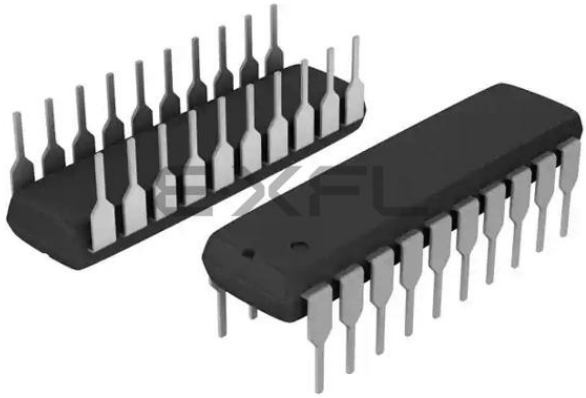

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## What is "Embedded - Microcontrollers"?

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## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | 8051 |
| Core Size | 8-Bit |
| Speed | 20MHz |
| Connectivity | SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, POR, PWM, WDT |
| Number of I/O | 15 |
| Program Memory Size | 4KB (4K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 256 x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.4V ~ 5.5V |
| Data Converters | - |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Through Hole |
| Package / Case | 20-DIP (0.300", 7.62mm) |
| Supplier Device Package | 20-PDIP |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/at89lp4052-20pu |

# 6. Special Function Registers

A map of the on-chip memory area called the Special Function Register (SFR) space is shown in Table 6-1.

Note that not all of the addresses are occupied, and unoccupied addresses may not be implemented on the chip. Read accesses to these addresses will in general return random data, and write accesses will have an indeterminate effect. User software should not write to these unlisted locations, since they may be used in future products to invoke new features.

**Table 6-1.** AT89LP2052/LP4052 SFR Map and Reset Values

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| 0F8H | | | | | | | | | 0FFH |
| 0F0H | B*<br>0000 0000 | | | | | | | | 0F7H |
| 0E8H | | | | | | | | | 0EFH |
| 0E0H | ACC*<br>0000 0000 | | | | | | | | 0E7H |
| 0D8H | | | | | | | | | 0DFH |
| 0D0H | PSW*<br>0000 0000 | | | | | SPCR<br>0000 0000 | | | 0D7H |
| 0C8H | | | | | | | | | 0CFH |
| 0C0H | | | P1M0<br>1111 1111 | P1M1<br>0000 0000 | | | P3M0<br>1111 1111 | P3M1<br>0000 0000 | 0C7H |
| 0B8H | IP*<br>x0x0 0000 | SADEN<br>0000 0000 | | | | | | | 0BFH |
| 0B0H | P3*<br>1111 1111 | | | | | | | IPH<br>x0x0 0000 | 0B7H |
| 0A8H | IE*<br>00x0 0000 | SADDR<br>0000 0000 | SPSR<br>000x xx00 | | | | | | 0AFH |
| 0A0H | | | | | | | WDTRST<br>(write-only) | WDTCON<br>0000 x000 | 0A7H |
| 98H | SCON*<br>0000 0000 | SBUF<br>xxxx xxxx | | | | | | | 9FH |
| 90H | P1*<br>1111 1111 | TCONB<br>0010 0100 | RL0<br>0000 0000 | RL1<br>0000 0000 | RH0<br>0000 0000 | RH1<br>0000 0000 | | ACSR<br>xx00 0000 | 97H |
| 88H | TCON*<br>0000 0000 | TMOD<br>0000 0000 | TL0<br>0000 0000 | TL1<br>0000 0000 | TH0<br>0000 0000 | TH1<br>0000 0000 | | | 8FH |
| 80H | | SP<br>0000 0111 | DPL<br>0000 0000 | DPH<br>0000 0000 | | | SPDR<br>xxxx xxxx | PCON<br>000x 0000 | 87H |

Note: *These SFRs are bit-addressable.

**Figure 8-2.** Single-cycle ALU Operation (Example: INC R0)

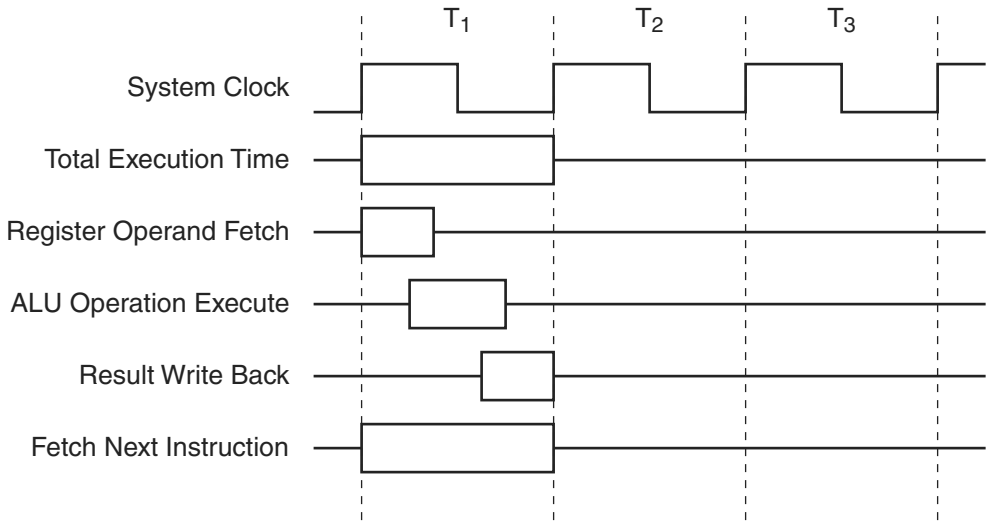
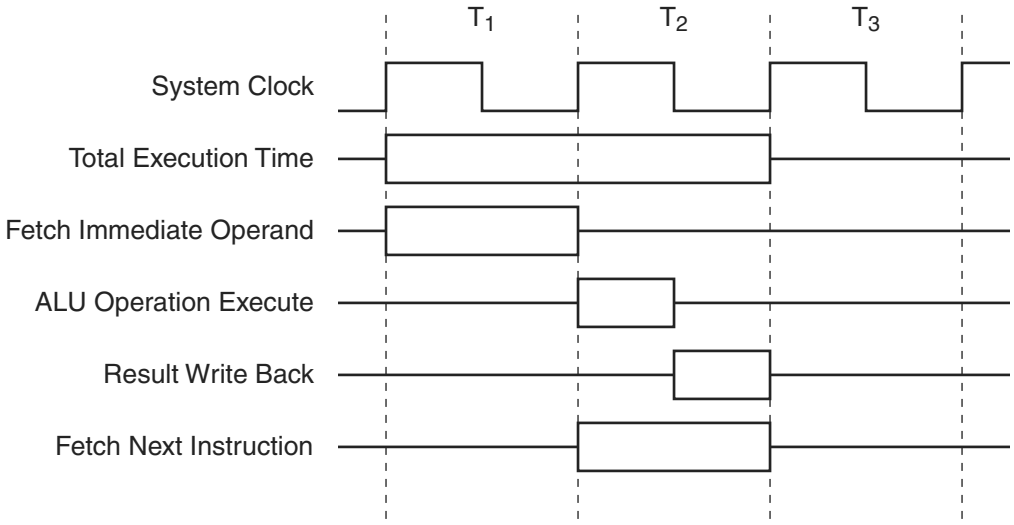



**Figure 8-3.** Two-Cycle ALU Operation (Example: ADD A, #data)



# 12. Reset

During reset, all I/O Registers are set to their initial values, the port pins are tri-stated, and the program starts execution from the Reset Vector, 0000H. The AT89LP2052/LP4052 has four sources of reset: power-on reset, brown-out reset, external reset, and watchdog reset.

## 12.1 Power-on Reset

A Power-on Reset (POR) is generated by an on-chip detection circuit. The detection level is nominally 1.4V. The POR is activated whenever $V_{CC}$ is below the detection level. The POR circuit can be used to trigger the start-up reset or to detect a supply voltage failure in devices without a brown-out detector. The POR circuit ensures that the device is reset from power-on. When $V_{CC}$ reaches the Power-on Reset threshold voltage, the POR delay counter determines how long the device is kept in POR after $V_{CC}$ rise. The POR signal is activated again, without any delay, when $V_{CC}$ falls below the POR threshold level. A Power-on Reset (i.e. a cold reset) will set the POF flag in PCON.

## 12.2 Brown-out Reset

The AT89LP2052/LP4052 has an on-chip Brown-out Detection (BOD) circuit for monitoring the $V_{CC}$ level during operation by comparing it to a fixed trigger level. The trigger level for the BOD is nominally 2.2V. The purpose of the BOD is to ensure that if $V_{CC}$ fails or dips while executing at speed, the system will gracefully enter reset without the possibility of errors induced by incorrect execution. When $V_{CC}$ decreases to a value below the trigger level, the Brown-out Reset is immediately activated. When $V_{CC}$ increases above the trigger level, the BOD delay counter starts the MCU after the time-out period has expired.

## 12.3 External Reset

The RST pin functions as an active-high reset input. The pin must be held high for at least two clock cycles to trigger the internal reset. RST also serves as the In-System Programming (ISP) enable. ISP is enabled when the external reset pin is held high and the ISP Enable fuse is enabled.

## 12.4 Watchdog Reset

When the Watchdog times out, it will generate an internal reset pulse lasting 16 clock cycles. Watchdog reset will also set the WDTOVF flag in WDTCON. To prevent a Watchdog reset, the watchdog reset sequence 1EH/E1H must be written to WDTRST before the Watchdog times out. A Watchdog reset will occur only if the Watchdog has been enabled. The Watchdog is disabled by default after any reset and must always be re-enabled if needed.

# 13. Power Saving Modes

The AT89LP2052/LP4052 supports two different power-reducing modes: Idle and Power-down. These modes are accessed through the PCON register.

**Table 13-1.** PCON – Power Control Register

PCON = 87H — Reset Value = 000X 0000B

Not Bit Addressable

| | SMOD1 | SMOD0 | PWDEX | POF | GF1 | GF0 | PD | IDL |
|---|---|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

| Symbol | Function |
|---|---|
| SMOD1 | Double Baud Rate bit. Doubles the baud rate of the UART in Modes 1, 2, or 3. |
| SMOD0 | Frame Error Select. When SMOD0 = 1, SCON.7 is SM0. When SMOD0 = 1, SCON.7 is FE. Note that FE will be set after a frame error regardless of the state of SMOD0. |
| PWDEX | Power-down Exit Mode. When PWDEX = 1, wake up from Power-down is externally controlled. When PWDEX = 0, wake up from Power-down is internally timed. |
| POF | Power Off Flag. POF is set to “1” during power up (i.e. cold reset). It can be set or reset under software control and is not affected by RST or BOD (i.e. warm resets). |
| GF1, GF0 | General-purpose Flags |
| PD | Power-down bit. Setting this bit activates power-down operation. |
| IDL | Idle Mode bit. Setting this bit activates Idle mode operation |

# 14. Interrupts

The AT89LP2052/LP4052 provides 6 interrupt sources: two external interrupts, two timer interrupts, a serial port interrupt, and an analog comparator interrupt. These interrupts and the system reset each have a separate program vector at the start of the program memory space. Each interrupt source can be individually enabled or disabled by setting or clearing a bit in the interrupt enable register IE. The IE register also contains a global disable bit, EA, which disables all interrupts.

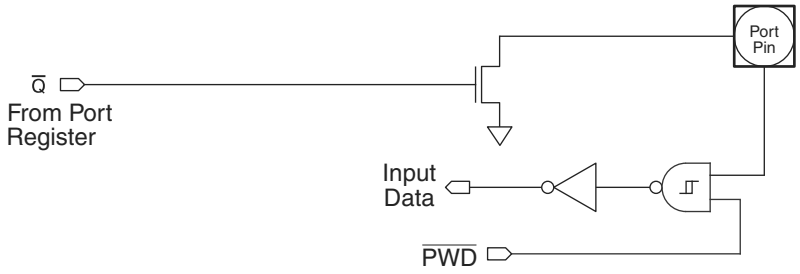
Each interrupt source can be individually programmed to one of four priority levels by setting or clearing bits in the interrupt priority registers IP and IPH. An interrupt service routine in progress can be interrupted by a higher priority interrupt, but not by another interrupt of the same or lower priority. The highest priority interrupt cannot be interrupted by any other interrupt source. If two requests of different priority levels are pending at the end of an instruction, the request of higher priority level is serviced. If requests of the same priority level are pending at the end of an instruction, an internal polling sequence determines which request is serviced. The polling sequence is based on the vector address; an interrupt with a lower vector address has higher priority than an interrupt with a higher vector address. Note that the polling sequence is only used to resolve pending requests of the same priority level.

The External Interrupts $\overline{\text{INT0}}$ and $\overline{\text{INT1}}$ can each be either level-activated or edge-activated, depending on bits IT0 and IT1 in Register TCON. The flags that actually generate these interrupts are the IE0 and IE1 bits in TCON. When the service routine is vectored to, hardware clears the flag that generated an external interrupt only if the interrupt was edge-activated. If the interrupt was level activated, then the external requesting source (rather than the on-chip hardware) controls the request flag.

## 15.3 Open-drain Output

The open-drain output configuration turns off all pull-ups and only drives the pull-down transistor of the port pin when the port register contains a logic “0”. To be used as a logic output, a port configured in this manner must have an external pull-up, typically a resistor tied to $V_{CC}$. The pull-down for this mode is the same as for the quasi-bidirectional mode. The open-drain port configuration is shown in Figure 15-4. The input circuitry of P3.2 and P3.3 is not disabled during Power-down (see Figure 15-3).

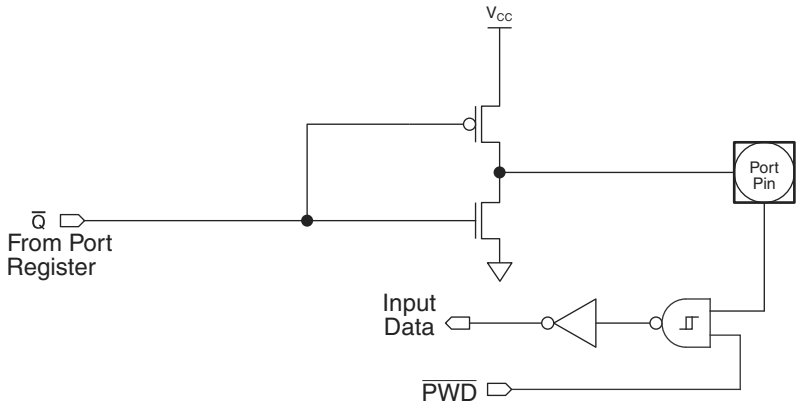
**Figure 15-4.** Open-Drain Output




## 15.4 Push-pull Output

The push-pull output configuration has the same pull-down structure as both the open-drain and the quasi-bidirectional output modes, but provides a continuous strong pull-up when the port register contains a logic “1”. The push-pull mode may be used when more source current is needed from a port output. The push-pull port configuration is shown in Figure 15-5. The input circuitry of P3.2 and P3.3 is not disabled during Power-down (see Figure 15-3).

**Figure 15-5.** Push-pull Output




## 15.5 Port 1 Analog Functions

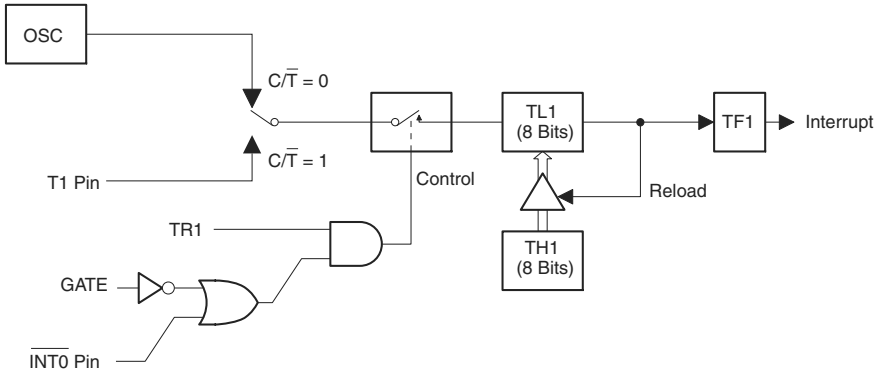
The AT89LP2052/LP4052 incorporates an analog comparator. In order to give the best analog performance and minimize power consumption, pins that are being used for analog functions must have both the digital outputs and digital inputs disabled. Digital outputs are disabled by putting the port pins into the input-only mode as described in Section 15. “I/O Ports” on page 20.

Digital inputs on P1.0 and P1.1 are disabled whenever the Analog Comparator is enabled by setting the CEN bit in ACSR. CEN forces the $\overline{PWD}$ input on P1.0 and P1.1 low, thereby disabling the Schmitt trigger circuitry.

## 16.3 Mode 2

Mode 2 configures the Timer register as an 8-bit Counter (TL1) with automatic reload, as shown in Figure 16-3. Overflow from TL1 not only sets TF1, but also reloads TL1 with the contents of TH1, which is preset by software. The reload leaves TH1 unchanged. Mode 2 operation is the same for Timer/Counter 0.

**Figure 16-3.** Timer/Counter 1 Mode 2: 8-bit Auto-Reload

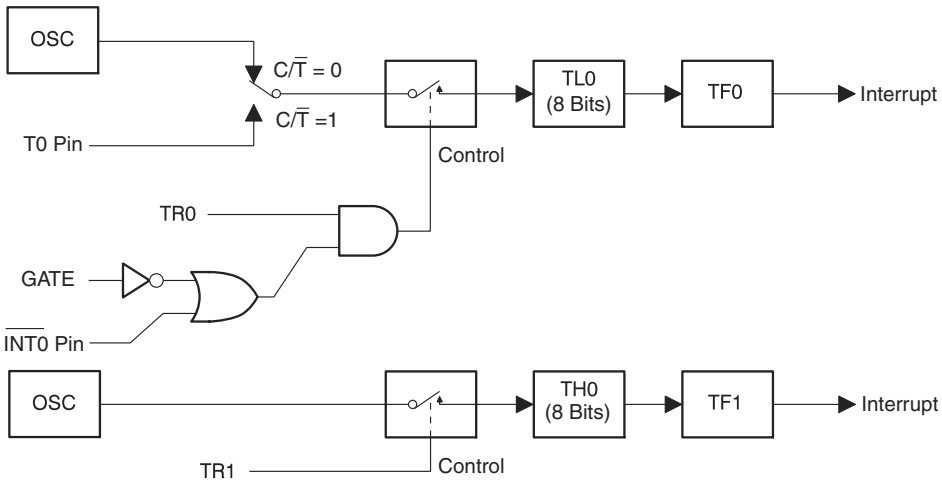



## 16.4 Mode 3

Timer 1 in Mode 3 simply holds its count. The effect is the same as setting TR1 = 0. Timer 0 in Mode 3 establishes TL0 and TH0 as two separate counters. The logic for Mode 3 on Timer 0 is shown in Figure 16-4. TL0 uses the Timer 0 control bits: C/T, GATE, TR0, INT0, and TF0. TH0 is locked into a timer function (counting machine cycles) and takes over the use of TR1 and TF1 from Timer 1. Thus, TH0 now controls the Timer 1 interrupt.

Mode 3 is for applications requiring an extra 8-bit timer or counter. With Timer 0 in Mode 3, the AT89LP2052/LP4052 can appear to have three Timer/Counters. When Timer 0 is in Mode 3, Timer 1 can be turned on and off by switching it out of and into its own Mode 3. In this case, Timer 1 can still be used by the serial port as a baud rate generator or in any application not requiring an interrupt.

**Figure 16-4.** Timer/Counter 0 Mode 3: Two 8-bit Counters



## 18.2 Baud Rates

The baud rate in Mode 0 is fixed as shown in the following equation.

$$\text{Mode 0 Baud Rate} = \frac{\text{Oscillator Frequency}}{2}$$

The baud rate in Mode 2 depends on the value of the SMOD1 bit in Special Function Register PCON.7. If SMOD1 = 0 (the value on reset), the baud rate is 1/32 of the oscillator frequency. If SMOD1 = 1, the baud rate is 1/16 of the oscillator frequency, as shown in the following equation.

$$\text{Mode 2 Baud Rate} = \frac{2^{\text{SMOD1}}}{32} \times (\text{Oscillator Frequency})$$

### 18.2.1 Using Timer 1 to Generate Baud Rates

The Timer 1 overflow rate determines the baud rates in Modes 1 and 3. When Timer 1 is the baud rate generator, the baud rates are determined by the Timer 1 overflow rate and the value of SMOD1 according to the following equation.

$$\text{Modes 1, 3 Baud Rate} = \frac{2^{\text{SMOD1}}}{32} \times (\text{Timer 1 Overflow Rate})$$

The Timer 1 interrupt should be disabled in this application. The Timer itself can be configured for either timer or counter operation in any of its 3 running modes. In the most typical applications, it is configured for timer operation in auto-reload mode (high nibble of TMOD = 0010B). In this case, the baud rate is given by the following formula.

$$\text{Modes 1, 3 Baud Rate} = \frac{2^{\text{SMOD1}}}{32} \times \frac{\text{Oscillator Frequency}}{[256 - (\text{TH1})]}$$

Programmers can achieve very low baud rates with Timer 1 by configuring the Timer to run as a 16-bit auto-reload timer (high nibble of TMOD = 0001B). In this case, the baud rate is given by the following formula.

$$\text{Modes 1, 3 Baud Rate} = \frac{2^{\text{SMOD1}}}{32} \times \frac{\text{Oscillator Frequency}}{[65536 - (\text{RH1,RL1})]}$$

Table 18-2 lists commonly used baud rates and how they can be obtained from Timer 1.

**Table 18-2.** Commonly Used Baud Rates Generated by Timer 1

| Baud Rate | $f_{osc}$ (MHz) | SMOD1 | Timer 1 | | |
|---|---|---|---|---|---|
| | | | C/$\overline{T}$ | Mode | Reload Value |
| Mode 0: 1 MHz | 2 | X | X | X | X |
| Mode 2: 375K | 12 | 0 | X | X | X |
| 62.5K | 12 | 1 | 0 | 2 | F4H |
| 19.2K | 11.059 | 1 | 0 | 2 | DCH |
| 9.6K | 11.059 | 0 | 0 | 2 | DCH |
| 4.8K | 11.059 | 0 | 0 | 2 | B8H |
| 2.4K | 11.059 | 0 | 0 | 2 | 70H |
| 1.2K | 11.059 | 0 | 0 | 1 | FEE0H |
| 137.5 | 11.986 | 0 | 0 | 1 | F55CH |
| 110 | 6 | 0 | 0 | 1 | F958H |
| 110 | 12 | 0 | 0 | 1 | F304H |

## 18.3 More About Mode 0

Serial data enters and exits through RXD. TXD outputs the shift clock. Eight data bits are transmitted/received, with the LSB first. The baud rate is fixed at 1/2 the oscillator frequency. Figure 18-1 shows a simplified functional diagram of the serial port in Mode 0 and associated timing.

Transmission is initiated by any instruction that uses SBUF as a destination register. The “write to SBUF” signal also loads a “1” into the ninth position of the transmit shift register and tells the TX Control block to begin a transmission. The internal timing is such that one full machine cycle will elapse between “write to SBUF” and activation of SEND.

SEND transfers the output of the shift register to the alternate output function line of P3.0, and also transfers Shift Clock to the alternate output function line of P3.1. At the falling edge of Shift Clock the contents of the transmit shift register are shifted one position to the right.

As data bits shift out to the right, “0”s come in from the left. When the MSB of the data byte is at the output position of the shift register, the “1” that was initially loaded into the ninth position is just to the left of the MSB, and all positions to the left of that contain “0”s. This condition flags the TX Control block to do one last shift, then deactivate SEND and set TI.

Reception is initiated by the condition REN = 1 and R1 = 0. At the next clock cycle, the RX Control unit writes the bits 11111110 to the receive shift register and activates RECEIVE in the next clock phase.

RECEIVE enables Shift Clock to the alternate output function line of P3.1. At the falling edge of Shift Clock the contents of the receive shift register are shifted one position to the left. The value that comes in from the right is the value that was sampled at the P3.0 pin at rising edge of Shift Clock.

As data bits come in from the right, “1”s shift out to the left. When the “0” that was initially loaded into the right-most position arrives at the left-most position in the shift register, it flags the RX Control block to do one last shift and load SBUF. Then RECEIVE is cleared and RI is set.

## 18.4 More About Mode 1

Ten bits are transmitted (through TXD), or received (through RXD): a start bit (0), 8 data bits (LSB first), and a stop bit (1). On receive, the stop bit goes into RB8 in SCON. In the AT89LP2052/LP4052, the baud rate is determined by the Timer 1 overflow rate. The baud rate is determined by the Timer 1 overflow rate. Figure 18-2 shows a simplified functional diagram of the serial port in Mode 1 and associated timings for transmit and receive.

Transmission is initiated by any instruction that uses SBUF as a destination register. The “write to SBUF” signal also loads a “1” into the ninth bit position of the transmit shift register and flags the TX Control unit that a transmission is requested. Transmission actually commences at S1P1 of the machine cycle following the next rollover in the divide-by-16 counter. Thus, the bit times are synchronized to the divide-by-16 counter, not to the “write to SBUF” signal.

The transmission begins when $\overline{\text{SEND}}$ is activated, which puts the start bit at TXD. One bit time later, DATA is activated, which enables the output bit of the transmit shift register to TXD. The first shift pulse occurs one bit time after that.

As data bits shift out to the right, “0”s are clocked in from the left. When the MSB of the data byte is at the output position of the shift register, the “1” that was initially loaded into the ninth position is just to the left of the MSB, and all positions to the left of that contain “0”s. This condition flags the TX Control unit to do one last shift, then deactivate $\overline{\text{SEND}}$ and set TI. This occurs at the tenth divide-by-16 rollover after “write to SBUF.”

Reception is initiated by a 1-to-0 transition detected at RXD. For this purpose, RXD is sampled at a rate of 16 times the established baud rate. When a transition is detected, the divide-by-16 counter is immediately reset, and 1FFH is written into the input shift register. Resetting the divide-by-16 counter aligns its roll-overs with the boundaries of the incoming bit times.

The 16 states of the counter divide each bit time into 16ths. At the seventh, eighth, and ninth counter states of each bit time, the bit detector samples the value of RXD. The value accepted is the value that was seen in at least 2 of the 3 samples. This is done to reject noise. In order to reject false bits, if the value accepted during the first bit time is not 0, the receive circuits are reset and the unit continues looking for another 1-to-0 transition. If the start bit is valid, it is shifted into the input shift register, and reception of the rest of the frame proceeds.

As data bits come in from the right, “1”s shift out to the left. When the start bit arrives at the left most position in the shift register, (which is a 9-bit register in Mode 1), it flags the RX Control block to do one last shift, load SBUF and RB8, and set RI. The signal to load SBUF and RB8 and to set RI is generated if, and only if, the following conditions are met at the time the final shift pulse is generated.

RI = 0 and

Either SM2 = 0, or the received stop bit = 1

If either of these two conditions is not met, the received frame is irretrievably lost. If both conditions are met, the stop bit goes into RB8, the 8 data bits go into SBUF, and RI is activated. At this time, whether or not the above conditions are met, the unit continues looking for a 1-to-0 transition in RXD.

**Figure 18-4.** Serial Port Mode 3

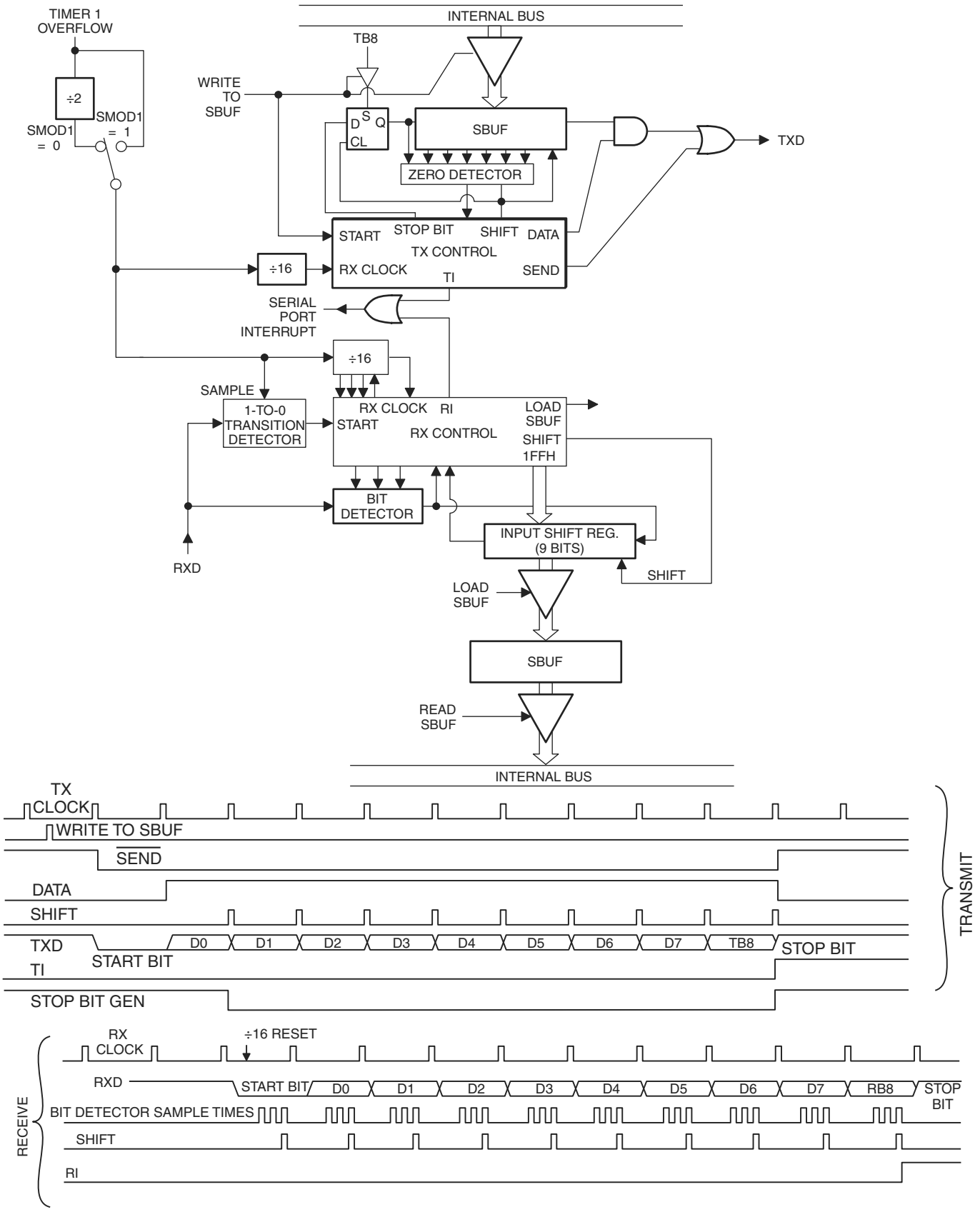


**Table 19-2.** SPSR – SPI Status Register

SPSR Address = AAH — Reset Value = 000X X000B

Not Bit Addressable

| | SPIF | WCOL | LDEN | – | – | – | DISSO | ENH |
|---|---|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

| Symbol | Function |
|---|---|
| SPIF | SP interrupt flag. When a serial transfer is complete, the SPIF bit is set and an interrupt is generated if SPIE = 1 and ES = 1. The SPIF bit is cleared by reading the SPI status register followed by reading/writing the SPI data register. |
| WCOL | When ENH = 0: Write collision flag. The WCOL bit is set if the SPI data register is written during a data transfer. During data transfer, the result of reading the SPDR register may be incorrect, and writing to it has no effect. The WCOL bit (and the SPIF bit) are cleared by reading the SPI status register followed by reading/writing the SPI data register.<br>When ENH = 1: WCOL works in Enhanced mode as Tx Buffer Full. Writing during WCOL = 1 in enhanced mode will overwrite the waiting data already present in the Tx Buffer. In this mode, WCOL is no longer reset by the SPIF reset but is reset when the write buffer has been unloaded into the serial shift register. |
| LDEN | Load enable for the Tx buffer in enhanced SPI mode.<br>When ENH is set, it is safe to load the Tx Buffer while LDEN = 1 and WCOL = 0. LDEN is high during bits 0 - 3 and is low during bits 4 - 7 of the SPI serial byte transmission time frame. |
| DISSO | Disable slave output bit.<br>When set, this bit causes the MISO pin to be tri-stated so more than one slave device can share the same interface with a single master. Normally, the first byte in a transmission could be the slave address and only the selected slave should clear its DISSO bit. |
| ENH | Enhanced SPI mode select bit. When ENH = 0, SPI is in normal mode, i.e. without write double buffering.<br>When ENH = 1, SPI is in enhanced mode with write double buffering. The Tx buffer shares the same address with the SPDR register. |

**Table 19-3.** SPDR – SPI Data Register

SPDR Address = 86H — Reset Value = 00H (after cold reset), unchanged (after warm reset)

Not Bit Addressable

| | SPD7 | SPD6 | SPD5 | SPD4 | SPD3 | SPD2 | SPD1 | SPD0 |
|---|---|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

# 21. Programmable Watchdog Timer

The programmable Watchdog Timer (WDT) protects the system from incorrect execution by triggering a system reset when it times out after the software has failed to feed the timer prior to the timer overflow. The WDT counts CPU clock cycles. The prescaler bits, PS0, PS1 and PS2 in SFR WDTCON are used to set the period of the Watchdog Timer from 16K to 2048K clock cycles. The WDT is disabled by Reset and during Power-down mode. When the WDT times out without being serviced, an internal RST pulse is generated to reset the CPU. See Table 21-1 for the available WDT period selections.

**Table 21-1.** Watchdog Timer Time-out Period Selection

| WDT Prescaler Bits | | | Period* (Clock Cycles) |
|---|---|---|---|
| PS2 | PS1 | PS0 | |
| 0 | 0 | 0 | 16K |
| 0 | 0 | 1 | 32K |
| 0 | 1 | 0 | 64K |
| 0 | 1 | 1 | 128K |
| 1 | 0 | 0 | 256K |
| 1 | 0 | 1 | 512K |
| 1 | 1 | 0 | 1024K |
| 1 | 1 | 1 | 2048K |

Note: *The WDT time-out period is dependent on the system clock frequency.

The Watchdog Timer consists of a 14-bit timer with 7-bit programmable prescaler. Writing the sequence 1EH/E1H to the WDTRST register enables the timer. When the WDT is enabled, the WDTEN bit in WDTCON will be set to “1”. To prevent the WDT from generating a reset when if overflows, the watchdog feed sequence must be written to WDTRST before the end of the time-out period. To feed the watchdog, two write instructions must be sequentially executed successfully. Between the two write instructions, SFR reads are allowed, but writes are not allowed. The instructions should move 1EH to the WDTRST register and then 1EH to the WDTRST register. An incorrect feed or enable sequence will cause an immediate watchdog reset. The program sequence to feed or enable the watchdog timer is as follows:

```
MOV WDTRST, #01Eh
MOV WDTRST, #0E1h
```

**Table 21-2.** WDTCON – Watchdog Control Register

WDTCON Address = A7H — Reset Value = 0000 XX00B

Not Bit Addressable

| | PS2 | PS1 | PS0 | WDIDLE | – | – | WDTOVF | WDTEN |
|---|---|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

| Symbol | Function |
|---|---|
| PS2<br>PS1<br>PS0 | Prescaler bits for the watchdog timer (WDT). When all three bits are cleared to 0, the watchdog timer has a nominal period of 16K clock cycles. When all three bits are set to 1, the nominal period is 2048K clock cycles. |
| WDIDLE | Disable/enable the Watchdog Timer in IDLE mode. When WDIDLE = 0, WDT continues to count in IDLE mode. When WDIDLE = 1, WDT freezes while the device is in IDLE mode. |
| WDTOVF | Watchdog Overflow Flag. Set when a WDT reset is generated by the WDT timer overflow. Also set when an incorrect sequence is written to WDTRST. Must be cleared by software. |
| WDTEN | Watchdog Enable Flag. This bit is READ-ONLY and reflects the status of the WDT (whether it is running or not). The WDT is disabled after any reset and must be re-enabled by writing 1EH/E1H to WDTRST |

**Table 21-3.** WDTRST – Watchdog Reset Register

WDTCON Address = A6H — **(Write-Only)**

Not Bit Addressable

| | – | – | – | – | – | – | – | – |
|---|---|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

The WDT is enabled by writing the sequence 1EH/E1H to the WDTRST SFR. The current status may be checked by reading the WDTEN bit in WDTCON. To prevent the WDT from resetting the device, the same sequence 1EH/E1H must be written to WDTRST before the time-out interval expires.

## 22. Instruction Set Summary

The AT89LP2052/LP4052 is fully binary compatible with the MCS-51 instruction set. The difference between the AT89LP2052/LP4052 and the standard 8051 is the number of cycles required to execute an instruction. Instructions in the AT89LP2052/LP4052 may take 1, 2, 3 or 4 clock cycles to complete. The execution times of most instructions may be computed using Table 22-1.

# 23. Programming the Flash Memory

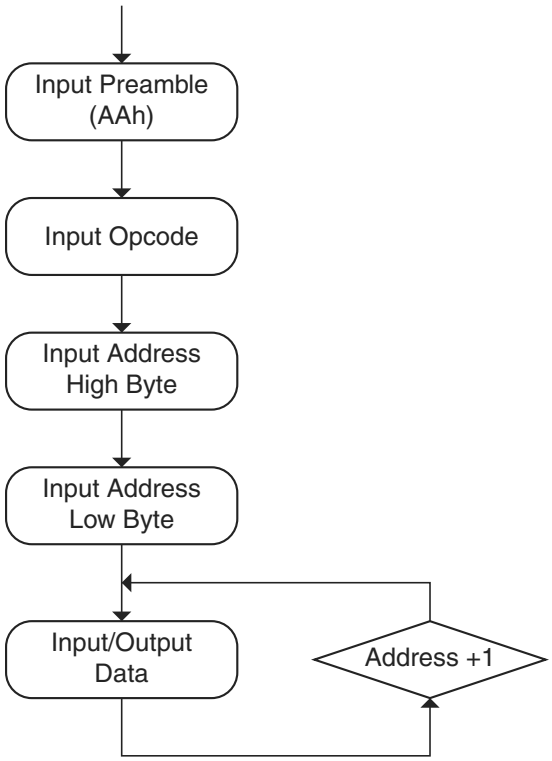
The AT89LP2052/LP4052 offers 2/4K bytes of In-System Programmable (ISP) non-volatile Flash code memory. In addition, the device contains a 32-byte User Signature Row and a 32-byte read-only Atmel Signature Row. The memory organization is shown in Table 23-1. The Memory is divided into pages of 32 bytes each. A single read or write command may only access a single page in the memory.

**Table 23-1.** Memory Organization

| Device # | Code Size | Page Size | # Pages | Address Range |
|---|---|---|---|---|
| AT89LP2052 | 2K bytes | 32 bytes | 64 | 0000H - 07FFH |
| AT89LP4052 | 4K bytes | 32 bytes | 128 | 0000H - 0FFFH |

The AT89LP2052/LP4052 provides two flexible interfaces for programming the Flash memory: a parallel interface which uses 10 pins; and a serial interface which uses the 4 SPI pins. The parallel and serial programming algorithms are identical. Both interfaces support the same command format where each command is issued to the device one byte at a time. Commands consist of a preamble byte for noise immunity, an opcode byte, two address bytes, and from 1 to 32 data bytes. Figure 23-1 shows a simplified flow chart of a command sequence.

**Figure 23-1.** Command Sequence Flow Chart



## 23.2 Status Register

The current state of the memory may be accessed by reading the status register. The status register is shown in Table 23-2.

**Table 23-2.** Status Register

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | – | – | – | – | $\overline{\text{LOAD}}$ | SUCCESS | $\overline{\text{WRTINH}}$ | $\overline{\text{BUSY}}$ |
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

| Symbol | Function |
|---|---|
| $\overline{\text{LOAD}}$ | Load flag. Cleared low by the load page buffer command and set high by the next memory write. This flag signals that the page buffer was previously loaded with data by the load page buffer command. |
| SUCCESS | Success flag. Cleared low at the start of a programming cycle and will only be set high if the programming cycle completes without interruption from the brownout detector. |
| $\overline{\text{WRTINH}}$ | Write Inhibit flag. Cleared low by the brownout detector (BOD) whenever programming is inhibited due to $V_{CC}$ falling below the minimum required programming voltage. If a BOD episode occurs during programming, the SUCCESS flag will remain low after the cycle is complete. $\overline{\text{WRTINH}}$ low also forces $\overline{\text{BUSY}}$ low. |
| $\overline{\text{BUSY}}$ | Busy flag. Cleared low whenever the memory is busy programming or if write is currently inhibited. |

## 23.3 $\overline{\text{DATA}}$ Polling

The AT89LP2052/LP4052 implements $\overline{\text{DATA}}$ polling to indicate the end of a programming cycle. While the device is busy, any attempted read of the last byte written will return the data byte with the MSB complemented. Once the programming cycle has completed, the true value will be accessible. During Erase the data is assumed to be FFH and $\overline{\text{DATA}}$ polling will return 7FH. When writing multiple bytes in a page, the $\overline{\text{DATA}}$ value will be the last data byte loaded before programming begins, not the written byte with the highest physical address within the page.

## 23.4 Parallel Programming

Parallel Programming Mode is enabled by applying $V_{PP}$ to the RST pin. The connections required during parallel mode are shown in Figure 23-2. During parallel programming, Port 1 is configured as an 8-bit wide bidirectional command bus. Data on P1 is strobed by a positive pulse on the XTAL1 pin. No other clock is required. The interface is enabled by pulling $\overline{\text{CS}}$ (P3.2) low. P3.1 acts as RDY/$\overline{\text{BSY}}$, and will be pulled low to indicate that the device is busy regardless of the state of $\overline{\text{CS}}$.

### 23.4.15 Read Status

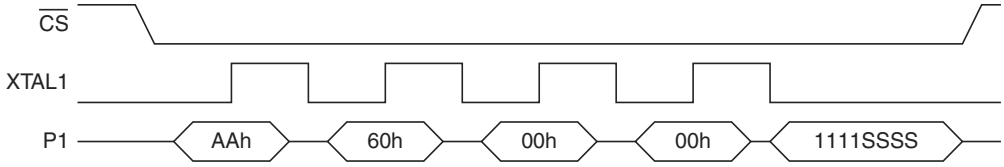
**Function**:

- Read memory status byte.

**Usage**:

1. Bring $\overline{CS}$ (P3.2) low.
2. Drive P1 to 0xAA and pulse XTAL1 high.
3. Drive P1 to 0x60 and pulse XTAL1 high.
4. Drive P1 to 0x00 and pulse XTAL1 high.
5. Drive P1 to 0x00 and bring XTAL1 high.
6. Tri-state P1.
7. Bring XTAL1 low.
8. Read data from P1.
9. Drive $\overline{CS}$ high.

**Figure 23-19.** Read Status Sequence



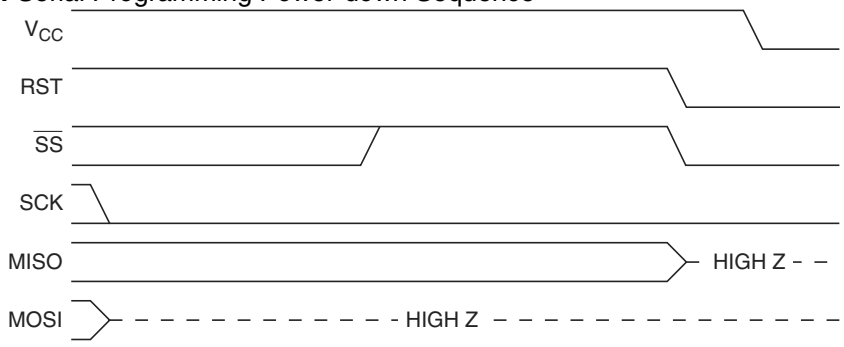

Note: The waveform on this page is not to scale.

### 23.5.2 Power-down Sequence

Execute this sequence to power-down the device **after** serial programming.

1. Tri-state MOSI (P1.5).
2. Bring SCK (P1.7) to “L”.
3. Bring RST to “L”.
4. Bring $\overline{SS}$ (P1.4) to “L”
5. Power off Vcc.

**Figure 23-23.** Serial Programming Power-down Sequence



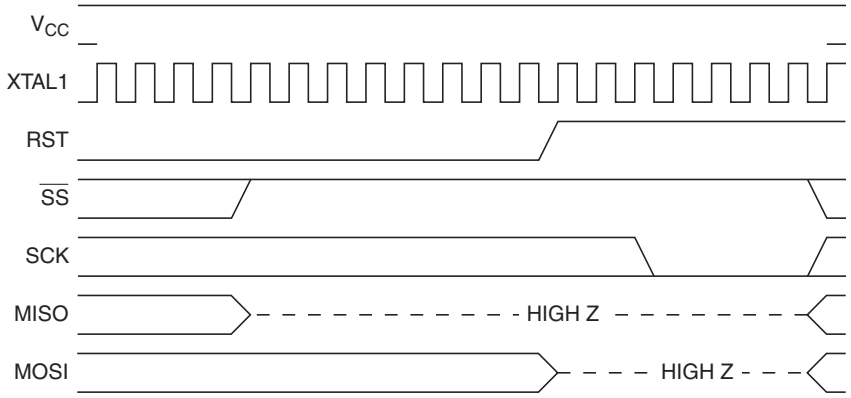

Note: The waveforms on this page are not to scale.

### 23.5.3 ISP Start Sequence

Execute this sequence to enter ISP when the device is **already** operational.

1. Bring $\overline{SS}$ (P1.4) to “H”.
2. Tri-state MISO (P1.6).
3. Bring RST to “H”.
4. Bring SCK (P1.7) to “L”.

**Figure 23-24.** In-System Programming (ISP) Start Sequence



## 24.2 DC Characteristics

$T_A$ = -40°C to 85°C, $V_{CC}$ = 2.4V to 5.5V (unless otherwise noted)

| Symbol | Parameter | Condition | Min | Max | Units |
|---|---|---|---|---|---|
| $V_{IL}$ | Input Low-voltage | (Except RST) | -0.5 | 0.25 $V_{CC}$ | V |
| $V_{IL1}$ | Input Low-voltage | (RST) | -0.5 | 0.3 $V_{CC}$ | V |
| $V_{IH}$ | Input High-voltage | (Except RST) | 0.65 $V_{CC}$ | $V_{CC}$ + 0.5 | V |
| $V_{IH1}$ | Input High-voltage | (RST) | 0.6 $V_{CC}$ | $V_{CC}$ + 0.5 | V |
| $V_{OL}$ | Output Low-voltage (Ports 1, 3)(1) | $I_{OL}$ = 10 mA, $V_{CC}$ = 2.7V, $T_A$ = 85°C | | 0.5 | V |
| $V_{OH}$ | Output High-voltage (Ports 1, 3) using Weak Pull-up(2) | $I_{OH}$ = -80 µA, $V_{CC}$ = 5V ±10% | 2.4 | | V |
| | | $I_{OH}$ = -30 µA | 0.75 $V_{CC}$ | | V |
| | | $I_{OH}$ = -12 µA | 0.9 $V_{CC}$ | | V |
| $V_{OH1}$ | Output High-voltage (Ports 1, 3) using Strong Pull-up(3) | $I_{OH}$ = -10 mA, $T_A$ = 85°C | 0.9 $V_{CC}$ | | |
| $I_{IL}$ | Logic 0 Input Current(2) (Ports 1, 3) | $V_{IN}$ = 0.45V | | -50 | µA |
| $I_{TL}$ | Logic 1 to 0 Transition Current(2) (Ports 1, 3) | $V_{IN}$ = 2V, $V_{CC}$ = 5V ±10% | | -300 | µA |
| $I_{LI}$ | Input-Only Leakage Current | 0 < $V_{IN}$ < $V_{CC}$ | | ±10 | µA |
| $V_{OS}$ | Comparator Input Offset Voltage | $V_{CC}$ = 5V | | 20 | mV |
| $V_{CM}$ | Comparator Input Common Mode Voltage | | 0 | $V_{CC}$ | V |
| RRST | Reset Pull-down Resistor | | 50 | 150 | kΩ |
| $C_{IO}$ | Pin Capacitance | Test Freq. = 1 MHz, $T_A$ = 25°C | | 10 | pF |
| $I_{CC}$ | Power Supply Current | Active Mode, 12 MHz, $V_{CC}$ = 5.5V/3V | | 5.5/3.5 | mA |
| | | Idle Mode, 12 MHz, $V_{CC}$ = 5.5V/3V | | 3/2 | mA |
| | Power-down Mode(4) | $V_{CC}$ = 5.5V | | 5 | µA |
| | | $V_{CC}$ = 3V | | 2 | µA |

Notes:
1. Under steady state (non-transient) conditions, $I_{OL}$ must be externally limited as follows:
   Maximum $I_{OL}$ per port pin: 10 mA
   Maximum total $I_{OL}$ for all output pins: 15 mA
   If $I_{OL}$ exceeds the test condition, $V_{OL}$ may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
2. Port in Quasi-Bidirectional Mode
3. Port in Push-Pull Output Mode
4. Minimum $V_{CC}$ for Power-down is 2V.

# 25. Ordering Information

## 25.1 Green Package Option (Pb/Halide-free)

| Speed (MHz) | Power Supply | Ordering Code | Package | Operation Range |
|---|---|---|---|---|
| 20 | 2.4V to 5.5V | AT89LP2052-20PU | 20P3 | Industrial (-40· C to 85· C) |
| | | AT89LP2052-20SU | 20S2 | |
| | | AT89LP2052-20XU | 20X | |
| | | AT89LP4052-20PU | 20P3 | |
| | | AT89LP4052-20SU | 20S2 | |
| | | AT89LP4052-20XU | 20X | |

| Package Type | |
|---|---|
| **20P3** | 20-lead, 0.300” Wide, Plastic Dual In-line Package (PDIP) |
| **20S2** | 20-lead, 0.300” Wide, Plastic Gull Wing Small Outline (SOIC) |
| **20X** | 20-lead, 4.4 mm Body Width, Plastic Thin Shrink Small Outline Package (TSSOP) |