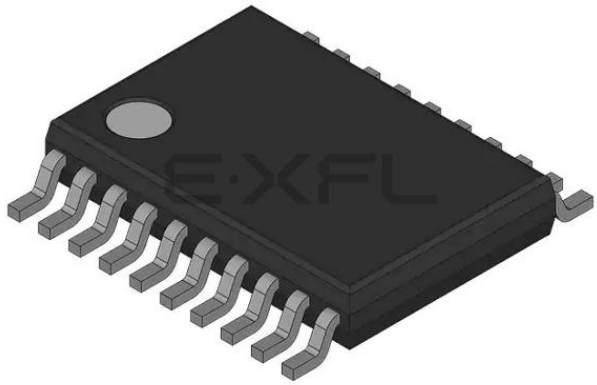

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	20MHz
Connectivity	SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	15
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/atmel/at89lp4052-20xu

12. Reset

During reset, all I/O Registers are set to their initial values, the port pins are tri-stated, and the program starts execution from the Reset Vector, 0000H. The AT89LP2052/LP4052 has four sources of reset: power-on reset, brown-out reset, external reset, and watchdog reset.

12.1 Power-on Reset

A Power-on Reset (POR) is generated by an on-chip detection circuit. The detection level is nominally 1.4V. The POR is activated whenever V_{CC} is below the detection level. The POR circuit can be used to trigger the start-up reset or to detect a supply voltage failure in devices without a brown-out detector. The POR circuit ensures that the device is reset from power-on. When V_{CC} reaches the Power-on Reset threshold voltage, the POR delay counter determines how long the device is kept in POR after V_{CC} rise. The POR signal is activated again, without any delay, when V_{CC} falls below the POR threshold level. A Power-on Reset (i.e. a cold reset) will set the POF flag in PCON.

12.2 Brown-out Reset

The AT89LP2052/LP4052 has an on-chip Brown-out Detection (BOD) circuit for monitoring the V_{CC} level during operation by comparing it to a fixed trigger level. The trigger level for the BOD is nominally 2.2V. The purpose of the BOD is to ensure that if V_{CC} fails or dips while executing at speed, the system will gracefully enter reset without the possibility of errors induced by incorrect execution. When V_{CC} decreases to a value below the trigger level, the Brown-out Reset is immediately activated. When V_{CC} increases above the trigger level, the BOD delay counter starts the MCU after the time-out period has expired.

12.3 External Reset

The RST pin functions as an active-high reset input. The pin must be held high for at least two clock cycles to trigger the internal reset. RST also serves as the In-System Programming (ISP) enable. ISP is enabled when the external reset pin is held high and the ISP Enable fuse is enabled.

12.4 Watchdog Reset

When the Watchdog times out, it will generate an internal reset pulse lasting 16 clock cycles. Watchdog reset will also set the WDTOVF flag in WDTCON. To prevent a Watchdog reset, the watchdog reset sequence 1EH/E1H must be written to WDTRST before the Watchdog times out. A Watchdog reset will occur only if the Watchdog has been enabled. The Watchdog is disabled by default after any reset and must always be re-enabled if needed.

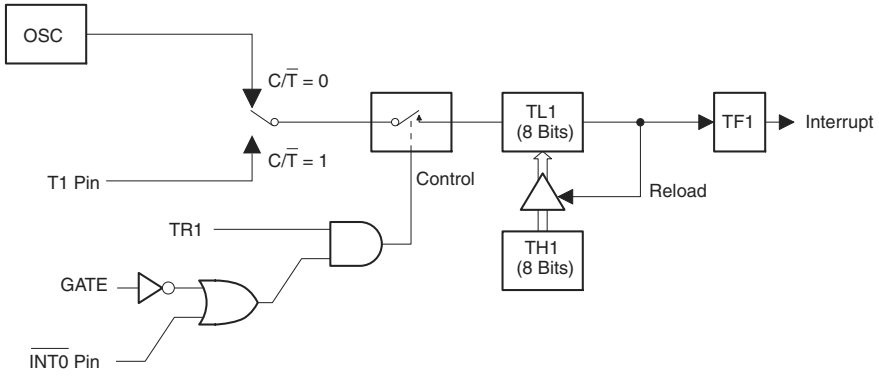
13. Power Saving Modes

The AT89LP2052/LP4052 supports two different power-reducing modes: Idle and Power-down. These modes are accessed through the PCON register.

16.3 Mode 2

Mode 2 configures the Timer register as an 8-bit Counter (TL1) with automatic reload, as shown in Figure 16-3. Overflow from TL1 not only sets TF1, but also reloads TL1 with the contents of TH1, which is preset by software. The reload leaves TH1 unchanged. Mode 2 operation is the same for Timer/Counter 0.

Figure 16-3. Timer/Counter 1 Mode 2: 8-bit Auto-Reload



16.4 Mode 3

Timer 1 in Mode 3 simply holds its count. The effect is the same as setting TR1 = 0. Timer 0 in Mode 3 establishes TL0 and TH0 as two separate counters. The logic for Mode 3 on Timer 0 is shown in Figure 16-4. TL0 uses the Timer 0 control bits: C/T, GATE, TR0, INT0, and TF0. TH0 is locked into a timer function (counting machine cycles) and takes over the use of TR1 and TF1 from Timer 1. Thus, TH0 now controls the Timer 1 interrupt.

Mode 3 is for applications requiring an extra 8-bit timer or counter. With Timer 0 in Mode 3, the AT89LP2052/LP4052 can appear to have three Timer/Counters. When Timer 0 is in Mode 3, Timer 1 can be turned on and off by switching it out of and into its own Mode 3. In this case, Timer 1 can still be used by the serial port as a baud rate generator or in any application not requiring an interrupt.

Figure 16-4. Timer/Counter 0 Mode 3: Two 8-bit Counters

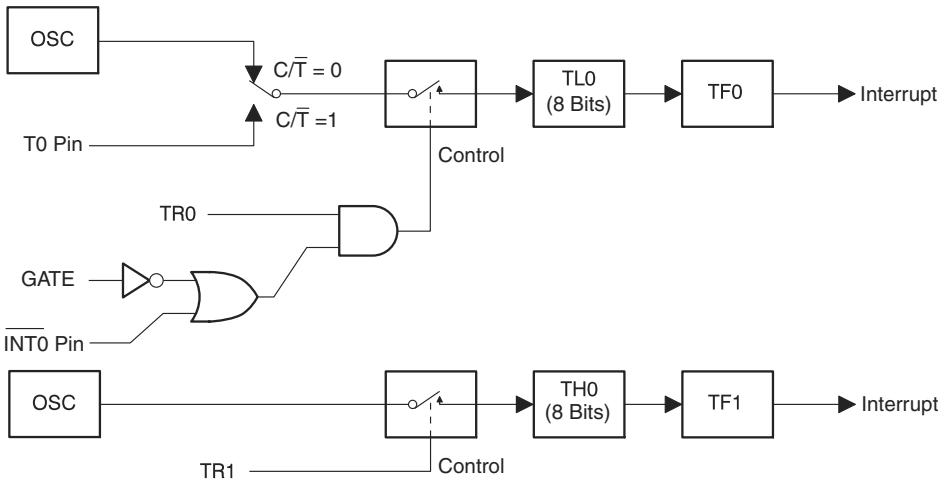


Table 16-3. TCONB – Timer/Counter Control Register B

TCONB = 91H — Reset Value = 0010 0100B

Not Bit Addressable

Bit	PWM1EN	PWM0EN	PSC12	PSC11	PSC10	PSC02	PSC01	PSC00
	7	6	5	4	3	2	1	0

Symbol	Function
PWM1EN	Configures Timer 1 for Pulse Width Modulation output on T1 (P3.5).
PWM0EN	Configures Timer 0 for Pulse Width Modulation output on T0 (P3.4).
PSC12 PSC11 PSC10	Prescaler for Timer 1 Mode 0. The number of active bits in TL1 equals PSC1 + 1. After reset PSC1 = 100B which enables 5 bits of TL1 for compatibility with the 13-bit Mode 0 in AT89S2051.
PSC02 PSC01 PSC00	Prescaler for Timer 0 Mode 0. The number of active bits in TL0 equals PSC0 + 1. After reset PSC0 = 100B which enables 5 bits of TL0 for compatibility with the 13-bit Mode 0 in AT89C52.

16.5 Pulse Width Modulation

Timer 0 and Timer 1 may be independently configured as 8-bit asymmetrical pulse width modulators (PWM) by setting the PWM0EN or PWM1EN bits in TCONB, respectively. In PWM Mode the generated waveform is output on the timer's pin, T0 or T1. C/$\overline{T}$ must be set to “0” when in PWM mode. In Timer 0's PWM mode, TH0 acts as an 8-bit counter while RH0 stores the 8-bit compare value. When TH0 is 00H the PWM output is set high. When the TH0 count reaches the value stored in RH0 the PWM output is set low. Therefore, the pulse width is proportional to the value in RH0. To prevent glitches writes to RH0 only take effect on the FFH to 00H overflow of TH0. Timer 1 has the same behavior using TH1 and RH1. See Figure 16-5 for PWM waveform example. Setting RH0 to 00H will keep the PWM output low.

The PWM will only function if the timer is in Mode 0 or Mode 1. In Mode 0, TL0 acts as a logarithmic prescaler driving TH0 (see Figure 16-6). The PSC0 bits in TCONB control the prescaler value. In Mode 1, TL0 provides linear prescaling with an 8-bit auto-reload from RL0 (see Figure 16-7).

Figure 16-5. Asymmetrical Pulse Width Modulation

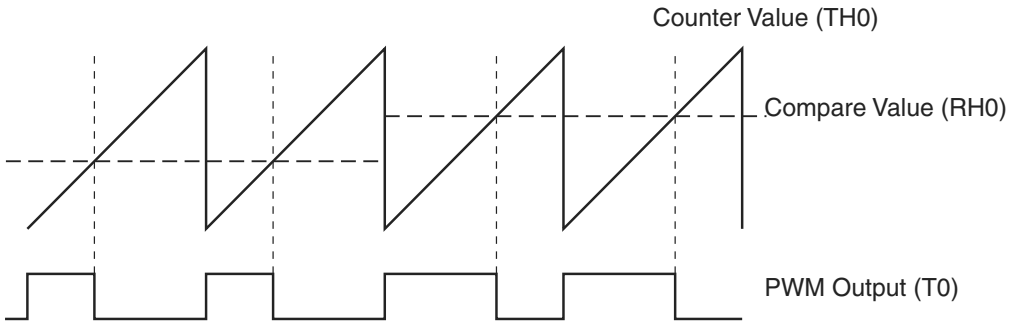


Table 18-2 lists commonly used baud rates and how they can be obtained from Timer 1.

Table 18-2. Commonly Used Baud Rates Generated by Timer 1

Baud Rate	f_{osc} (MHz)	SMOD1	Timer 1		
			C/$\overline{T}$	Mode	Reload Value
Mode 0: 1 MHz	2	X	X	X	X
Mode 2: 375K	12	0	X	X	X
62.5K	12	1	0	2	F4H
19.2K	11.059	1	0	2	DCH
9.6K	11.059	0	0	2	DCH
4.8K	11.059	0	0	2	B8H
2.4K	11.059	0	0	2	70H
1.2K	11.059	0	0	1	FEE0H
137.5	11.986	0	0	1	F55CH
110	6	0	0	1	F958H
110	12	0	0	1	F304H

18.3 More About Mode 0

Serial data enters and exits through RXD. TXD outputs the shift clock. Eight data bits are transmitted/received, with the LSB first. The baud rate is fixed at 1/2 the oscillator frequency. Figure 18-1 shows a simplified functional diagram of the serial port in Mode 0 and associated timing.

Transmission is initiated by any instruction that uses SBUF as a destination register. The “write to SBUF” signal also loads a “1” into the ninth position of the transmit shift register and tells the TX Control block to begin a transmission. The internal timing is such that one full machine cycle will elapse between “write to SBUF” and activation of SEND.

SEND transfers the output of the shift register to the alternate output function line of P3.0, and also transfers Shift Clock to the alternate output function line of P3.1. At the falling edge of Shift Clock the contents of the transmit shift register are shifted one position to the right.

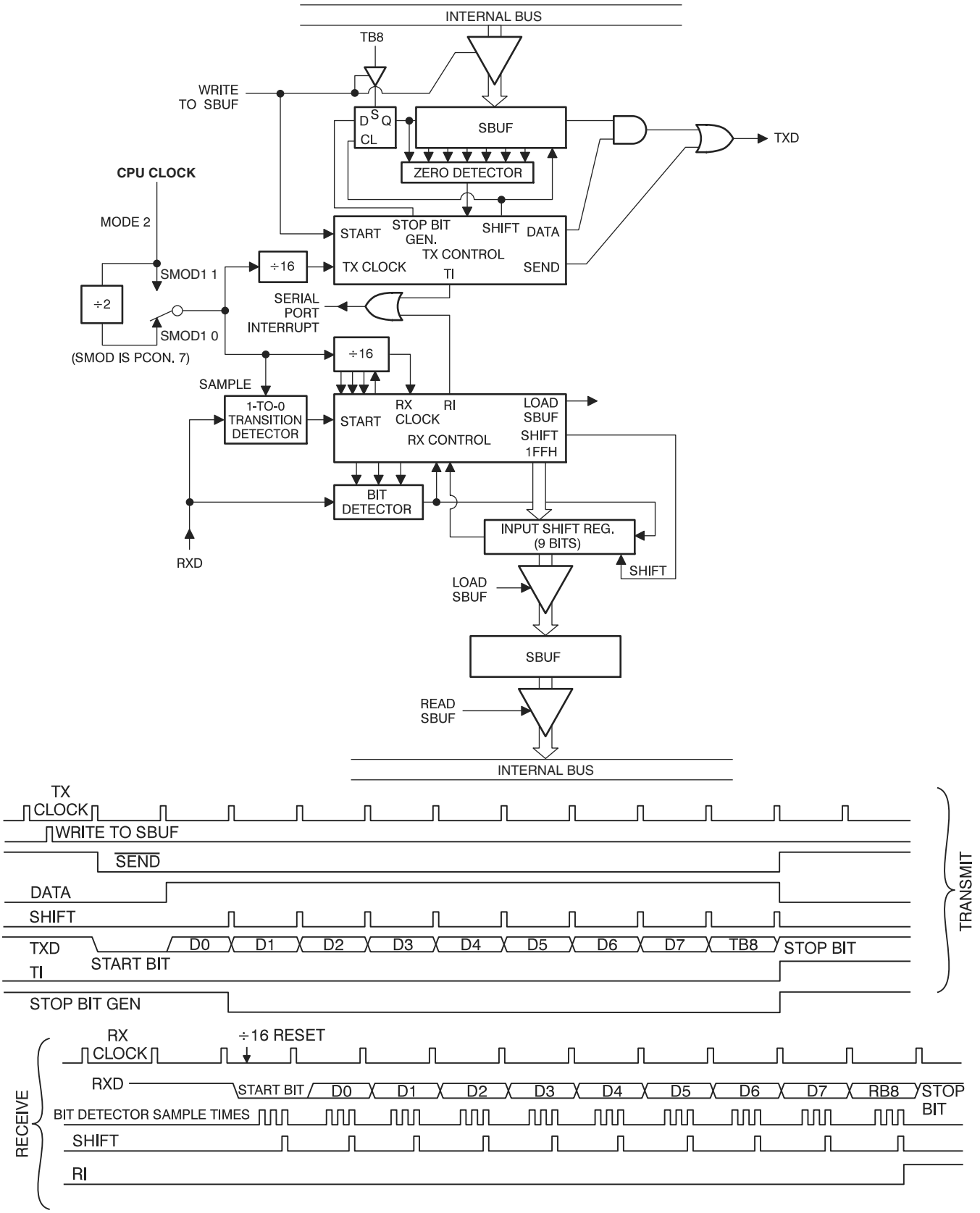
As data bits shift out to the right, “0”s come in from the left. When the MSB of the data byte is at the output position of the shift register, the “1” that was initially loaded into the ninth position is just to the left of the MSB, and all positions to the left of that contain “0”s. This condition flags the TX Control block to do one last shift, then deactivate SEND and set TI.

Reception is initiated by the condition REN = 1 and R1 = 0. At the next clock cycle, the RX Control unit writes the bits 11111110 to the receive shift register and activates RECEIVE in the next clock phase.

RECEIVE enables Shift Clock to the alternate output function line of P3.1. At the falling edge of Shift Clock the contents of the receive shift register are shifted one position to the left. The value that comes in from the right is the value that was sampled at the P3.0 pin at rising edge of Shift Clock.

As data bits come in from the right, “1”s shift out to the left. When the “0” that was initially loaded into the right-most position arrives at the left-most position in the shift register, it flags the RX Control block to do one last shift and load SBUF. Then RECEIVE is cleared and RI is set.

Figure 18-3. Serial Port Mode 2



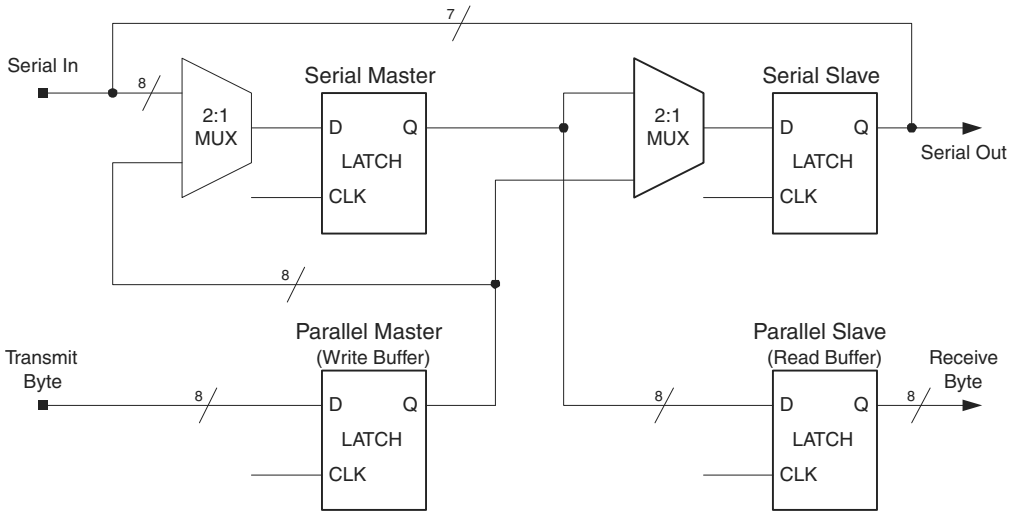
19.1 Normal Mode

The SPI has two modes of operation: normal (non-buffered write) and enhanced (buffered write). In normal mode, writing to the SPI data register (SPDR) of the master CPU starts the SPI clock generator and the data written shifts out of the MOSI pin and into the MOSI pin of the slave CPU. Transmission may start after an initial delay while the clock generator waits for the next full bit slot of the specified baud rate. After shifting one byte, the SPI clock generator stops, setting the end of transmission flag (SPIF) and transferring the received byte to the read buffer (SPDR). If both the SPI interrupt enable bit (SPIE) and the serial port interrupt enable bit (ES) are set, an interrupt is requested. Note that SPDR refers to either the write data buffer or the read data buffer, depending on whether the access is a write or read. In normal mode, because the write buffer is transparent (and a write access to SPDR will be directed to the shift buffer), any attempt to write to SPDR while a transmission is in progress will result in a write collision with WCOL set. However, the transmission will still complete normally, but the new byte will be ignored and a new write access to SPDR will be necessary.

19.2 Enhanced Mode

Enhanced mode is similar to normal mode except that the write buffer holds the next byte to be transmitted. Writing to SPDR loads the write buffer and sets WCOL to signify that the buffer is full and any further writes will overwrite the buffer. WCOL is cleared by hardware when the buffered byte is loaded into the shift register and transmission begins. If the master SPI is currently idle, i.e. if this is the first byte, then after loading SPDR, transmission of the byte starts and WCOL is cleared immediately. While this byte is transmitting, the next byte may be written to SPDR. The Load Enable flag (LDEN) in SPSR can be used to determine when transmission has started. LDEN is asserted during the first four bit slots of a SPI transfer. The master CPU should first check that LDEN is set and that WCOL is cleared before loading the next byte. In enhanced mode, if WCOL is set when a transfer completes, i.e. the next byte is available, then the SPI immediately loads the buffered byte into the shift register, resets WCOL, and continues transmission without stopping and restarting the clock generator. As long as the CPU can keep the write buffer full in this manner, multiple bytes may be transferred with minimal latency between bytes.

Figure 19-3. SPI Shift Register Diagram



19.3 Serial Clock Generator

The CPHA (Clock PHAse), CPOL (Clock POLarity), and SPR (Serial Peripheral clock Rate = baud rate) bits in SPCR control the shape and rate of SCK. The two SPR bits provide four possible clock rates when the SPI is in master mode. In slave mode, the SPI will operate at the rate of the incoming SCK as long as it does not exceed the maximum bit rate. There are also four possible combinations of SCK phase and polarity with respect to the serial data. CPHA and CPOL determine which format is used for transmission. The SPI data transfer formats are shown in Figures 19-4 and and 19-5. To prevent glitches on SCK from disrupting the interface, CPHA, CPOL, and SPR should be set up before the interface is enabled, and the master device should be enabled before the slave device(s).

Table 22-1. Generic Instruction Execution Times and Exceptions

Instruction Type	Cycle Count
Most arithmetic, logical, bit and transfer instructions	# bytes
Branches and Calls	# bytes + 1
Single Byte Indirect (i.e. ADD A, @Ri, etc.)	2
RET, RETI	4
MOVC	3
MUL	2
DIV	4
INC DPTR	2

Table 22-2. Detailed Arithmetic Instruction Summary

		Clock Cycles		
Arithmetic Instruction	**Bytes**	**8051**	**LP2052**	**Hex Code**
ADD A, Rn	1	12	1	28-2F
ADD A, direct	2	12	2	25
ADD A, @Ri	1	12	2	26-27
ADD A, #data	2	12	2	24
ADDC A, Rn	1	12	1	38-3F
ADDC A, direct	2	12	2	35
ADDC A, @Ri	1	12	2	36-37
ADDC A, #data	2	12	2	34
SUBB A, Rn	1	12	1	98-9F
SUBB A, direct	2	12	2	95
SUBB A, @Ri	1	12	2	96-97
SUBB A, #data	2	12	2	94
INC Rn	1	12	1	08-0F
INC direct	2	12	2	05
INC @Ri	1	12	2	06-07
INC A	1	12	1	04
DEC Rn	1	12	1	18-1F
DEC direct	2	12	2	15
DEC @Ri	1	12	2	16-17
DEC A	1	12	1	14
INC DPTR	1	24	2	A3
MUL AB	1	48	2	A4
DIV AB	1	48	4	84
DA A	1	12	1	D4

23.1 Programming Command Summary

Command	Preamble	Opcode	Addr High	Addr Low	Data 0	Data n
Program Enable[1]	1010 1010	1010 1100	0101 0011			
Chip Erase	1010 1010	1000 1010				
Read Status	1010 1010	0110 0000	xxxx xxxx	xxxx xxxx	Status Out	
Load Code **Page Buffer**[2]	1010 1010	0101 0001	xxxx xxxx	xxxB BBBB	DataIn 0 ... DataIn n	
Write Code **Page**[2]	1010 1010	0101 0000	xxxx AAAA	AAAB BBBB	DataIn 0 ... DataIn n	
Read Code **Page**[2]	1010 1010	0011 0000	xxxx AAAA	AAAB BBBB	DataOut 0 ... DataOut n	
Write User Fuses[3]	1010 1010	1110 0001	xxxx xxxx	xxxx xxxx	xxxx FFFF	
Read User Fuses[3]	1010 1010	0110 0001	xxxx xxxx	xxxx xxxx	xxxx FFFF	
Write Lock Bits[4]	1010 1010	1110 0100	xxxx xxxx	xxxx xxxx	xxxx xxLL	
Read Lock Bits[4]	1010 1010	0110 0100	xxxx xxxx	xxxx xxxx	xxxx xxLL	
Write User Signature Page[2]	1010 1010	0101 0010	xxxx xxxx	xxxB BBBB	DataIn 0 ... DataIn n	
Read User Signature Page[2]	1010 1010	0011 0010	xxxx xxxx	xxxB BBBB	DataOut 0 ... DataOut n	
Read Atmel Signature Page[2][5]	1010 1010	0011 1000	xxxx xxxx	xxxB BBBB	DataOut 0 ... DataOut n	

Notes:
1. Program Enable must be the **first** command issued after entering into programming mode.
2. Any number of Data bytes from 1 to 32 may be written/read. The internal address is incremented between each byte.
3. **Fuse Bit Definitions**:

Bit 0	ISP Enable*	Enable = 0/Disable = 1
Bit 1	XTAL Osc Bypass	Enable = 0/Disable = 1
Bit 2	User Row Programming	Enable = 0/Disable = 1
Bit 3	System Clock Out	Enable = 0/Disable = 1

*The AT89LP2052/LP4052 has ISP enabled by default from the factory. However, if ISP is later disabled, the ISP Enable Fuse must be enabled by using Parallel Programming before entering ISP mode.
When disabling the ISP fuse during ISP, the current ISP session will remain active until RST is brought low.

4. **Lock Bit Definitions**:

Bit 0	Lock Bit 1	Locked = 0/Unlocked = 1
Bit 1	Lock Bit 2	Locked = 0/Unlocked = 1

5. **Atmel Signature Byte**:

AT89LP2052: Address 00H = 1EH
01H = 25H
02H = FFH

AT89LP4052: Address 00H = 1EH
01H = 45H
02H = FFH

6. **Symbol Key**:

A: Page Address Bit
B: Byte Address Bit
F: Fuse Bit Data
L: Lock Bit Data
x: Don't Care

23.2 Status Register

The current state of the memory may be accessed by reading the status register. The status register is shown in Table 23-2.

Table 23-2. Status Register

	–	–	–	–	$\overline{\text{LOAD}}$	SUCCESS	$\overline{\text{WRTINH}}$	$\overline{\text{BUSY}}$
Bit	7	6	5	4	3	2	1	0

Symbol	Function
$\overline{\text{LOAD}}$	Load flag. Cleared low by the load page buffer command and set high by the next memory write. This flag signals that the page buffer was previously loaded with data by the load page buffer command.
SUCCESS	Success flag. Cleared low at the start of a programming cycle and will only be set high if the programming cycle completes without interruption from the brownout detector.
$\overline{\text{WRTINH}}$	Write Inhibit flag. Cleared low by the brownout detector (BOD) whenever programming is inhibited due to V_{CC} falling below the minimum required programming voltage. If a BOD episode occurs during programming, the SUCCESS flag will remain low after the cycle is complete. $\overline{\text{WRTINH}}$ low also forces $\overline{\text{BUSY}}$ low.
$\overline{\text{BUSY}}$	Busy flag. Cleared low whenever the memory is busy programming or if write is currently inhibited.

23.3 $\overline{\text{DATA}}$ Polling

The AT89LP2052/LP4052 implements $\overline{\text{DATA}}$ polling to indicate the end of a programming cycle. While the device is busy, any attempted read of the last byte written will return the data byte with the MSB complemented. Once the programming cycle has completed, the true value will be accessible. During Erase the data is assumed to be FFH and $\overline{\text{DATA}}$ polling will return 7FH. When writing multiple bytes in a page, the $\overline{\text{DATA}}$ value will be the last data byte loaded before programming begins, not the written byte with the highest physical address within the page.

23.4 Parallel Programming

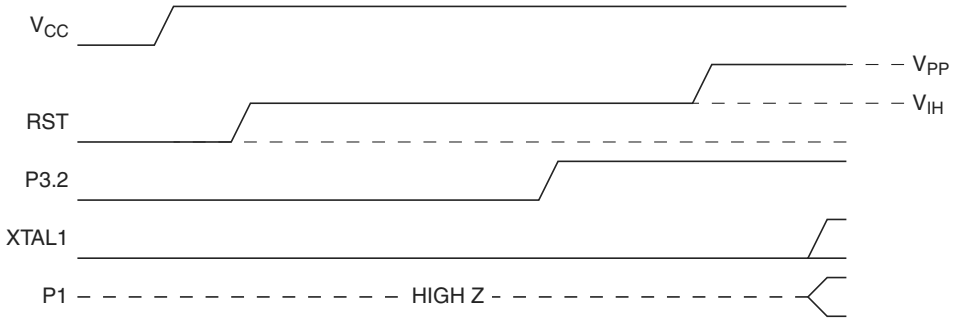
Parallel Programming Mode is enabled by applying V_{PP} to the RST pin. The connections required during parallel mode are shown in Figure 23-2. During parallel programming, Port 1 is configured as an 8-bit wide bidirectional command bus. Data on P1 is strobed by a positive pulse on the XTAL1 pin. No other clock is required. The interface is enabled by pulling $\overline{\text{CS}}$ (P3.2) low. P3.1 acts as RDY/$\overline{\text{BSY}}$, and will be pulled low to indicate that the device is busy regardless of the state of $\overline{\text{CS}}$.

23.4.1 Power-up Sequence

Execute the following sequence to power-up the device **before** parallel programming.

1. Apply power between VCC and GND pins.
2. After V_{CC} has settled, wait 10 µs and bring RST to “H”.
3. Wait 2 ms for the internal Power-on Reset to time out.
4. Bring P3.2 to “H” and then wait 10 µs.
5. Raise RST/V_{PP} to 12V to enable the parallel programming modes.
6. After V_{PP} has settled, wait an additional 10 µs before programming.

Figure 23-5. Parallel Mode Power-up Operation

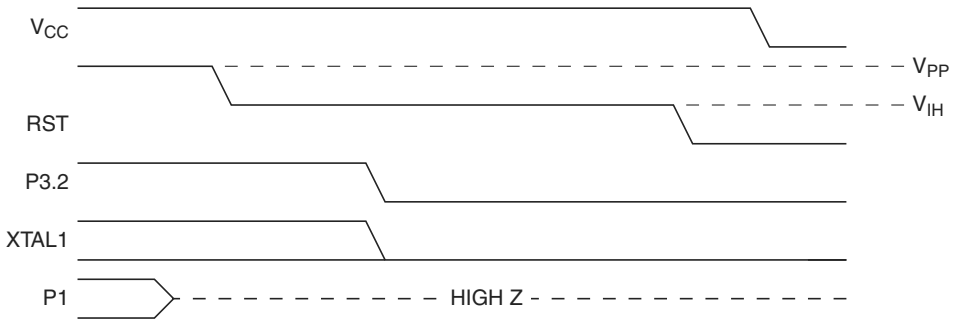


23.4.2 Power-down Sequence

Execute the following sequence to power-down the device **after** parallel programming.

1. Tri-state P1.
2. Bring RST/V_{PP} down from 12V to V_{CC} and wait 10 µs.
3. Bring XTAL and P3.2 to “L”.
4. Bring RST to “L” and wait 10 µs.
5. Power off V_{CC}.

Figure 23-6. Parallel Mode Power-down Operation



Note: The waveforms on this page are not to scale.

23.4.10 Read Atmel Signature Page

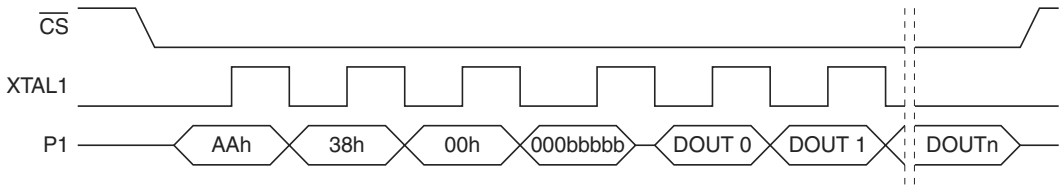
Function:

- Read 1 to 32 bytes of data from the Atmel Signature Row.
- The byte address (offset in page) is initialized to bits [4:0] of the low address byte. The internal address is incremented by one on the negative edge of the XTAL1 pulse. The address will wrap around to the 1st byte of the page when incremented past 31.
- Read data will be output on P1 after the falling edge of fourth XTAL1 pulse (address low byte strobe). The programmer should tri-state P1 prior to this edge to avoid bus contention on P1.

Usage:

1. Bring $\overline{CS}$ (P3.2) low.
2. Drive P1 to AAh and pulse XTAL1 high.
3. Drive P1 to 38h and pulse XTAL1 high.
4. Drive P1 to 00h and pulse XTAL1 high.
5. Drive P1 with bits [4:0] of address and bring XTAL1 high.
6. Tri-state P1.
7. Bring XTAL1 low.
8. Read data from P1.
9. To read additional data bytes in the page, pulse XTAL1 high to increment to the next address.
10. Drive $\overline{CS}$ high.

Figure 23-14. Read Atmel Signature Page Sequence



Note: The waveform on this page is not to scale.

23.4.11 Write Lock Bits

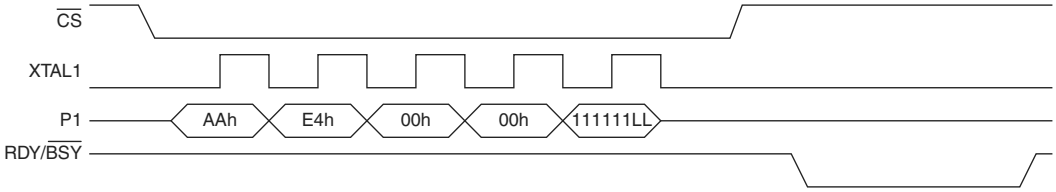
Function:

- Program (lock) Lock Bits 1 and 2.

Usage:

1. Bring $\overline{CS}$ (P3.2) low.
2. Drive P1 to AAh and pulse XTAL1 high.
3. Drive P1 to E4h and pulse XTAL1 high.
4. Drive P1 to 00h and pulse XTAL1 high.
5. Drive P1 to 00h and pulse XTAL1 high.
6. Drive data on P1 and pulse XTAL1 high.
7. Drive $\overline{CS}$ high.
8. Wait 4 ms, monitor P3.1, or poll data/status.

Figure 23-15. Write Lock Bits Sequence



23.4.12 Read Lock Bits

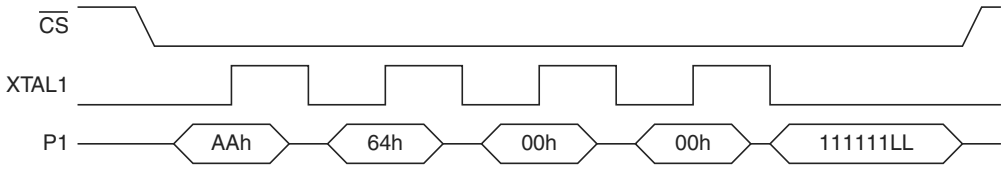
Function:

- Read status of Lock Bits 1 and 2.

Usage:

1. Bring $\overline{CS}$ (P3.2) low.
2. Drive P1 to 0xAA and pulse XTAL1 high.
3. Drive P1 to 0x64 and pulse XTAL1 high.
4. Drive P1 to 0x00 and pulse XTAL1 high.
5. Drive P1 to 0x00 and bring XTAL1 high.
6. Tri-state P1.
7. Bring XTAL1 low.
8. Read data from P1.
9. Drive $\overline{CS}$ high.

Figure 23-16. Read Lock Bits Sequence



Note: The waveforms on this page are not to scale.

23.4.15 Read Status

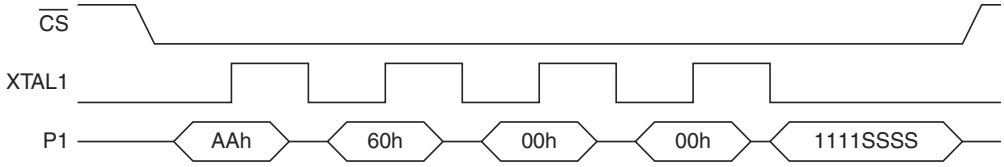
Function:

- Read memory status byte.

Usage:

1. Bring $\overline{CS}$ (P3.2) low.
2. Drive P1 to 0xAA and pulse XTAL1 high.
3. Drive P1 to 0x60 and pulse XTAL1 high.
4. Drive P1 to 0x00 and pulse XTAL1 high.
5. Drive P1 to 0x00 and bring XTAL1 high.
6. Tri-state P1.
7. Bring XTAL1 low.
8. Read data from P1.
9. Drive $\overline{CS}$ high.

Figure 23-19. Read Status Sequence



Note: The waveform on this page is not to scale.

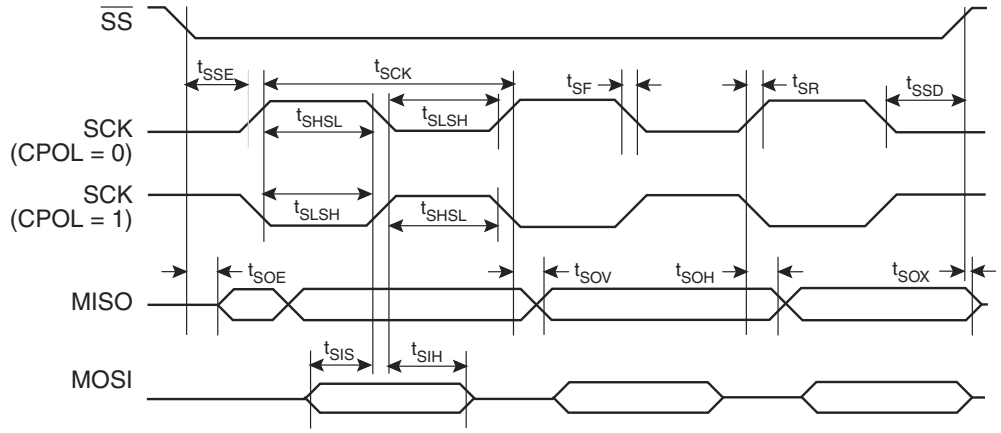
24.2 DC Characteristics

T_A = -40°C to 85°C, V_{CC} = 2.4V to 5.5V (unless otherwise noted)

Symbol	Parameter	Condition	Min	Max	Units
V_{IL}	Input Low-voltage	(Except RST)	-0.5	0.25 V_{CC}	V
V_{IL1}	Input Low-voltage	(RST)	-0.5	0.3 V_{CC}	V
V_{IH}	Input High-voltage	(Except RST)	0.65 V_{CC}	V_{CC} + 0.5	V
V_{IH1}	Input High-voltage	(RST)	0.6 V_{CC}	V_{CC} + 0.5	V
V_{OL}	Output Low-voltage (Ports 1, 3)(1)	I_{OL} = 10 mA, V_{CC} = 2.7V, T_A = 85°C		0.5	V
V_{OH}	Output High-voltage (Ports 1, 3) using Weak Pull-up(2)	I_{OH} = -80 µA, V_{CC} = 5V ±10%	2.4		V
		I_{OH} = -30 µA	0.75 V_{CC}		V
		I_{OH} = -12 µA	0.9 V_{CC}		V
V_{OH1}	Output High-voltage (Ports 1, 3) using Strong Pull-up(3)	I_{OH} = -10 mA, T_A = 85°C	0.9 V_{CC}		
I_{IL}	Logic 0 Input Current(2) (Ports 1, 3)	V_{IN} = 0.45V		-50	µA
I_{TL}	Logic 1 to 0 Transition Current(2) (Ports 1, 3)	V_{IN} = 2V, V_{CC} = 5V ±10%		-300	µA
I_{LI}	Input-Only Leakage Current	0 < V_{IN} < V_{CC}		±10	µA
V_{OS}	Comparator Input Offset Voltage	V_{CC} = 5V		20	mV
V_{CM}	Comparator Input Common Mode Voltage		0	V_{CC}	V
RRST	Reset Pull-down Resistor		50	150	kΩ
C_{IO}	Pin Capacitance	Test Freq. = 1 MHz, T_A = 25°C		10	pF
I_{CC}	Power Supply Current	Active Mode, 12 MHz, V_{CC} = 5.5V/3V		5.5/3.5	mA
		Idle Mode, 12 MHz, V_{CC} = 5.5V/3V		3/2	mA
	Power-down Mode(4)	V_{CC} = 5.5V		5	µA
		V_{CC} = 3V		2	µA

Notes:
1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per port pin: 10 mA
   Maximum total I_{OL} for all output pins: 15 mA
   If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
2. Port in Quasi-Bidirectional Mode
3. Port in Push-Pull Output Mode
4. Minimum V_{CC} for Power-down is 2V.

Figure 24-4. SPI Slave Timing (CPHA = 1)



24.4 External Clock Drive

Figure 24-5. External Clock Drive Waveform

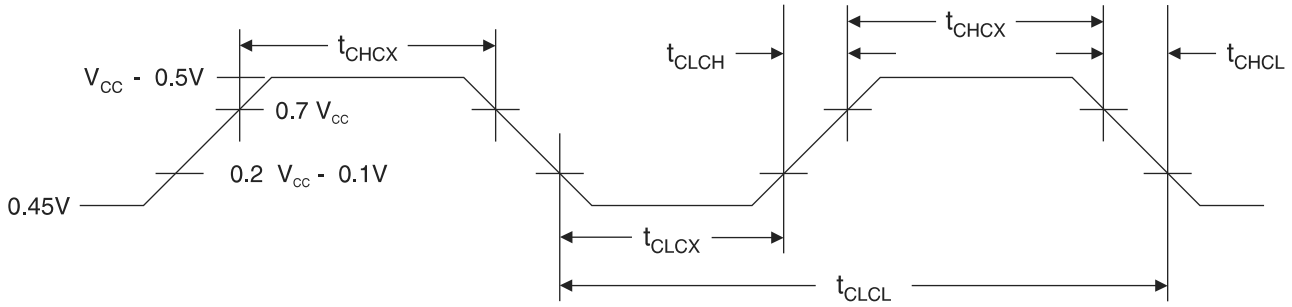


Table 24-3. External Clock Drive Parameters

Symbol	Parameter	V_{CC} = 2.4V to 5.5V		Units
		Min	Max	
$1/t_{CLCL}$	Oscillator Frequency	0	20	MHz
t_{CLCL}	Clock Period	50		ns
t_{CHCX}	High Time	12		ns
t_{CLCX}	Low Time	12		ns
t_{CLCH}	Rise Time		5	ns
t_{CHCL}	Fall Time		5	ns

25. Ordering Information

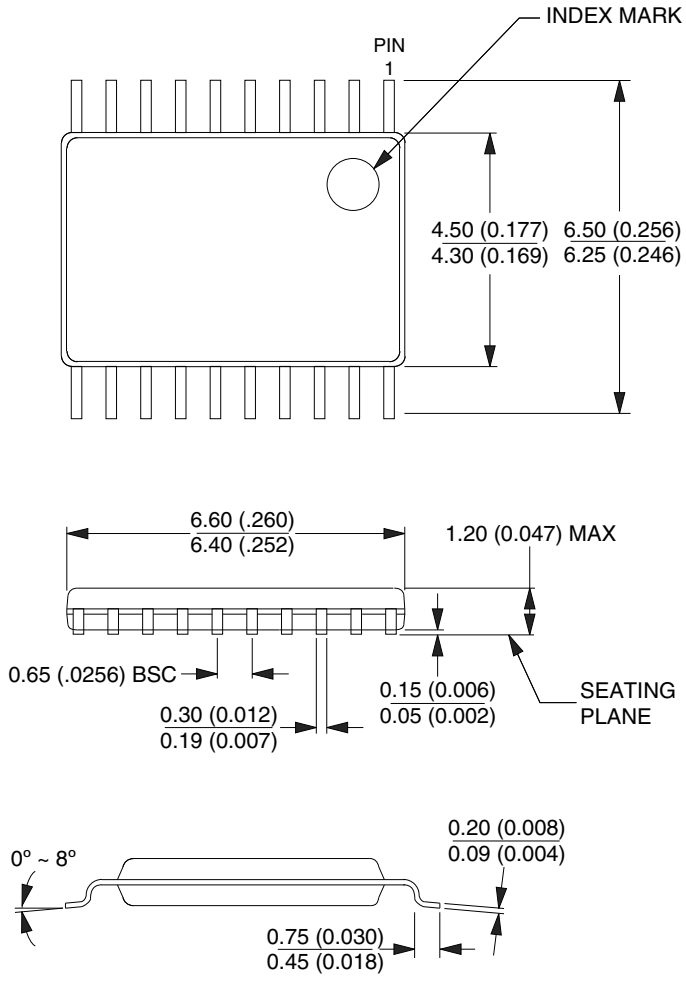
25.1 Green Package Option (Pb/Halide-free)

Speed (MHz)	Power Supply	Ordering Code	Package	Operation Range
20	2.4V to 5.5V	AT89LP2052-20PU	20P3	Industrial (-40· C to 85· C)
		AT89LP2052-20SU	20S2	
		AT89LP2052-20XU	20X	
		AT89LP4052-20PU	20P3	
		AT89LP4052-20SU	20S2	
		AT89LP4052-20XU	20X	

Package Type	
20P3	20-lead, 0.300” Wide, Plastic Dual In-line Package (PDIP)
20S2	20-lead, 0.300” Wide, Plastic Gull Wing Small Outline (SOIC)
20X	20-lead, 4.4 mm Body Width, Plastic Thin Shrink Small Outline Package (TSSOP)

26.3 20X – TSSOP

Dimensions in Millimeters and (Inches).
Controlling dimension: Millimeters.
JEDEC Standard MO-153 AC



10/23/03

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**20X**, (Formerly 20T), 20-lead, 4.4 mm Body Width, Plastic Thin Shrink Small Outline Package (TSSOP)	20X	C

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