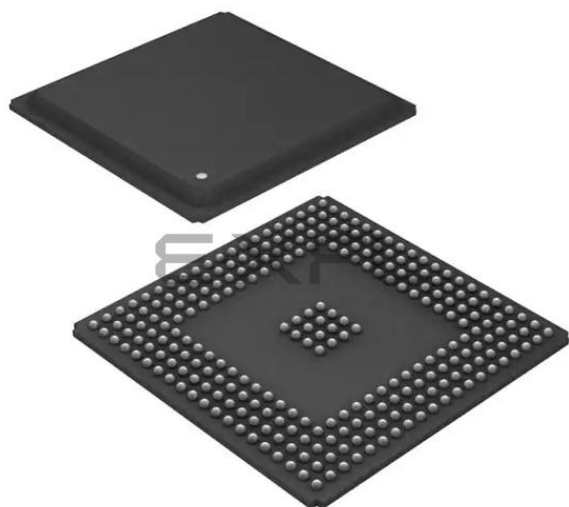




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Details

Product Status	Obsolete
Core Processor	PowerPC
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	CANbus, EBI/EMI, SCI, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	101
Program Memory Size	448KB (448K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	26K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 32x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	272-BBGA
Supplier Device Package	272-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc555lfmzp40r2

Product Brief

MPC555PB/D
Rev. 3, 2/2003

MPC555 Product Brief

This document provides an overview of the MPC555 microcontroller, including a block diagram showing the major modular components and sections that list the major features. The MPC555 member of the Freescale MPC500 RISC Microcontroller family.

Table 1. MPC555 Features

Device	Flash	Code Compression
MPC555	448 Kbytes	Code compression not supported

1 Introduction

The MPC555 device offers the following features:

- PowerPC™ core with floating-point unit
- 26 Kbytes fast RAM and 6 Kbytes TPU microcode RAM
- 448 Kbytes Flash EEPROM with 5-V programming
- 5-V I/O system
- Serial system: queued serial multi-channel module (QSMCM), dual CAN 2.0B controller modules (TouCAN™)
- 50-channel timer system: dual time processor units (TPU3), modular I/O system (MIOS1)
- 32 analog inputs: dual queued analog-to-digital converters (QADC64)
- Submicron HCMOS (CDR1) technology
- 272-pin plastic ball grid array (PBGA) packaging
- 40-MHz operation, -40 °C to 125 °C with dual supply (3.3 V, 5 V) (-55 °C to 125 °C for the suffix A device)
- 32-bit architecture (PowerPC ISA architecture compliant)
- Core performance measured at 52.7-Kbyte Dhrystones (v2.1) @ 40 MHz
- Fully static, low power operation
- Integrated double-precision floating-point unit
- Precise exception model

- Extensive system development support
 - On-chip watchpoints and breakpoints
 - Program flow tracking
 - BDM on-chip emulation development interface

1.1 Block Diagram

Figure 1 is a block diagram of the MPC555.

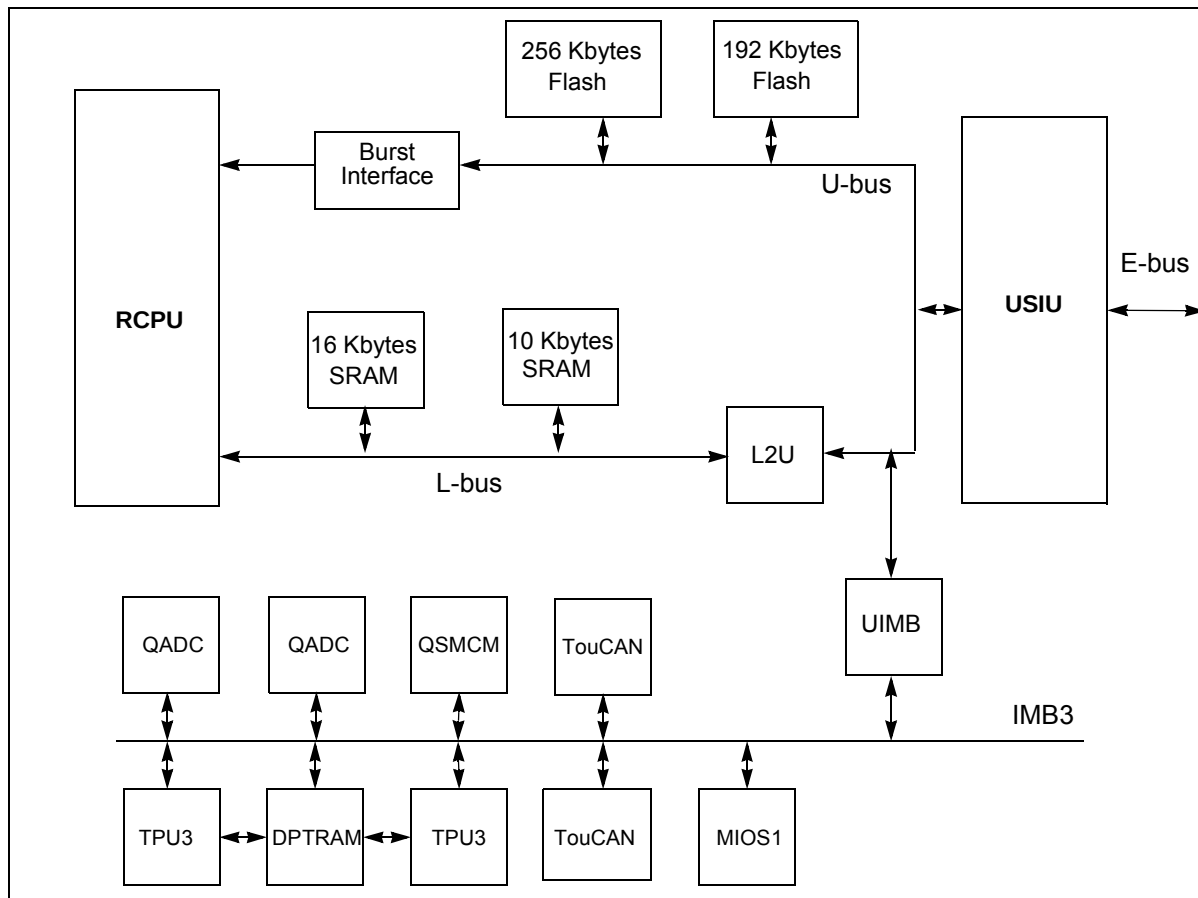


Figure 1. MPC555 Block Diagram

1.2 Key Features

The MPC555 key features are explained in the following sections.

1.2.1 Four-Bank Memory Controller

- Works with SRAM, EPROM, Flash EEPROM, and other peripherals
- Byte write enables
- 32-bit address decodes with bit masks

1.2.2 U-Bus System Interface Unit (USIU)

- Clock synthesizer
- Power management
- Reset controller
- MPC555 decrements and time base
- Real-time clock register
- Periodic interrupt timer
- Hardware bus monitor and software watchdog timer
- Interrupt controller that supports up to eight external and eight internal interrupts
- IEEE 1149.1 JTAG test access port
- External bus interface
 - 24 address pins, 32 data pins
 - Supports multiple master designs
 - Four-beat transfer bursts, two-clock minimum bus transactions
 - Supports 5V inputs, provides 3.3-V outputs

1.2.3 Flexible Memory Protection Unit

- Four instruction regions and four data regions
- 4-Kbyte to 16-Mbyte region size support
- Default attributes available in one global entry
- Attribute support for speculative accesses

1.2.4 448-Kbyte Flash EEPROM Memory

- One 256-Kbyte and one 192-Kbyte module
- Page read mode
- Block (32-Kbyte) erasable
- External 4.75-V to 5.25-V program and erase power supply

1.2.5 26-Kbytes of Static RAM

- One 16-Kbyte and one 10-Kbyte module
- Fast (one-clock) access
- Keep-alive power
- Soft defect detection (SDD)

1.2.6 General-Purpose I/O Support

- Address (24) and data (32) pins can be used for general-purpose I/O in single-chip mode
- Nine general-purpose I/O pins in MIO1 unit
- Many peripheral pins can be used for general-purpose I/O when not used for primary function
- 5-V tolerant inputs/outputs

1.2.7 Two Time Processor Units (TPU3)

- Each TPU3 module provides these features:
 - A dedicated micro-engine operates independently of the RCPu
 - 16 independent programmable channels and pins
 - Each channel has an event register consisting of a 16-bit capture register, a 16-bit compare register and a 16-bit comparator
 - Nine pre-programmed timer functions are available
 - Any channel can perform any time function
 - Each timer function can be assigned to more than one channel
 - Two timer count registers with programmable prescalers
 - Each channel can be synchronized to one or both counters
 - Selectable channel priority levels
 - 5-V tolerant inputs/outputs
- 6-Kbyte dual port TPU RAM (DPTRAM) is shared by the two TPU3 modules for TPU microcode

1.2.8 18-Channel Modular I/O System (MIOS1)

- Ten double action submodules (DASM)
- Eight dedicated PWM sub-modules (PWMSM)
- Two 16-bit modulus counter submodules (MCSM)
- Two parallel port I/O submodules (PIOSM)
- 5-V tolerant inputs/outputs

1.2.9 Two Queued Analog-to-Digital Converter Modules (QADC64)

Each QADC provides:

- Up to 16 analog input channels, using internal multiplexing
- Up to 41 total input channels, using internal and external multiplexing
- 10-bit A/D converter with internal sample/hold
- Typical conversion time of 10 μ s (100,000 samples per second)
- Two conversion command queues of variable length
- Automated queue modes initiated by:
 - External edge trigger/level gate
 - Software command
- 64 result registers
- Output data that is right- or left-justified, signed or unsigned
- 5-V reference and range

1.2.10 Two CAN 2.0B Controller Modules (TouCAN)

Each TouCAN provides these features:

- Full implementation of CAN protocol specification, version 2.0A and 2.0B
- Each module has 16 receive/transmit message buffers of 0 to 8 bytes data length
- Global mask register for message buffers 0 to 13
- Independent mask registers for message buffers 14 and 15
- Programmable transmit-first scheme: lowest ID or lowest buffer number
- 16-bit free-running timer for message time-stamping
- Low power sleep mode with programmable wake-up on bus activity
- Programmable I/O modes
- Maskable interrupts
- Independent of the transmission medium (external transceiver is assumed)
- Open network architecture
- Multimaster concept
- High immunity to EMI
- Short latency time for high-priority messages
- Low power sleep mode with programmable wakeup on bus activity

1.2.11 Queued Serial Multi-Channel Module (QSMCM)

- Queued serial peripheral interface (QSPI)
 - Provides full-duplex communication port for peripheral expansion or interprocessor communication
 - Up to 32 preprogrammed transfers, reducing overhead
 - 160-byte queue buffer
 - Programmable transfer length: from 8 to 16 bits, inclusive
 - Synchronous interface with baud rate of up to system clock divided by 4
 - Four programmable peripheral-select pins support up to 16 devices
 - Wrap-around mode allows continuous sampling for efficient interfacing to serial peripherals (e.g., – serial A/D converters, I/O latches, etc.)
- Two serial communications interfaces (SCI). Each SCI offers these features:
 - UART mode provides NRZ format and half-or full-duplex interface
 - 16 register receive buffer and 16 register transmit buffer (SCI1 only)
 - Advanced error detection and optional parity generation and detection
 - Word length programmable as 8 or 9 bits
 - Separate transmitter and receiver enable bits and double buffering of data
 - Wakeup functions allow the CPU to run uninterrupted until either a true idle line is detected or a new address byte is received
 - External source clock for baud generation
 - Multiplexing of transmit data pins with discrete outputs and receive data pins with discrete inputs, allowing realization of a low-speed serial protocol

2 MPC555 Address Map

The internal memory map is shown in Figure 2.

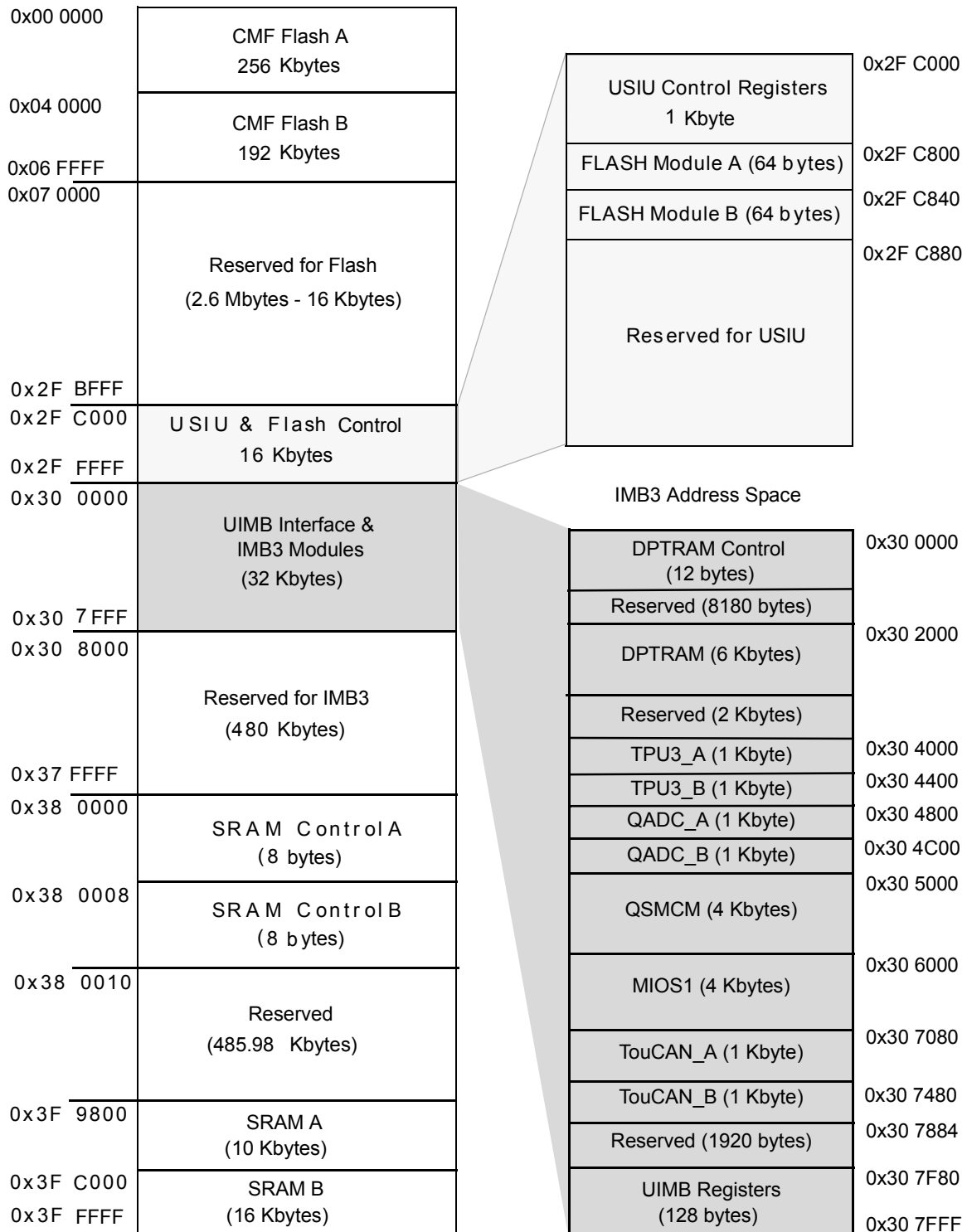


Figure 2. MPC555 Internal Memory Map

3 MPC555 Pinout Diagram

Figure 3 shows the pinout for the MPC555.

MPC555
Ball Map

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
A	VDDH	A_TPUCH1	A_TPUCH4	A_TPUCH8	A_TPUCH12	A_TPUCH16	VRL	AA0_P0B0	AA04_P0B4	AA08_P0B8	AA12_P0B12	AA16_P0B16	AA20_P0B20	BA0_P0B0	BA04_P0B4	BA08_P0B8	BA12_P0B12	BA16_P0B16	BA20_P0B20	VDDH	
B	B_T2CLK	VDDH	A_TPUCH8	A_TPUCH10	A_TPUCH11	A_TPUCH14	VRH	AA08_P0B8	AA16_P0B16	AA24_P0B24	AA32_P0B32	AA40_P0B40	AA48_P0B48	BA04_P0B4	BA12_P0B12	BA20_P0B20	BA28_P0B28	BA36_P0B36	BA44_P0B44	VDDH	
C	B_TPUCH15	A_T2CLK	A_TPUCH0	A_TPUCH7	A_TPUCH0	A_TPUCH13	VDDA	AA02_P0B2	AA06_P0B6	AA10_P0B10	AA14_P0B14	AA18_P0B18	AA22_P0B22	BA06_P0B6	BA14_P0B14	BA22_P0B22	BA30_P0B30	BA38_P0B38	BA46_P0B46	MDA31	
D	B_TPUCH11	B_TPUCH13	A_TPUCH0	A_TPUCH2	A_TPUCH5	VDDI	VSSA	AA01_P0B1	AA05_P0B5	AA09_P0B9	AA13_P0B13	AA17_P0B17	AA21_P0B21	BA01_P0B1	BA05_P0B5	BA09_P0B9	BA13_P0B13	BA17_P0B17	BA21_P0B21	MPWM2	
E	B_TPUCH7	B_TPUCH10	B_TPUCH14	VDDL																MPWM3	
F	B_TPUCH5	B_TPUCH6	B_TPUCH8	B_TPUCH12																MPWM19	
G	B_TPUCH2	B_TPUCH3	B_TPUCH4	B_TPUCH9																MPIC9	
H	B_TPUCH1	B_TPUCH0	B_ONRX0	B_ONTX0																MPIC10	
J	TOK_DS0CK	TDO_DS00	TRST_B	VDDSRAM																MPIC12	
K	TMS	TDI_DS01	SGP_FRZ	VDDL																MPIC14	
L	IMP1_VFLS	IMP0_VFLS	IRQ3B_SGP	IRQ4B_SGP																MPIC15	
M	IRQ0B_SGP	IRQ1B_SGP	IRQ2B_SGP	SGP_IRQOUTB																MPIC16	
N	WEB_AT[0]	BRB_WP2	BBB_WP1	BBB_WP3																MPIC17	
P	WEB_AT[1]	WEB_AT[2]	WEB_AT[3]	CS0B																MPIC18	
R	RD_WRB	CS0B	CS1B	CS1B																MPIC19	
T	OEB	TEAB	TSIZ1	VDDL																MPIC20	
U	TSIZ0	TAB	TSB	BDPB	VDDI	Addr_SGP14	Addr_SGP30	Addr_SGP28	Addr_SGP26	VDDL	Data_SGP24	Data_SGP28	Data_SGP27	Data_SGP25	Data_SGP23	Data_SGP21	Data_SGP19	PCB_TXP	EXTCLK	XTAL	
V	BURSTB	BIB_STSB	Addr_SGP11	Addr_SGP10	Addr_SGP9	Addr_SGP8	Addr_SGP27	Addr_SGP21	Data_SGP30	Data_SGP28	Data_SGP26	Data_SGP24	Data_SGP22	Data_SGP20	Data_SGP18	Data_SGP16	Data_SGP14	CLKOUT	PORESETB	SRESETB	
W	Addr_SGP12	VDDH	Addr_SGP14	Addr_SGP16	Addr_SGP18	Addr_SGP20	Addr_SGP22	Addr_SGP24	Data_SGP1	Data_SGP3	Data_SGP5	Data_SGP7	Data_SGP9	Data_SGP11	Data_SGP13	Data_SGP15	Data_SGP17	ROCB_SGP	HRESETB		
Y	VDDH	Addr_SGP13	Addr_SGP15	Addr_SGP17	Addr_SGP19	Addr_SGP21	Addr_SGP23	Addr_SGP25	Data_SGP0	Data_SGP2	Data_SGP4	Data_SGP6	Data_SGP8	Data_SGP10	Data_SGP12	Data_SGP14	Data_SGP16	Data_SGP18	IRQ0B_m02	IRQ7B_m02	VDDH
	VDDH		+3 volt power (I/O)	VDDI1		+3 volt power (internal)			VSS	-ground					VDDH	=5 volt power				-Misc power	

Substrate 9/30/97a

21 November 1997

Version 10.2

Dees

Figure 3. MPC555 Pinout Diagram

4 Supporting Documentation List

This list contains references to currently available and planned documentation.

- *MPC555 User's Manual* (MPC555UM/AD)
- *RCPUR Reference Manual* (RCPURM/AD)
- *Board Strategies for Ensuring Optimum Frequency Synthesizer Performance* (AN1282/D)
- *Using the MIOS on the MPC555 Evaluation Board* (AN1778/D)
- *Exception Table Relocation and Multi-Processor Address Mapping in the Embedded MPC5XX Family* (AN1821/D)
- *Non-Volatile Memory Technology Overview* (AN1837/D)
- *Designing Expansion Boards for the Freescale EVB555/ETAS ES200* (AN2001/D)
- *MPC555 Interrupts* (AN2109/D)
- *EMC Guidelines for MPC500-Based Automotive Powertrain Systems* (AN2127/D)
- Nexus Standard Specification (non-Freescale document)
- Nexus Web Site: <http://www.nexus5001.org/>
- IEEE 1149.1 Specification (non-Freescale document)

5 Revision History

Table 2. Revision History

Revision Number	Substantive Changes	Date of Release
2	Existing Document.	September 2001
2.1	Added temperature range for suffix A device.	11 December 2002
3	Updated template and formats.	11 February 2003



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