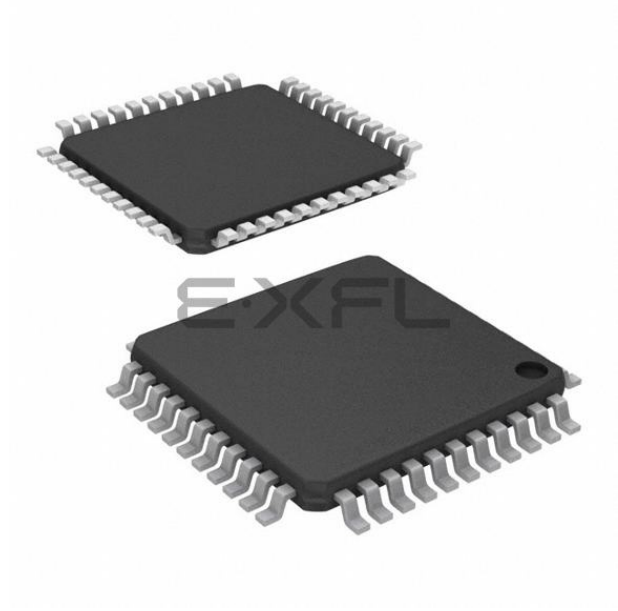


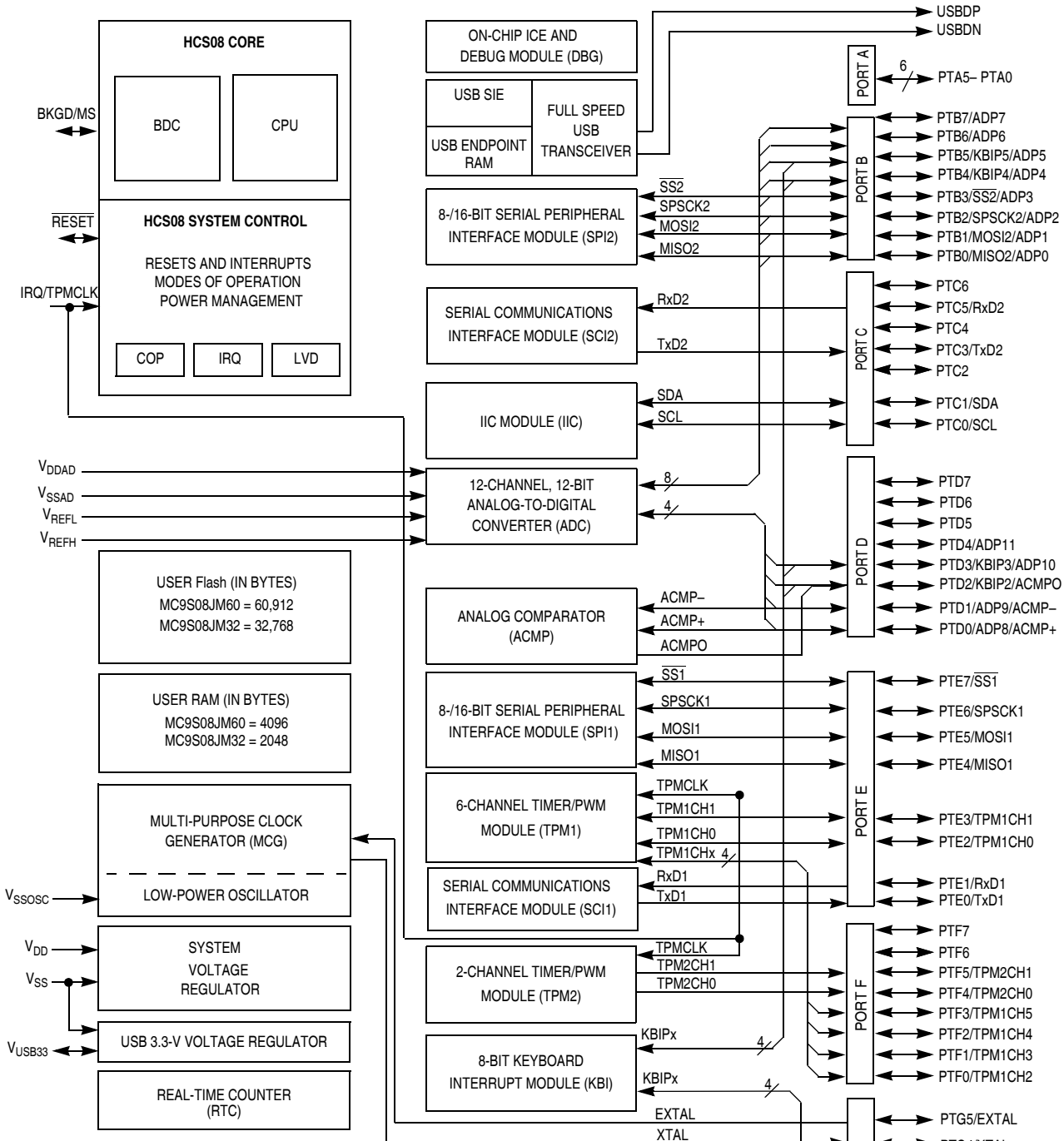
Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	S08
Core Size	8-Bit
Speed	48MHz
Connectivity	I²C, LINbus, SCI, SPI, USB
Peripherals	LVD, POR, PWM, WDT
Number of I/O	33
Program Memory Size	60KB (60K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 8x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	44-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9s08jm60cldr



NOTES:
1. Port pins are software configurable with pullup device if input port.
2. Pin contains software configurable pullup/pull-down device if IRQ is enabled (IRQPE = 1). Pull-down is enabled if rising edge detect is selected (IRQEDG = 1)
3. IRQ does not have a clamp diode to V_{DD}. IRQ must not be driven above V_{DD}.
4. Pin contains integrated pullup device.
5. When pin functions as KBI (KBIPEn = 1) and associated pin is configured to enable the pullup device, KBEDGn can be used to reconfigure the pullup as a pull-down device.

Figure 1-1. MC9S08JM60 Series Block Diagram

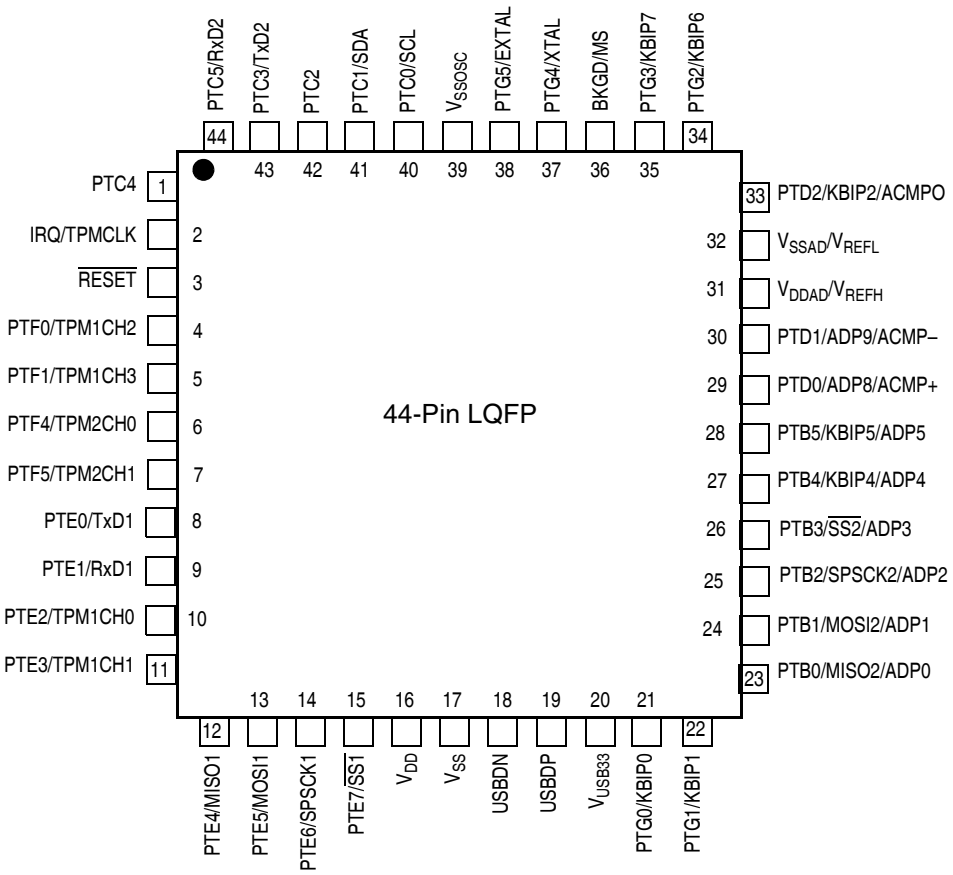


Figure 2-3. MC9S08JM60 Series in 44-Pin LQFP Package

2.3 Recommended System Connections

Figure 2-4 shows pin connections that are common to almost all MC9S08JM60 series application systems.

writing to PPDACK, the pins will be controlled by their associated port control registers when the I/O latches are opened.

3.6.3 On-Chip Peripheral Modules in Stop Modes

When the MCU enters any stop mode, system clocks to the internal peripheral modules are stopped. Even in the exception case (ENBDM = 1), where clocks to the background debug logic continue to operate, clocks to the peripheral systems are halted to reduce power consumption. Refer to Section 3.6.2, "Stop2 Mode," and Section 3.6.1, "Stop3 Mode," for specific information on system behavior in stop modes.

Table 3-2. Stop Mode Behavior

Peripheral	Mode	
	Stop2	Stop3
CPU	Off	Standby
RAM	Standby	Standby
Flash	Off	Standby
Parallel Port Registers	Off	Standby
ADC	Off	Optionally On[1]
ACMP	Off	Optionally On[2]
MCG	Off	Optionally On[3]
IIC	Off	Standby
RTC	Optionally on[4]	Optionally on[4]
SCI	Off	Standby
SPI	Off	Standby
TPM	Off	Standby
System Voltage Regulator	Off	Standby
XOSC	Off	Optionally On[5]
I/O Pins	States Held	States Held
USB (SIE and Transceiver)	Off	Optionally On[6]
USB 3.3-V Regulator	Off	Standby
USB RAM	Standby	Standby

1 Requires the asynchronous ADC clock and LVD to be enabled, else in standby.

2 If ACGBS in ACMPSC is set, LVD must be enabled, else in standby.

3 IRCLKEN and IREFSTEN set in MCGC1, else in standby.

4 RTCPS[3:0] in RTCSC does not equal 0 before entering stop, else off.

5 ERCLKEN and EREFSTEN set in MCGC2, else in standby. For high frequency range (RANGE in MCGC2 set) requires the LVD to also be enabled in stop3.

6 USBEN in CTL is set and USBPHYEN in USBCTL0 is set, else off.

	7	6	5	4	3	2	1	0
R W		PTCPE6	PTCPE5	PTCPE4	PTCPE3	PTCPE2	PTCPE1	PTCPE0
Reset	0	0	0	0	0	0	0	0

Figure 6-14. Internal Pullup Enable for Port C (PTCPE)

Table 6-13. PTCPE Register Field Descriptions

Field	Description
6:0 PTCPE[6:0]	**Internal Pullup Enable for Port C Bits** — Each of these control bits determines if the internal pullup device is enabled for the associated PTC pin. For port C pins that are configured as outputs, these bits have no effect and the internal pullup devices are disabled. 0 Internal pullup device disabled for port C bit n. 1 Internal pullup device enabled for port C bit n.

	7	6	5	4	3	2	1	0
R W		PTCSE6	PTCSE5	PTCSE4	PTCSE3	PTCSE2	PTCSE1	PTCSE0
Reset	0	1	1	1	1	1	1	1

Figure 6-15. Output Slew Rate Control Enable for Port C (PTCSE)

Table 6-14. PTCSE Register Field Descriptions

Field	Description
6:0 PTCSE[6:0]	**Output Slew Rate Control Enable for Port C Bits** — Each of these control bits determine whether output slew rate control is enabled for the associated PTC pin. For port C pins that are configured as inputs, these bits have no effect. 0 Output slew rate control disabled for port C bit n. 1 Output slew rate control enabled for port C bit n.

	7	6	5	4	3	2	1	0
R W		PTCDS6	PTCDS5	PTCDS4	PTCDS3	PTCDS2	PTCDS1	PTCDS0
Reset	0	0	0	0	0	0	0	0

Figure 6-16. Output Drive Strength Selection for Port C (PTCDS)

Table 6-15. PTCDS Register Field Descriptions

Field	Description
6:0 PTCDS[6:0]	**Output Drive Strength Selection for Port C Bits** — Each of these control bits selects between low and high output drive for the associated PTC pin. 0 Low output drive enabled for port C bit n. 1 High output drive enabled for port C bit n.

	7	6	5	4	3	2	1	0
R W	PTFPE7	PTFPE6	PTFPE5	PTFPE4	PTFPE3	PTFPE2	PTFPE1	PTFPE0
Reset	0	0	0	0	0	0	0	0

Figure 6-29. Internal Pullup Enable for Port F (PTFPE)

Table 6-28. PTFPE Register Field Descriptions

Field	Description
7:0 PTFPE[7:0]	**Internal Pullup Enable for Port F Bits** — Each of these control bits determines if the internal pullup device is enabled for the associated PTF pin. For port F pins that are configured as outputs, these bits have no effect and the internal pullup devices are disabled. 0 Internal pullup device disabled for port F bit n. 1 Internal pullup device enabled for port F bit n.

	7	6	5	4	3	2	1	0
R W	PTFSE7	PTFSE6	PTFSE5	PTFSE4	PTFSE3	PTFSE2	PTFSE1	PTFSE0
Reset	1	1	1	1	1	1	1	1

Figure 6-30. Output Slew Rate Control Enable for Port F (PTFSE)

Table 6-29. PTFSE Register Field Descriptions

Field	Description
7:0 PTFSE[7:0]	**Output Slew Rate Control Enable for Port F Bits** — Each of these control bits determine whether output slew rate control is enabled for the associated PTF pin. For port F pins that are configured as inputs, these bits have no effect. 0 Output slew rate control disabled for port F bit n. 1 Output slew rate control enabled for port F bit n.

	7	6	5	4	3	2	1	0
R W	PTFDS7	PTFDS6	PTFDS5	PTFDS4	PTFDS3	PTFDS2	PTFDS1	PTFDS0
Reset	0	0	0	0	0	0	0	0

Figure 6-31. Output Drive Strength Selection for Port F (PTFDS)

Table 6-30. PTFDS Register Field Descriptions

Field	Description
7:0 PTFDS[7:0]	**Output Drive Strength Selection for Port F Bits** — Each of these control bits selects between low and high output drive for the associated PTF pin. 0 Low output drive enabled for port F bit n. 1 High output drive enabled for port F bit n.

Table 7-2. . Instruction Set Summary (Sheet 8 of 9)

Source Form	Operation	Address Mode	Object Code	Cycles	Cyc-by-Cyc Details	Affect on CCR	
						VH	I N Z C

SUB #*opr8i*
SUB *opr8a*
SUB *opr16a*
SUB *oprx16*,X
SUB *oprx8*,X
SUB ,X
SUB *oprx16*,SP
SUB *oprx8*,SP
	Subtract
	A ← (A) – (M)
		IMM
		DIR
		EXT
		IX2
		IX1
		IX
		SP2
		SP1
			A0 ii
			B0 dd
			C0 hh ll
			D0 ee ff
			E0 ff
			F0
			9E D0 ee ff
			9E E0 ff
				2
				3
				4
				4
				3
				3
				5
				4
					pp
					rpp
					prpp
					prpp
					rpp
					rfp
					pprpp
					prpp
						↕ –	– ↕ ↕ ↕

SWI	Software Interrupt PC ← (PC) + $0001 Push (PCL); SP ← (SP) – $0001 Push (PCH); SP ← (SP) – $0001 Push (X); SP ← (SP) – $0001 Push (A); SP ← (SP) – $0001 Push (CCR); SP ← (SP) – $0001 I ← 1; PCH ← Interrupt Vector High Byte PCL ← Interrupt Vector Low Byte	INH	83	11	ssssvvfppp	– –	1 – – –
TAP	Transfer Accumulator to CCR CCR ← (A)	INH	84	1	p	↕ ↕	↕ ↕ ↕ ↕
TAX	Transfer Accumulator to X (Index Register Low) X ← (A)	INH	97	1	p	– –	– – – –
TPA	Transfer CCR to Accumulator A ← (CCR)	INH	85	1	p	– –	– – – –
TST *opr8a* TSTA TSTX TST *oprx8*,X TST ,X TST *oprx8*,SP	Test for Negative or Zero (M) – $00 (A) – $00 (X) – $00 (M) – $00 (M) – $00 (M) – $00	DIR INH INH IX1 IX SP1	3D dd 4D 5D 6D ff 7D 9E 6D ff	4 1 1 4 3 5	rfpp p p rfpp rfp prfpp	0 –	– ↕ ↕ –
TSX	Transfer SP to Index Reg. H:X ← (SP) + $0001	INH	95	2	fp	– –	– – – –
TXA	Transfer X (Index Reg. Low) to Accumulator A ← (X)	INH	9F	1	p	– –	– – – –

11.7 Initialization/Application Information

Module Initialization (Slave)

1. Write: IICC2
   - to enable or disable general call
   - to select 10-bit or 7-bit addressing mode
2. Write: IICA
   - to set the slave address
3. Write: IICC1
   - to enable IIC and interrupts
4. Initialize RAM variables (IICEN = 1 and IICIE = 1) for transmit data
5. Initialize RAM variables used to achieve the routine shown in Figure 11-12

Module Initialization (Master)

1. Write: IICF
   - to set the IIC baud rate (example provided in this chapter)
2. Write: IICC1
   - to enable IIC and interrupts
3. Initialize RAM variables (IICEN = 1 and IICIE = 1) for transmit data
4. Initialize RAM variables used to achieve the routine shown in Figure 11-12
5. Write: IICC1
   - to enable TX

Register Model

IICA	AD[7:1]							0
	When addressed as a slave (in slave mode), the module responds to this address							
IICF	MULT		ICR					
	Baud rate = BUSCLK / (2 x MULT x (SCL DIVIDER))							
IICC1	IICEN	IICIE	MST	TX	TXAK	RSTA	0	0
	Module configuration							
IICS	TCF	IAAS	BUSY	ARBL	0	SRW	IICIF	RXAK
	Module status flags							
IICD	DATA							
	Data register; Write to transmit IIC data read to read IIC data							
IICC2	GCAEN	ADEXT	0	0	0	AD10	AD9	AD8
	Address configuration							

Figure 11-11. IIC Module Quick Start

12.1.1 Features

Key features of the MCG module are:

- Frequency-locked loop (FLL)
  - 0.2% resolution using internal 32-kHz reference
  - 2% deviation over voltage and temperature using internal 32-kHz reference
  - Internal or external reference can be used to control the FLL
- Phase-locked loop (PLL)
  - Voltage-controlled oscillator (VCO)
  - Modulo VCO frequency divider
  - Phase/Frequency detector
  - Integrated loop filter
  - Lock detector with interrupt capability
- Internal reference clock
  - Nine trim bits for accuracy
  - Can be selected as the clock source for the MCU
- External reference clock
  - Control for external oscillator
  - Clock monitor with reset capability
  - Can be selected as the clock source for the MCU
- Reference divider is provided
- Clock source selected can be divided down by 1, 2, 4, or 8
- BDC clock (MCGLCLK) is provided as a constant divide by 2 of the DCO output whether in an FLL or PLL mode.

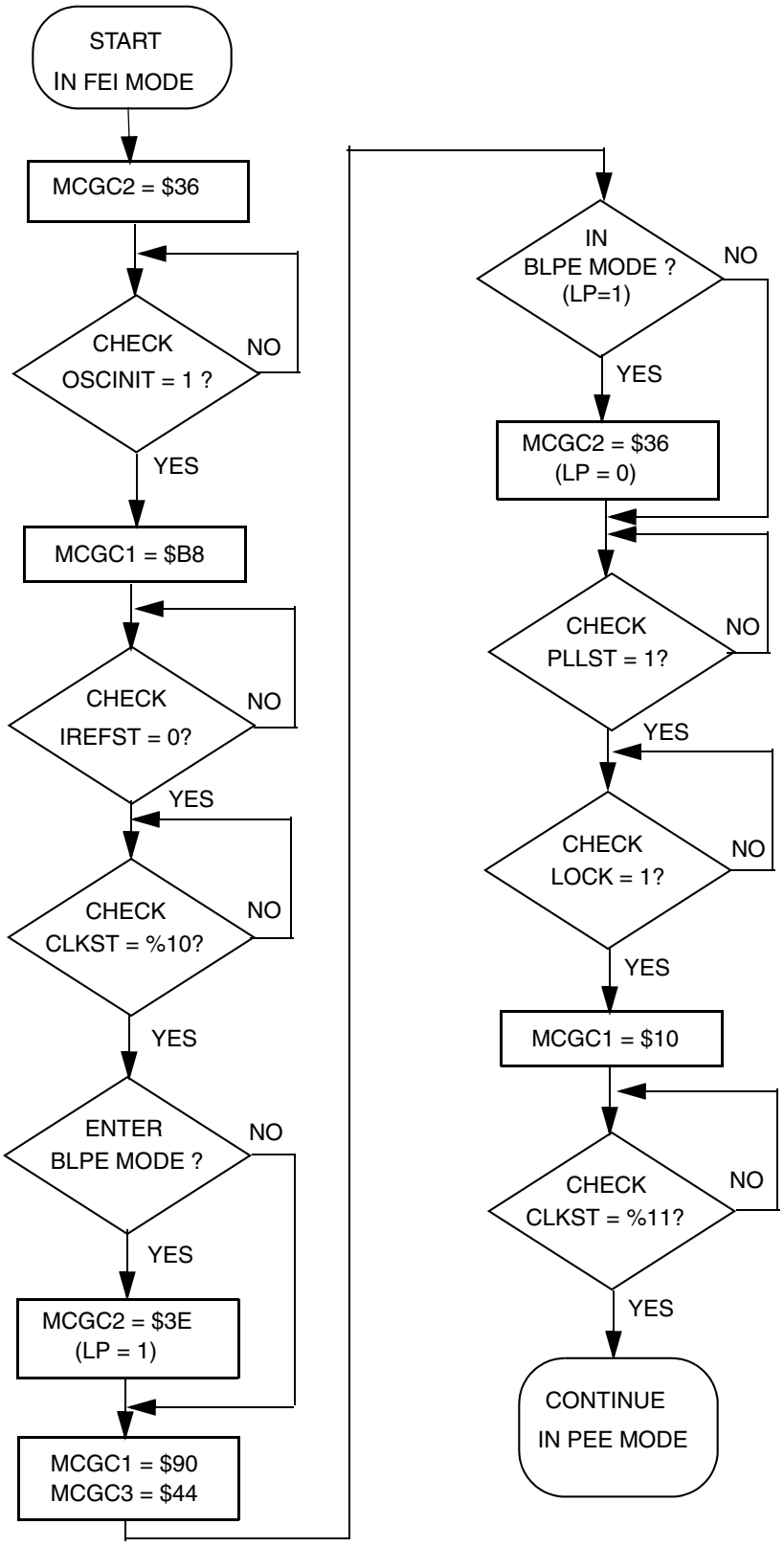


Figure 12-9. Flowchart of FEI to PEE Mode Transition using a 4 MHz Crystal

the flag bits to determine what event caused the interrupt. The service routine should also clear the flag bit(s) before returning from the ISR (usually near the beginning of the ISR).

15.4.10.1 MODF

MODF occurs when the master detects an error on the $\overline{SS}$ pin. The master SPI must be configured for the MODF feature (see Table 15-2). Once MODF is set, the current transfer is aborted and the following bit is changed:

- MSTR=0, The master bit in SPIxC1 resets.

The MODF interrupt is reflected in the status register MODF flag. Clearing the flag will also clear the interrupt. This interrupt will stay active while the MODF flag is set. MODF has an automatic clearing process which is described in Section 15.3.4, “SPI Status Register (SPIxS).”

15.4.10.2 SPRF

SPRF occurs when new data has been received and copied to the SPI receive data buffer. In 8-bit mode, SPRF is set only after all 8 bits have been shifted out of the shift register and into SPIxDL. In 16-bit mode, SPRF is set only after all 16 bits have been shifted out of the shift register and into SPIxDH:SPIxDL.

Once SPRF is set, it does not clear until it is serviced. SPRF has an automatic clearing process which is described in Section 15.3.4, “SPI Status Register (SPIxS).” In the event that the SPRF is not serviced before the end of the next transfer (i.e. SPRF remains active throughout another transfer), the latter transfers will be ignored and no new data will be copied into the SPIxDH:SPIxDL.

15.4.10.3 SPTEF

SPTEF occurs when the SPI transmit buffer is ready to accept new data. In 8-bit mode, SPTEF is set only after all 8 bits have been moved from SPIxDL into the shifter. In 16-bit mode, SPTEF is set only after all 16 bits have been moved from SPIxDH:SPIxDL into the shifter.

Once SPTEF is set, it does not clear until it is serviced. SPTEF has an automatic clearing process which is described in Section 15.3.4, “SPI Status Register (SPIxS).

15.4.10.4 SPMF

SPMF occurs when the data in the receive data buffer is equal to the data in the SPI match register. In 8-bit mode, SPMF is set only after bits 8–0 in the receive data buffer are determined to be equivalent to the value in SPIxML. In 16-bit mode, SPMF is set after bits 15–0 in the receive data buffer are determined to be equivalent to the value in SPIxMH:SPIxML.

Table 16-6. Mode, Edge, and Level Selection

CPWMS	MSnB:MSnA	ELSnB:ELSnA	Mode	Configuration
X	XX	00	Pin not used for TPM - revert to general purpose I/O or other peripheral control	
0	00	01	Input capture	Capture on rising edge only
		10		Capture on falling edge only
		11		Capture on rising or falling edge
	01	01	Output compare	Toggle output on compare
		10		Clear output on compare
		11		Set output on compare
	1X	10	Edge-aligned PWM	High-true pulses (clear output on compare)
		X1		Low-true pulses (set output on compare)
1	XX	10	Center-aligned PWM	High-true pulses (clear output on compare-up)
		X1		Low-true pulses (set output on compare-up)

16.3.5 TPM Channel Value Registers (TPMxCnVH:TPMxCnVL)

These read/write registers contain the captured TPM counter value of the input capture function or the output compare value for the output compare or PWM functions. The channel registers are cleared by reset.

	7	6	5	4	3	2	1	0
R W	Bit 15	14	13	12	11	10	9	Bit 8
Reset	0	0	0	0	0	0	0	0

Figure 16-13. TPM Channel Value Register High (TPMxCnVH)

	7	6	5	4	3	2	1	0
R W	Bit 7	6	5	4	3	2	1	Bit 0
Reset	0	0	0	0	0	0	0	0

Figure 16-14. TPM Channel Value Register Low (TPMxCnVL)

When the external clock source shares the TPM channel pin, this pin should not be used for other channel timing functions. For example, it would be ambiguous to configure channel 0 for input capture when the TPM channel 0 pin was also being used as the timer external clock source. (It is the user's responsibility to avoid such settings.) The TPM channel could still be used in output compare mode for software timing functions (pin controls set not to affect the TPM channel pin).

16.4.1.2 Counter Overflow and Modulo Reset

An interrupt flag and enable are associated with the 16-bit main counter. The flag (TOF) is a software-accessible indication that the timer counter has overflowed. The enable signal selects between software polling (TOIE=0) where no hardware interrupt is generated, or interrupt-driven operation (TOIE=1) where a static hardware interrupt is generated whenever the TOF flag is equal to one.

The conditions causing TOF to become set depend on whether the TPM is configured for center-aligned PWM (CPWMS=1). In the simplest mode, there is no modulus limit and the TPM is not in CPWMS=1 mode. In this case, the 16-bit timer counter counts from 0x0000 through 0xFFFF and overflows to 0x0000 on the next counting clock. TOF becomes set at the transition from 0xFFFF to 0x0000. When a modulus limit is set, TOF becomes set at the transition from the value set in the modulus register to 0x0000. When the TPM is in center-aligned PWM mode (CPWMS=1), the TOF flag gets set as the counter changes direction at the end of the count value set in the modulus register (that is, at the transition from the value set in the modulus register to the next lower count value). This corresponds to the end of a PWM period (the 0x0000 count value corresponds to the center of a period).

16.4.1.3 Counting Modes

The main timer counter has two counting modes. When center-aligned PWM is selected (CPWMS=1), the counter operates in up/down counting mode. Otherwise, the counter operates as a simple up counter. As an up counter, the timer counter counts from 0x0000 through its terminal count and then continues with 0x0000. The terminal count is 0xFFFF or a modulus value in TPMxMODH:TPMxMODL.

When center-aligned PWM operation is specified, the counter counts up from 0x0000 through its terminal count and then down to 0x0000 where it changes back to up counting. Both 0x0000 and the terminal count value are normal length counts (one timer clock period long). In this mode, the timer overflow flag (TOF) becomes set at the end of the terminal-count period (as the count changes to the next lower count value).

16.4.1.4 Manual Counter Reset

The main timer counter can be manually reset at any time by writing any value to either half of TPMxCNTH or TPMxCNTL. Resetting the counter in this manner also resets the coherency mechanism in case only half of the counter was read before resetting the count.

16.4.2 Channel Mode Selection

Provided CPWMS=0, the MSnB and MSnA control bits in the channel n status and control registers determine the basic mode of operation for the corresponding channel. Choices include input capture, output compare, and edge-aligned PWM.

	7	6	5	4	3	2	1	0
R	0	0	ID5	ID4	ID3	ID2	ID1	ID0
W								
Reset	0	0	0	0	0	1	0	0

= Unimplemented or Reserved

Figure 17-4. Peripheral ID Register (PERID)

Table 17-5. PERID Field Descriptions

Field	Description
5:0 ID[5:0]	**Peripheral Configuration Number** —This number is set to 0x04 and indicates that the peripheral is the full-speed USB module.

17.3.3 Peripheral ID Complement Register (IDCOMP)

The IDCOMP reads back the complement of the peripheral ID register. For the USB module peripheral this will be 0xFB.

	7	6	5	4	3	2	1	0
R	1	1	NID5	NID4	NID3	NID2	NID1	NID0
W								
Reset	1	1	1	1	1	0	1	1

= Unimplemented or Reserved

Figure 17-5. Peripheral ID Complement Register (IDCOMP)

Table 17-6. IDCOMP Field Descriptions

Field	Description
5:0 NID[5:0]	**Compliment ID Number** — One's complement version of ID[5:0].

17.3.4 Peripheral Revision Register (REV)

The REV reads back the value of the USB peripheral revision.

	7	6	5	4	3	2	1	0
R	REV7	REV6	REV5	REV4	REV3	REV2	REV1	REV0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 17-6. Peripheral Revision Register (REV)

17.4.1.5 USB On-Chip Voltage Regulator (VREG)

The on-chip 3.3-V regulator provides a stable power source to power the USB internal transceiver and provide for the termination of an internal or external pullup resistor. When the on-chip regulator is enabled, it requires a voltage supply input in the range from 3.9 V to 5.5 V, and the voltage regulator output will be in the range of 3.0 V to 3.6 V.

With a dedicated on-chip USB 3.3-V regulator and a separate power supply for the MCU, the MCU and USB can operate at different voltages (See the USB electricals regarding the USB voltage regulator electrical characteristics). When the on-chip 3.3-V regulator is disabled, a 3.3-V source must be provided through the V_{USB33} pin to power the USB transceiver. In this case, the power supply voltage to the MCU must not fall below the input voltage at the V_{USB33} pin.

The 3.3-V regulator has 3 modes including:

- Active mode — This mode is entered when USB is active. Current requirement is sufficient to power the transceiver and the USBDP pullup resistor.
- Standby — The voltage regulator standby mode is entered automatically when the USB device is in suspend mode. When the USB device is forced into suspend mode by the USB bus, the firmware must configure the MCU for stop3 mode. In standby mode, the requirement is to maintain the USBDP pin voltage at 3.0 V to 3.6 V, with a 900 Ω (worst-case) pullup.
- Power off — This mode is entered anytime when stop2 or stop1 is entered or when the voltage regulator is disabled.

17.4.1.6 USB On-Chip USBDP Pullup Resistor

The pullup resistor on the USBDP line required for full-speed operation by the USB Specification Rev. 2.0 can be internal or external to the MCU, depending on the application requirements. An on-chip pullup resistor, implemented as specified in the USB 2.0 resistor ECN, is optionally available via firmware configuration. Alternatively, this on-chip pullup resistor can be disabled, and the USB module can be configured to use an external pullup resistor for the USBDP line instead. If using an external pullup resistor on the USBDP line, the resistor must comply with the requirements in the USB 2.0 resistor ECN found at http://www.usb.org.

The USBPU bit in the USBCTL0 register can be used to indicate if the pullup resistor is internal or external to the MCU. If USBPU is clear, the internal pullup resistor on USBDP is disabled, and an external USBDP pullup can be used. When using an external USBDP pullup, if the voltage regulator is enabled, the V_{USB33} voltage output can be used with the USBDP pullup. While the use of the internal USBDP pullup resistor is generally recommended, the figure below shows the USBDP pullup resistor configuration for a USB device using an external resistor tied to V_{USB33}.

17.4.6 Suspend/Resume

The USB supports a single low-power mode called suspend. Getting into and out of the suspend state is described in the following sections.

17.4.6.1 Suspend

The USB host can put a single device or the entire bus into the suspend state at any time. The MCU supports suspend mode for low power. Suspend mode will be entered when the USB data lines are in the idle state for more than 3 ms. Entry into suspend mode is announced by the SLEEPF bit in the INTSTAT register.

Per the USB specification, a low-power bus-powered USB device is required to draw less than 500 µA in suspend state. A high-power device that supports remote wakeup and has its remote wake-up feature enabled by the host can draw up to 2.5 mA of current. After the initial 3-ms idle, the USB device will reach this state within 7 ms. This low-current requirement means that firmware is responsible for entering stop3 mode once the SLEEPF flag has been set and before the USB module has been placed in the suspend state.

On receipt of resume signaling from the USB, the module can generate an asynchronous interrupt to the MCU which brings the device out of stop mode and wakes up the clocks. Setting the USBRESMEN bit in the USBCTL0 register immediately after the SLEEPF bit is set enables this asynchronous notification feature. The USB resume signaling will then cause the LPRESF bit to be set, indicating a low-power SUSPEND resume, which will wake the CPU from stop3 mode.

During normal operation, while the host is sending SOF packets, the USB module will not enter suspend mode.

17.4.6.2 Resume

There are three ways to get out of the suspend state. When the USB module is in suspend state, the resume detection is active even if all the clocks are disabled and the MCU is in stop3 mode. The MCU can be activated from the suspend state by normal bus activity, a USB reset signal, or upstream resume (remote wakeup).

17.4.6.2.1 Host Initiated Resume

The host signals a resume from suspend by initiating resume signaling (K state) for at least 20 ms followed by a standard low-speed EOP signal. This 20 ms ensures that all devices in the USB network are awakened. After resuming the bus, the host must begin sending bus traffic within 3 ms to prevent the device from re-entering suspend mode.

Depending on the power mode the device is in while suspended, the notification for a host initiated resume will be different:

- Run mode - RESUME must be set after SLEEPF becomes set to enable the RESUMEF interrupt. Then, upon resume signaling, the RESUMEF interrupt will trigger after a K-state has been observed on the USBDP/USBDN lines for 2.5 µs.
- Stop3 mode - USBRESMEN must be set after SLEEPF becomes set to arm the LPRESF bit. Then, upon a K-state on the bus while the device is in stop3 mode, the LPRESF bit will be set, indicating

18.4.3.6 Debug FIFO Low Register (DBGFL)

This register provides read-only access to the low-order eight bits of the FIFO. Writes to this register have no meaning or effect.

Reading DBGFL causes the FIFO to shift to the next available word of information. When the debug module is operating in event-only modes, only 8-bit data is stored into the FIFO (high-order half of each FIFO word is unused). When reading 8-bit words out of the FIFO, simply read DBGFL repeatedly to get successive bytes of data from the FIFO. It isn't necessary to read DBGFH in this case.

Do not attempt to read data from the FIFO while it is still armed (after arming but before the FIFO is filled or ARMF is cleared) because the FIFO is prevented from advancing during reads of DBGFL. This can interfere with normal sequencing of reads from the FIFO.

Reading DBGFL while the debugger is not armed causes the address of the most-recently fetched opcode to be stored to the last location in the FIFO. By reading DBGFH then DBGFL periodically, external host software can develop a profile of program execution. After eight reads from the FIFO, the ninth read will return the information that was stored as a result of the first read. To use the profiling feature, read the FIFO eight times without using the data to prime the sequence and then begin using the data to get a delayed picture of what addresses were being executed. The information stored into the FIFO on reads of DBGFL (while the FIFO is not armed) is the address of the most-recently fetched opcode.

Table A-6. DC Characteristics (continued)

Num	C	Parameter	Symbol	Min	Typical[1]	Max.	Unit
5	P	Output low current — Max. total I_{OL} for all ports 5 V 3 V	I_{OLT}	 — —	 — —	 100 60	mA
6	C	Input high voltage; all digital inputs 5 V 3 V	V_{IH}	 $0.65 \times V_{DD}$ $0.70 \times V_{DD}$	 —	 —	V
7	C	Input low voltage; all digital inputs	V_{IL}	—	—	$0.35 \times V_{DD}$	
8	C	Input hysteresis; all digital inputs	V_{hys}	$0.06 \times V_{DD}$			mV
9	C	Input leakage current (per pin); input only pins	$\lvert I_{In} \rvert$	—	0.1	1	µA
10	P	Hi-Z (off-state) leakage current (per pin)	$\lvert I_{OZ} \rvert$	—	0.1	1	µA
11	P	Internal pullup resistors[3]	R_{PU}	20	45	65	kΩ
12	P	Internal pulldown resistors[4]	R_{PD}	20	45	65	kΩ
13	T	Internal pullup resistor to USBDP (to V_{USB33}) Idle Transmit	R_{PUPD}	 900 1425	 1300 2400	 1575 3090	kΩ
14	D	DC injection current[5 6 7 8] (single pin limit) $V_{IN} > V_{DD}$ $V_{IN} < V_{SS}$	I_{IC}	 0 0	 — —	 2 –0.2	mA
		DC injection current (Total MCU limit, includes sum of all stressed pins) $V_{IN} > V_{DD}$ $V_{IN} < V_{SS}$		 0 0	 — —	 25 –5	mA
15	D	Input capacitance; all non-supply pins	C_{In}	—	—	8	pF
16	D	RAM retention voltage	V_{RAM}	—	0.6	1.0	V
17	D	POR re-arm voltage	V_{POR}	0.9	1.4	2.0	V
18	D	POR re-arm time	t_{POR}	10	—	—	µs

A.10 External Oscillator (XOSC) Characteristics

Table A-11. Oscillator Electrical Specifications (Temperature Range = –40 to 85°C Ambient)

Num	C	Rating	Symbol	Min	Typ[1]	Max	Unit
1	C	Oscillator crystal or resonator (EREFS = 1, ERCLKEN = 1) Low range (RANGE = 0) High range (RANGE = 1) FEE or FBE mode [2] High range (RANGE = 1) PEE or PBE mode [3] High range (RANGE = 1, HGO = 1) BLPE mode High range (RANGE = 1, HGO = 0) BLPE mode	 f_{lo} $f_{hi\text{-}fll}$ $f_{hi\text{-}pll}$ $f_{hi\text{-}hgo}$ $f_{hi\text{-}lp}$	 32 1 1 1 1	 — — — — —	 38.4 5 16 16 8	 kHz MHz MHz MHz MHz
2	—	Load capacitors	C_1, C_2	See crystal or resonator manufacturer's recommendation.			
3	—	Feedback resistor Low range (32 kHz to 38.4 kHz) High range (1 MHz to 16 MHz)	R_F		 10 1		 MΩ MΩ
4	—	Series resistor Low range, low gain (RANGE = 0, HGO = 0) Low range, high gain (RANGE = 0, HGO = 1) High range, low gain (RANGE = 1, HGO = 0) High range, high gain (RANGE = 1, HGO = 1) ≥ 8 MHz 4 MHz 1 MHz	R_S	 — — — — — —	 0 100 0 0 0 0	 — — — 0 10 20	kΩ
5	T	Crystal start-up time [4] Low range, low gain (RANGE = 0, HGO = 0) Low range, high gain (RANGE = 0, HGO = 1) High range, low gain (RANGE = 1, HGO = 0)[5] High range, high gain (RANGE = 1, HGO = 1)[5]	 $t_{CSTL\text{-}LP}$ $t_{CSTL\text{-}HGO}$ $t_{CSTH\text{-}LP}$ $t_{CSTH\text{-}HGO}$	 — — — —	 200 400 5 15	 — — — —	ms
6	T	Square wave input clock frequency (EREFS = 0, ERCLKEN = 1) FEE or FBE mode [2] PEE or PBE mode [3] BLPE mode	f_{extal}	 0.03125 1 0	 — — —	 5 16 40	 MHz MHz MHz

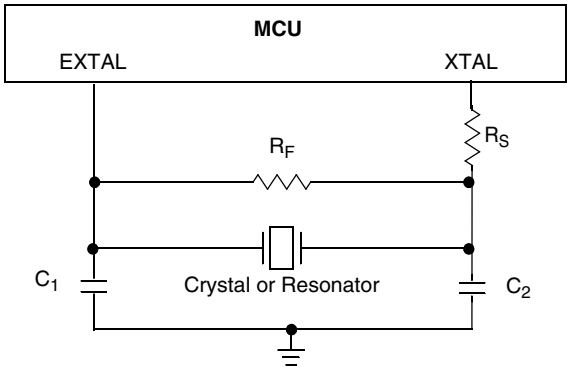
1 Typical data was characterized at 3.0 V, 25°C or is recommended value.

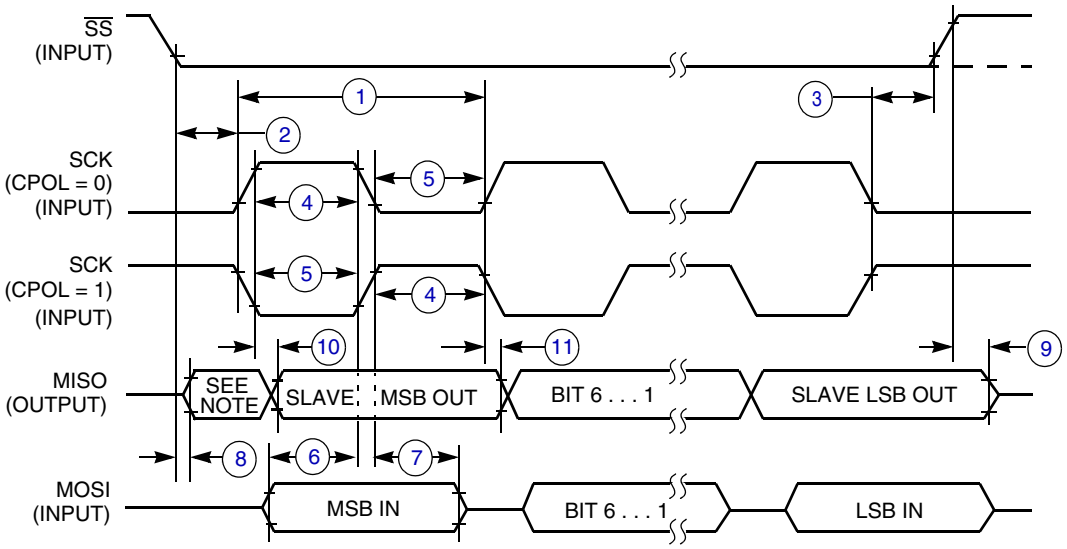
2 When MCG is configured for FEE or FBE mode, input clock source must be divided using RDIV to within the range of 31.25 kHz to 39.0625 kHz.

3 When MCG is configured for PEE or PBE mode, input clock source must be divided using RDIV to within the range of 1 MHz to 2 MHz.

4 This parameter is characterized and not tested on each device. Proper PC board layout procedures must be followed to achieve specifications.

5 4 MHz crystal





NOTE:
1. Not defined but normally LSB of character just received

Figure A-13. SPI Slave Timing (CPHA = 1)

A.13 Flash Specifications

This section provides details about program/erase times and program-erase endurance for the flash memory.

Program and erase operations do not require any special power sources other than the normal V_{DD} supply. For more detailed information about program/erase operations.

Table A-16. Flash Characteristics

Num	C	Characteristic	Symbol	Min	Typ[1]	Max	Unit
1		Supply voltage for program/erase	$V_{prog/erase}$	2.7		5.5	V
2		Supply voltage for read operation	V_{Read}	2.7		5.5	V
3		Internal FCLK frequency[2]	f_{FCLK}	150		200	kHz
4		Internal FCLK period (1/FCLK)	t_{Fcyc}	5		6.67	µs
5		Byte program time (random location)(2)	t_{prog}	9			t_{Fcyc}
6		Byte program time (burst mode)(2)	t_{Burst}	4			t_{Fcyc}
7		Page erase time[3]	t_{Page}	4000			t_{Fcyc}
8		Mass erase time(2)	t_{Mass}	20,000			t_{Fcyc}
9	C	Program/erase endurance[4] T_L to T_H = –40°C to + 85°C T = 25°C		10,000 —	— 100,000	— —	cycles
10		Data retention[5]	t_{D_ret}	15	100	—	years

1 Typical values are based on characterization data at V_{DD} = 5.0 V, 25°C unless otherwise stated.