Infineon Technologies - C161PIL25MCAFXUMA1 Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	C166
Core Size	16-Bit
Speed	25MHz
Connectivity	EBI/EMI, I²C, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	76
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	3K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	PG-MQFP-100-2
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/c161pil25mcafxuma1

Table 1 Pin Definitions and Functions (continued)

Symbol	Pin Num. TQFP	Pin Num. MQFP	Input Outp.	Function
P6			IO	Port 6 is an 8-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 6 outputs can be configured as push/pull or open drain drivers. The Port 6 pins also serve for alternate functions:
P6.0	79	81	O	$\overline{CS0}$ Chip Select 0 Output
P6.1	80	82	O	$\overline{CS1}$ Chip Select 1 Output
P6.2	81	83	O	$\overline{CS2}$ Chip Select 2 Output
P6.3	82	84	O	$\overline{CS3}$ Chip Select 3 Output
P6.4	83	85	O	CS4 Chip Select 4 Output
P6.5	84	86	I/O	SDA1 I^2C Bus Data Line 1
P6.6	85	87	I/O	SCL1 I^2C Bus Clock Line 1
P6.7	86	88	I/O	SDA2 I^2C Bus Data Line 2
				Note: Pins P6.7-5 are open drain outputs only.
P2			IO	Port 2 is an 8-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 2 outputs can be configured as push/pull or open drain drivers. The input threshold of Port 2 is selectable (TTL or special). The Port 2 pins also serve for alternate functions:
P2.8	87	89	I	EX0IN Fast External Interrupt 0 Input
P2.9	88	90	I	EX1IN Fast External Interrupt 1 Input
P2.10	89	91	I	EX2IN Fast External Interrupt 2 Input
P2.11	90	92	I	EX3IN Fast External Interrupt 3 Input
P2.12	91	93	I	EX4IN Fast External Interrupt 4 Input
P2.13	92	94	I	EX5IN Fast External Interrupt 5 Input
P2.14	93	95	I	EX6IN Fast External Interrupt 6 Input
P2.15	94	96	I	EX7IN Fast External Interrupt 7 Input
V_{AREF}	95	97	-	Reference voltage for the A/D converter.
V_{AGND}	96	98	-	Reference ground for the A/D converter.

Functional Description

The architecture of the C161PI combines advantages of both RISC and CISC processors and of advanced peripheral subsystems in a very well-balanced way. The following block diagram gives an overview of the different on-chip components and of the advanced, high bandwidth internal bus structure of the C161PI.

Note: All time specifications refer to a CPU clock of 25 MHz (see definition in the AC Characteristics section).

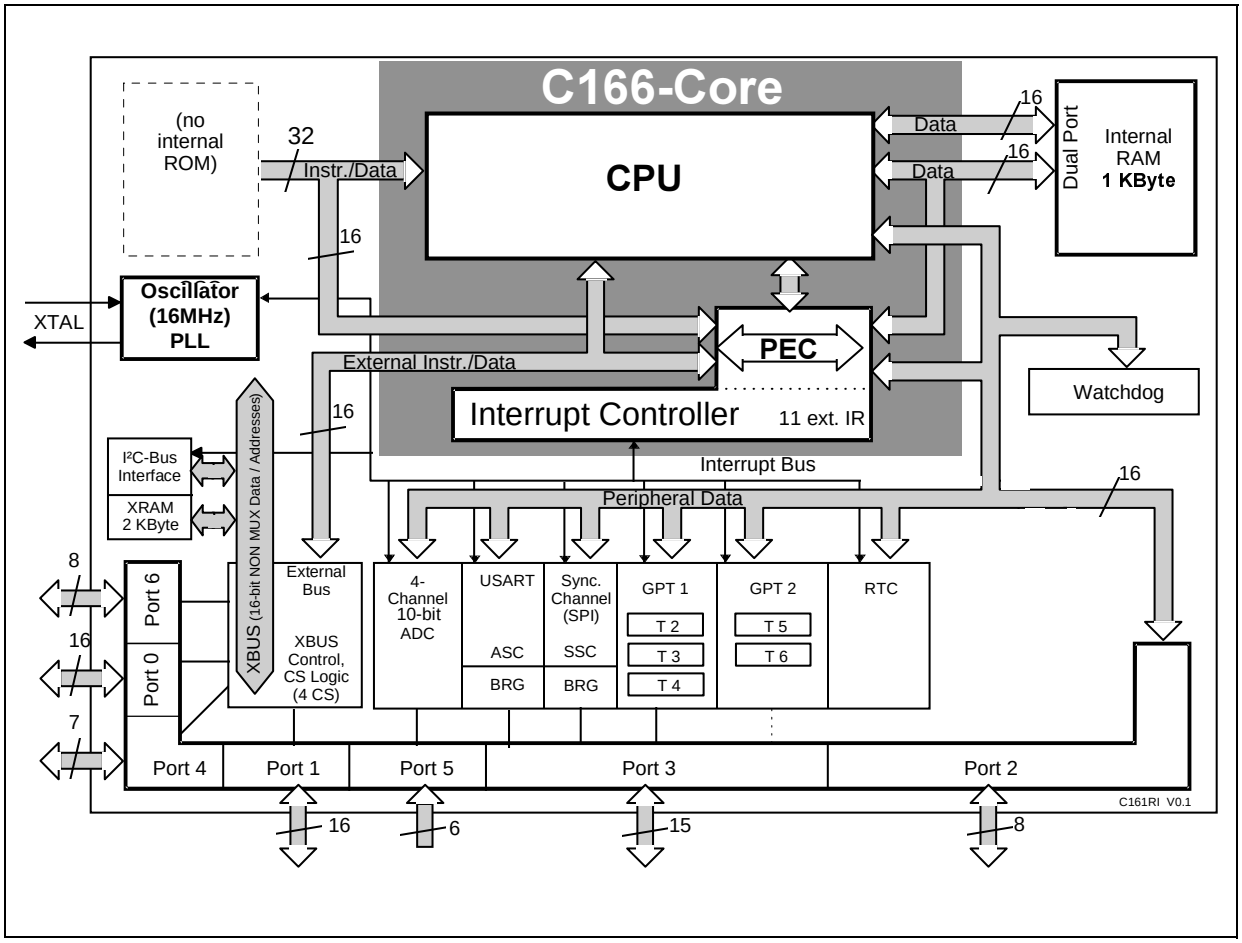

Figure 4 Block Diagram

Interrupt System

With an interrupt response time within a range from just 5 to 12 CPU clocks (in case of internal program execution), the C161PI is capable of reacting very fast to the occurrence of non-deterministic events.

The architecture of the C161PI supports several mechanisms for fast and flexible response to service requests that can be generated from various sources internal or external to the microcontroller. Any of these interrupt requests can be programmed to being serviced by the Interrupt Controller or by the Peripheral Event Controller (PEC).

In contrast to a standard interrupt service where the current program execution is suspended and a branch to the interrupt vector table is performed, just one cycle is ‘stolen’ from the current CPU activity to perform a PEC service. A PEC service implies a single byte or word data transfer between any two memory locations with an additional increment of either the PEC source or the destination pointer. An individual PEC transfer counter is implicity decremented for each PEC service except when performing in the continuous transfer mode. When this counter reaches zero, a standard interrupt is performed to the corresponding source related vector location. PEC services are very well suited, for example, for supporting the transmission or reception of blocks of data. The C161PI has 8 PEC channels each of which offers such fast interrupt-driven data transfer capabilities.

A separate control register which contains an interrupt request flag, an interrupt enable flag and an interrupt priority bitfield exists for each of the possible interrupt sources. Via its related register, each source can be programmed to one of sixteen interrupt priority levels. Once having been accepted by the CPU, an interrupt service can only be interrupted by a higher prioritized service request. For the standard interrupt processing, each of the possible interrupt sources has a dedicated vector location.

Fast external interrupt inputs are provided to service external interrupts with high precision requirements. These fast interrupt inputs feature programmable edge detection (rising edge, falling edge or both edges).

Software interrupts are supported by means of the ‘TRAP’ instruction in combination with an individual trap (interrupt) number.

The following table shows all of the possible C161PI interrupt sources and the corresponding hardware-related interrupt flags, vectors, vector locations and trap (interrupt) numbers.

Note: Interrupt nodes which are not used by associated peripherals, may be used to generate software controlled interrupt requests by setting the respective interrupt request bit (xIR).

The state of this latch may be used to clock timer T5. The overflows/underflows of timer T6 can additionally be used to cause a reload from the CAPREL register. The CAPREL register may capture the contents of timer T5 based on an external signal transition on the corresponding port pin (CAPIN), and timer T5 may optionally be cleared after the capture procedure. This allows absolute time differences to be measured or pulse multiplication to be performed without software overhead.

The capture trigger (timer T5 to CAPREL) may also be generated upon transitions of GPT1 timer T3's inputs T3IN and/or T3EUD. This is especially advantageous when T3 operates in Incremental Interface Mode.

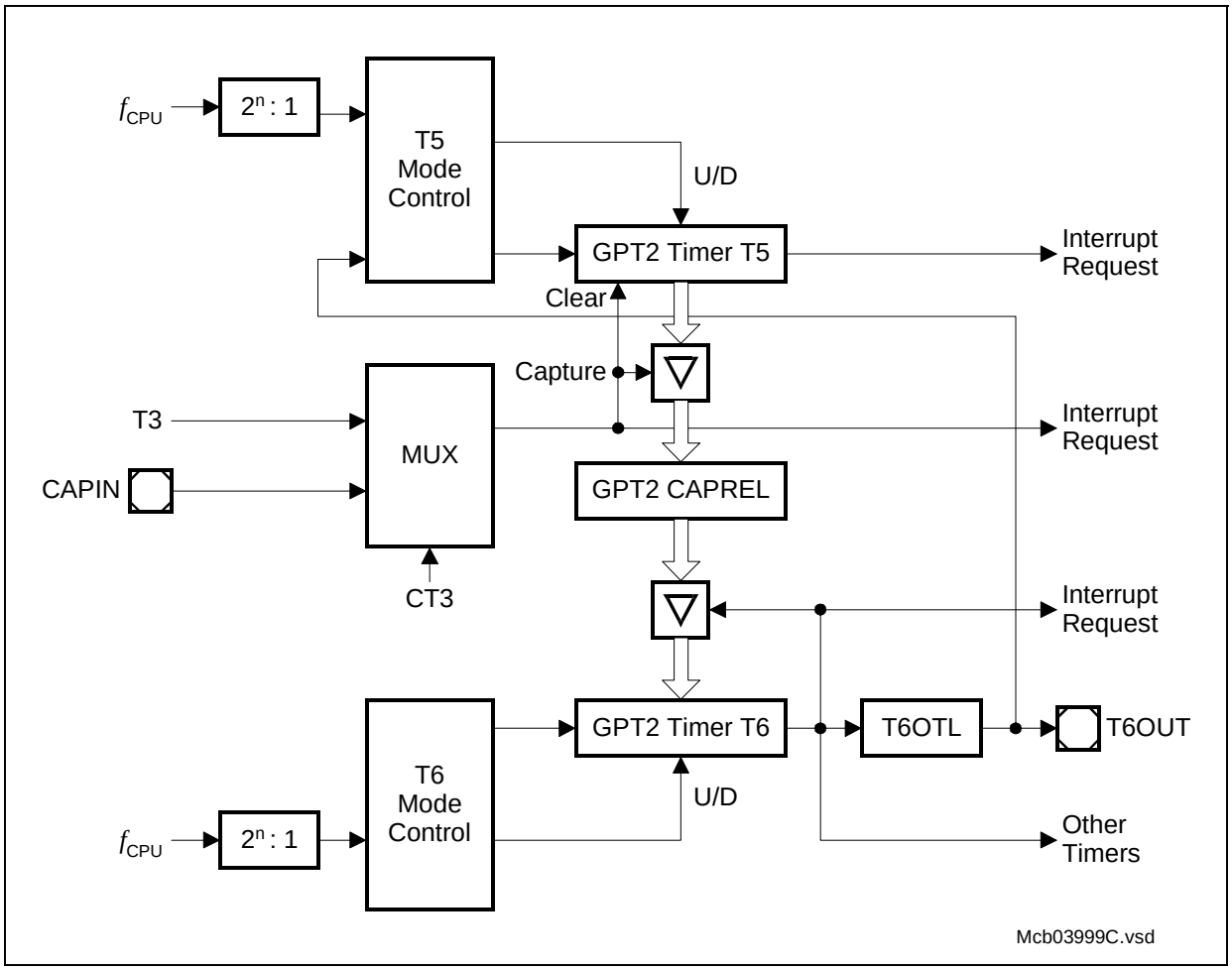

Figure 7 Block Diagram of GPT2

DC Characteristics (Standard Supply Voltage Range) (continued)
(Operating Conditions apply)

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Output low voltage (all other outputs)	V_{OL1} CC	–	0.45	V	I_{OL} = 1.6 mA
Output high voltage [1] (PORT0, PORT1, Port 4, ALE, $\overline{RD}$, $\overline{WR}$, $\overline{BHE}$, CLKOUT, $\overline{RSTOUT}$)	V_{OH} CC	2.4	–	V	I_{OH} = -2.4 mA
		0.9 V_{DD}	–	V	I_{OH} = -0.5 mA
Output high voltage [1] (all other outputs)	V_{OH1} CC	2.4	–	V	I_{OH} = -1.6 mA
		0.9 V_{DD}	–	V	I_{OH} = -0.5 mA
Input leakage current (Port 5)	I_{OZ1} CC	–	±200	nA	0.45V < V_{IN} < V_{DD}
Input leakage current (all other)	I_{OZ2} CC	–	±500	nA	0.45V < V_{IN} < V_{DD}
$\overline{RSTIN}$ inactive current [2]	I_{RSTH} [3]	–	-10	µA	V_{IN} = V_{IH1}
$\overline{RSTIN}$ active current [2]	I_{RSTL} [4]	-100	–	µA	V_{IN} = V_{IL}
Read/Write inactive current [5]	I_{RWH} [3]	–	-40	µA	V_{OUT} = 2.4 V
Read/Write active current [5]	I_{RWL} [4]	-500	–	µA	V_{OUT} = V_{OLmax}
ALE inactive current [5]	I_{ALEL} [3]	–	40	µA	V_{OUT} = V_{OLmax}
ALE active current [5]	I_{ALEH} [4]	500	–	µA	V_{OUT} = 2.4 V
Port 6 inactive current [5]	I_{P6H} [3]	–	-40	µA	V_{OUT} = 2.4 V
Port 6 active current [5]	I_{P6L} [4]	-500	–	µA	V_{OUT} = V_{OL1max}
PORT0 configuration current [5]	I_{P0H} [3]	–	-10	µA	V_{IN} = V_{IHmin}
	I_{P0L} [4]	-100	–	µA	V_{IN} = V_{ILmax}
XTAL1 input current	I_{IL} CC	–	±20	µA	0 V < V_{IN} < V_{DD}
Pin capacitance [6] (digital inputs/outputs)	C_{IO} CC	–	10	pF	f = 1 MHz T_A = 25 °C
Power supply current (5V active) with all peripherals active	I_{DD5}	–	1 + 2*f_{CPU}	mA	$\overline{RSTIN}$ = V_{IL2} f_{CPU} in [MHz] [7]
Idle mode supply current (5V) with all peripherals active	I_{IDX5}	–	1 + 0.8*f_{CPU}	mA	$\overline{RSTIN}$ = V_{IH1} f_{CPU} in [MHz] [7]
Idle mode supply current (5V) with all peripherals deactivated, PLL off, SDD factor = 32	I_{IDO5} [8]	–	500 + 50*f_{OSC}	µA	$\overline{RSTIN}$ = V_{IH1} f_{OSC} in [MHz] [7]

DC Characteristics (Reduced Supply Voltage Range)

(Operating Conditions apply)

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input low voltage XTAL1, P3.0, P3.1, P6.5, P6.6, P6.7	V_{IL1} SR	– 0.5	0.3 V_{DD}	V	–
Input low voltage (TTL)	V_{IL} SR	– 0.5	0.8	V	–
Input low voltage (Special Threshold)	V_{ILS} SR	– 0.5	1.3	V	–
Input high voltage $\overline{\text{RSTIN}}$	V_{IH1} SR	0.6 V_{DD}	V_{DD} + 0.5	V	–
Input high voltage XTAL1, P3.0, P3.1, P6.5, P6.6, P6.7	V_{IH2} SR	0.7 V_{DD}	V_{DD} + 0.5	V	–
Input high voltage (TTL)	V_{IH} SR	1.8	V_{DD} + 0.5	V	–
Input high voltage (Special Threshold)	V_{IHS} SR	0.8 V_{DD} - 0.2	V_{DD} + 0.5	V	–
Input Hysteresis (Special Threshold)	HYS	250	–	mV	–
Output low voltage (PORT0, PORT1, Port 4, ALE, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{BHE}}$, CLKOUT, $\overline{\text{RSTOUT}}$)	V_{OL} CC	–	0.45	V	I_{OL} = 1.6 mA
Output low voltage P3.0, P3.1, P6.5, P6.6, P6.7	V_{OL2} CC	–	0.4	V	I_{OL2} = 1.6 mA
Output low voltage (all other outputs)	V_{OL1} CC	–	0.45	V	I_{OL} = 1.0 mA
Output high voltage [1] (PORT0, PORT1, Port 4, ALE, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{BHE}}$, CLKOUT, $\overline{\text{RSTOUT}}$)	V_{OH} CC	0.9 V_{DD}	–	V	I_{OH} = -0.5 mA
Output high voltage [1] (all other outputs)	V_{OH1} CC	0.9 V_{DD}	–	V	I_{OH} = -0.25 mA
Input leakage current (Port 5)	I_{OZ1} CC	–	±200	nA	0.45V < V_{IN} < V_{DD}
Input leakage current (all other)	I_{OZ2} CC	–	±500	nA	0.45V < V_{IN} < V_{DD}
$\overline{\text{RSTIN}}$ inactive current [2]	I_{RSTH} [3]	–	-10	µA	V_{IN} = V_{IH1}

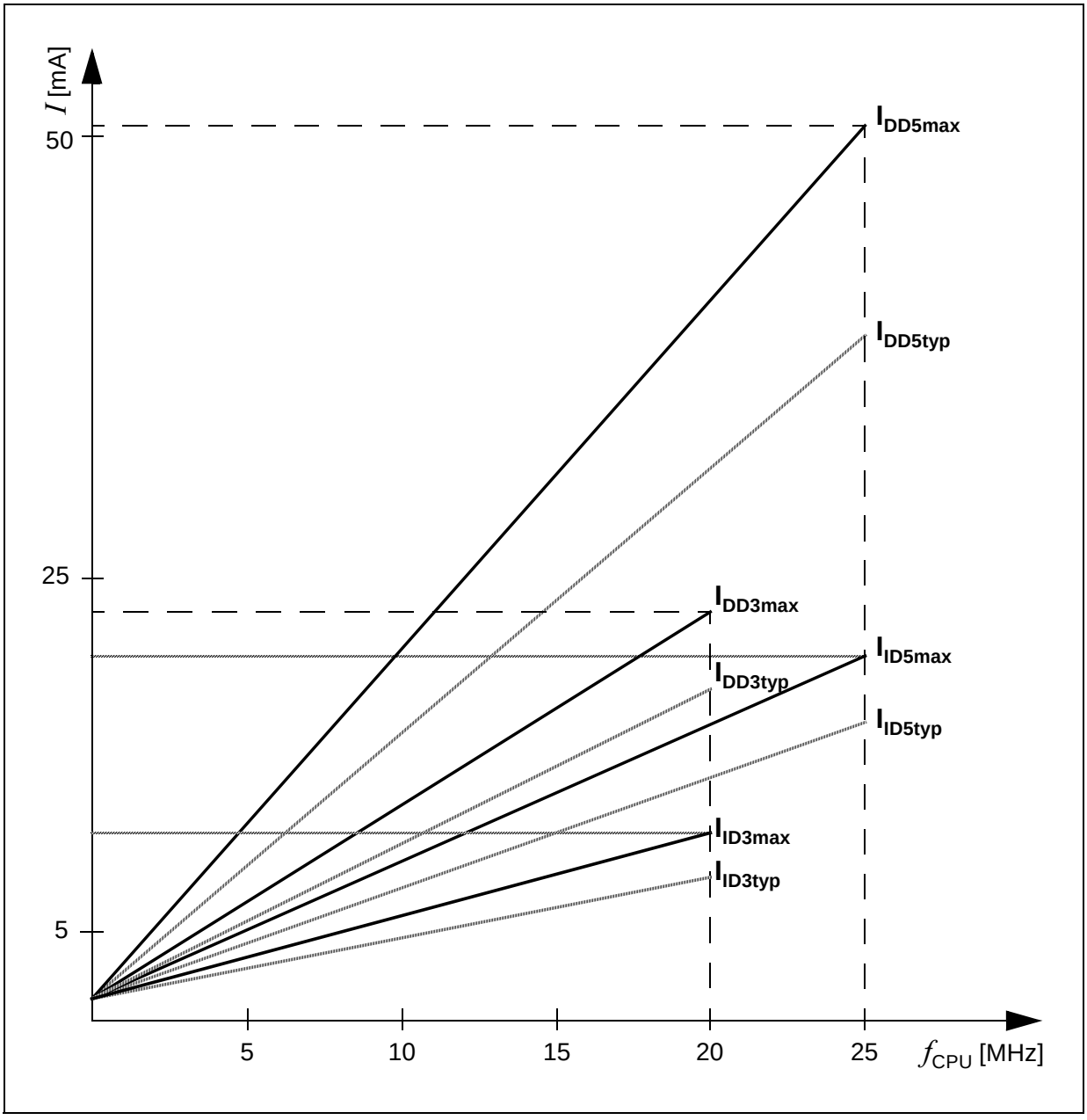

Figure 10 Supply/Idle Current as a Function of Operating Frequency

A/D Converter Characteristics

(Operating Conditions apply)

4.0V (2.6V) ≤ V_{AREF} ≤ V_{DD} + 0.1V (Note the influence on TUE.)

V_{SS} - 0.1V ≤ V_{AGND} ≤ V_{SS} + 0.2V

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Analog input voltage range	V_{AIN} SR	V_{AGND}	V_{AREF}	V	1)
Basic clock frequency	f_{BC}	0.5	6.25	MHz	2)
Conversion time	t_C CC	–	40 t_{BC} + t_S+2t_{CPU}		3) t_{CPU} = 1 / f_{CPU}
Total unadjusted error	TUE CC 4)	–	± 2	LSB	V_{AREF} ≥ 4.0 V 5)
		–	± 4	LSB	V_{AREF} ≥ 2.6 V
Internal resistance of reference voltage source	R_{AREF} SR	–	t_{BC} / 60 - 0.25	kΩ	t_{BC} in [ns] 6) 7)
Internal resistance of analog source	R_{ASRC} SR	–	t_S / 450 - 0.25	kΩ	t_S in [ns] 7) 8)
ADC input capacitance	C_{AIN} CC	–	33	pF	7)

1) V_{AIN} may exceed V_{AGND} or V_{AREF} up to the absolute maximum ratings. However, the conversion result in these cases will be $X000_H$ or $X3FF_H$, respectively.

2) The limit values for f_{BC} must not be exceeded when selecting the CPU frequency and the ADCTC setting.

3) This parameter includes the sample time t_S, the time for determining the digital result and the time to load the result register with the conversion result.
Values for the basic clock t_{BC} depend on the conversion time programming.
This parameter depends on the ADC control logic. It is not a real maximum value, but rather a fixum.

4) TUE is tested at V_{AREF}=5.0V (3.3V), V_{AGND}=0V, V_{DD}=4.9V (3.2V). It is guaranteed by design for all other voltages within the defined voltage range.
The specified TUE is guaranteed only if an overload condition (see I_{OV} specification) occurs on maximum 2 not selected analog input pins and the absolute sum of input overload currents on all analog input pins does not exceed 10 mA.
During the reset calibration sequence the maximum TUE may be ±4 LSB (±8 LSB @ 3V).

5) This case is not applicable for the reduced supply voltage range.

6) During the conversion the ADC's capacitance must be repeatedly charged or discharged. The internal resistance of the reference voltage source must allow the capacitance to reach its respective voltage level within each conversion step. The maximum internal resistance results from the programmed conversion timing.

7) Not 100% tested, guaranteed by design.

8) During the sample time the input capacitance C_I can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_S. After the end of the sample time t_S, changes of the analog input voltage have no effect on the conversion result. Values for the sample time t_S depend on programming and can be taken from the table below.

Sample time and conversion time of the C161PI's A/D Converter are programmable. The table below should be used to calculate the above timings.
The limit values for f_{BC} must not be exceeded when selecting ADCTC.

Table 9 A/D Converter Computation Table

ADCON.15|14 (ADCTC)	A/D Converter Basic clock f_{BC}	ADCON.13|12 (ADSTC)	Sample time t_S
00	f_{CPU} / 4	00	t_{BC} * 8
01	f_{CPU} / 2	01	t_{BC} * 16
10	f_{CPU} / 16	10	t_{BC} * 32
11	f_{CPU} / 8	11	t_{BC} * 64

Converter Timing Example:

Assumptions:	f_{CPU}	= 25 MHz (i.e. t_{CPU} = 40 ns), ADCTC = '00', ADSTC = '00'.
Basic clock	f_{BC}	= f_{CPU} / 4 = 6.25 MHz, i.e. t_{BC} = 160 ns.
Sample time	t_S	= t_{BC} * 8 = 1280 ns.
Conversion time	t_C	= t_S + 40 t_{BC} + 2 t_{CPU} = (1280 + 6400 + 80) ns = 7.8 µs.

Memory Cycle Variables

The timing tables below use three variables which are derived from the BUSCONx registers and represent the special characteristics of the programmed memory cycle. The following table describes, how these variables are to be computed.

Table 10 Memory Cycle Variables

Description	Symbol	Values
ALE Extension	t_A	TCL * <ALECTL>
Memory Cycle Time Waitstates	t_C	2TCL * (15 - <MCTC>)
Memory Tristate Time	t_F	2TCL * (1 - <MTTC>)

AC Characteristics

Multiplexed Bus (Reduced Supply Voltage Range)

(Operating Conditions apply)

ALE cycle time = 6 TCL + 2t_A + t_C + t_F (150 ns at 20 MHz CPU clock without waitstates)

Parameter	Symbol		Max. CPU Clock = 20 MHz		Variable CPU Clock 1 / 2TCL = 1 to 20 MHz		Unit
			min.	max.	min.	max.	
ALE high time	t_5	CC	11 + t_A	–	TCL - 14 + t_A	–	ns
Address setup to ALE	t_6	CC	5 + t_A	–	TCL - 20 + t_A	–	ns
Address hold after ALE	t_7	CC	15 + t_A	–	TCL - 10 + t_A	–	ns
ALE falling edge to $\overline{RD}$, $\overline{WR}$ (with RW-delay)	t_8	CC	15 + t_A	–	TCL - 10 + t_A	–	ns
ALE falling edge to $\overline{RD}$, $\overline{WR}$ (no RW-delay)	t_9	CC	-10 + t_A	–	-10 + t_A	–	ns
Address float after $\overline{RD}$, $\overline{WR}$ (with RW-delay)	t_{10}	CC	–	6	–	6	ns
Address float after $\overline{RD}$, $\overline{WR}$ (no RW-delay)	t_{11}	CC	–	31	–	TCL + 6	ns
$\overline{RD}$, $\overline{WR}$ low time (with RW-delay)	t_{12}	CC	34 + t_C	–	2TCL - 16 + t_C	–	ns
$\overline{RD}$, $\overline{WR}$ low time (no RW-delay)	t_{13}	CC	59 + t_C	–	3TCL - 16 + t_C	–	ns
$\overline{RD}$ to valid data in (with RW-delay)	t_{14}	SR	–	22 + t_C	–	2TCL - 28 + t_C	ns
$\overline{RD}$ to valid data in (no RW-delay)	t_{15}	SR	–	47 + t_C	–	3TCL - 28 + t_C	ns
ALE low to valid data in	t_{16}	SR	–	49 + t_A + t_C	–	3TCL - 30 + t_A + t_C	ns
Address to valid data in	t_{17}	SR	–	57 + 2t_A + t_C	–	4TCL - 43 + 2t_A + t_C	ns
Data hold after $\overline{RD}$ rising edge	t_{18}	SR	0	–	0	–	ns
Data float after $\overline{RD}$	t_{19}	SR	–	36 + t_F	–	2TCL - 14 + t_F	ns

Multiplexed Bus (Reduced Supply Voltage Range) (continued)
(Operating Conditions apply)
ALE cycle time = 6 TCL + $2t_A$ + t_C + t_F (150 ns at 20 MHz CPU clock without waitstates)

Parameter	Symbol		Max. CPU Clock = 20 MHz		Variable CPU Clock 1 / 2TCL = 1 to 20 MHz		Unit
			min.	max.	min.	max.	
Data hold after $\overline{\text{RdCS}}$	t_{51}	SR	0	–	0	–	ns
Data float after $\overline{\text{RdCS}}$	t_{52}	SR	–	30 + t_F	–	2TCL - 20 + t_F	ns
Address hold after $\overline{\text{RdCS}}$, $\overline{\text{WrCS}}$	t_{54}	CC	30 + t_F	–	2TCL - 20 + t_F	–	ns
Data hold after $\overline{\text{WrCS}}$	t_{56}	CC	30 + t_F	–	2TCL - 20 + t_F	–	ns

1) These parameters refer to the latched chip select signals ($\overline{\text{CSxL}}$). The early chip select signals ($\overline{\text{CSxE}}$) are specified together with the address and signal $\overline{\text{BHE}}$ (see figures below).

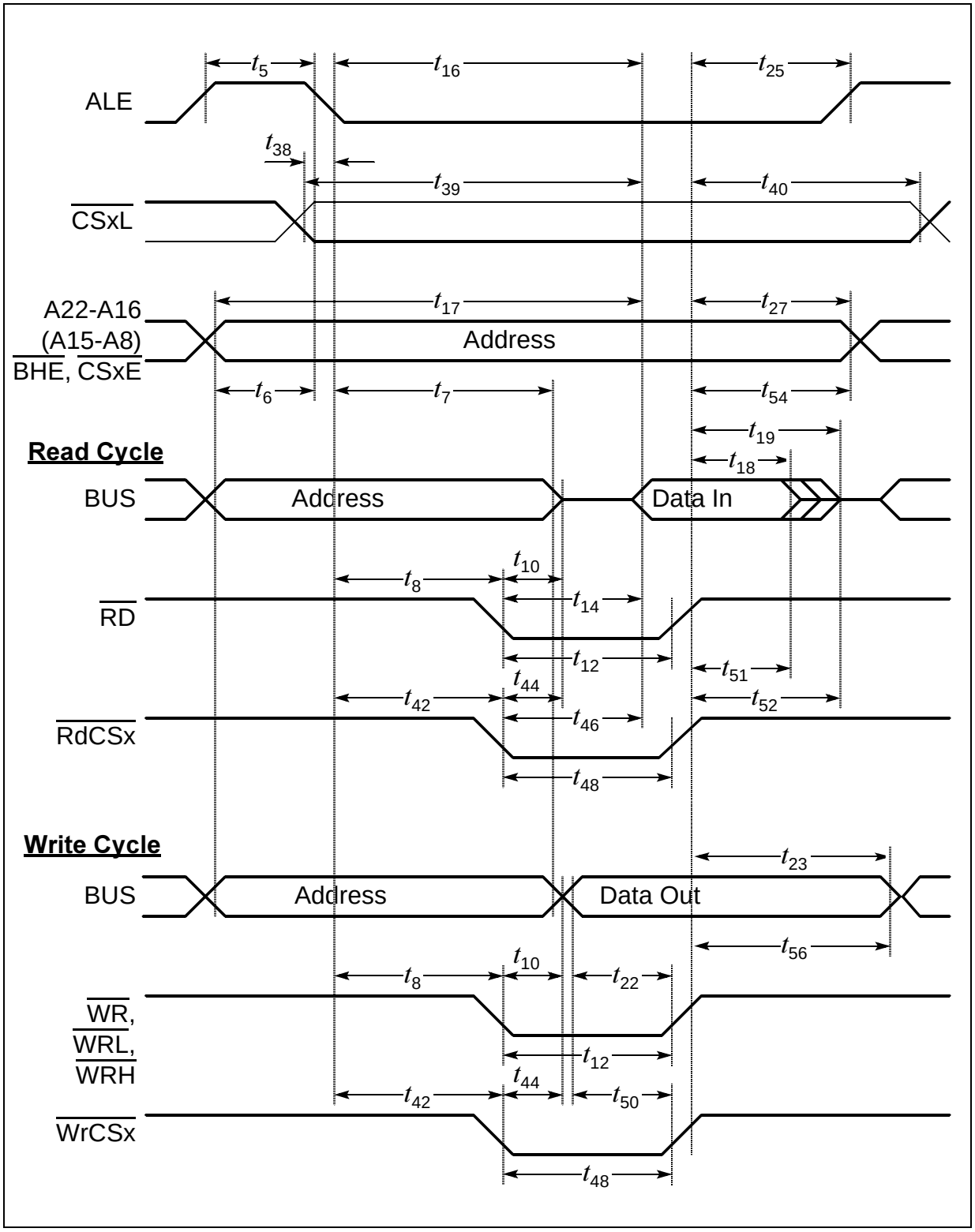

Figure 17 External Memory Cycle:
Multiplexed Bus, With Read/Write Delay, Extended ALE

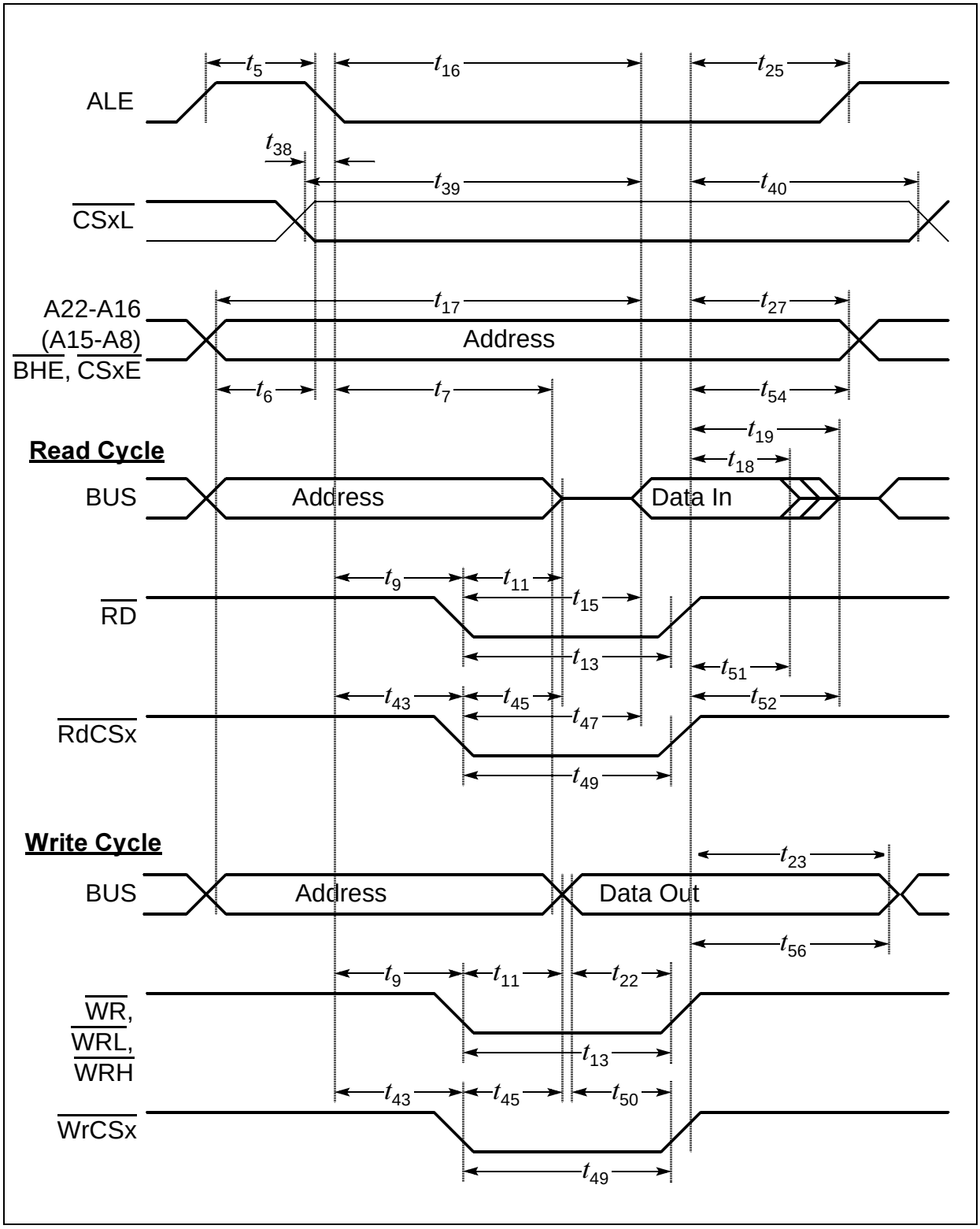

Figure 19 External Memory Cycle:
Multiplexed Bus, No Read/Write Delay, Extended ALE

Demultiplexed Bus (Standard Supply Voltage Range) (continued)
(Operating Conditions apply)
ALE cycle time = 4 TCL + 2t_A + t_C + t_F (80 ns at 25 MHz CPU clock without waitstates)

Parameter	Symbol		Max. CPU Clock = 25 MHz		Variable CPU Clock 1 / 2TCL = 1 to 25 MHz		Unit
			min.	max.	min.	max.	
Data hold after $\overline{WR}$	t_{24}	CC	10 + t_F	–	TCL - 10 + t_F	–	ns
$\overline{ALE}$ rising edge after $\overline{RD}$, $\overline{WR}$	t_{26}	CC	-10 + t_F	–	-10 + t_F	–	ns
Address hold after $\overline{WR}$ [2]	t_{28}	CC	0 + t_F	–	0 + t_F	–	ns
$\overline{ALE}$ falling edge to $\overline{CS}$ [3]	t_{38}	CC	-4 - t_A	10 - t_A	-4 - t_A	10 - t_A	ns
$\overline{CS}$ low to Valid Data In [3]	t_{39}	SR	–	40 + t_C + 2t_A	–	3TCL - 20 + t_C + 2t_A	ns
$\overline{CS}$ hold after $\overline{RD}$, $\overline{WR}$ [3]	t_{41}	CC	6 + t_F	–	TCL - 14 + t_F	–	ns
$\overline{ALE}$ falling edge to $\overline{RdCS}$, $\overline{WrCS}$ (with RW-delay)	t_{42}	CC	16 + t_A	–	TCL - 4 + t_A	–	ns
$\overline{ALE}$ falling edge to $\overline{RdCS}$, $\overline{WrCS}$ (no RW-delay)	t_{43}	CC	-4 + t_A	–	-4 + t_A	–	ns
$\overline{RdCS}$ to Valid Data In (with RW-delay)	t_{46}	SR	–	16 + t_C	–	2TCL - 24 + t_C	ns
$\overline{RdCS}$ to Valid Data In (no RW-delay)	t_{47}	SR	–	36 + t_C	–	3TCL - 24 + t_C	ns
$\overline{RdCS}$, $\overline{WrCS}$ Low Time (with RW-delay)	t_{48}	CC	30 + t_C	–	2TCL - 10 + t_C	–	ns
$\overline{RdCS}$, $\overline{WrCS}$ Low Time (no RW-delay)	t_{49}	CC	50 + t_C	–	3TCL - 10 + t_C	–	ns
Data valid to $\overline{WrCS}$	t_{50}	CC	26 + t_C	–	2TCL - 14 + t_C	–	ns
Data hold after $\overline{RdCS}$	t_{51}	SR	0	–	0	–	ns
Data float after $\overline{RdCS}$ (with RW-delay) [1]	t_{53}	SR	–	20 + t_F	–	2TCL - 20 + 2t_A + t_F [1]	ns
Data float after $\overline{RdCS}$ (no RW-delay) [1]	t_{68}	SR	–	0 + t_F	–	TCL - 20 + 2t_A + t_F [1]	ns

Demultiplexed Bus (Reduced Supply Voltage Range) (continued)
(Operating Conditions apply)
ALE cycle time = 4 TCL + 2t_A + t_C + t_F (100 ns at 20 MHz CPU clock without waitstates)

Parameter	Symbol		Max. CPU Clock = 20 MHz		Variable CPU Clock 1 / 2TCL = 1 to 20 MHz		Unit
			min.	max.	min.	max.	
Data hold after $\overline{WR}$	t_{24}	CC	15 + t_F	–	TCL - 10 + t_F	–	ns
$\overline{ALE}$ rising edge after $\overline{RD}$, $\overline{WR}$	t_{26}	CC	-12 + t_F	–	-12 + t_F	–	ns
Address hold after $\overline{WR}$ [2]	t_{28}	CC	0 + t_F	–	0 + t_F	–	ns
$\overline{ALE}$ falling edge to $\overline{CS}$ [3]	t_{38}	CC	-8 - t_A	10 - t_A	-8 - t_A	10 - t_A	ns
$\overline{CS}$ low to Valid Data In [3]	t_{39}	SR	–	47 + t_C + 2t_A	–	3TCL - 28 + t_C + 2t_A	ns
$\overline{CS}$ hold after $\overline{RD}$, $\overline{WR}$ [3]	t_{41}	CC	9 + t_F	–	TCL - 16 + t_F	–	ns
$\overline{ALE}$ falling edge to $\overline{RdCS}$, $\overline{WrCS}$ (with RW-delay)	t_{42}	CC	19 + t_A	–	TCL - 6 + t_A	–	ns
$\overline{ALE}$ falling edge to $\overline{RdCS}$, $\overline{WrCS}$ (no RW-delay)	t_{43}	CC	-6 + t_A	–	-6 + t_A	–	ns
$\overline{RdCS}$ to Valid Data In (with RW-delay)	t_{46}	SR	–	20 + t_C	–	2TCL - 30 + t_C	ns
$\overline{RdCS}$ to Valid Data In (no RW-delay)	t_{47}	SR	–	45 + t_C	–	3TCL - 30 + t_C	ns
$\overline{RdCS}$, $\overline{WrCS}$ Low Time (with RW-delay)	t_{48}	CC	38 + t_C	–	2TCL - 12 + t_C	–	ns
$\overline{RdCS}$, $\overline{WrCS}$ Low Time (no RW-delay)	t_{49}	CC	63 + t_C	–	3TCL - 12 + t_C	–	ns
Data valid to $\overline{WrCS}$	t_{50}	CC	28 + t_C	–	2TCL - 22 + t_C	–	ns
Data hold after $\overline{RdCS}$	t_{51}	SR	0	–	0	–	ns
Data float after $\overline{RdCS}$ (with RW-delay) [1]	t_{53}	SR	–	30 + t_F	–	2TCL - 20 + 2t_A + t_F [1]	ns
Data float after $\overline{RdCS}$ (no RW-delay) [1]	t_{68}	SR	–	5 + t_F	–	TCL - 20 + 2t_A + t_F [1]	ns

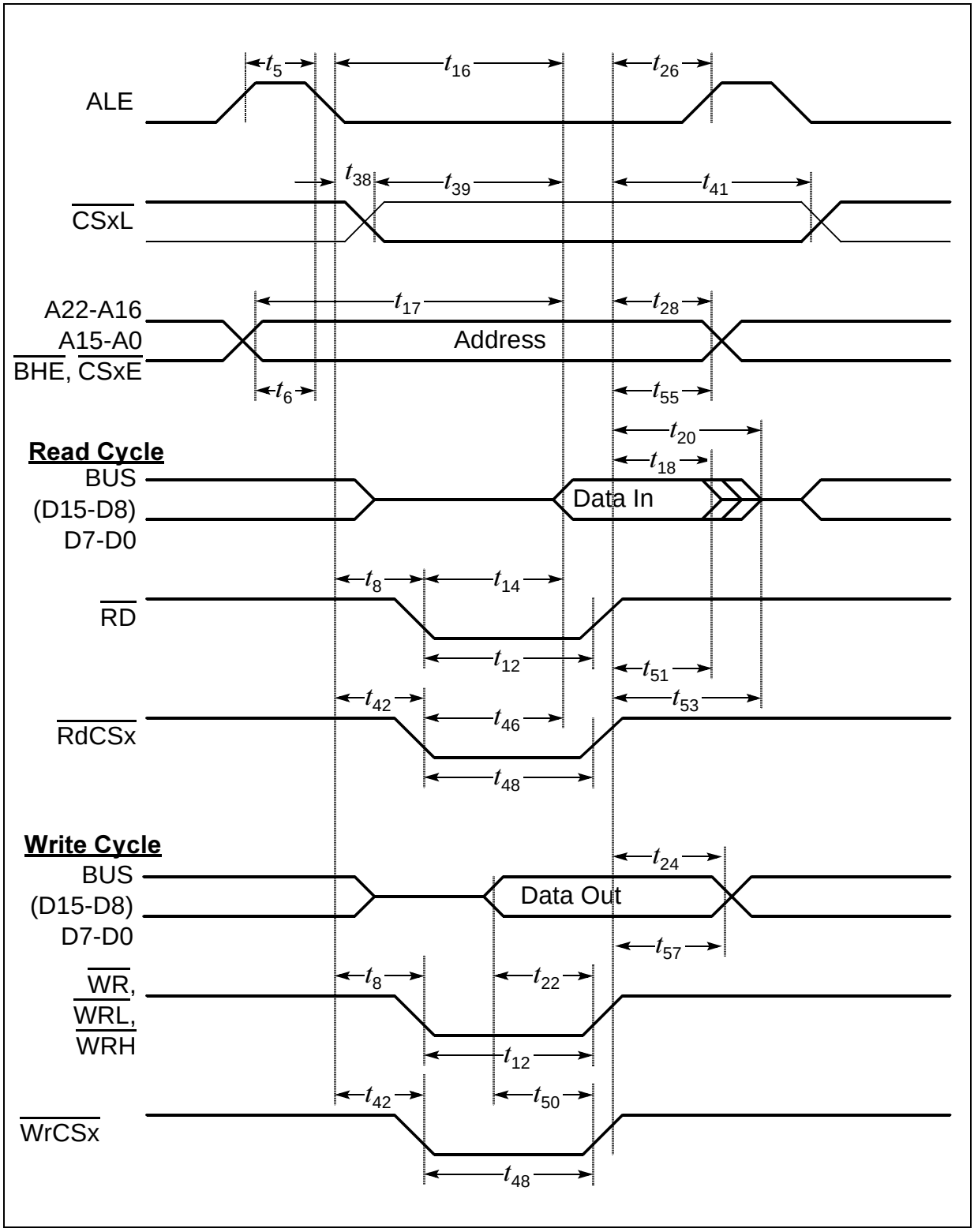

Figure 20 External Memory Cycle: Demultiplexed Bus, With Read/Write Delay, Normal ALE

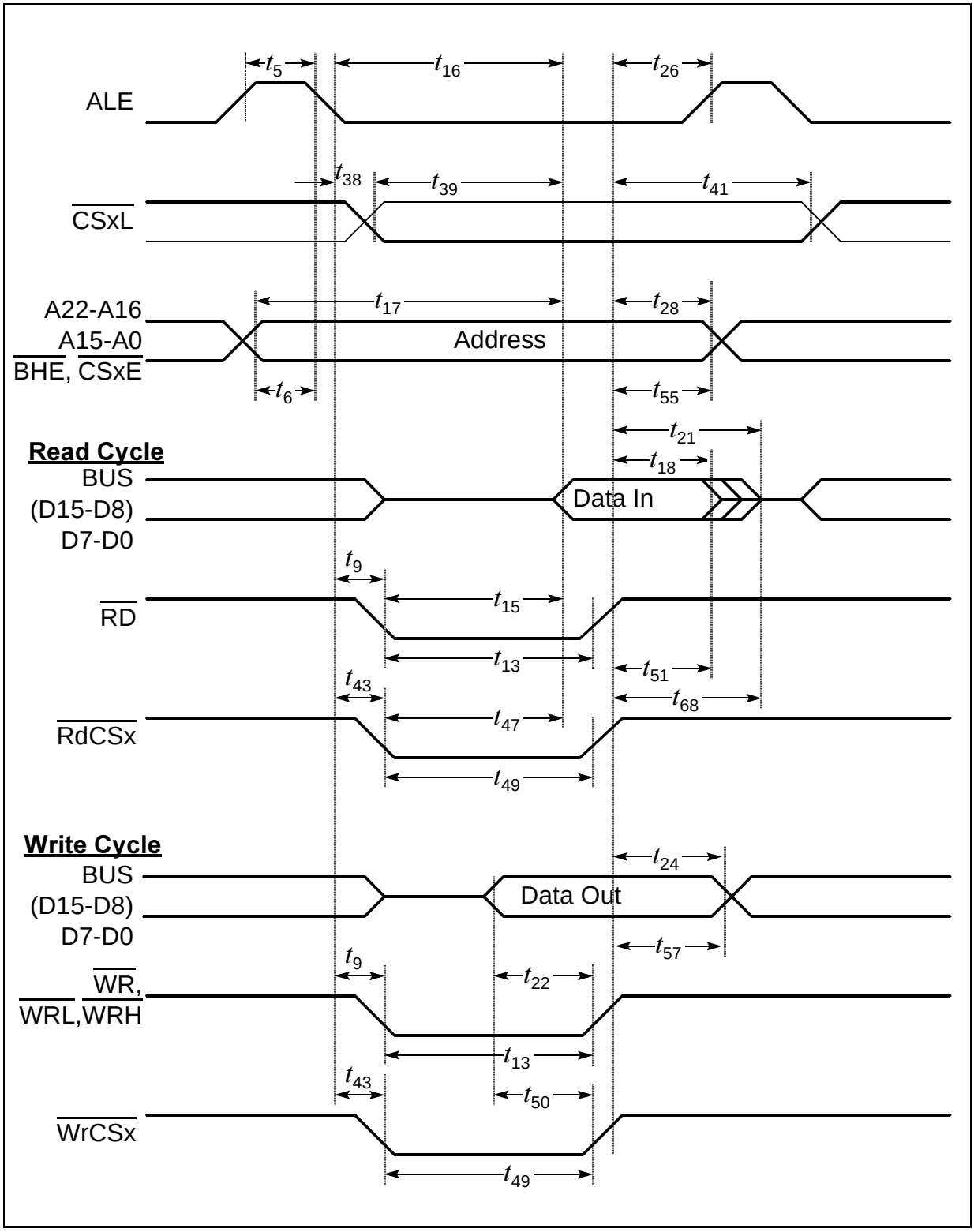

Figure 22 External Memory Cycle: Demultiplexed Bus, No Read/Write Delay, Normal ALE

AC Characteristics

CLKOUT and $\overline{\text{READY}}$ (Reduced Supply Voltage Range)

(Operating Conditions apply)

Parameter	Symbol		Max. CPU Clock = 20 MHz		Variable CPU Clock 1 / 2TCL = 1 to 20 MHz		Unit
			min.	max.	min.	max.	
CLKOUT cycle time	t_{29}	CC	40	40	2TCL	2TCL	ns
CLKOUT high time	t_{30}	CC	15	–	TCL – 10	–	ns
CLKOUT low time	t_{31}	CC	13	–	TCL – 12	–	ns
CLKOUT rise time	t_{32}	CC	–	12	–	12	ns
CLKOUT fall time	t_{33}	CC	–	8	–	8	ns
CLKOUT rising edge to ALE falling edge	t_{34}	CC	$0 + t_A$	$8 + t_A$	$0 + t_A$	$8 + t_A$	ns
Synchronous $\overline{\text{READY}}$ setup time to CLKOUT	t_{35}	SR	18	–	18	–	ns
Synchronous $\overline{\text{READY}}$ hold time after CLKOUT	t_{36}	SR	4	–	4	–	ns
Asynchronous $\overline{\text{READY}}$ low time	t_{37}	SR	68	–	$2TCL + t_{58}$	–	ns
Asynchronous $\overline{\text{READY}}$ setup time [1]	t_{58}	SR	18	–	18	–	ns
Asynchronous $\overline{\text{READY}}$ hold time [1]	t_{59}	SR	4	–	4	–	ns
Async. $\overline{\text{READY}}$ hold time after $\overline{\text{RD}}$, $\overline{\text{WR}}$ high (Demultiplexed Bus) [2]	t_{60}	SR	0	$0 + 2t_A + t_C + t_F$ [2]	0	$\text{TCL} - 25 + 2t_A + t_C + t_F$ [2]	ns

1) These timings are given for test purposes only, in order to assure recognition at a specific clock edge.

2) Demultiplexed bus is the worst case. For multiplexed bus 2TCL are to be added to the maximum values. This adds even more time for deactivating $\overline{\text{READY}}$.
The $2t_A$ and t_C refer to the next following bus cycle, t_F refers to the current bus cycle.
The maximum limit for t_{60} must be fulfilled if the next following bus cycle is $\overline{\text{READY}}$ controlled.

Package Outlines (continued)

Plastic Package, P-TQFP-100-1 (SMD)
(Plastic Thin Metric Quad Flat Package)

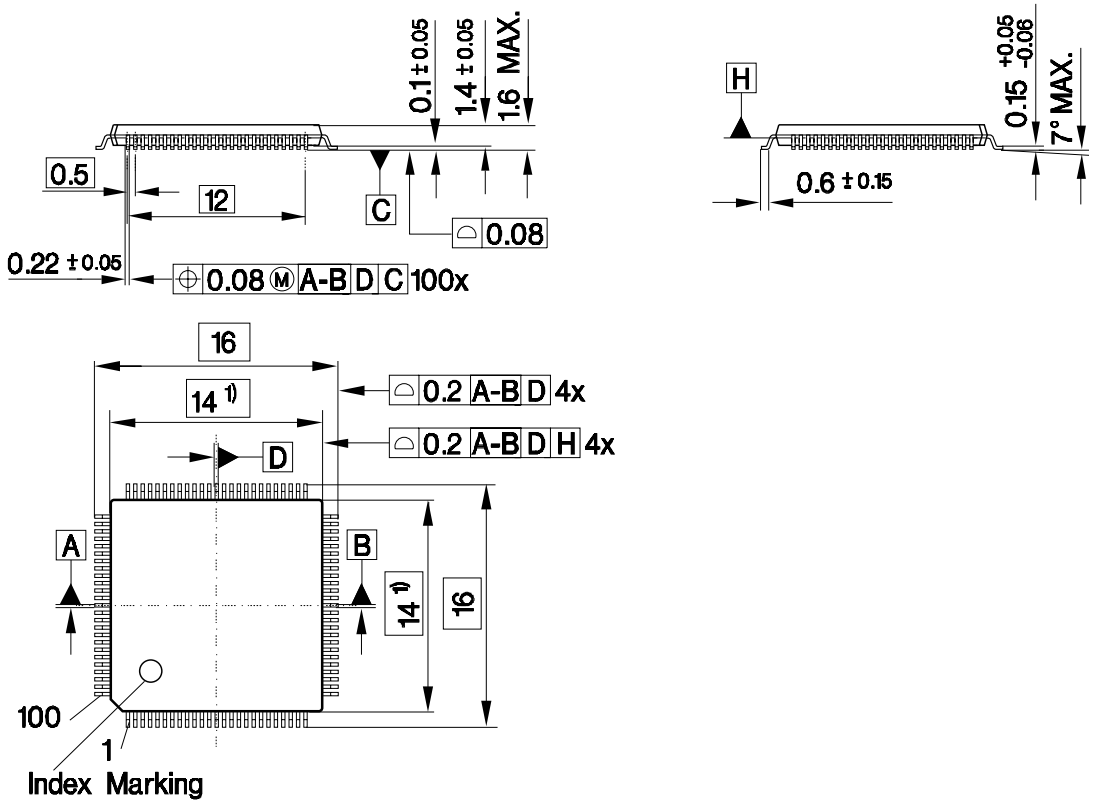

Figure 26

Sorts of Packing

Package outlines for tubes, trays, etc. are contained in our Data Book “Package Information”

SMD = Surface Mounted Device

Dimensions in mm