Infineon Technologies - C161PILM3VCABXUMA1 Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	C166
Core Size	16-Bit
Speed	20MHz
Connectivity	EBI/EMI, I²C, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	76
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	3K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	PG-MQFP-100-2
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/c161pilm3vcabxuma1

C161PI Revision History:	1999-07 Preliminary	
Previous Versions:	1998-05 1998-01 1997-12	(C161RI / Preliminary) (C161RI / Advance Information) (C161RI / Advance Information)

Page	Subjects
---	3 V specification introduced
4, 5, 7	Signal FOUT added
14	XRAM description added
15	Unlatched $\overline{CS}$ description added
23	Block Diagram corrected
24	Description of divider chain improved
25, 51, 52	ADC description updated to 10-bit
36, 37	Revised description of Absolute Max. Ratings and Operating Conditions
39, 44	Power supply values improved
45 - 50	Revised description for clock generation including PLL
54 ff.	Standard 25-MHz timing

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Please send your proposal (including a reference to this document) to:

mcdocu.comments@infineon.com

The C161PI is the successor of the C161RI. Therefore this data sheet also replaces the C161RI data sheet (see also revision history).

Edition 1999-07

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St.-Martin-Strasse 53
D-81541 München

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Pin Configuration TQFP Package

(top view)

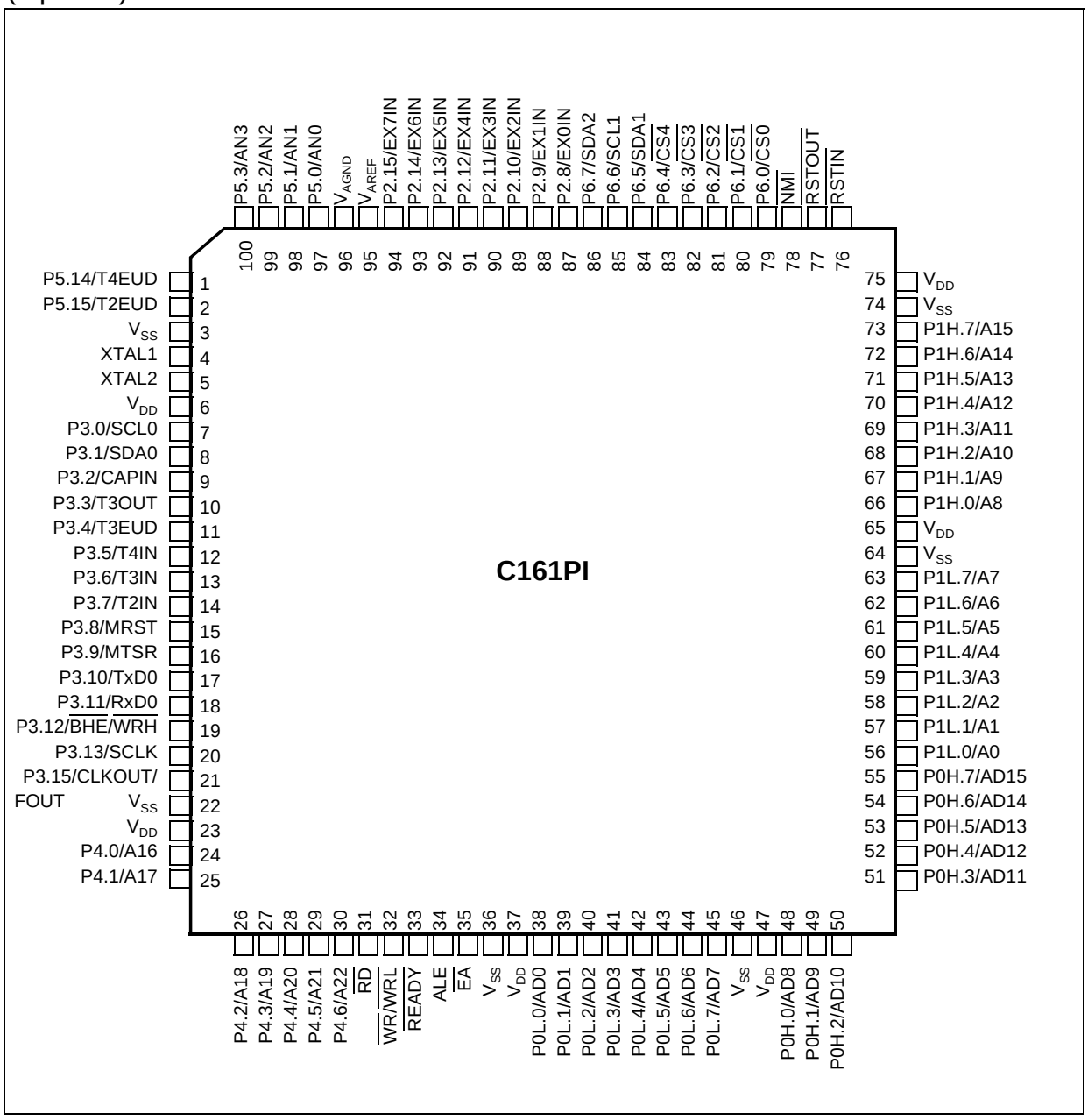

Figure 3

Table 1 Pin Definitions and Functions

Symbol	Pin Num. TQFP	Pin Num. MQFP	Input Outp.	Function
P5			I	Port 5 is a 6-bit input-only port with Schmitt-Trigger characteristics. The pins of Port 5 also serve as (up to 4) analog input channels for the A/D converter, or they serve as timer inputs:
P5.0	97	99	I	AN0
P5.1	98	100	I	AN1
P5.2	99	1	I	AN2
P5.3	100	2	I	AN3
P5.14	1	3	I	T4EUD GPT1 Timer T4 Ext. Up/Down Ctrl. Input
P5.15	2	4	I	T2EUD GPT1 Timer T5 Ext. Up/Down Ctrl. Input
XTAL1	4	6	I	XTAL1: Input to the oscillator amplifier and input to the internal clock generator
XTAL2	5	7	O	XTAL2: Output of the oscillator amplifier circuit. To clock the device from an external source, drive XTAL1, while leaving XTAL2 unconnected. Minimum and maximum high/low and rise/fall times specified in the AC Characteristics must be observed.

Table 1 Pin Definitions and Functions (continued)

Symbol	Pin Num. TQFP	Pin Num. MQFP	Input Outp.	Function
P4			IO	Port 4 is a 7-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 4 outputs can be configured as push/pull or open drain drivers. The input threshold of Port 4 is selectable (TTL or special). Port 4 can be used to output the segment address lines:
P4.0	24	26	O	A16 Least Significant Segment Address Line
P4.1	25	27	O	A17 Segment Address Line
P4.2	26	28	O	A18 Segment Address Line
P4.3	27	29	O	A19 Segment Address Line
P4.4	28	30	O	A20 Segment Address Line
P4.5	29	31	O	A21 Segment Address Line
P4.6	30	32	O	A22 Most Significant Segment Address Line
$\overline{RD}$	31	33	O	External Memory Read Strobe. $\overline{RD}$ is activated for every external instruction or data read access.
$\overline{WR}$/ WRL	32	34	O	External Memory Write Strobe. In $\overline{WR}$-mode this pin is activated for every external data write access. In WRL-mode this pin is activated for low byte data write accesses on a 16-bit bus, and for every data write access on an 8-bit bus. See WRCFG in register SYSCON for mode selection.
$\overline{READY}$	33	35	I	Ready Input. When the Ready function is enabled, a high level at this pin during an external memory access will force the insertion of memory cycle time waitstates until the pin returns to a low level. An internal pullup device will hold this pin high when nothing is driving it.
ALE	34	36	O	Address Latch Enable Output. Can be used for latching the address into external memory or an address latch in the multiplexed bus modes.

Table 2 C161PI Interrupt Nodes

Source of Interrupt or PEC Service Request	Request Flag	Enable Flag	Interrupt Vector	Vector Location	Trap Number
External Interrupt 0	CC8IR	CC8IE	CC8INT	$00'0060_H$	18_H
External Interrupt 1	CC9IR	CC9IE	CC9INT	$00'0064_H$	19_H
External Interrupt 2	CC10IR	CC10IE	CC10INT	$00'0068_H$	$1A_H$
External Interrupt 3	CC11IR	CC11IE	CC11INT	$00'006C_H$	$1B_H$
External Interrupt 4	CC12IR	CC12IE	CC12INT	$00'0070_H$	$1C_H$
External Interrupt 5	CC13IR	CC13IE	CC13INT	$00'0074_H$	$1D_H$
External Interrupt 6	CC14IR	CC14IE	CC14INT	$00'0078_H$	$1E_H$
External Interrupt 7	CC15IR	CC15IE	CC15INT	$00'007C_H$	$1F_H$
GPT1 Timer 2	T2IR	T2IE	T2INT	$00'0088_H$	22_H
GPT1 Timer 3	T3IR	T3IE	T3INT	$00'008C_H$	23_H
GPT1 Timer 4	T4IR	T4IE	T4INT	$00'0090_H$	24_H
GPT2 Timer 5	T5IR	T5IE	T5INT	$00'0094_H$	25_H
GPT2 Timer 6	T6IR	T6IE	T6INT	$00'0098_H$	26_H
GPT2 CAPREL Register	CRIR	CRIE	CRINT	$00'009C_H$	27_H
A/D Conversion Complete	ADCIR	ADCIE	ADCINT	$00'00A0_H$	28_H
A/D Overrun Error	ADEIR	ADEIE	ADEINT	$00'00A4_H$	29_H
ASC0 Transmit	S0TIR	S0TIE	S0TINT	$00'00A8_H$	$2A_H$
ASC0 Transmit Buffer	S0TBIR	S0TBIE	S0TBINT	$00'011C_H$	47_H
ASC0 Receive	S0RIR	S0RIE	S0RINT	$00'00AC_H$	$2B_H$
ASC0 Error	S0EIR	S0EIE	S0EINT	$00'00B0_H$	$2C_H$
SSC Transmit	SCTIR	SCTIE	SCTINT	$00'00B4_H$	$2D_H$
SSC Receive	SCRIR	SCRIE	SCRINT	$00'00B8_H$	$2E_H$
SSC Error	SCEIR	SCEIE	SCEINT	$00'00BC_H$	$2F_H$
I^2C Data Transfer Event	XP0IR	XP0IE	XP0INT	$00'0100_H$	40_H
I^2C Protocol Event	XP1IR	XP1IE	XP1INT	$00'0104_H$	41_H
X-Peripheral Node 2	XP2IR	XP2IE	XP2INT	$00'0108_H$	42_H
PLL Unlock / RTC	XP3IR	XP3IE	XP3INT	$00'010C_H$	43_H

The state of this latch may be used to clock timer T5. The overflows/underflows of timer T6 can additionally be used to cause a reload from the CAPREL register. The CAPREL register may capture the contents of timer T5 based on an external signal transition on the corresponding port pin (CAPIN), and timer T5 may optionally be cleared after the capture procedure. This allows absolute time differences to be measured or pulse multiplication to be performed without software overhead.

The capture trigger (timer T5 to CAPREL) may also be generated upon transitions of GPT1 timer T3's inputs T3IN and/or T3EUD. This is especially advantageous when T3 operates in Incremental Interface Mode.

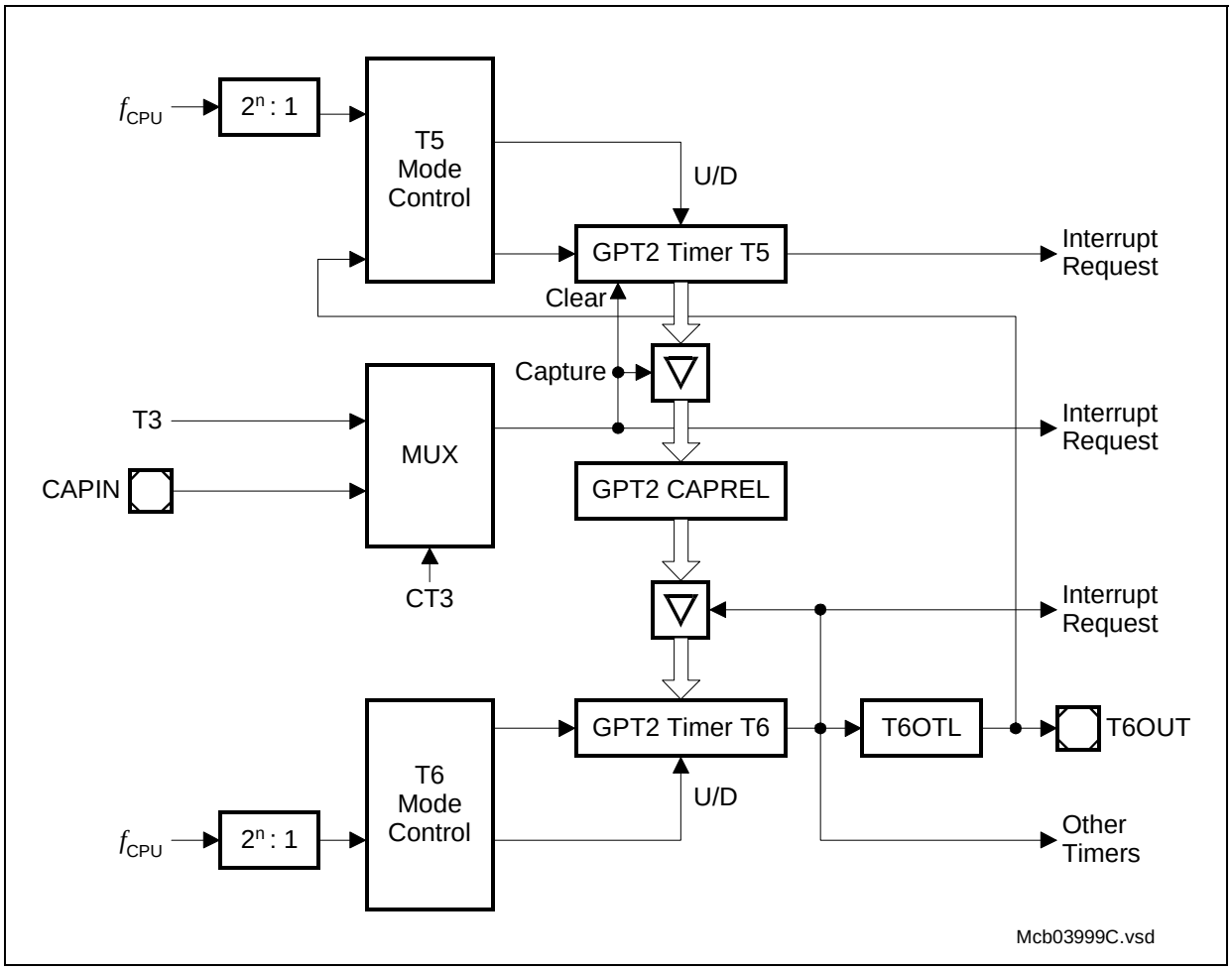

Figure 7 Block Diagram of GPT2

Table 5 C161PI Registers, Ordered by Name (continued)

Name	Physical Address	8-Bit Addr.	Description	Reset Value
T14REL	F0D0$_H$ **E**	68$_H$	RTC Timer 14 Reload Register	no
T2	FE40$_H$	20$_H$	GPT1 Timer 2 Register	0000$_H$
T2CON b	FF40$_H$	A0$_H$	GPT1 Timer 2 Control Register	0000$_H$
T2IC b	FF60$_H$	B0$_H$	GPT1 Timer 2 Interrupt Control Register	0000$_H$
T3	FE42$_H$	21$_H$	GPT1 Timer 3 Register	0000$_H$
T3CON b	FF42$_H$	A1$_H$	GPT1 Timer 3 Control Register	0000$_H$
T3IC b	FF62$_H$	B1$_H$	GPT1 Timer 3 Interrupt Control Register	0000$_H$
T4	FE44$_H$	22$_H$	GPT1 Timer 4 Register	0000$_H$
T4CON b	FF44$_H$	A2$_H$	GPT1 Timer 4 Control Register	0000$_H$
T4IC b	FF64$_H$	B2$_H$	GPT1 Timer 4 Interrupt Control Register	0000$_H$
T5	FE46$_H$	23$_H$	GPT2 Timer 5 Register	0000$_H$
T5CON b	FF46$_H$	A3$_H$	GPT2 Timer 5 Control Register	0000$_H$
T5IC b	FF66$_H$	B3$_H$	GPT2 Timer 5 Interrupt Control Register	0000$_H$
T6	FE48$_H$	24$_H$	GPT2 Timer 6 Register	0000$_H$
T6CON b	FF48$_H$	A4$_H$	GPT2 Timer 6 Control Register	0000$_H$
T6IC b	FF68$_H$	B4$_H$	GPT2 Timer 6 Interrupt Control Register	0000$_H$
TFR b	FFAC$_H$	D6$_H$	Trap Flag Register	0000$_H$
WDT	FEAE$_H$	57$_H$	Watchdog Timer Register (read only)	0000$_H$
WDTCON	FFAE$_H$	D7$_H$	Watchdog Timer Control Register	[2] 00xx$_H$
XP0IC b	F186$_H$ **E**	C3$_H$	I²C Data Interrupt Control Register	0000$_H$
XP1IC b	F18E$_H$ **E**	C7$_H$	I²C Protocol Interrupt Control Register	0000$_H$
XP2IC b	F196$_H$ **E**	CB$_H$	X-Peripheral 2 Interrupt Control Register	0000$_H$
XP3IC b	F19E$_H$ **E**	CF$_H$	RTC Interrupt Control Register	0000$_H$
ZEROS b	FF1C$_H$	8E$_H$	Constant Value 0's Register (read only)	0000$_H$

1) The system configuration is selected during reset.

2) The reset value depends on the indicated reset source.

Operating Conditions

The following operating conditions must not be exceeded in order to ensure correct operation of the C161PI. All parameters specified in the following sections refer to these operating conditions, unless otherwise noticed.

Table 7 Operating Condition Parameters

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Standard digital supply voltage	V_{DD}	4.5	5.5	V	Active mode, f_{CPUmax} = 25 MHz
		2.5 [1]	5.5	V	PowerDown mode
Reduced digital supply voltage	V_{DD}	3.0	3.6	V	Active mode, f_{CPUmax} = 20 MHz
		2.5 [1]	3.6	V	PowerDown mode
Digital ground voltage	V_{SS}	0		V	Reference voltage
Overload current	I_{OV}	-	±5	mA	Per pin [2] [3]
Absolute sum of overload currents	$\Sigma\|I_{OV}\|$	-	50	mA	[3]
External Load Capacitance	C_L	-	100	pF	Pin drivers in **fast edge** mode (PDCR.BIPEC = '0')
		-	50	pF	Pin drivers in **reduced edge** mode (PDCR.BIPEC = '1') [3]
Ambient temperature	T_A	0	70	°C	SAB-C161PI...
		-40	85	°C	SAF-C161PI...
		-40	125	°C	SAK-C161PI...

1) Output voltages and output currents will be reduced when V_{DD} leaves the range defined for active mode.

2) Overload conditions occur if the standard operatings conditions are exceeded, i.e. the voltage on any pin exceeds the specified range (i.e. $V_{OV} > V_{DD}$+0.5V or $V_{OV} < V_{SS}$-0.5V). The absolute sum of input overload currents on all port pins may not exceed **50 mA**. The supply voltage must remain within the specified limits.

3) Not 100% tested, guaranteed by design characterization.

Parameter Interpretation

The parameters listed in the following partly represent the characteristics of the C161PI and partly its demands on the system. To aid in interpreting the parameters right, when evaluating them for a design, they are marked in column “Symbol”:

CC (**C**ontroller **C**haracteristics):
The logic of the C161PI will provide signals with the respective timing characteristics.

SR (**S**ystem **R**equirement):
The external system must provide signals with the respective timing characteristics to the C161PI.

DC Characteristics (Standard Supply Voltage Range)

(Operating Conditions apply)

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input low voltage XTAL1, P3.0, P3.1, P6.5, P6.6, P6.7	V_{IL1} SR	– 0.5	0.3 V_{DD}	V	–
Input low voltage (TTL)	V_{IL} SR	– 0.5	0.2 V_{DD} – 0.1	V	–
Input low voltage (Special Threshold)	V_{ILS} SR	– 0.5	2.0	V	–
Input high voltage $\overline{\text{RSTIN}}$	V_{IH1} SR	0.6 V_{DD}	V_{DD} + 0.5	V	–
Input high voltage XTAL1, P3.0, P3.1, P6.5, P6.6, P6.7	V_{IH2} SR	0.7 V_{DD}	V_{DD} + 0.5	V	–
Input high voltage (TTL)	V_{IH} SR	0.2 V_{DD} + 0.9	V_{DD} + 0.5	V	–
Input high voltage (Special Threshold)	V_{IHS} SR	0.8 V_{DD} - 0.2	V_{DD} + 0.5	V	–
Input Hysteresis (Special Threshold)	HYS	400	–	mV	–
Output low voltage (PORT0, PORT1, Port 4, ALE, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{BHE}}$, CLKOUT, $\overline{\text{RSTOUT}}$)	V_{OL} CC	–	0.45	V	I_{OL} = 2.4 mA
Output low voltage (P3.0, P3.1, P6.5, P6.6, P6.7)	V_{OL2} CC	–	0.4	V	I_{OL2} = 3 mA

AC Characteristics
Definition of Internal Timing

The internal operation of the C161PI is controlled by the internal CPU clock f_{CPU}. Both edges of the CPU clock can trigger internal (e.g. pipeline) or external (e.g. bus cycles) operations.

The specification of the external timing (AC Characteristics) therefore depends on the time between two consecutive edges of the CPU clock, called “TCL” (see figure below).

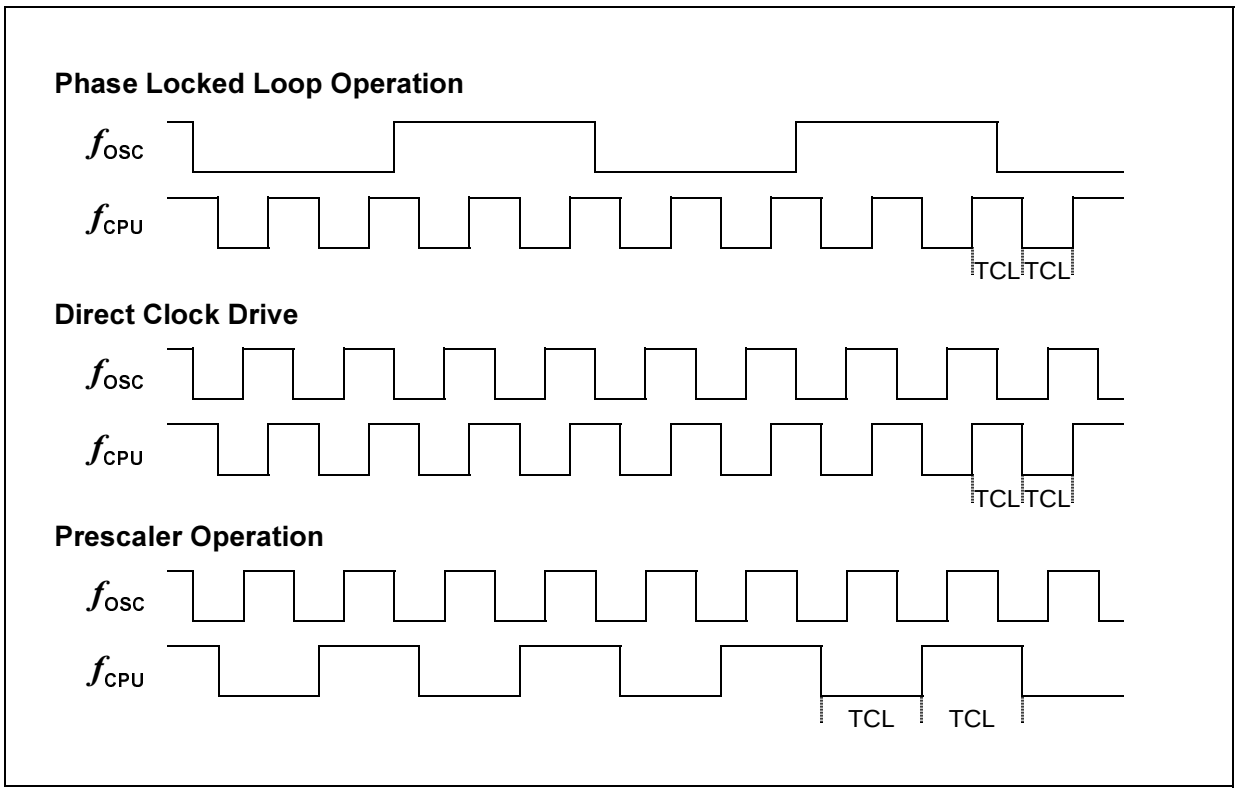

Figure 11 Generation Mechanisms for the CPU Clock

The CPU clock signal f_{CPU} can be generated from the oscillator clock signal f_{OSC} via different mechanisms. The duration of TCLs and their variation (and also the derived external timing) depends on the used mechanism to generate f_{CPU}. This influence must be regarded when calculating the timings for the C161PI.

Note: The example for PLL operation shown in the fig. above refers to a PLL factor of 4.

The used mechanism to generate the CPU clock is selected during reset via the logic levels on pins P0.15-13 (P0H.7-5).

The table below associates the combinations of these three bits with the respective clock generation mode.

Table 8 C161PI Clock Generation Modes

P0.15-13 (P0H.7-5)	CPU Frequency $f_{CPU} = f_{OSC} * F$	External Clock Input Range [1]	Notes
1 1 1	$f_{OSC} * 4$	2.5 to 6.25 MHz	Default configuration
1 1 0	$f_{OSC} * 3$	3.33 to 8.33 MHz	
1 0 1	$f_{OSC} * 2$	5 to 12.5 MHz	
1 0 0	$f_{OSC} * 5$	2 to 5 MHz	
0 1 1	$f_{OSC} * 1$	1 to 25 MHz	Direct drive [2]
0 1 0	$f_{OSC} * 1.5$	6.66 to 16.6 MHz	
0 0 1	$f_{OSC} / 2$	2 to 50 MHz	CPU clock via prescaler
0 0 0	$f_{OSC} * 2.5$	4 to 10 MHz	

1) The external clock input range refers to a CPU clock range of 10...25 MHz.

2) The maximum frequency depends on the duty cycle of the external clock signal.

Prescaler Operation

When pins P0.15-13 (P0H.7-5) equal 001_B during reset the CPU clock is derived from the internal oscillator (input clock signal) by a 2:1 prescaler.
The frequency of f_{CPU} is half the frequency of f_{OSC} and the high and low time of f_{CPU} (i.e. the duration of an individual TCL) is defined by the period of the input clock f_{OSC}.

The timings listed in the AC Characteristics that refer to TCLs therefore can be calculated using the period of f_{OSC} for any TCL.

Phase Locked Loop

For all combinations of pins P0.15-13 (P0H.7-5) except for 001_B and 011_B the on-chip phase locked loop is enabled and provides the CPU clock (see table above). The PLL multiplies the input frequency by the factor **F** which is selected via the combination of pins P0.15-13 (i.e. $f_{CPU} = f_{OSC} * \mathbf{F}$). With every **F**'th transition of f_{OSC} the PLL circuit synchronizes the CPU clock to the input clock. This synchronization is done smoothly, i.e. the CPU clock frequency does not change abruptly.

Due to this adaptation to the input clock the frequency of f_{CPU} is constantly adjusted so it is locked to f_{OSC}. The slight variation causes a jitter of f_{CPU} which also effects the duration of individual TCLs.

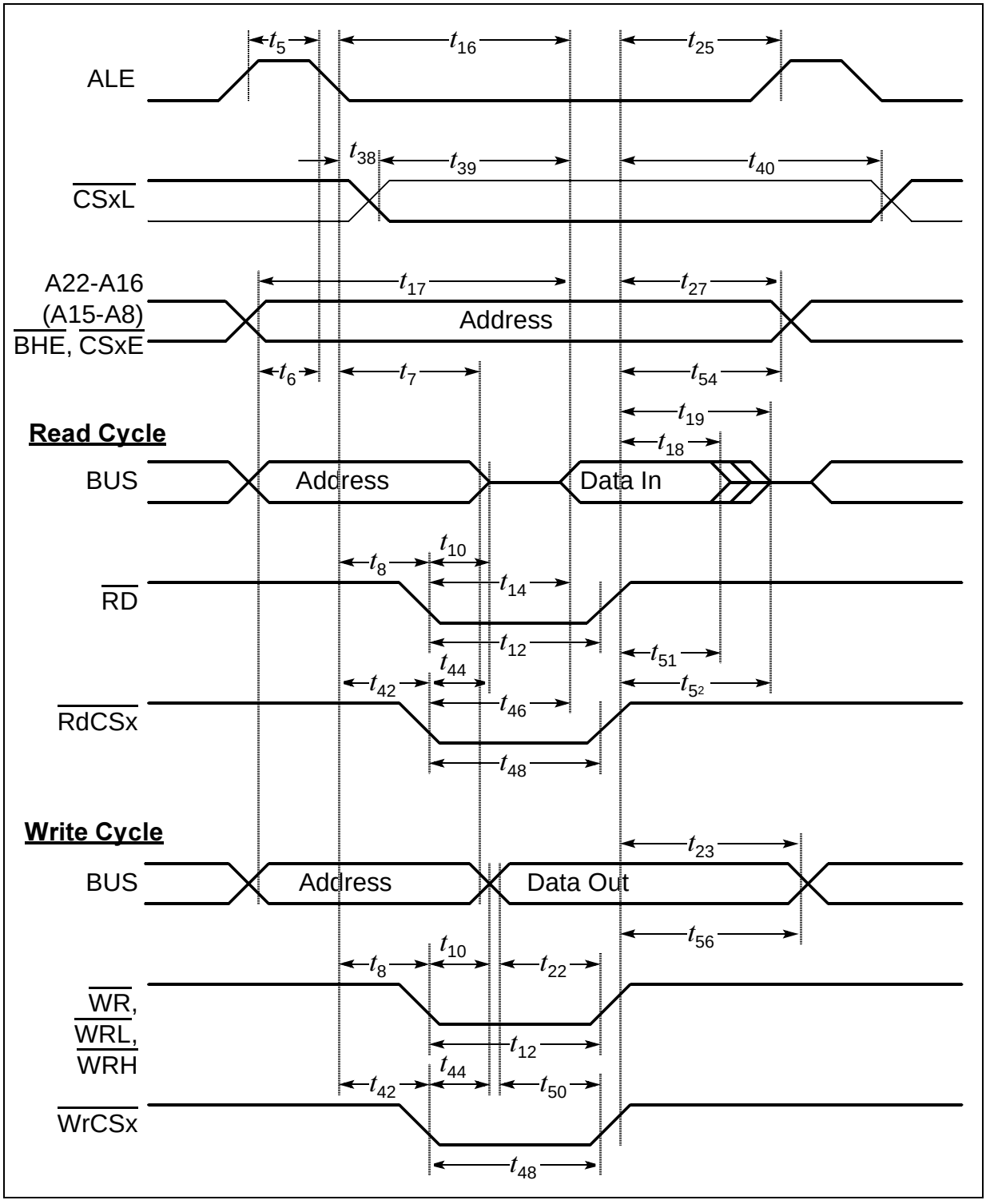

Figure 16 External Memory Cycle: Multiplexed Bus, With Read/Write Delay, Normal ALE

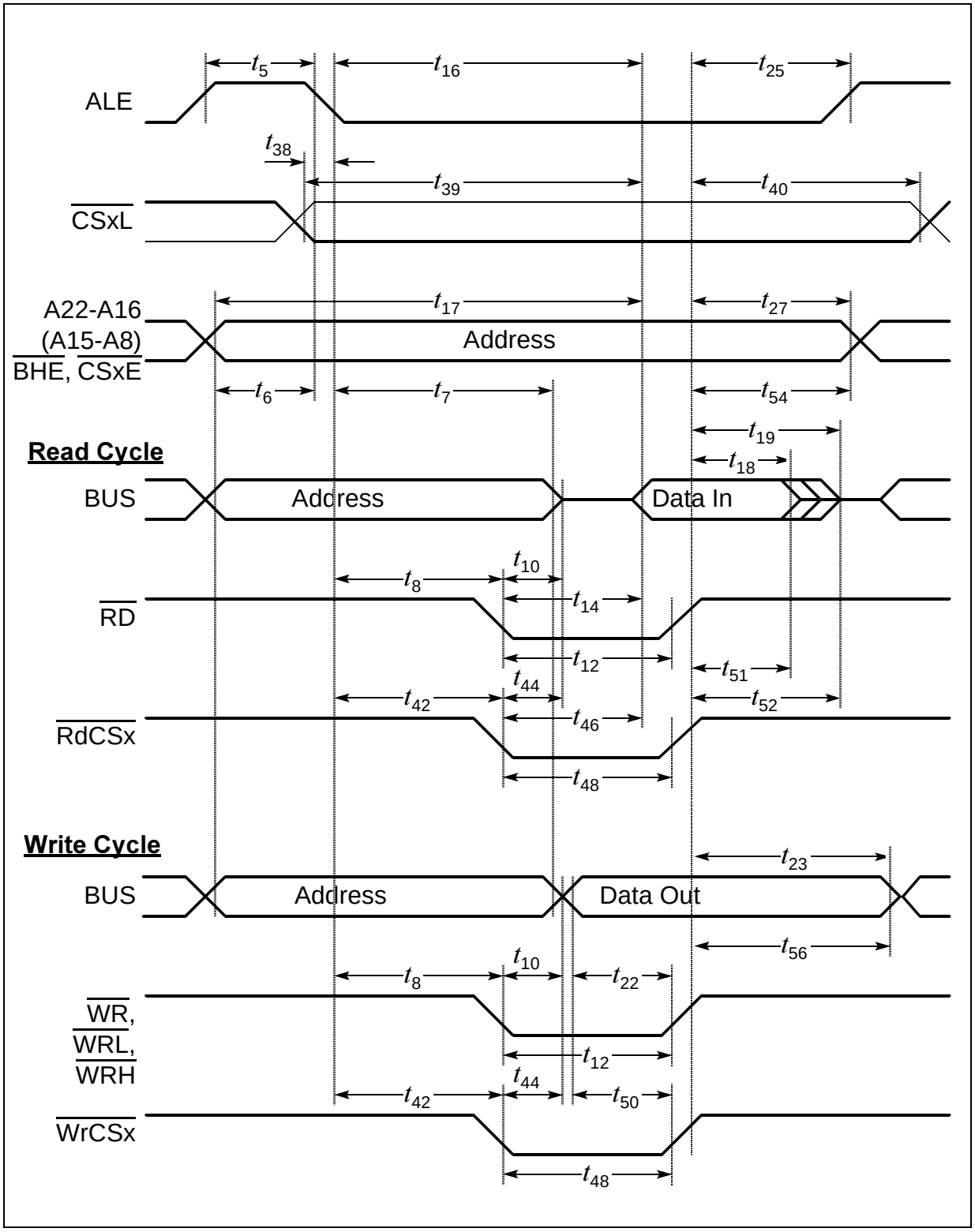

Figure 17 External Memory Cycle:
Multiplexed Bus, With Read/Write Delay, Extended ALE

Demultiplexed Bus (Standard Supply Voltage Range) (continued)
(Operating Conditions apply)
ALE cycle time = 4 TCL + 2t_A + t_C + t_F (80 ns at 25 MHz CPU clock without waitstates)

Parameter	Symbol	Max. CPU Clock = 25 MHz		Variable CPU Clock 1 / 2TCL = 1 to 25 MHz		Unit
		min.	max.	min.	max.	
Address hold after RdCS, WrCS	t_{55} CC	-6 + t_F	–	-6 + t_F	–	ns
Data hold after WrCS	t_{57} CC	6 + t_F	–	TCL - 14 + t_F	–	ns

1) RW-delay and t_A refer to the next following bus cycle (including an access to an on-chip X-Peripheral).

2) Read data are latched with the same clock edge that triggers the address change and the rising RD edge. Therefore address changes before the end of RD have no impact on read cycles.

3) These parameters refer to the latched chip select signals (CSxL). The early chip select signals (CSxE) are specified together with the address and signal BHE (see figures below).

Demultiplexed Bus (Reduced Supply Voltage Range) (continued)
(Operating Conditions apply)
ALE cycle time = 4 TCL + 2t_A + t_C + t_F (100 ns at 20 MHz CPU clock without waitstates)

Parameter	Symbol		Max. CPU Clock = 20 MHz		Variable CPU Clock 1 / 2TCL = 1 to 20 MHz		Unit
			min.	max.	min.	max.	
Data hold after $\overline{WR}$	t_{24}	CC	15 + t_F	–	TCL - 10 + t_F	–	ns
$\overline{ALE}$ rising edge after $\overline{RD}$, $\overline{WR}$	t_{26}	CC	-12 + t_F	–	-12 + t_F	–	ns
Address hold after $\overline{WR}$ [2]	t_{28}	CC	0 + t_F	–	0 + t_F	–	ns
$\overline{ALE}$ falling edge to $\overline{CS}$ [3]	t_{38}	CC	-8 - t_A	10 - t_A	-8 - t_A	10 - t_A	ns
$\overline{CS}$ low to Valid Data In [3]	t_{39}	SR	–	47 + t_C + 2t_A	–	3TCL - 28 + t_C + 2t_A	ns
$\overline{CS}$ hold after $\overline{RD}$, $\overline{WR}$ [3]	t_{41}	CC	9 + t_F	–	TCL - 16 + t_F	–	ns
$\overline{ALE}$ falling edge to $\overline{RdCS}$, $\overline{WrCS}$ (with RW-delay)	t_{42}	CC	19 + t_A	–	TCL - 6 + t_A	–	ns
$\overline{ALE}$ falling edge to $\overline{RdCS}$, $\overline{WrCS}$ (no RW-delay)	t_{43}	CC	-6 + t_A	–	-6 + t_A	–	ns
$\overline{RdCS}$ to Valid Data In (with RW-delay)	t_{46}	SR	–	20 + t_C	–	2TCL - 30 + t_C	ns
$\overline{RdCS}$ to Valid Data In (no RW-delay)	t_{47}	SR	–	45 + t_C	–	3TCL - 30 + t_C	ns
$\overline{RdCS}$, $\overline{WrCS}$ Low Time (with RW-delay)	t_{48}	CC	38 + t_C	–	2TCL - 12 + t_C	–	ns
$\overline{RdCS}$, $\overline{WrCS}$ Low Time (no RW-delay)	t_{49}	CC	63 + t_C	–	3TCL - 12 + t_C	–	ns
Data valid to $\overline{WrCS}$	t_{50}	CC	28 + t_C	–	2TCL - 22 + t_C	–	ns
Data hold after $\overline{RdCS}$	t_{51}	SR	0	–	0	–	ns
Data float after $\overline{RdCS}$ (with RW-delay) [1]	t_{53}	SR	–	30 + t_F	–	2TCL - 20 + 2t_A + t_F [1]	ns
Data float after $\overline{RdCS}$ (no RW-delay) [1]	t_{68}	SR	–	5 + t_F	–	TCL - 20 + 2t_A + t_F [1]	ns

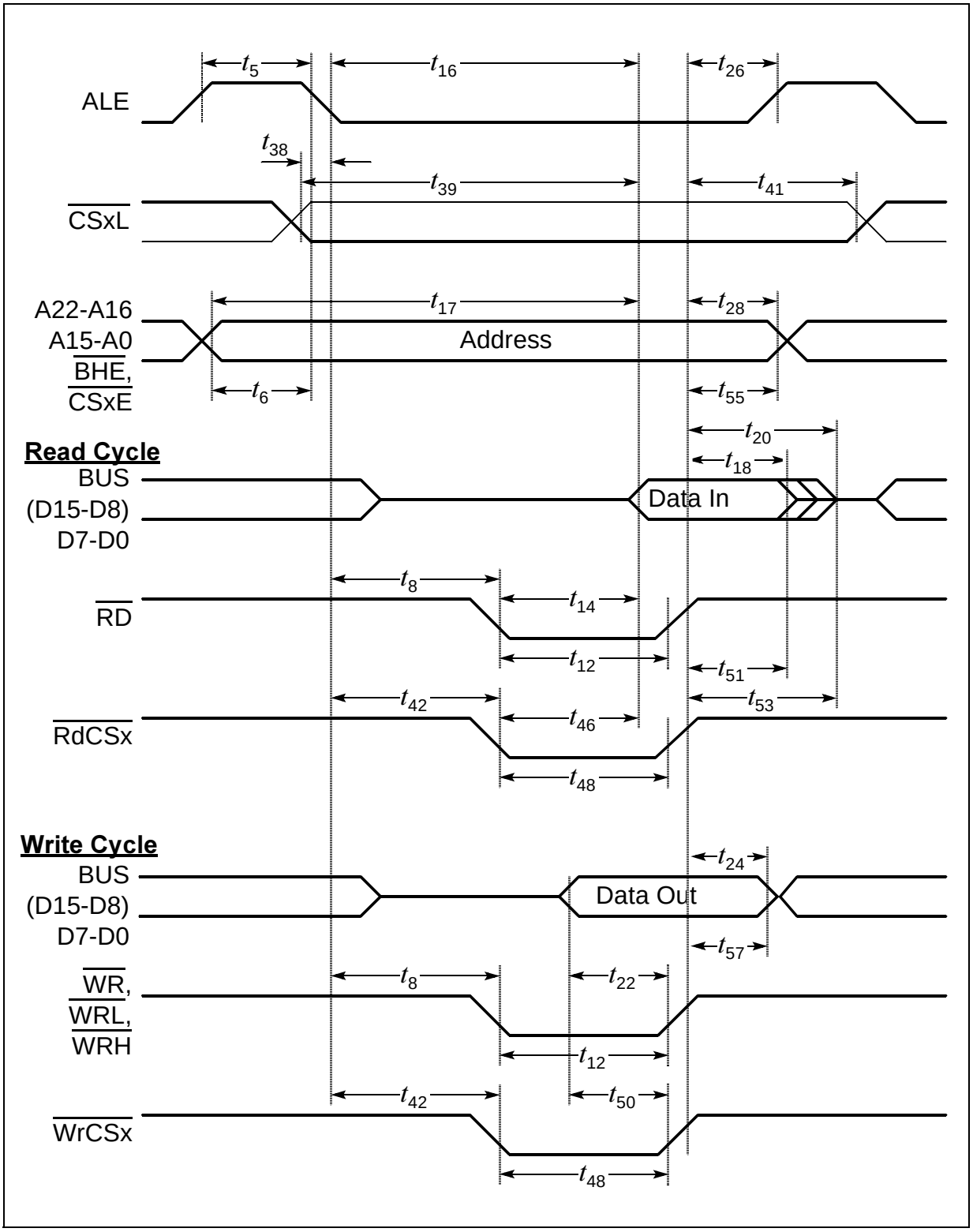

Figure 21 External Memory Cycle: Demultiplexed Bus, With Read/Write Delay, Extended ALE

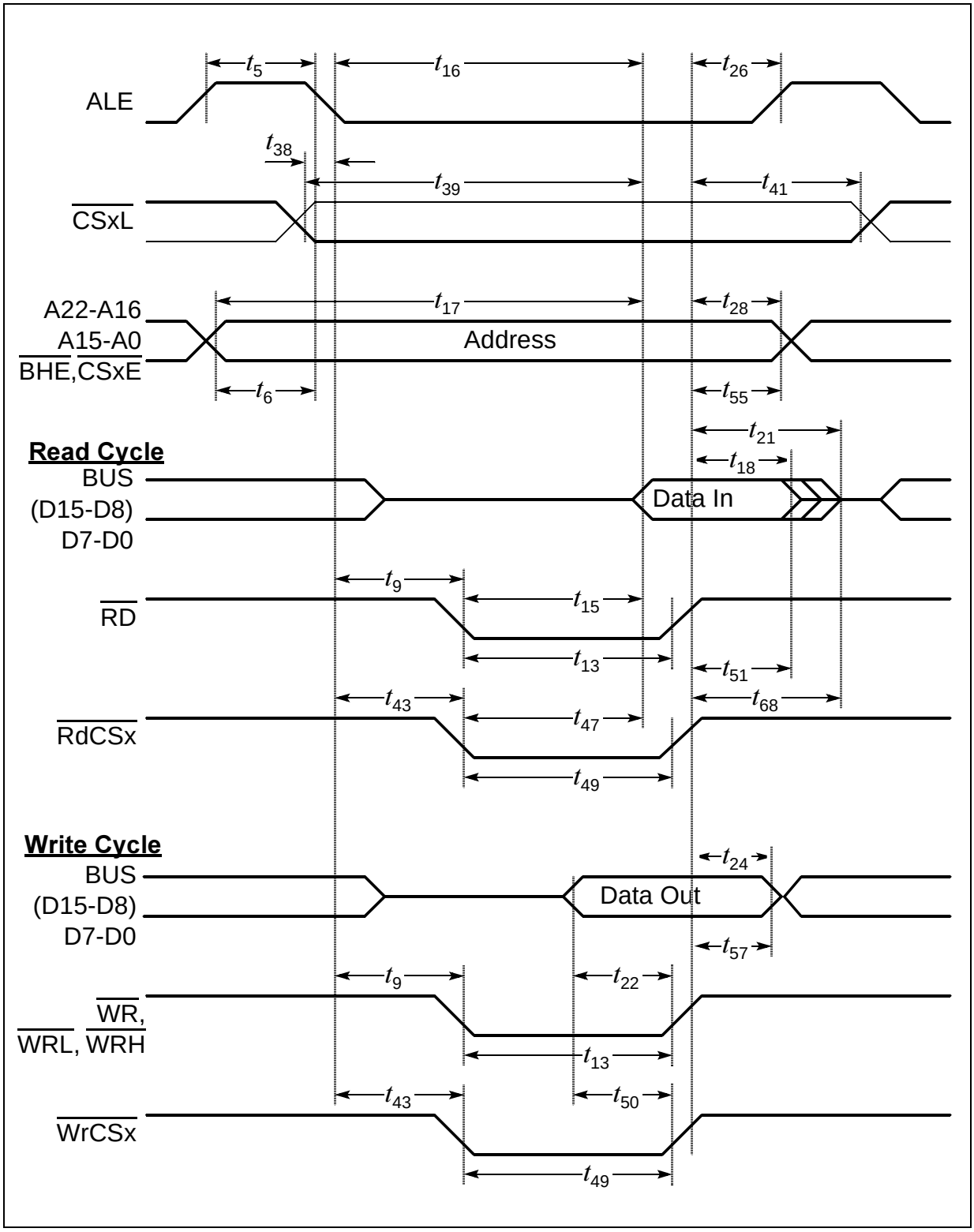

Figure 23 External Memory Cycle: Demultiplexed Bus, No Read/Write Delay, Extended ALE

AC Characteristics

CLKOUT and $\overline{\text{READY}}$ (Standard Supply Voltage Range)

(Operating Conditions apply)

Parameter	Symbol		Max. CPU Clock = 25 MHz		Variable CPU Clock 1 / 2TCL = 1 to 25 MHz		Unit
			min.	max.	min.	max.	
CLKOUT cycle time	t_{29}	CC	40	40	2TCL	2TCL	ns
CLKOUT high time	t_{30}	CC	14	–	TCL – 6	–	ns
CLKOUT low time	t_{31}	CC	10	–	TCL – 10	–	ns
CLKOUT rise time	t_{32}	CC	–	4	–	4	ns
CLKOUT fall time	t_{33}	CC	–	4	–	4	ns
CLKOUT rising edge to ALE falling edge	t_{34}	CC	0 + t_A	10 + t_A	0 + t_A	10 + t_A	ns
Synchronous $\overline{\text{READY}}$ setup time to CLKOUT	t_{35}	SR	14	–	14	–	ns
Synchronous $\overline{\text{READY}}$ hold time after CLKOUT	t_{36}	SR	4	–	4	–	ns
Asynchronous $\overline{\text{READY}}$ low time	t_{37}	SR	54	–	2TCL + t_{58}	–	ns
Asynchronous $\overline{\text{READY}}$ setup time [1]	t_{58}	SR	14	–	14	–	ns
Asynchronous $\overline{\text{READY}}$ hold time [1]	t_{59}	SR	4	–	4	–	ns
Async. $\overline{\text{READY}}$ hold time after $\overline{\text{RD}}$, $\overline{\text{WR}}$ high (Demultiplexed Bus) [2]	t_{60}	SR	0	0 + 2t_A + t_C + t_F [2]	0	TCL - 20 + 2t_A + t_C + t_F [2]	ns

1) These timings are given for test purposes only, in order to assure recognition at a specific clock edge.

2) Demultiplexed bus is the worst case. For multiplexed bus 2TCL are to be added to the maximum values. This adds even more time for deactivating $\overline{\text{READY}}$.
The 2t_A and t_C refer to the next following bus cycle, t_F refers to the current bus cycle.
The maximum limit for t_{60} must be fulfilled if the next following bus cycle is $\overline{\text{READY}}$ controlled.

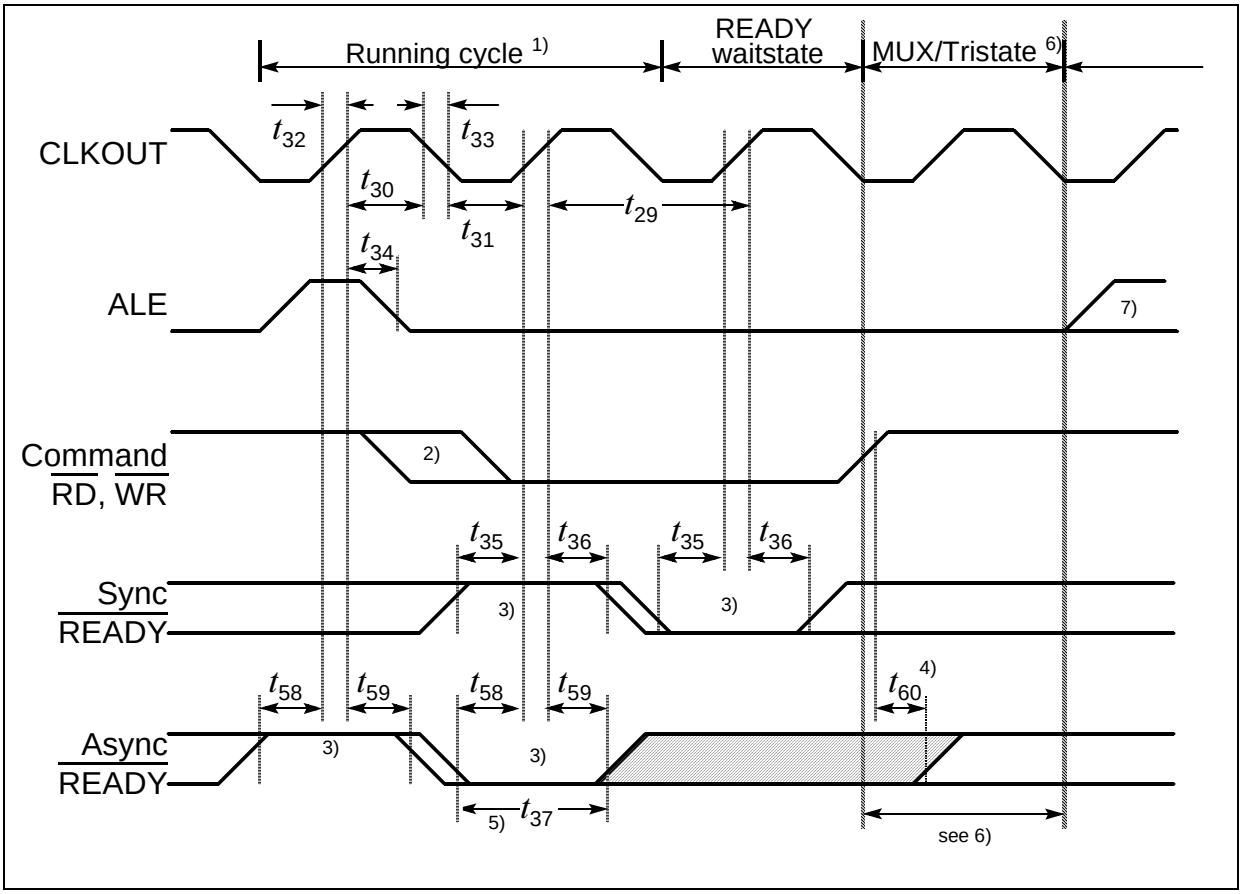

Figure 24 CLKOUT and READY

Notes

1) Cycle as programmed, including MCTC waitstates (Example shows 0 MCTC WS).
2) The leading edge of the respective command depends on RW-delay.
3) READY sampled HIGH at this sampling point generates a READY controlled waitstate,
READY sampled LOW at this sampling point terminates the currently running bus cycle.
4) READY may be deactivated in response to the trailing (rising) edge of the corresponding command (RD or WR).
5) If the Asynchronous READY signal does not fulfill the indicated setup and hold times with respect to CLKOUT (e.g. because CLKOUT is not enabled), it must fulfill t_{37} in order to be safely synchronized. This is guaranteed, if READY is removed in reponse to the command (see Note 4)).
6) Multiplexed bus modes have a MUX waitstate added after a bus cycle, and an additional MTTC waitstate may be inserted here.
For a multiplexed bus with MTTC waitstate this delay is 2 CLKOUT cycles, for a demultiplexed bus without MTTC waitstate this delay is zero.
7) The next external bus cycle may start here.

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