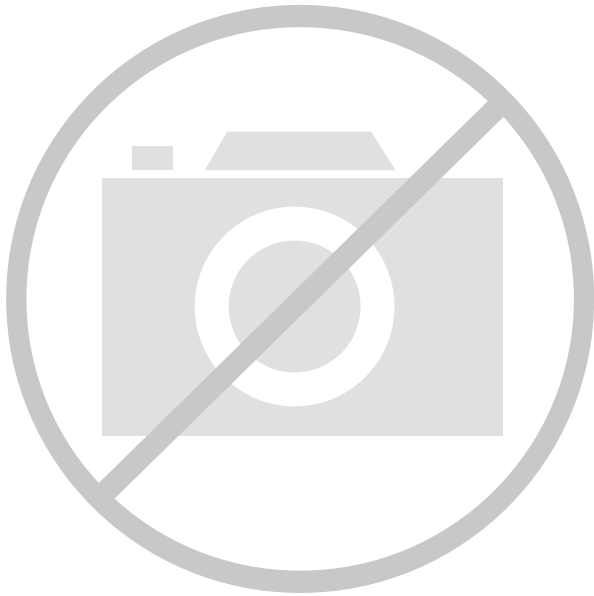




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Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details

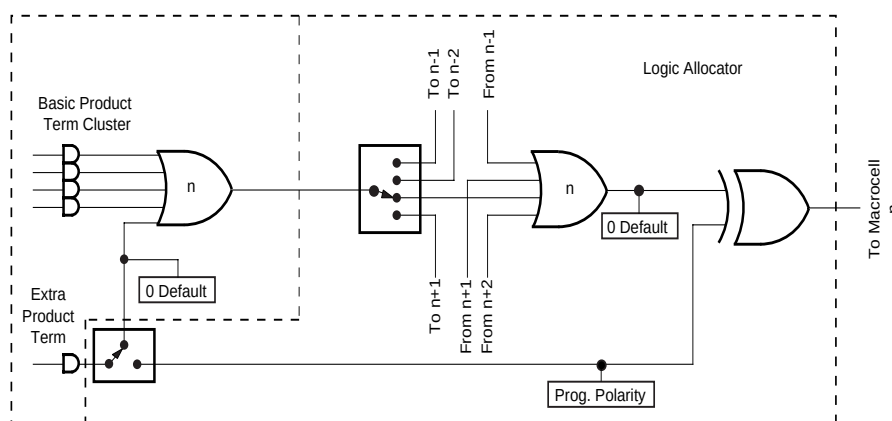
Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	12 ns
Voltage Supply - Internal	3V ~ 3.6V
Number of Logic Elements/Blocks	-
Number of Macrocells	192
Number of Gates	-
Number of I/O	96
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-BGA
Supplier Device Package	144-FPBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/m4a3-192-96-12fai

Table 6. Logic Allocator for All ispMACH 4A Devices (except M4A(3,5)-32/32)

Output Macrocell	Available Clusters	Output Macrocell	Available Clusters
M ₀	C ₀ , C ₁ , C ₂	M ₈	C ₇ , C ₈ , C ₉ , C ₁₀
M ₁	C ₀ , C ₁ , C ₂ , C ₃	M ₉	C ₈ , C ₉ , C ₁₀ , C ₁₁
M ₂	C ₁ , C ₂ , C ₃ , C ₄	M ₁₀	C ₉ , C ₁₀ , C ₁₁ , C ₁₂
M ₃	C ₂ , C ₃ , C ₄ , C ₅	M ₁₁	C ₁₀ , C ₁₁ , C ₁₂ , C ₁₃
M ₄	C ₃ , C ₄ , C ₅ , C ₆	M ₁₂	C ₁₁ , C ₁₂ , C ₁₃ , C ₁₄
M ₅	C ₄ , C ₅ , C ₆ , C ₇	M ₁₃	C ₁₂ , C ₁₃ , C ₁₄ , C ₁₅
M ₆	C ₅ , C ₆ , C ₇ , C ₈	M ₁₄	C ₁₃ , C ₁₄ , C ₁₅
M ₇	C ₆ , C ₇ , C ₈ , C ₉	M ₁₅	C ₁₄ , C ₁₅

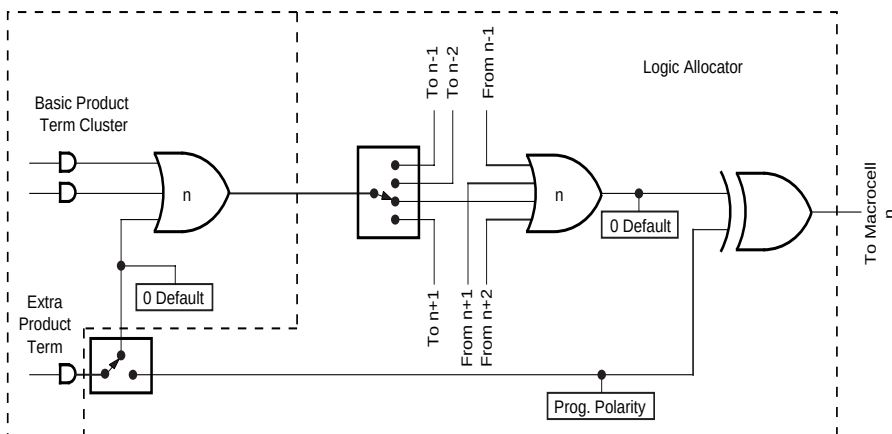
Table 7. Logic Allocator for M4A(3,5)-32/32

Output Macrocell	Available Clusters	Output Macrocell	Available Clusters
M ₀	C ₀ , C ₁ , C ₂	M ₈	C ₈ , C ₉ , C ₁₀
M ₁	C ₀ , C ₁ , C ₂ , C ₃	M ₉	C ₈ , C ₉ , C ₁₀ , C ₁₁
M ₂	C ₁ , C ₂ , C ₃ , C ₄	M ₁₀	C ₉ , C ₁₀ , C ₁₁ , C ₁₂
M ₃	C ₂ , C ₃ , C ₄ , C ₅	M ₁₁	C ₁₀ , C ₁₁ , C ₁₂ , C ₁₃
M ₄	C ₃ , C ₄ , C ₅ , C ₆	M ₁₂	C ₁₁ , C ₁₂ , C ₁₃ , C ₁₄
M ₅	C ₄ , C ₅ , C ₆ , C ₇	M ₁₃	C ₁₂ , C ₁₃ , C ₁₄ , C ₁₅
M ₆	C ₅ , C ₆ , C ₇	M ₁₄	C ₁₃ , C ₁₄ , C ₁₅
M ₇	C ₆ , C ₇	M ₁₅	C ₁₄ , C ₁₅



a. Synchronous Mode

17466G-005

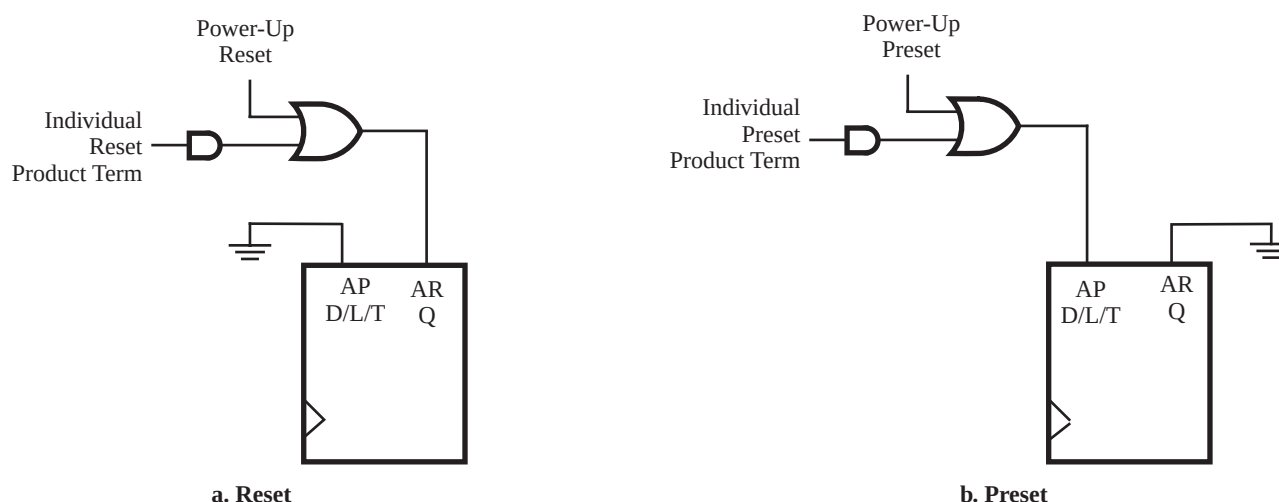


b. Asynchronous Mode

17466G-006

Figure 2. Logic Allocator: Configuration of Cluster “n” Set by Mode of Macrocell “n”

A reset/preset swapping feature in each macrocell allows for reset and preset to be exchanged, providing flexibility. In asynchronous mode (Figure 8), a single individual product term is provided for initialization. It can be selected to control reset or preset.



17466G-014

17466G-015

Figure 8. Asynchronous Mode Initialization Configurations

Note that the reset/preset swapping selection feature effects power-up reset as well. The initialization functionality of the flip-flops is illustrated in Table 9. The macrocell sends its data to the output switch matrix and the input switch matrix. The output switch matrix can route this data to an output if so desired. The input switch matrix can send the signal back to the central switch matrix as feedback.

Table 9. Asynchronous Reset/Preset Operation

AR	AP	CLK/LE ¹	Q+
0	0	X	See Table 8
0	1	X	1
1	0	X	0
1	1	X	0

Note:

1. Transparent latch is unaffected by AR, AP

Table 11. Output Switch Matrix Combinations for M4A3-256/160 and M4A3-256/192

Macrocell	Routable to I/O Cells							
I/O8	M8	M9	M10	M11	M12	M13	M14	M15
I/O9	M8	M9	M10	M11	M12	M13	M14	M15
I/O10	M8	M9	M10	M11	M12	M13	M14	M15
I/O11	M8	M9	M10	M11	M12	M13	M14	M15
I/O12	M8	M9	M10	M11	M12	M13	M14	M15
I/O13	M8	M9	M10	M11	M12	M13	M14	M15
I/O14	M8	M9	M10	M11	M12	M13	M14	M15
I/O15	M8	M9	M10	M11	M12	M13	M14	M15

Table 12. Output Switch Matrix Combinations for M4A(3,5)-32/32

Macrocell	Routable to I/O Cells
M0, M1, M2, M3, M4, M5, M6, M7	I/O0, I/O1, I/O2, I/O3, I/O4, I/O5, I/O6, I/O7
M8, M9, M10, M11, M12, M13, M14, M15	I/O8, I/O9, I/O10, I/O11, I/O12, I/O13, I/O14, I/O15

I/O Cell	Available Macrocells
I/O0, I/O1, I/O2, I/O3, I/O4, I/O5, I/O6, I/O7	M0, M1, M2, M3, M4, M5, M6, M7
I/O8, I/O9, I/O10, I/O11, I/O12, I/O13, I/O14, I/O15	M8, M9, M10, M11, M12, M13, M14, M15

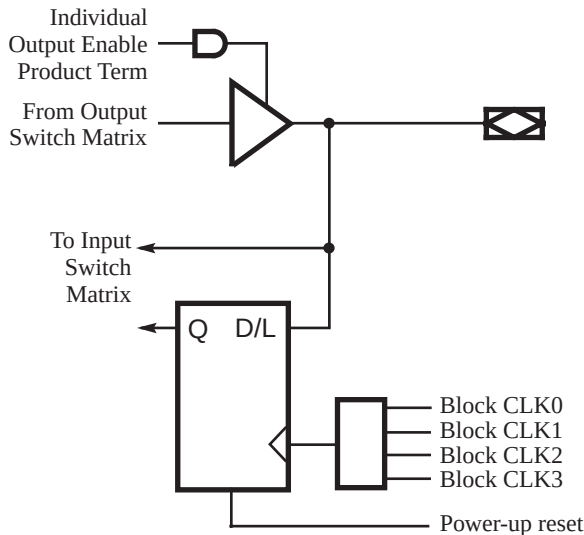
Table 13. Output Switch Matrix Combinations for M4A3-64/64

Macrocell	Routable to I/O Cells
M0, M1	I/O0, I/O1, I/O10, I/O11, I/O12, I/O13, I/O14, I/O15
M2, M3	I/O0, I/O1, I/O2, I/O3, I/O12, I/O13, I/O14, I/O15
M4, M5	I/O0, I/O1, I/O2, I/O3, I/O4, I/O5, I/O14, I/O15
M6, M7	I/O0, I/O1, I/O2, I/O3, I/O4, I/O5, I/O6, I/O7
M8, M9	I/O2, I/O3, I/O4, I/O5, I/O6, I/O7, I/O8, I/O9
M10, M11	I/O4, I/O5, I/O6, I/O7, I/O8, I/O9, I/O10, I/O11
M12, M13	I/O6, I/O7, I/O8, I/O9, I/O10, I/O11, I/O12, I/O13
M14, M15	I/O8, I/O9, I/O10, I/O11, I/O12, I/O13, I/O14, I/O15

I/O Cell	Available Macrocells
I/O0, I/O1	M0, M1, M2, M3, M4, M5, M6, M7
I/O2, I/O3	M2, M3, M4, M5, M6, M7, M8, M9
I/O4, I/O5	M4, M5, M6, M7, M8, M9, M10, M11
I/O6, I/O7	M6, M7, M8, M9, M10, M11, M12, M13
I/O8, I/O9	M8, M9, M10, M11, M12, M13, M14, M15
I/O10, I/O11	M0, M1, M10, M11, M12, M13, M14, M15
I/O12, I/O13	M0, M1, M2, M3, M12, M13, M14, M15
I/O14, I/O15	M0, M1, M2, M3, M4, M5, M14, M15

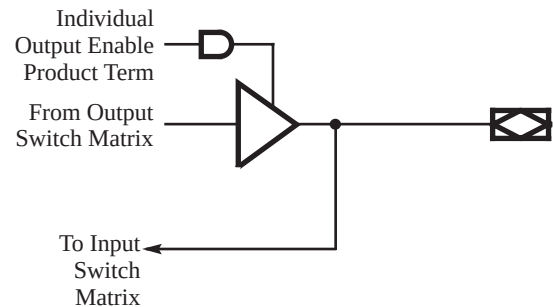
I/O Cell

The I/O cell (Figures 10 and 11) simply consists of a programmable output enable, a feedback path, and flip-flop (except ispMACH 4A devices with 1:1 macrocell-I/O cell ratio). An individual output enable product term is provided for each I/O cell. The feedback signal drives the input switch matrix.



17466G-017

Figure 10. I/O Cell for ispMACH 4A Devices with 2:1 Macrocell-I/O Cell Ratio



17466G-018

Figure 11. I/O Cell for ispMACH 4A Devices with 1:1 Macrocell-I/O Cell Ratio

The I/O cell (Figure 10) contains a flip-flop, which provides the capability for storing the input in a D-type register or latch. The clock can be any of the PAL block clocks. Both the direct and registered versions of the input are sent to the input switch matrix. This allows for such functions as “time-domain-multiplexed” data comparison, where the first data value is stored, and then the second data value is put on the I/O pin and compared with the previous stored value.

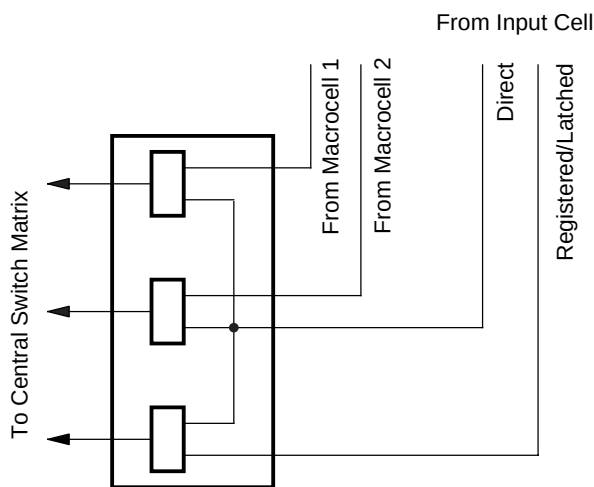
Note that the flip-flop used in the ispMACH 4A I/O cell is independent of the flip-flops in the macrocells. It powers up to a logic low.

Zero-Hold-Time Input Register

The ispMACH 4A devices have a zero-hold-time (ZHT) fuse which controls the time delay associated with loading data into all I/O cell registers and latches. When programmed, the ZHT fuse increases the data path setup delays to input storage elements, matching equivalent delays in the clock path. When the fuse is erased, the setup time to the input storage element is minimized. This feature facilitates doing worst-case designs for which data is loaded from sources which have low (or zero) minimum output propagation delays from clock edges.

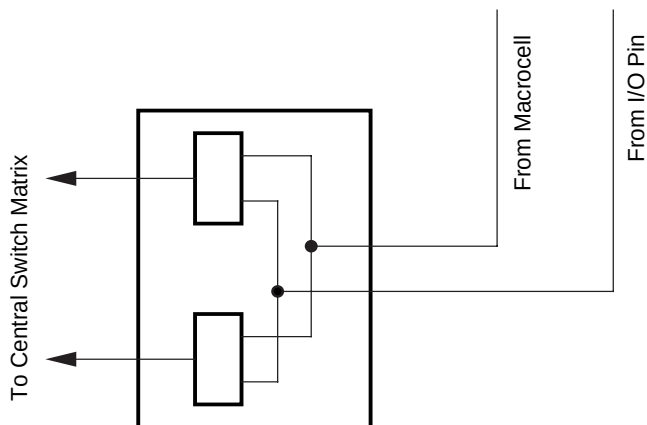
Input Switch Matrix

The input switch matrix (Figures 12 and 13) optimizes routing of inputs to the central switch matrix. Without the input switch matrix, each input and feedback signal has only one way to enter the central switch matrix. The input switch matrix provides additional ways for these signals to enter the central switch matrix.



17466G-002

Figure 12. ispMACH 4A with 2:1 Macrocell-I/O Cell Ratio - Input Switch Matrix



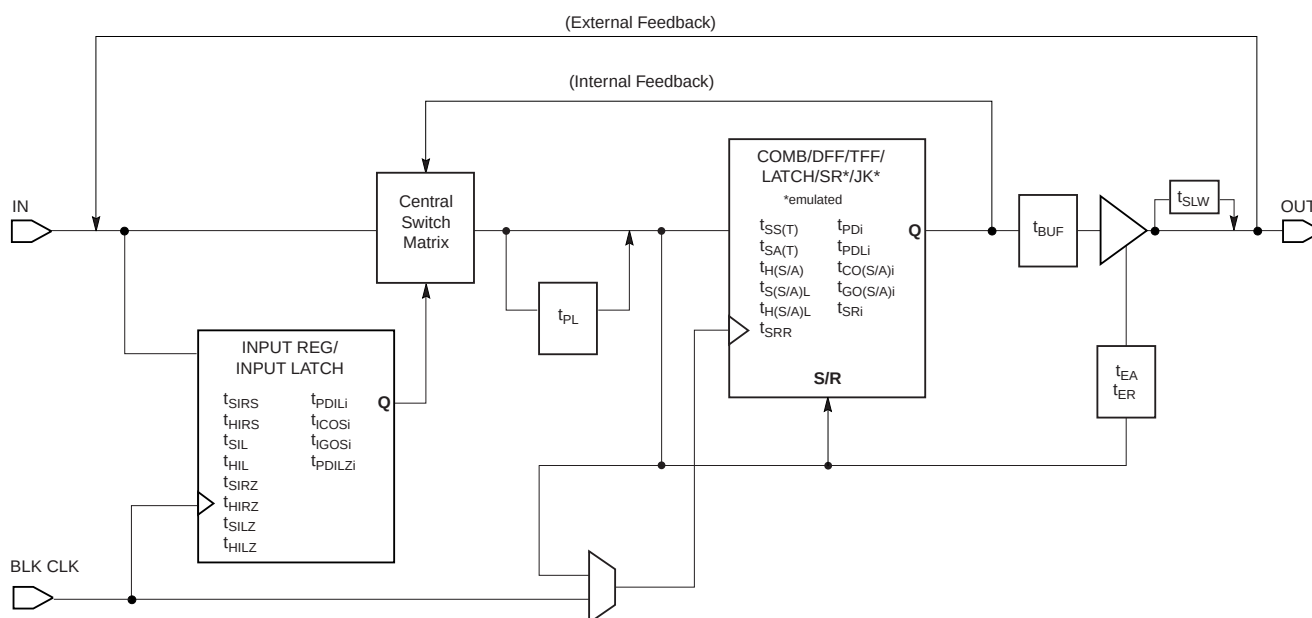
17466G-003

Figure 13. ispMACH 4A with 1:1 Macrocell-I/O Cell Ratio - Input Switch Matrix

ispMACH 4A TIMING MODEL

The primary focus of the ispMACH 4A timing model is to accurately represent the timing in a ispMACH 4A device, and at the same time, be easy to understand. This model accurately describes all combinatorial and registered paths through the device, making a distinction between internal feedback and external feedback. A signal uses internal feedback when it is fed back into the switch matrix or block without having to go through the output buffer. The input register specifications are also reported as internal feedback. When a signal is fed back into the switch matrix after having gone through the output buffer, it is using external feedback.

The parameter, t_{BUF} , is defined as the time it takes to go from feedback through the output buffer to the I/O pad. If a signal goes to the internal feedback rather than to the I/O pad, the parameter designator is followed by an “i”. By adding t_{BUF} to this internal parameter, the external parameter is derived. For example, $t_{PD} = t_{PDi} + t_{BUF}$. A diagram representing the modularized ispMACH 4A timing model is shown in Figure 15. Refer to the application note entitled *MACH 4 Timing and High Speed Design* for a more detailed discussion about the timing parameters.



17466G-025

Figure 15. ispMACH 4A Timing Model

SPEEDLOCKING FOR GUARANTEED FIXED TIMING

The ispMACH 4A architecture allows allocation of up to 20 product terms to an individual macrocell with the assistance of an XOR gate without incurring additional timing delays.

The design of the switch matrix and PAL blocks guarantee a fixed pin-to-pin delay that is independent of the logic required by the design. Other competitive CPLDs incur serious timing delays as product terms expand beyond their typical 4 or 5 product term limits. Speed and SpeedLocking combine to give designs easy access to the performance required in today's designs.

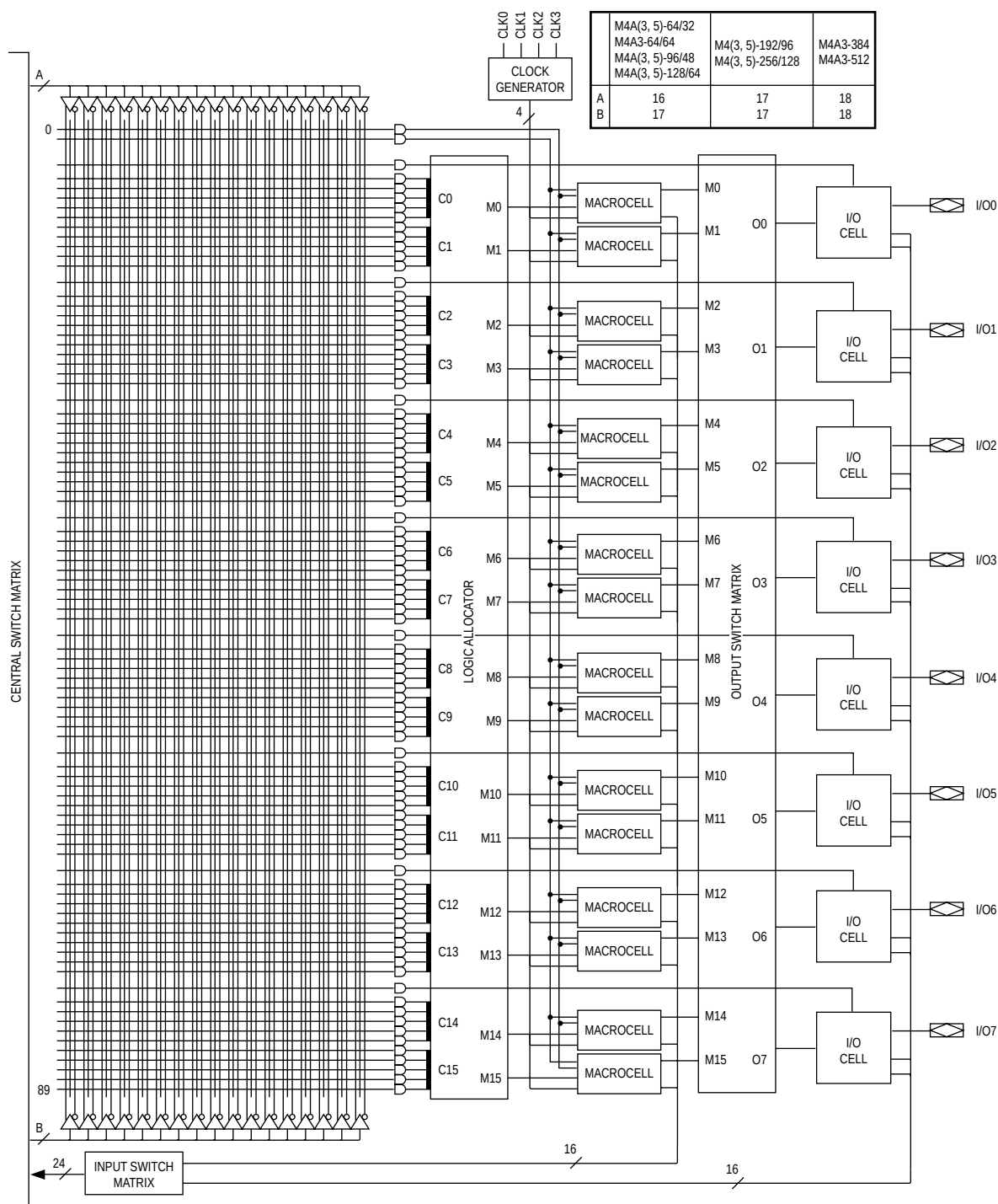
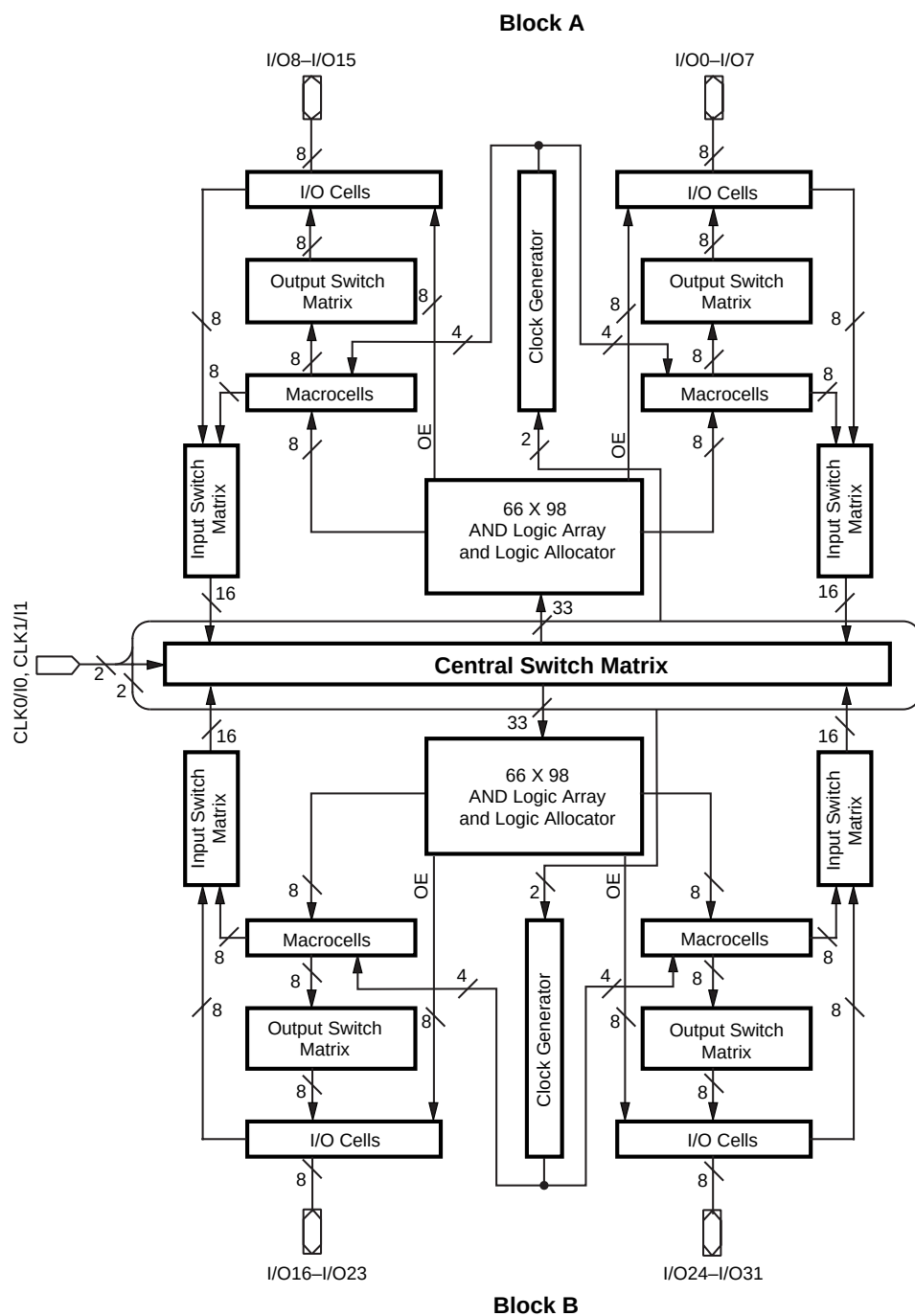


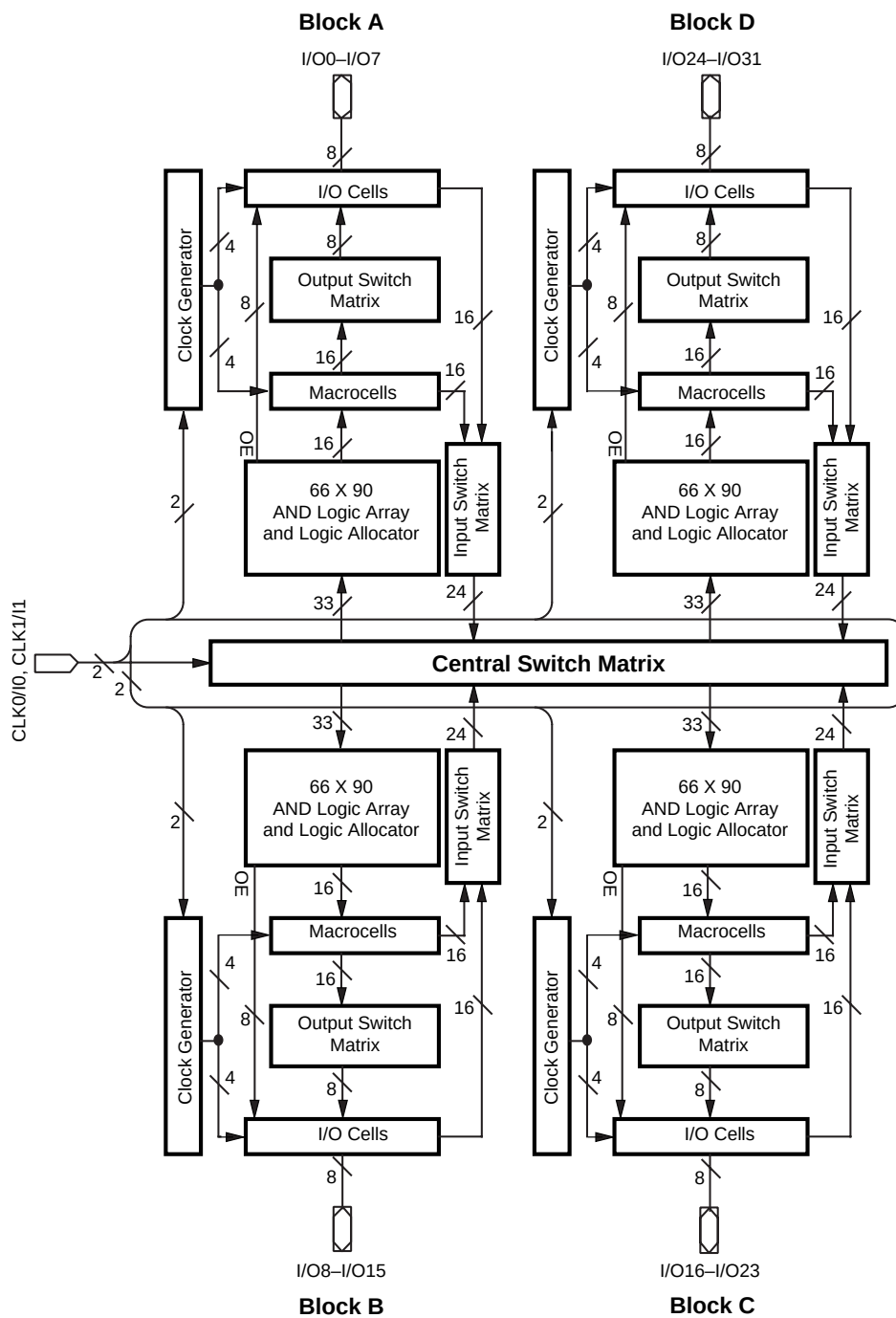
Figure 16. PAL Block for ispMACH 4A with 2:1 Macrocell - I/O Cell Ratio

BLOCK DIAGRAM – M4A(3,5)-32/32



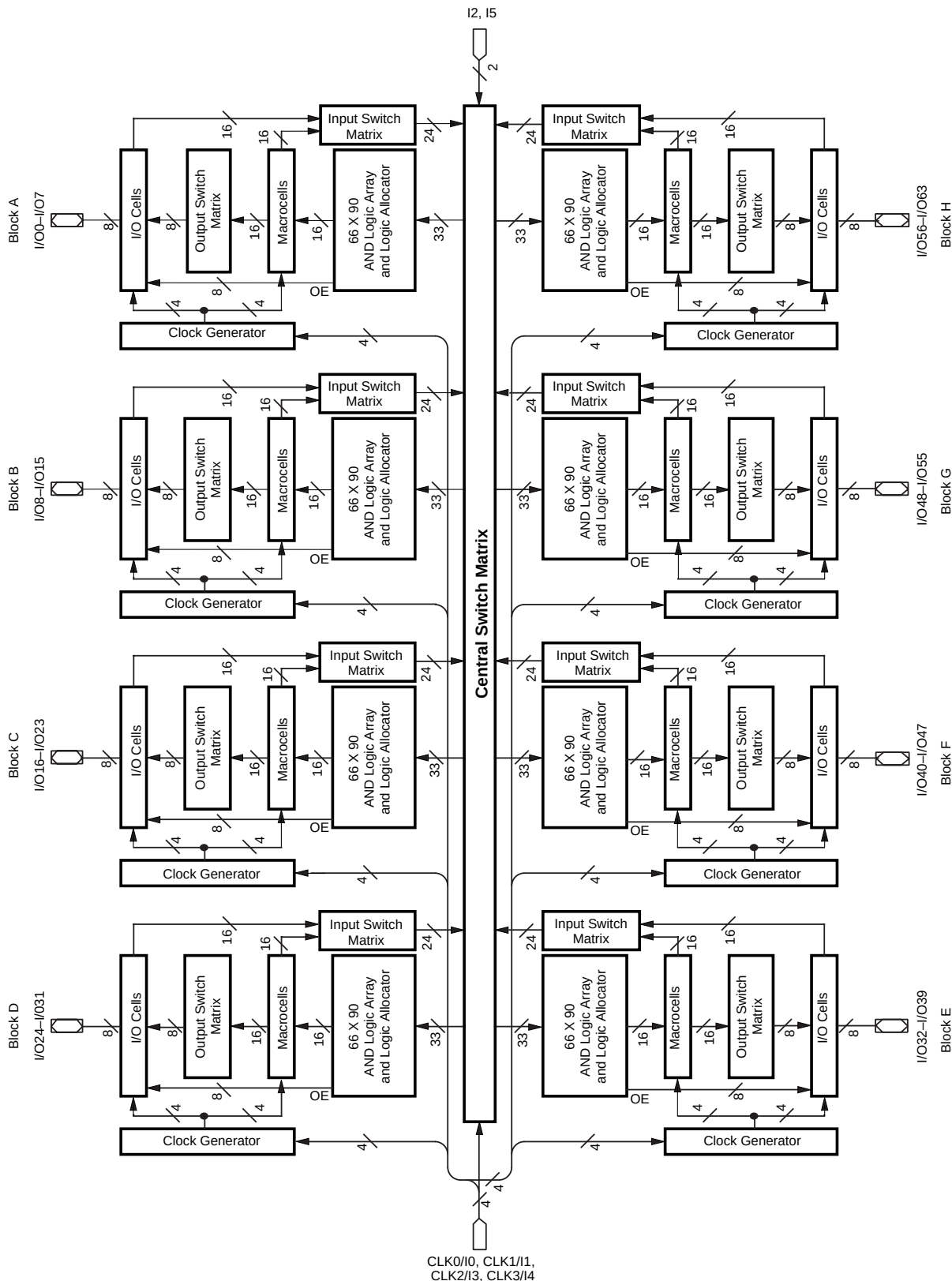
17466H-019

BLOCK DIAGRAM – M4A(3,5)-64/32



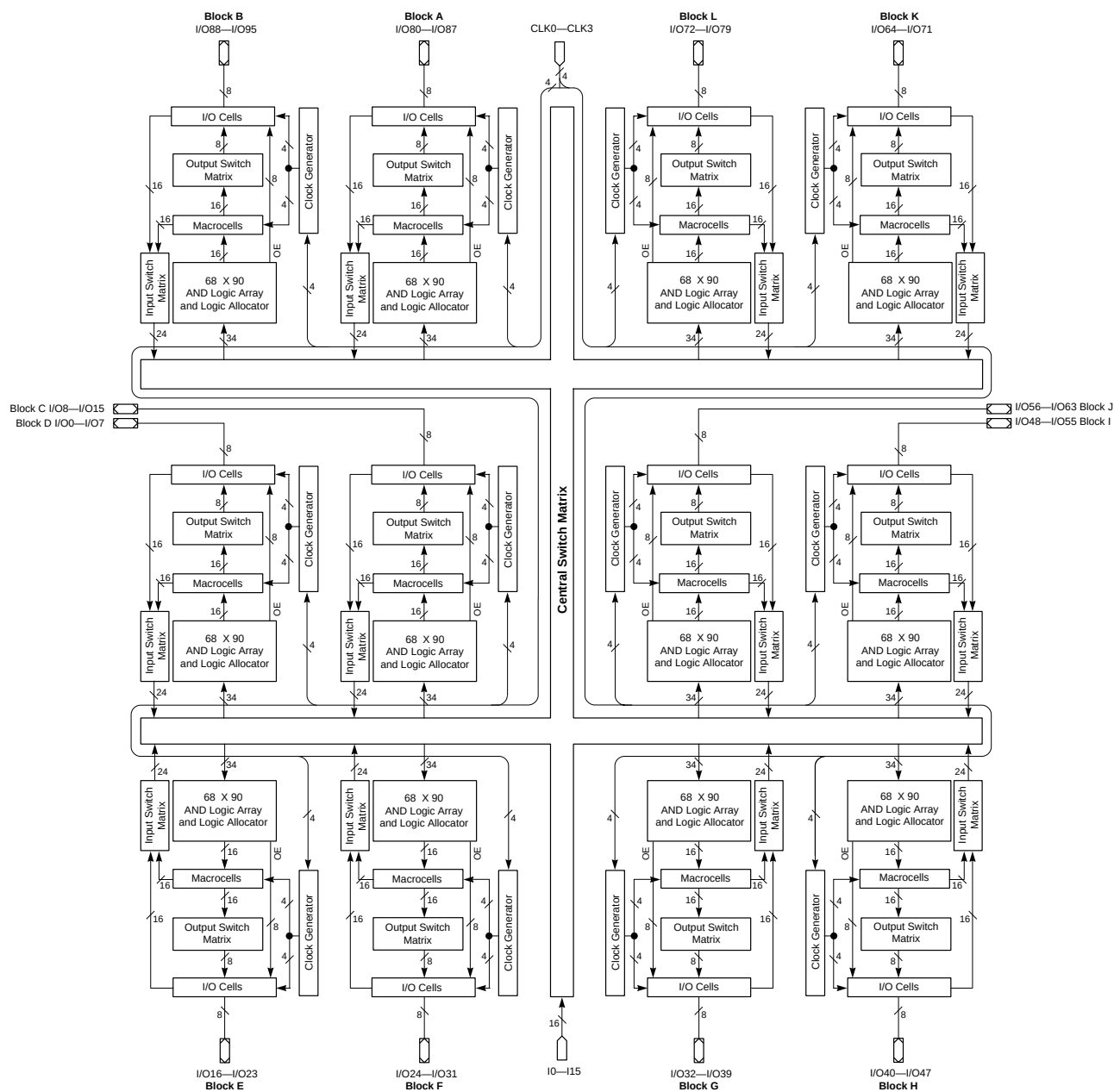
17466H-020

BLOCK DIAGRAM – M4A(3,5)-128/64



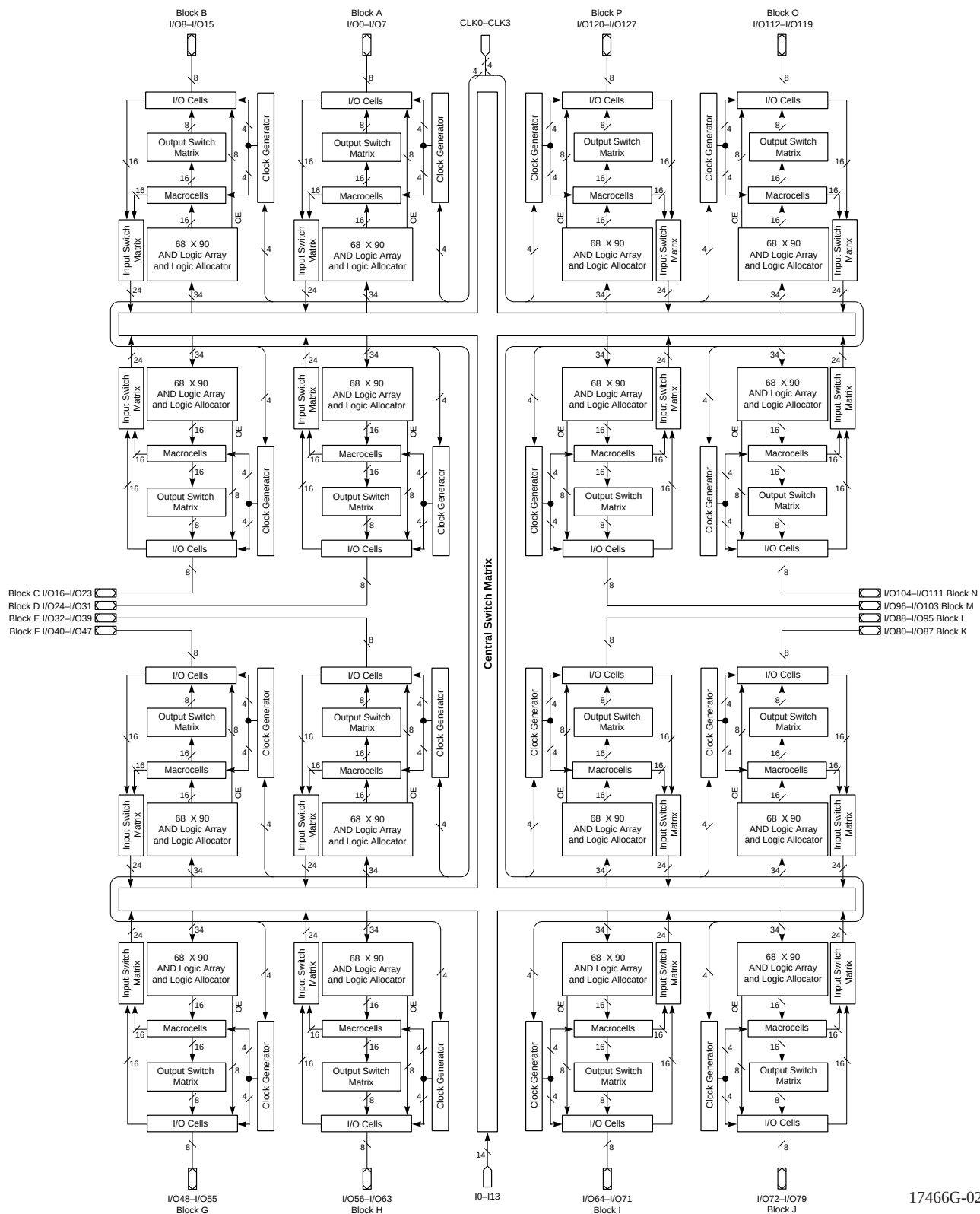
17466H-022

BLOCK DIAGRAM – M4A(3,5)-192/96



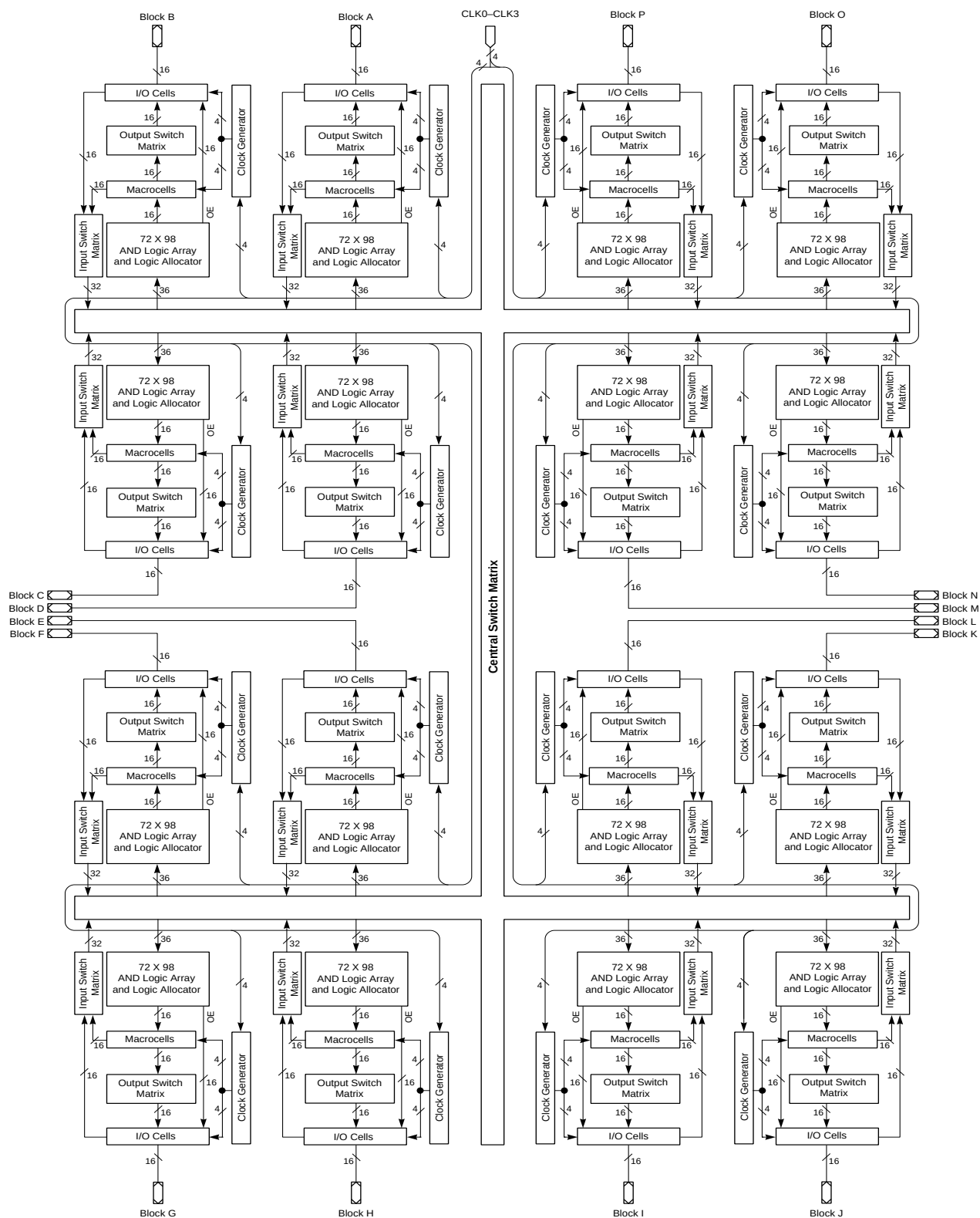
17466G-067

BLOCK DIAGRAM – M4A(3,5)-256/128



17466G-024

BLOCK DIAGRAM – M4A3-256/160, M4A3-256/192



17466G-050

ABSOLUTE MAXIMUM RATINGS

M4A5

Storage Temperature. -65°C to +150°C
 Ambient Temperature
 with Power Applied. -55°C to +100°C
 Device Junction Temperature. +130°C
 Supply Voltage
 with Respect to Ground -0.5 V to +7.0 V
 DC Input Voltage -0.5 V to $V_{CC} + 0.5$ V
 Static Discharge Voltage 2000 V
 Latchup Current ($T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$) 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)
 Operating in Free Air. 0°C to $+70^\circ\text{C}$
 Supply Voltage (V_{CC})
 with Respect to Ground. +4.75 V to +5.25 V

Industrial (I) Devices

Ambient Temperature (T_A)
 Operating in Free Air. -40°C to $+85^\circ\text{C}$
 Supply Voltage (V_{CC})
 with Respect to Ground. +4.50 V to +5.5 V
Operating ranges define those limits between which the functionality of the device is guaranteed.

5-V DC CHARACTERISTICS OVER OPERATING RANGES

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	$I_{OH} = -3.2$ mA, $V_{CC} = \text{Min}$, $V_{IN} = V_{IH}$ or V_{IL}	2.4			V
		$I_{OH} = -100$ μA , $V_{CC} = \text{Max}$, $V_{IN} = V_{IH}$ or V_{IL}		3.3	3.6	V
V_{OL}	Output LOW Voltage	$I_{OL} = 24$ mA, $V_{CC} = \text{Min}$, $V_{IN} = V_{IH}$ or V_{IL} (Note 1)			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 2)	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 2)			0.8	V
I_{IH}	Input HIGH Leakage Current	$V_{IN} = 5.25$ V, $V_{CC} = \text{Max}$ (Note 3)			10	μA
I_{IL}	Input LOW Leakage Current	$V_{IN} = 0$ V, $V_{CC} = \text{Max}$ (Note 3)			-10	μA
I_{OZH}	Off-State Output Leakage Current HIGH	$V_{OUT} = 5.25$ V, $V_{CC} = \text{Max}$, $V_{IN} = V_{IH}$ or V_{IL} (Note 3)			10	μA
I_{OZL}	Off-State Output Leakage Current LOW	$V_{OUT} = 0$ V, $V_{CC} = \text{Max}$, $V_{IN} = V_{IH}$ or V_{IL} (Note 3)			-10	μA
I_{SC}	Output Short-Circuit Current	$V_{OUT} = 0.5$ V, $V_{CC} = \text{Max}$ (Note 4)	-30		-160	mA

Notes:

1. Total I_{OL} for one PAL block should not exceed 64 mA.
2. These are absolute values with respect to device ground, and all overshoots due to system or tester noise are included.
3. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
4. Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
 $V_{OUT} = 0.5$ V has been chosen to avoid test problems caused by tester ground degradation.

ispMACH 4A TIMING PARAMETERS OVER OPERATING RANGES¹

		-5		-55		-6		-65		-7		-10		-12		-14		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Combinatorial Delay:																		
t _{PDi}	Internal combinatorial propagation delay		3.5		4.0		4.3		4.5		5.0		7.0		9.0		11.0	ns
t _{PD}	Combinatorial propagation delay		5.0		5.5		6.0		6.5		7.5		10.0		12.0		14.0	ns
Registered Delays:																		
t _{SS}	Synchronous clock setup time, D-type register	3.0		3.5		3.5		3.5		5.0		5.5		7.0		10.0		ns
t _{SST}	Synchronous clock setup time, T-type register	4.0		4.0		4.0		4.0		6.0		6.5		8.0		11.0		ns
t _{SA}	Asynchronous clock setup time, D-type register	2.5		2.5		2.5		3.0		3.5		4.0		5.0		8.0		ns
t _{SAT}	Asynchronous clock setup time, T-type register	3.0		3.0		3.0		3.5		4.5		5.0		6.0		9.0		ns
t _{HS}	Synchronous clock hold time	0.0		0.0		0.0		0.0		0.0		0.0		0.0		0.0		ns
t _{HA}	Asynchronous clock hold time	2.5		2.5		2.5		3.0		3.5		4.0		5.0		8.0		ns
t _{COsi}	Synchronous clock to internal output		2.5		2.5		2.8		3.0		3.0		3.0		3.5		3.5	ns
t _{COS}	Synchronous clock to output		4.0		4.0		4.5		5.0		5.5		6.0		6.5		6.5	ns
t _{COAi}	Asynchronous clock to internal output		5.0		5.0		5.0		5.0		6.0		8.0		10.0		12.0	ns
t _{COA}	Asynchronous clock to output		6.5		6.5		6.8		7.0		8.5		11.0		13.0		15.0	ns
Latched Delays:																		
t _{SSL}	Synchronous latch setup time	4.0		4.0		4.0		4.5		6.0		7.0		8.0		10.0		ns
t _{SAL}	Asynchronous latch setup time	3.0		3.0		3.5		3.5		4.0		4.0		5.0		8.0		ns
t _{HSL}	Synchronous latch hold time	0.0		0.0		0.0		0.0		0.0		0.0		0.0		0.0		ns
t _{HAL}	Asynchronous latch hold time	3.0		3.0		3.5		3.5		4.0		4.0		5.0		8.0		ns
t _{PDLi}	Transparent latch to internal output		5.5		5.5		5.8		6.0		7.5		9.0		11.0		12.0	ns
t _{PDL}	Propagation delay through transparent latch to output		7.0		7.0		7.5		8.0		10.0		12.0		14.0		15.0	ns
t _{GOSi}	Synchronous gate to internal output		3.0		3.0		3.0		3.0		3.5		4.5		7.0		8.0	ns
t _{GOS}	Synchronous gate to output		4.5		4.5		4.8		5.0		6.0		7.5		10.0		11.0	ns
t _{GOAi}	Asynchronous gate to internal output		6.0		6.0		6.0		6.0		8.5		10.0		13.0		15.0	ns
t _{GOA}	Asynchronous gate to output		7.5		7.5		7.8		8.0		11.0		13.0		16.0		18.0	ns
Input Register Delays:																		
t _{SIRS}	Input register setup time	1.5		1.5		2.0		2.0		2.0		2.0		2.0		2.0		ns
t _{HIRS}	Input register hold time	2.5		2.5		3.0		3.0		3.0		3.0		3.0		4.0		ns
t _{ICOSi}	Input register clock to internal feedback		3.0		3.0		3.0		3.0		3.5		4.5		6.0		6.0	ns
Input Latch Delays:																		
t _{SIL}	Input latch setup time	1.5		1.5		1.5		2.0		2.0		2.0		2.0		2.0		ns
t _{HIL}	Input latch hold time	2.5		2.5		2.5		3.0		3.0		3.0		3.0		4.0		ns
t _{IGOSi}	Input latch gate to internal feedback		3.5		3.5		3.8		4.0		4.0		4.0		4.0		5.0	ns
t _{PDILi}	Transparent input latch to internal feedback		1.5		1.5		1.5		1.5		2.0		2.0		2.0		2.0	ns

100-BALL caBGA CONNECTION DIAGRAM (M4A3-128/64)

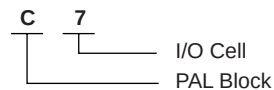
Bottom View

100-Ball caBGA

	10	9	8	7	6	5	4	3	2	1	
A	GND	I/O63 H7	I/O60 H4	I/O57 H1	GND	GND	I/O1 A1	I/O4 A4	I/O7 A7	GND	A
B	TRST	GND	I/O61 H5	I5	VCC	I/O0 A0	I/O6 A6	GND	TDI	I/O15 B7	B
C	I/O53 G5	TDO	I/O62 H6	I/O58 H2	I/O56 H0	I/O2 A2	GND	I/O14 B6	I/O13 B5	I/O12 B4	C
D	I/O50 G2	I/O55 G7	GND	I/O59 H3	I/O3 A3	I/O5 A5	I/O11 B3	I/O10 B2	CLK0/I0	I/O9 B1	D
E	CLK3/I4	I/O49 G1	I/O51 G3	I/O54 G6	VCC	I/O16 C0	I/O20 C4	I/O8 B0	VCC	GND	E
F	GND	VCC	I/O40 F0	I/O52 G4	I/O48 G0	VCC	I/O22 C6	I/O19 C3	I/O17 C1	CLK1/I1	F
G	I/O41 F1	CLK2/I3	I/O42 F2	I/O43 F3	I/O37 E5	I/O35 E3	I/O27 D3	GND	I/O23 C7	I/O18 C2	G
H	I/O44 F4	I/O45 F5	I/O46 F6	GND	I/O34 E2	I/O24 D0	I/O26 D2	I/O30 D6	TCK	I/O21 C5	H
J	I/O47 F7	ENABLE	GND	I/O38 E6	I/O32 E0	VCC	I2	I/O29 D5	GND	TMS	J
K	GND	I/O39 E7	I/O36 E4	I/O33 E1	GND	GND	I/O25 D1	I/O28 D4	I/O31 D7	GND	K
	10	9	8	7	6	5	4	3	2	1	

PIN DESIGNATIONS

CLK = Clock
 GND = Ground
 I = Input
 I/O = Input/Output
 N/C = No Connect
 VCC = Supply Voltage
 TDI = Test Data In
 TCK = Test Clock
 TMS = Test Mode Select
 TDO = Test Data Out
 TRST = Test Reset
 ENABLE = Program



17466G-100cabga

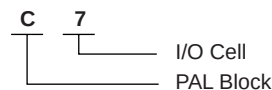
144-BALL FPBGA CONNECTION DIAGRAM (M4A3-192/96)

Bottom View

144-Ball fpBGA													
	12	11	10	9	8	7	6	5	4	3	2	1	
A	GND	I/O72 L7	I/O76 L3	I13	GBCLK3	I0	I/O82 A2	I/O86 A6	I/O88 B0	I/O93 B5	I/O95 B7	GND	A
B	GND	I/O73 L6	I/O77 L2	I/O79 L0	VCC	I1	I/O83 A3	I/O87 A7	I/O90 B2	I/O94 B6	I/O0 D7	TDI	B
C	GND	TD0	I/O74 L5	I14	GND	I/O80 A0	I/O84 A4	GND	I/O92 B4	I/O1 D6	I/O4 D3	I/O3 D4	C
D	I/O67 K4	I/O69 K2	I/O71 K0	I/O75 L4	GBCLK0	I/O81 A1	VCC	I/O91 B3	I/O2 D5	I2	I/O6 D1	I/O7 D0	D
E	I12	I/O64 K7	I/O66 K5	I/O70 K1	I/O78 L1	I/O85 A5	I/O89 B1	I/O5 D2	I/O8 C7	I4	GND	VCC	E
F	I10	I11	GND	I/O65 K6	I/O68 K3	I15	I3	GND	I/O12 C3	I/O11 C4	I/O10 C5	I/O9 C6	F
G	I/O60 J3	I/O61 J2	I/O62 J1	I/O63 J0	VCC	GND	I7	I/O20 E3	I/O17 E6	I/O15 C0	I/O14 C1	I/O13 C2	G
H	I/O56 J7	I/O57 J6	I/O58 J5	I/O59 J4	I/O53 I2	I/O41 H1	I/O37 G5	I/O30 F1	I/O22 E1	I/O18 E5	I/O16 E7	VCC	H
J	I/O55 I0	I/O54 I1	VCC	I/O50 I5	I/O43 H3	VCC	I/O33 G1	GBCLK2	I/O27 F4	I/O23 E0	I/O21 E2	I/O19 E4	J
K	I/O51 I4	I/O52 I3	I/O49 I6	I/O44 H4	GND	I/O36 G4	I/O32 G0	VCC	I6	I/O26 F5	TCK	TMS	K
L	GND	I/O48 I7	I/O46 H6	I/O42 H2	I/O39 G7	I/O35 G3	I9	GND	I/O31 F0	I/O29 F2	I/O25 F6	GND	L
M	GND	I/O47 H7	I/O45 H5	I/O40 H0	I/O38 G6	I/O34 G2	I8	GBCLK1	I5	I/O28 F3	I/O24 F7	GND	M
	12	11	10	9	8	7	6	5	4	3	2	1	

PIN DESIGNATIONS

CLK = Clock
 GND = Ground
 I = Input
 I/O = Input/Output
 N/C = No Connect
 VCC = Supply Voltage
 TDI = Test Data In
 TCK = Test Clock
 TMS = Test Mode Select
 TD0 = Test Data Out

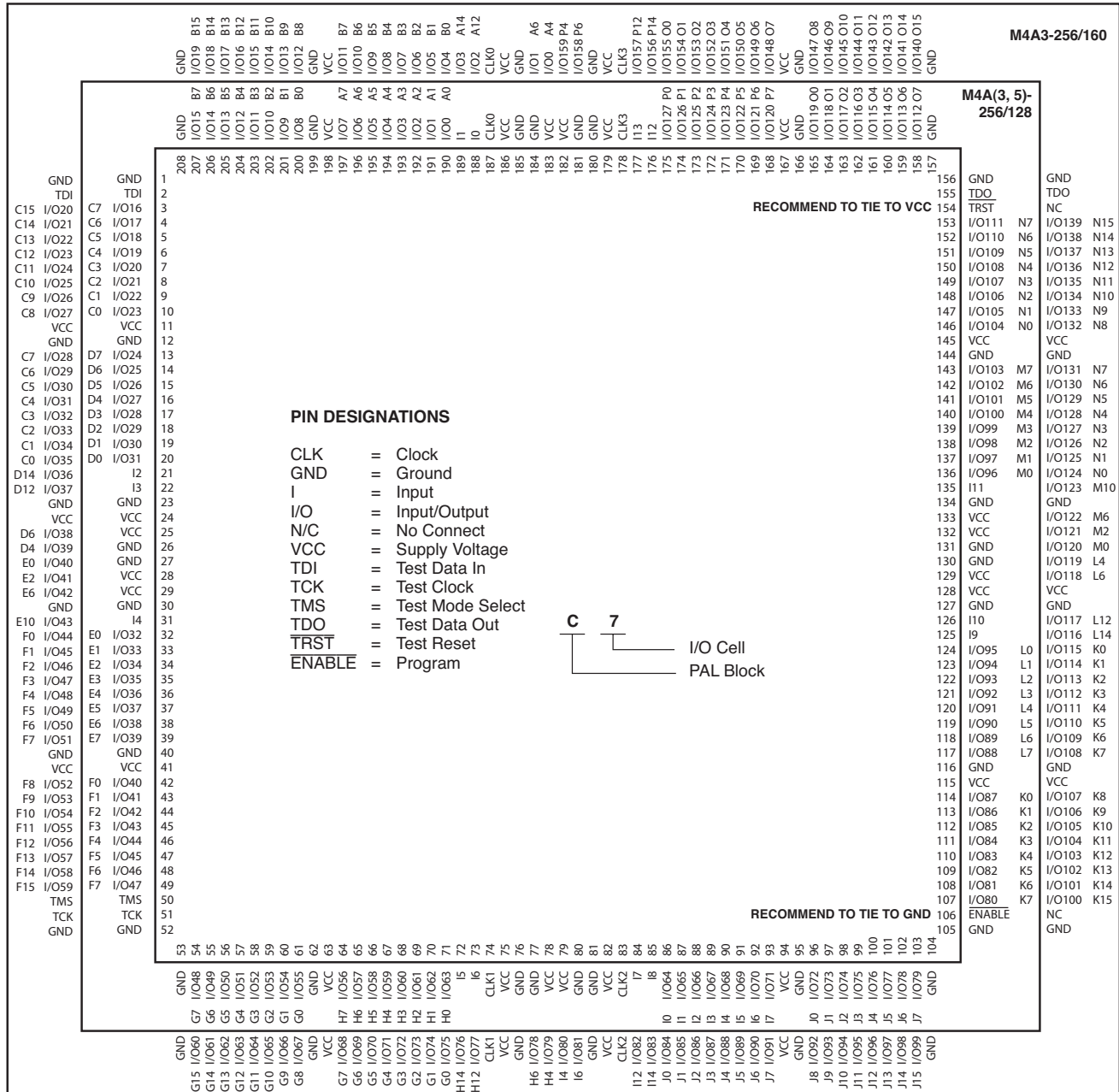


m4a3.192.96_144bga

208-PIN PQFP CONNECTION DIAGRAM (M4A(3,5)-256/128 AND M4A3-256/160)

Top View

208-Pin PQFP



17466G-044

256-BALL fpBGA CONNECTION DIAGRAM (M4A3-384/192)

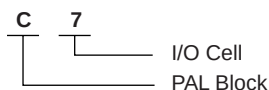
Bottom View

256-Ball fpBGA

	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	I/O175 FX7	I/O181 GX5	I/O180 GX4	I/O177 GX1	I/O166 EX6	I/O164 EX4	I/O191 HX7	I/O186 HX2	I/O1 A1	I/O3 A3	CLK0	I/O25 D1	I/O29 D5	I/O31 D7	I/O10 B2	I/O12 B4	A
B	I/O173 FX5	I/O174 FX6	I/O182 GX6	I/O179 GX3	I/O167 EX7	I/O165 EX5	I/O160 EX0	I/O187 HX3	I/O0 A0	I/O5 A5	I/O7 A7	I/O26 D2	I/O8 B0	I/O11 B3	I/O13 B5	N/C	B
C	I/O171 FX3	I/O172 FX4	N/C	I/O183 GX7	I/O178 GX2	I/O162 EX2	I/O163 EX3	I/O189 HX5	I/O184 HX0	I/O6 A6	I/O28 D4	I/O30 D6	I/O15 B7	I/O14 B6	TDI	I/O23 C7	C
D	I/O150 CX6	I/O151 CX7	TDO	GND	GND	VCC	GND	VCC	GND	GND	VCC	GND	VCC	I/O9 B1	I/O22 C6	I/O21 C5	D
E	I/O148 CX4	N/C	I/O170 FX2	VCC	I/O168 FX0	169 FX1	I/O190 HX6	CLK3	I/O188 HX4	I/O2 A2	I/O24 D0	N/C	GND	I/O20 C4	I/O19 C3	I/O47 F7	E
F	I/O144 CX0	I/O149 CX5	I/O147 CX3	GND	I/O146 CX2	I/O145 CX1	I/O176 GX0	I/O161 EX1	I/O185 HX1	I/O4 A4	I/O27 D3	I/O18 C2	VCC	I/O16 C0	I/O46 F6	I/O45 F5	F
G	I/O155 DX3	I/O158 DX6	I/O157 DX5	VCC	I/O156 DX4	I/O159 DX7	VCC	GND	GND	VCC	I/O17 C1	I/O44 F4	GND	I/O42 F2	I/O41 F1	I/O39 E7	G
H	I/O152 DX0	I/O154 DX2	I/O153 DX1	GND	I/O128 AX0	I/O129 AX1	GND	VCC	VCC	GND	I/O43 F3	I/O40 F0	VCC	I/O36 E4	I/O35 E3	I/O34 E2	H
J	I/O130 AX2	I/O131 AX3	I/O132 AX4	GND	I/O134 AX6	I/O133 AX5	GND	VCC	VCC	GND	I/O38 E6	I/O37 E5	GND	I/O57 H1	I/O56 H0	I/O58 H2	J
K	I/O135 AX7	I/O136 BX0	I/O137 BX1	VCC	I/O139 BX3	I/O138 BX2	VCC	GND	GND	VCC	I/O33 E1	I/O32 E0	VCC	I/O63 H7	I/O62 H6	I/O48 G0	K
L	I/O140 BX4	I/O141 BX5	I/O143 BX7	GND	I/O114 O2	I/O142 BX6	I/O98 M2	I/O91 L3	I/O67 I3	I/O69 I5	I/O60 H4	I/O59 H3	GND	I/O51 G3	I/O52 G4	I/O49 G1	L
M	I/O112 O0	I/O113 O1	I/O115 O3	GND	I/O123 P3	I/O121 P1	I/O100 M4	I/O90 L2	I/O66 I2	I/O80 K0	I/O83 K3	I/O61 H5	VCC	I/O76 J4	I/O55 G7	I/O50 G2	M
N	I/O116 O4	I/O117 O5	I/O119 O7	VCC	GND	VCC	GND	VCC	GND	GND	VCC	GND	GND	TCK	I/O72 J0	I/O53 G5	N
P	I/O118 O6	I/O109 N5	I/O110 N6	I/O111 N7	I/O124 P4	I/O122 P2	I/O101 M5	I/O89 L1	I/O93 L5	I/O94 L6	I/O71 I7	I/O84 K4	I/O87 K7	TMS	I/O73 J1	I/O54 G6	P
R	I/O108 N4	I/O107 N3	I/O104 N0	I/O127 P7	I/O120 P0	I/O102 M6	I/O99 M3	I/O96 M0	I/O92 L4	I/O64 I0	I/O68 I4	I/O81 K1	I/O85 K5	I/O79 J7	I/O75 J3	I/O74 J2	R
T	I/O106 N2	I/O105 N1	I/O126 P6	I/O125 P5	I/O103 M7	CLK2	I/O97 M1	I/O88 L0	CLK1	I/O95 L7	I/O65 I1	I/O70 I6	I/O82 K2	I/O86 K6	I/O78 J6	I/O77 J5	T
	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

PIN DESIGNATIONS

CLK = Clock
 GND = Ground
 I = Input
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 TDO = Test Data Out



m4a3.384.192_256bga

ispMACH 4A PRODUCT ORDERING INFORMATION

ispMACH 4A Devices Commercial and Industrial - 3.3V and 5V

Lattice programmable logic products are available with several ordering options. The order number (Valid Combination) is formed by a combination of:

M4A3- 256 / 128 -7 Y C		48	
FAMILY TYPE		= 48-pin TQFP for M4A3-32/32 or M4A3-64/32 M4A5-32/32 or M4A5-64/32	
M4A3- = ispMACH 4A Family Low Voltage Advanced Feature (3.3-V V_{CC})		OPERATING CONDITIONS	
M4A5- = ispMACH 4A Family Advanced Feature (5-V V_{CC})		C = Commercial (0°C to +70°C)	
MACROCELL DENSITY		I = Industrial (-40°C to +85°C)	
32 = 32 Macrocells 192 = 192 Macrocells		PACKAGE TYPE	
64 = 64 Macrocells 256 = 256 Macrocells		SA = Ball Grid Array (BGA)	
96 = 96 Macrocells 384 = 384 Macrocells		J = Plastic Leaded Chip Carrier (PLCC)	
128 = 128 Macrocells 512 = 512 Macrocells		JN = Lead-free Plastic Leaded Chip Carrier (PLCC)	
I/Os		V = Thin Quad Flat Pack (TQFP)	
/32 = 32 I/Os in 44-pin PLCC, 44-pin TQFP or 48-pin TQFP		VN = Lead-free Thin Quad Flat Pack (TQFP)	
/48 = 48 I/Os in 100-pin TQFP		Y = Plastic Quad Flat Pack (PQFP)	
/64 = 64 I/Os in 100-pin TQFP, 100-pin PQFP, or 100-ball caBGA		YN = Lead-free Plastic Quad Flat Pack (PQFP)	
/96 = 96 I/Os in 144-pin TQFP or 144-ball fpBGA		FA = Fine-pitch Ball Grid Array (fpBGA)	
/128 = 128 I/Os in 208-pin PQFP, 256-ball BGA or 256-ball fpBGA		FAN = Lead-free Fine-pitch Ball Grid Array (fpBGA)	
/160 = 160 I/Os in 208-pin PQFP		CA = Chip-array Ball Grid Array (caBGA)	
/192 = 192 I/Os in 256-ball BGA or 256-ball fpBGA		SPEED	
/256 = 256 I/Os in 388-ball fpBGA		-5 = 5.0 ns t_{PD}	
		-55 = 5.5 ns t_{PD}	
		-6 = 6.0 ns t_{PD}	
		-65 = 6.5 ns t_{PD}	
		-7 = 7.5 ns t_{PD}	
		-10 = 10 ns t_{PD}	
		-12 = 12 ns t_{PD}	
		-14 = 14 ns t_{PD}	

*Package obsolete, contact factory.

Conventional Packaging

3.3V Commercial Combinations			3.3V Industrial Combinations		
M4A3-32/32	-5, -7, -10	JC, VC, VC48	M4A3-32/32	-7, -10, -12	JI, VI, VI48
M4A3-64/32	-55, -7, -10	JC, VC, VC48	M4A3-64/32		JI, VI, VI48
M4A3-64/64		VC	M4A3-64/64		VI
M4A3-96/48		VC	M4A3-96/48		VI
M4A3-128/64		YC, VC, CAC	M4A3-128/64		YI, VI, CAI
M4A3-192/96	-6, -7, -10	VC, FAC	M4A3-192/96		VI, FAI
M4A3-256/128	-55, -65 ¹ , -7, -10	YC, FAC, SAC	M4A3-256/128	-10, -12	YI, FAI, SAI
M4A3-256/160	-7, -10	YC	M4A3-256/160		YI
M4A3-256/192		FAC	M4A3-256/192	-10, -12, -14	FAI
M4A3-384/160	-65, -10, -12	YC	M4A3-384/160		YI
M4A3-384/192		SAC, FAC	M4A3-384/192		FAI
M4A3-512/160	-7, -10, -12	YC	M4A3-512/160		YI
M4A3-512/192		FAC	M4A3-512/192		FAI
M4A3-512/256		FAC	M4A3-512/256		FAI

1. Use 5.5ns for new designs.