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Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details

Product Status	Not For New Designs
Programmable Type	In System Programmable
Delay Time tpd(1) Max	10 ns
Voltage Supply - Internal	3V ~ 3.6V
Number of Logic Elements/Blocks	-
Number of Macrocells	256
Number of Gates	-
Number of I/O	160
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/m4a3-256-160-10yni

Table 1. ispMACH 4A Device Features

3.3 V Devices								
Feature	M4A3-32	M4A3-64	M4A3-96	M4A3-128	M4A3-192	M4A3-256	M4A3-384	M4A3-512
Macrocells	32	64	96	128	192	256	384	512
User I/O options	32	32/64	48	64	96	128/160/192	160/192	160/192/256
t_{PD} (ns)	5.0	5.5	5.5	5.5	6.0	5.5	6.5	7.5
f_{CNT} (MHz)	182	167	167	167	160	167	154	125
t_{COS} (ns)	4.0	4.0	4.0	4.0	4.5	4.0	4.5	5.5
t_{SS} (ns)	3.0	3.5	3.5	3.5	3.5	3.5	3.5	5.0
Static Power (mA)	20	25/52	40	55	85	110/150	149/155	179
JTAG Compliant	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
PCI Compliant	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes

5 V Devices						
Feature	M4A5-32	M4A5-64	M4A5-96	M4A5-128	M4A5-192	M4A5-256
Macrocells	32	64	96	128	192	256
User I/O options	32	32	48	64	96	128
t_{PD} (ns)	5.0	5.5	5.5	5.5	6.0	6.5
f_{CNT} (MHz)	182	167	167	167	160	154
t_{COS} (ns)	4.0	4.0	4.0	4.0	4.5	5.0
t_{SS} (ns)	3.0	3.5	3.5	3.5	3.5	3.5
Static Power (mA)	20	25	40	55	74	110
JTAG Compliant	Yes	Yes	Yes	Yes	Yes	Yes
PCI Compliant	Yes	Yes	Yes	Yes	Yes	Yes

GENERAL DESCRIPTION

The ispMACH™ 4A family from Lattice offers an exceptionally flexible architecture and delivers a superior Complex Programmable Logic Device (CPLD) solution of easy-to-use silicon products and software tools. The overall benefits for users are a guaranteed and predictable CPLD solution, faster time-to-market, greater flexibility and lower cost. The ispMACH 4A devices offer densities ranging from 32 to 512 macrocells with 100% utilization and 100% pin-out retention. The ispMACH 4A families offer 5-V (M4A5-xxx) and 3.3-V (M4A3-xxx) operation.

ispMACH 4A products are 5-V or 3.3-V in-system programmable through the JTAG (IEEE Std. 1149.1) interface. JTAG boundary scan testing also allows product testability on automated test equipment for device connectivity.

All ispMACH 4A family members deliver First-Time-Fit and easy system integration with pin-out retention after any design change and refit. For both 3.3-V and 5-V operation, ispMACH 4A products can deliver guaranteed fixed timing as fast as 5.0 ns t_{PD} and 182 MHz f_{CNT} through the SpeedLocking feature when using up to 20 product terms per output (Table 2).

Table 2. ispMACH 4A Speed Grades

Device	Speed Grade							
	-5	-55	-6	-65	-7	-10	-12	-14
M4A3-32 M4A5-32	C				C, I	C, I	I	
M4A3-64/32 M4A5-64/32		C			C, I	C, I	I	
M4A3-64/64		C			C, I	C, I	I	
M4A3-96 M4A5-96		C			C, I	C, I	I	
M4A3-128 M4A5-128		C			C, I	C, I	I	
M4A3-192 M4A5-192			C		C, I	C, I	I	
M4A3-256/128		C		C	C, I	C, I	I	
M4A5-256/128				C	C	C, I	I	
M4A3-256/192 M4A3-256/160					C	C, I	I	
M4A3-384				C		C, I	C, I	I
M4A3-512					C	C, I	C, I	I

Note:

1. C = Commercial, I = Industrial

Table 4. Architectural Summary of ispMACH 4A devices

	ispMACH 4A Devices	
	M4A3-64/32, M4A5-64/32 M4A3-96/48, M4A5-96/48 M4A3-128/64, M4A5-128/64 M4A3-192/96, M4A5-192/96 M4A3-256/128, M4A5-256/128 M4A3-384 M4A3-512	M4A3-32/32 M4A5-32/32 M4A3-64/64 M4A3-256/160 M4A3-256/192
Macrocell-I/O Cell Ratio	2:1	1:1
Input Switch Matrix	Yes	Yes ¹
Input Registers	Yes	No
Central Switch Matrix	Yes	Yes
Output Switch Matrix	Yes	Yes

The Macrocell-I/O cell ratio is defined as the number of macrocells versus the number of I/O cells internally in a PAL block (Table 4).

The central switch matrix takes all dedicated inputs and signals from the input switch matrices and routes them as needed to the PAL blocks. Feedback signals that return to the same PAL block still must go through the central switch matrix. This mechanism ensures that PAL blocks in ispMACH 4A devices communicate with each other with consistent, predictable delays.

The central switch matrix makes a ispMACH 4A device more advanced than simply several PAL devices on a single chip. It allows the designer to think of the device not as a collection of blocks, but as a single programmable device; the software partitions the design into PAL blocks through the central switch matrix so that the designer does not have to be concerned with the internal architecture of the device.

Each PAL block consists of:

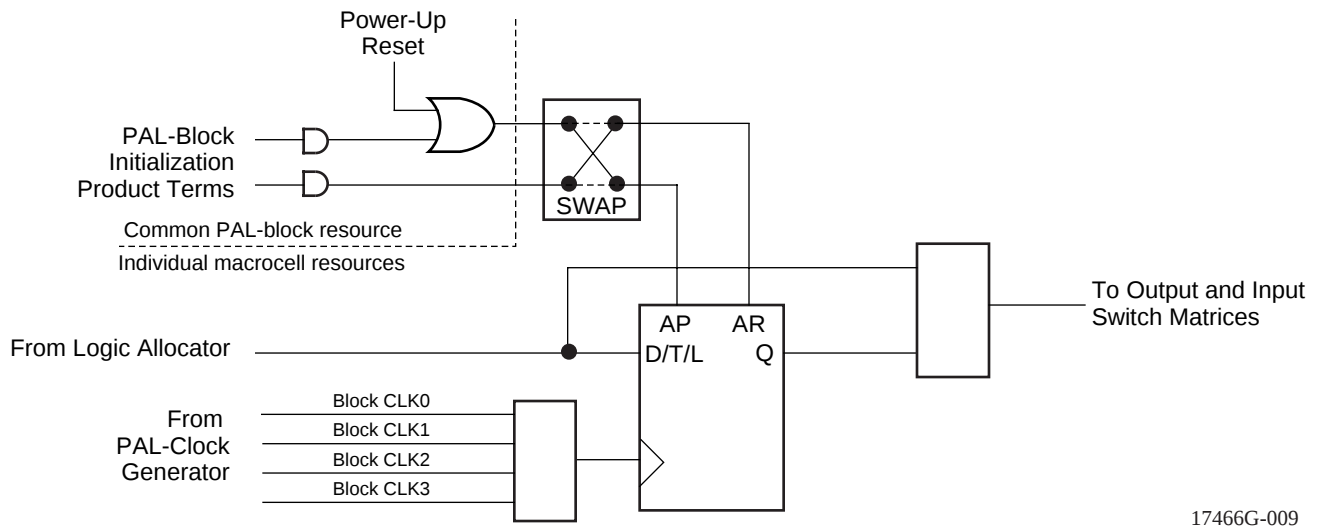
- ◆ Product-term array
- ◆ Logic allocator
- ◆ Macrocells
- ◆ Output switch matrix
- ◆ I/O cells
- ◆ Input switch matrix
- ◆ Clock generator

Notes:

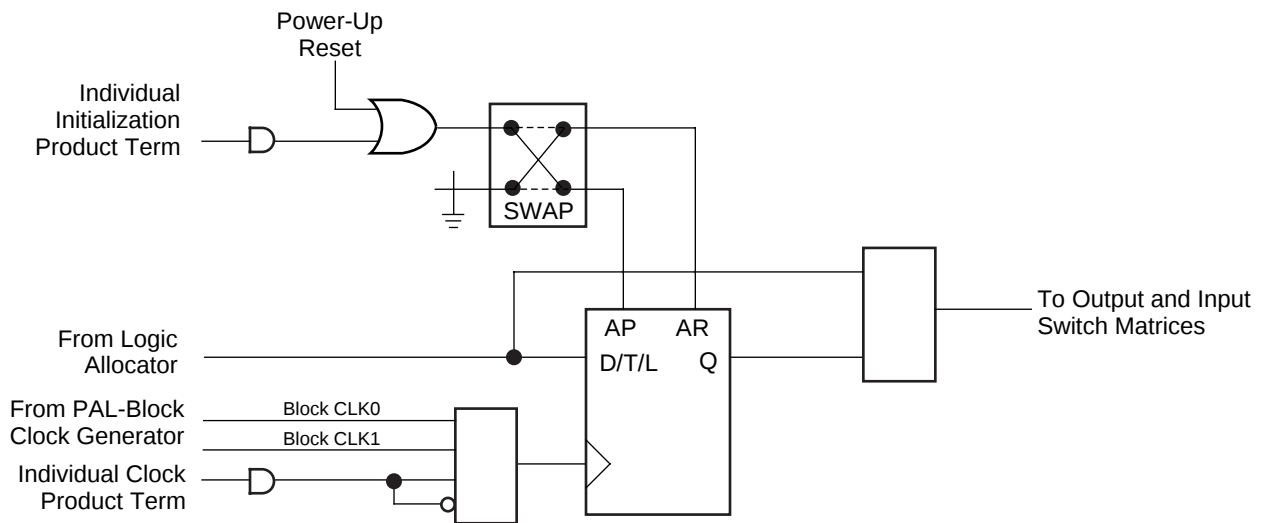
1. M4A3-64/64 internal switch matrix functionality embedded in central switch matrix.

Macrocell

The macrocell consists of a storage element, routing resources, a clock multiplexer, and initialization control. The macrocell has two fundamental modes: synchronous and asynchronous (Figure 5). The mode chosen only affects clocking and initialization in the macrocell.



a. Synchronous mode



b. Asynchronous mode

Figure 5. Macrocell

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In either mode, a combinatorial path can be used. For combinatorial logic, the synchronous mode will generally be used, since it provides more product terms in the allocator.

Table 8. Register/Latch Operation

Configuration	Input(s)	CLK/LE ¹	Q+
D-type Register	D=X	0, 1, ↓ (↑)	Q
	D=0	↑ (↓)	0
	D=1	↑ (↓)	1
T-type Register	T=X	0, 1, ↓ (↑)	Q
	T=0	↑ (↓)	Q
	T=1	↑ (↓)	$\overline{Q}$
D-type Latch	D=X	1(0)	Q
	D=0	0(1)	0
	D=1	0(1)	1

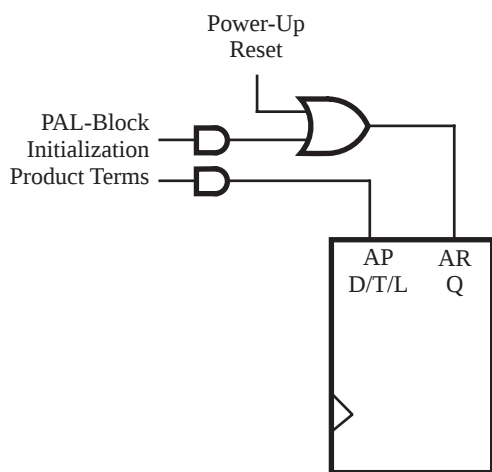
Note:

1. Polarity of CLK/LE can be programmed

Although the macrocell shows only one input to the register, the XOR gate in the logic allocator allows the D-, T-type register to emulate J-K, and S-R behavior. In this case, the available product terms are divided between J and K (or S and R). When configured as J-K, S-R, or T-type, the extra product term must be used on the XOR gate input for flip-flop emulation. In any register type, the polarity of the inputs can be programmed.

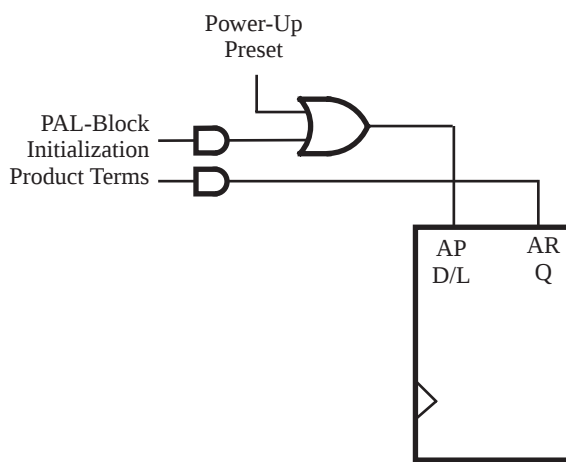
The clock input to the flip-flop can select any of the four PAL block clocks in synchronous mode, with the additional choice of either polarity of an individual product term clock in the asynchronous mode.

The initialization circuit depends on the mode. In synchronous mode (Figure 7), asynchronous reset and preset are provided, each driven by a product term common to the entire PAL block.



a. Power-up reset

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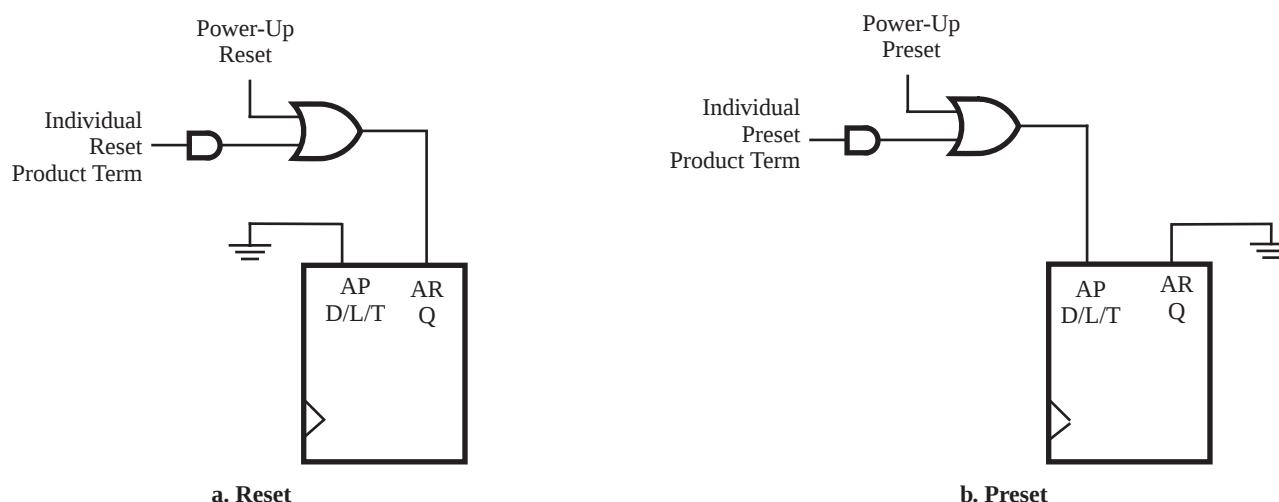


b. Power-up preset

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Figure 7. Synchronous Mode Initialization Configurations

A reset/preset swapping feature in each macrocell allows for reset and preset to be exchanged, providing flexibility. In asynchronous mode (Figure 8), a single individual product term is provided for initialization. It can be selected to control reset or preset.



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17466G-015

Figure 8. Asynchronous Mode Initialization Configurations

Note that the reset/preset swapping selection feature effects power-up reset as well. The initialization functionality of the flip-flops is illustrated in Table 9. The macrocell sends its data to the output switch matrix and the input switch matrix. The output switch matrix can route this data to an output if so desired. The input switch matrix can send the signal back to the central switch matrix as feedback.

Table 9. Asynchronous Reset/Preset Operation

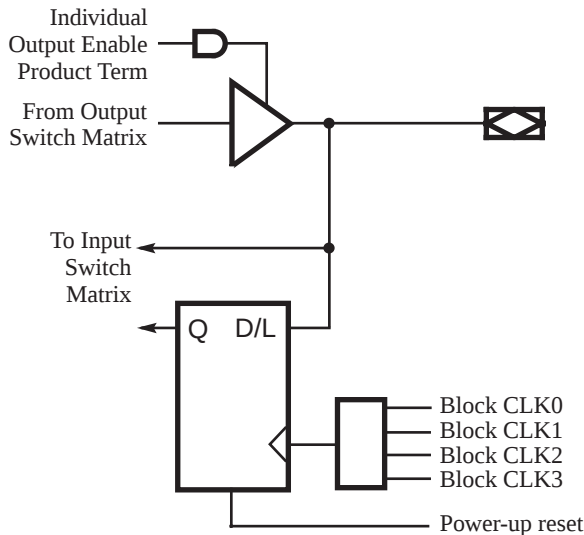
AR	AP	CLK/LE ¹	Q+
0	0	X	See Table 8
0	1	X	1
1	0	X	0
1	1	X	0

Note:

1. Transparent latch is unaffected by AR, AP

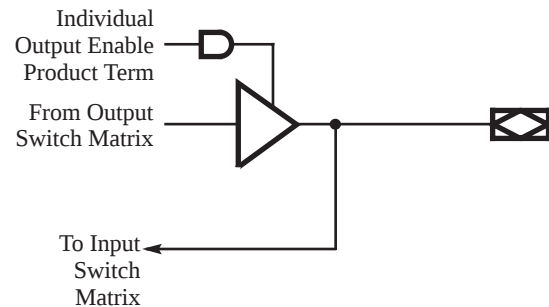
I/O Cell

The I/O cell (Figures 10 and 11) simply consists of a programmable output enable, a feedback path, and flip-flop (except ispMACH 4A devices with 1:1 macrocell-I/O cell ratio). An individual output enable product term is provided for each I/O cell. The feedback signal drives the input switch matrix.



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Figure 10. I/O Cell for ispMACH 4A Devices with 2:1 Macrocell-I/O Cell Ratio



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Figure 11. I/O Cell for ispMACH 4A Devices with 1:1 Macrocell-I/O Cell Ratio

The I/O cell (Figure 10) contains a flip-flop, which provides the capability for storing the input in a D-type register or latch. The clock can be any of the PAL block clocks. Both the direct and registered versions of the input are sent to the input switch matrix. This allows for such functions as “time-domain-multiplexed” data comparison, where the first data value is stored, and then the second data value is put on the I/O pin and compared with the previous stored value.

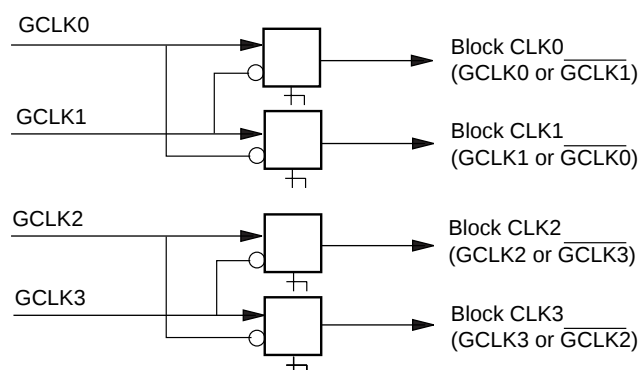
Note that the flip-flop used in the ispMACH 4A I/O cell is independent of the flip-flops in the macrocells. It powers up to a logic low.

Zero-Hold-Time Input Register

The ispMACH 4A devices have a zero-hold-time (ZHT) fuse which controls the time delay associated with loading data into all I/O cell registers and latches. When programmed, the ZHT fuse increases the data path setup delays to input storage elements, matching equivalent delays in the clock path. When the fuse is erased, the setup time to the input storage element is minimized. This feature facilitates doing worst-case designs for which data is loaded from sources which have low (or zero) minimum output propagation delays from clock edges.

PAL Block Clock Generation

Each ispMACH 4A device has four clock pins that can also be used as inputs. These pins drive a clock generator in each PAL block (Figure 14). The clock generator provides four clock signals that can be used anywhere in the PAL block. These four PAL block clock signals can consist of a large number of combinations of the true and complement edges of the global clock signals. Table 14 lists the possible combinations.



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Figure 14. PAL Block Clock Generator¹

1. M4A(3,5)-32/32 and M4A(3,5)-64/32 have only two clock pins, GCLK0 and GCLK1. GCLK2 is tied to GCLK0, and GCLK3 is tied to GCLK1.

Table 14. PAL Block Clock Combinations¹

Block CLK0	Block CLK1	Block CLK2	Block CLK3
GCLK0	GCLK1	X	X
$\overline{\text{GCLK1}}$	GCLK1	X	X
GCLK0	$\overline{\text{GCLK0}}$	X	X
$\overline{\text{GCLK1}}$	$\overline{\text{GCLK0}}$	X	X
X	X	GCLK2 (GCLK0)	GCLK3 (GCLK1)
X	X	$\overline{\text{GCLK3}}$ ($\overline{\text{GCLK1}}$)	GCLK3 (GCLK1)
X	X	GCLK2 (GCLK0)	$\overline{\text{GCLK2}}$ ($\overline{\text{GCLK0}}$)
X	X	$\overline{\text{GCLK3}}$ (GCLK1)	$\overline{\text{GCLK2}}$ ($\overline{\text{GCLK0}}$)

Note:

1. Values in parentheses are for the M4A(3,5)-32/32 and M4A(3,5)-64/32.

This feature provides high flexibility for partitioning state machines and dual-phase clocks. It also allows latches to be driven with either polarity of latch enable, and in a master-slave configuration.

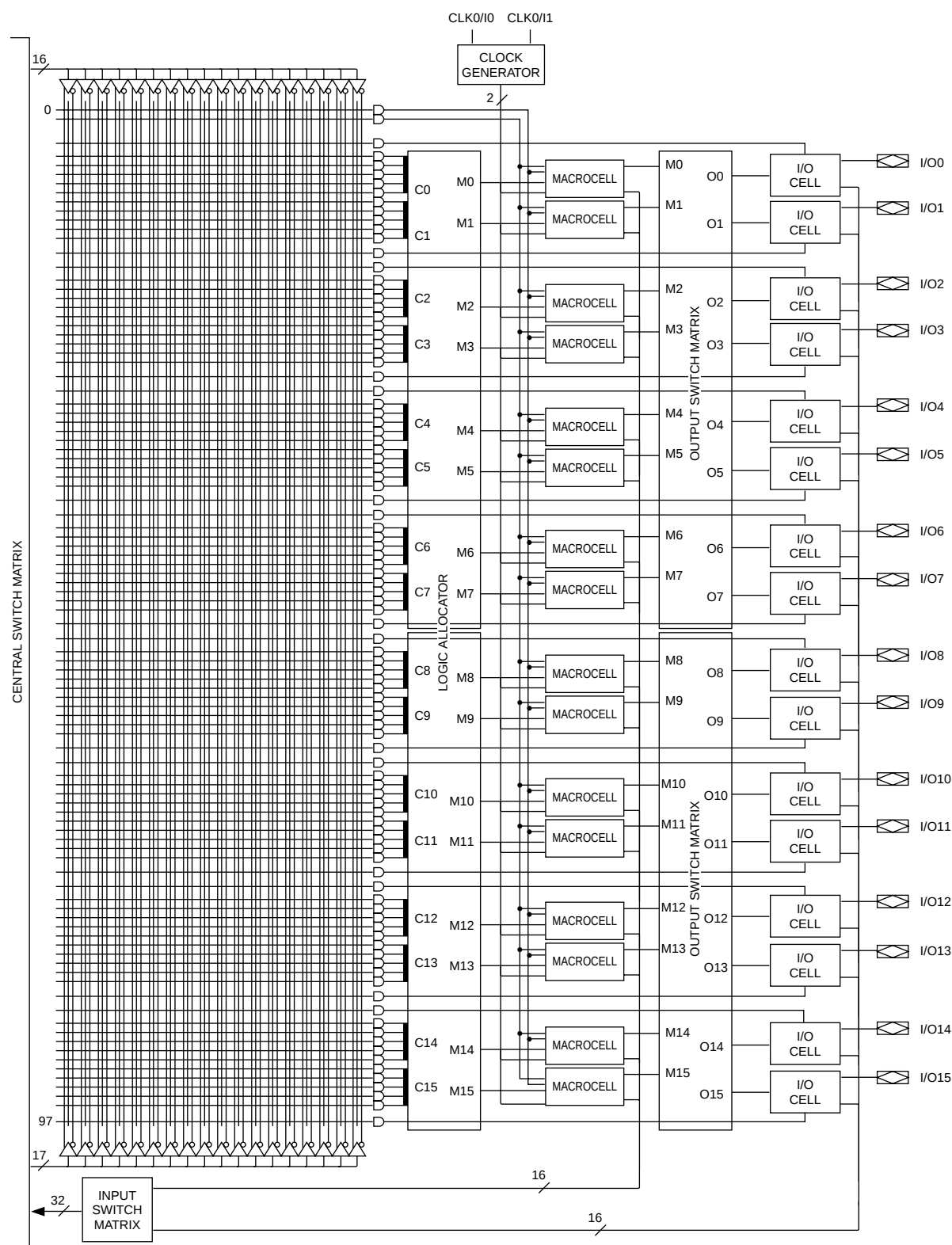
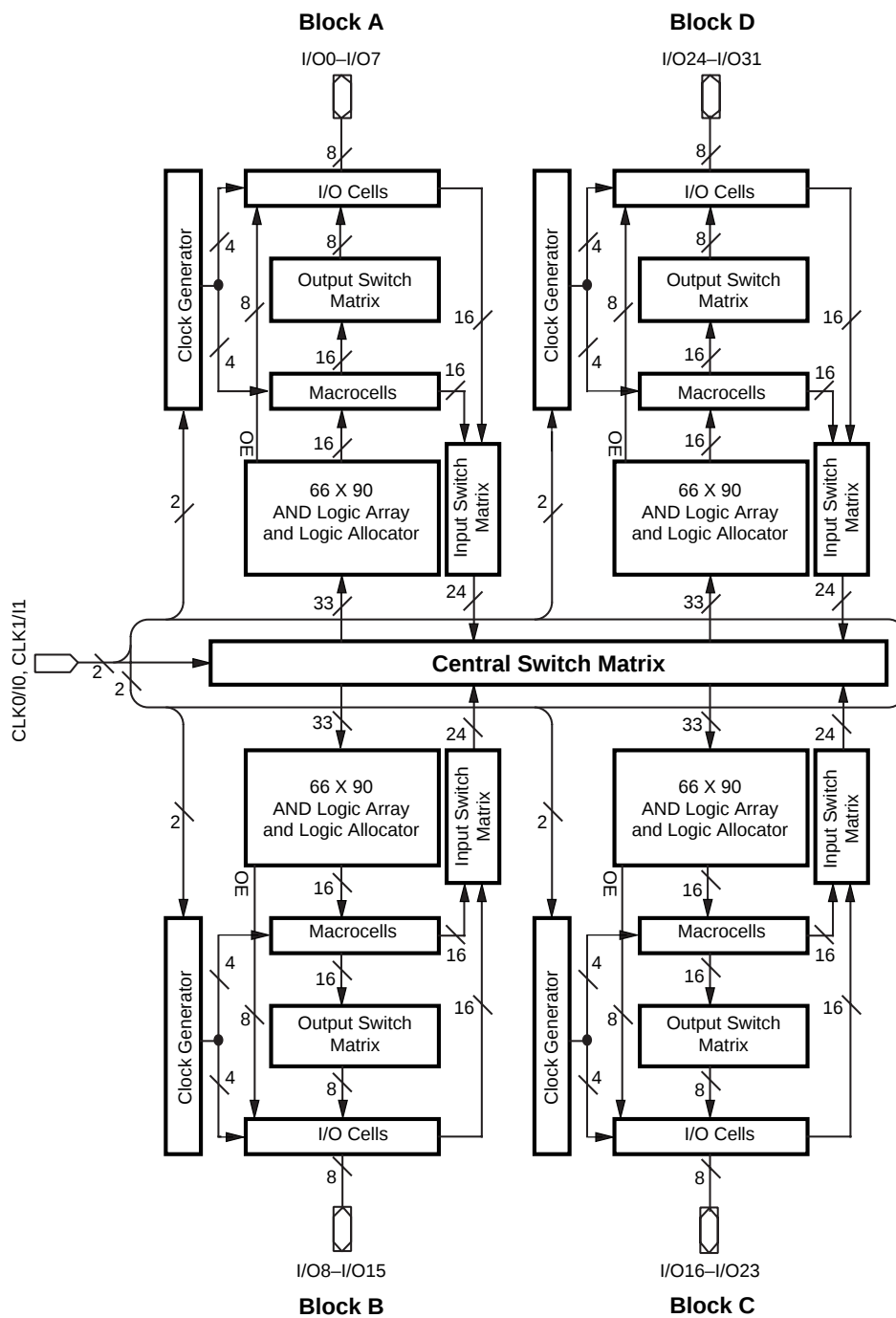


Figure 18. PAL Block for M4A (3,5)-32/32

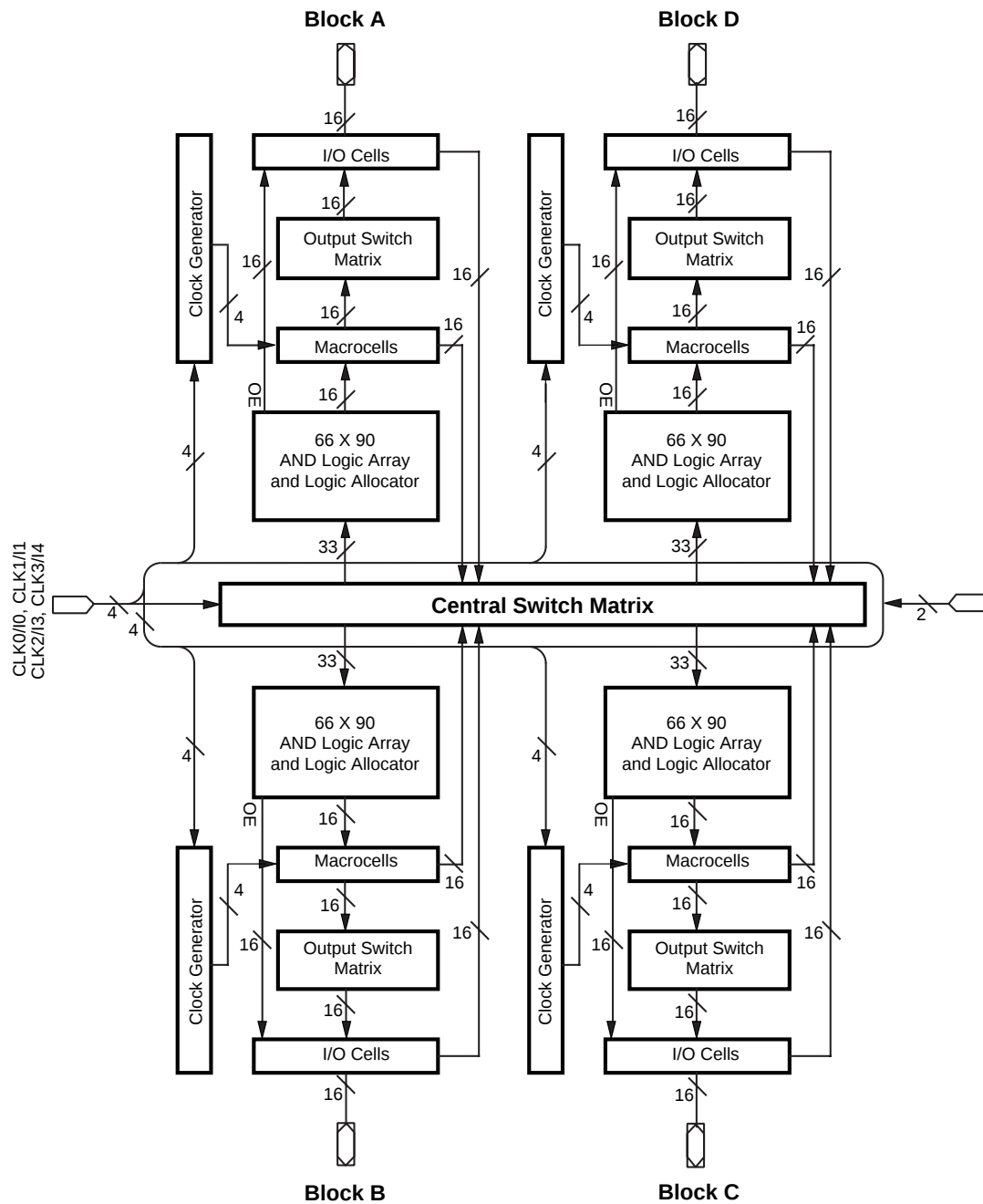
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BLOCK DIAGRAM – M4A(3,5)-64/32



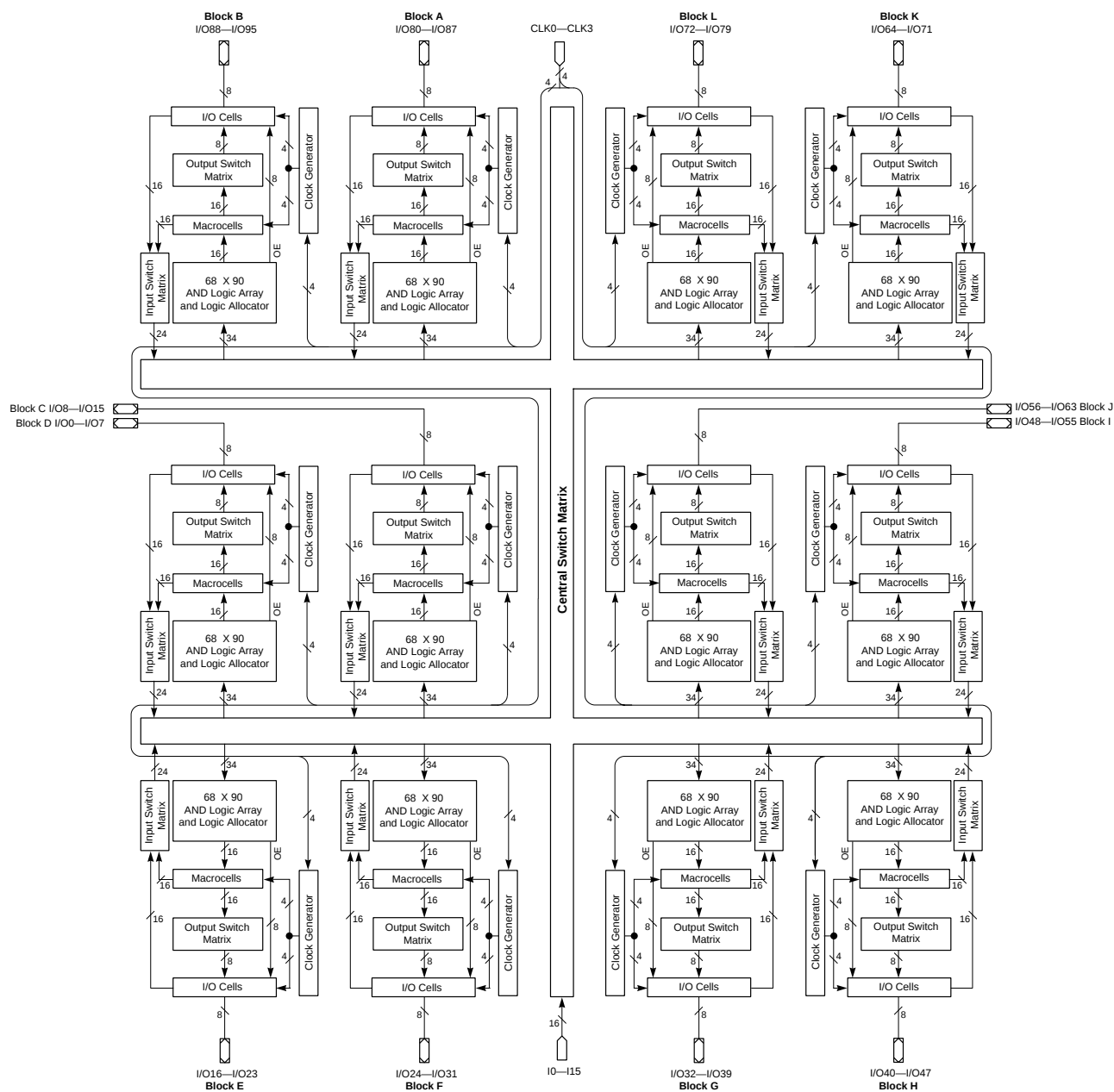
17466H-020

BLOCK DIAGRAM – M4A3-64/64



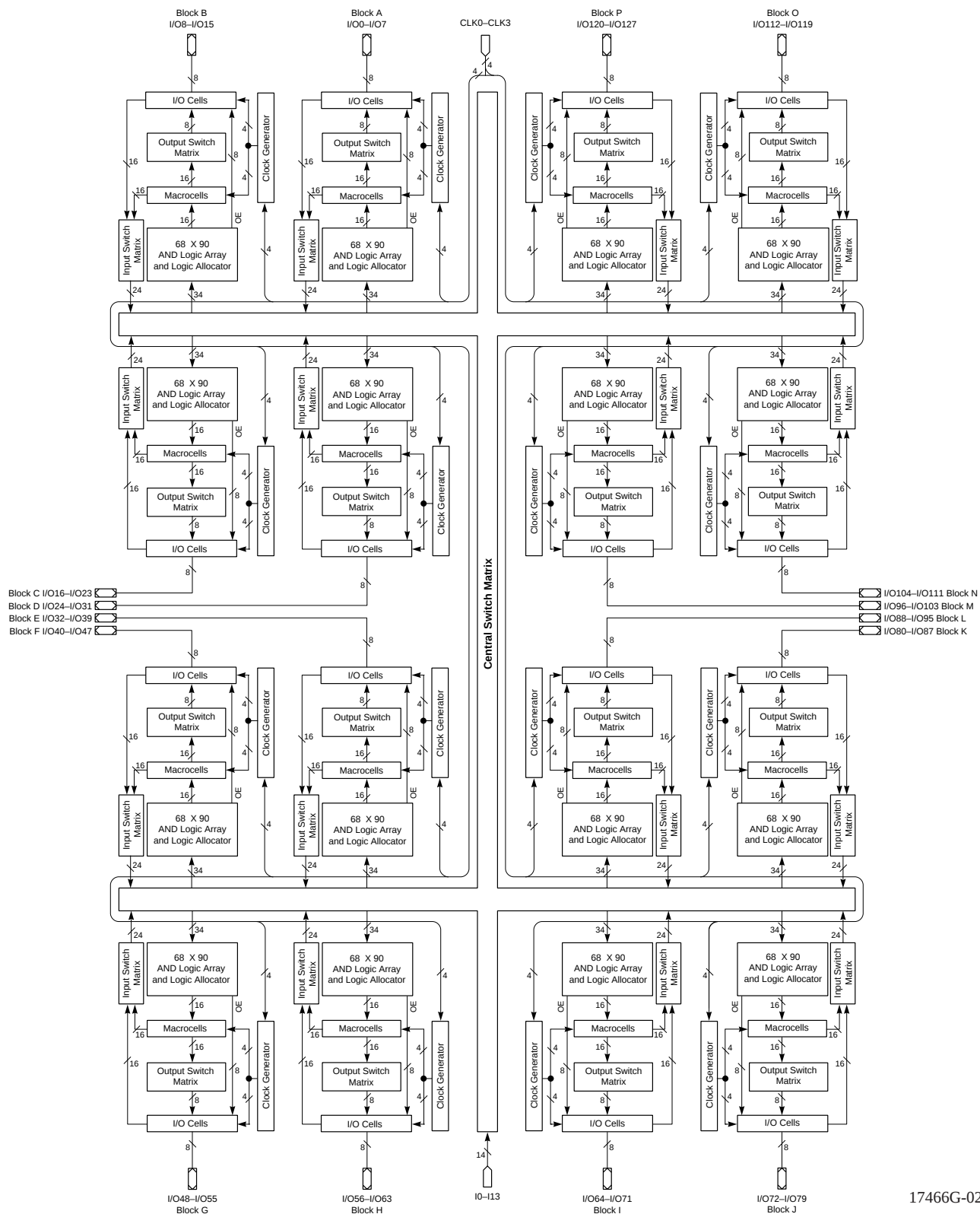
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BLOCK DIAGRAM – M4A(3,5)-192/96



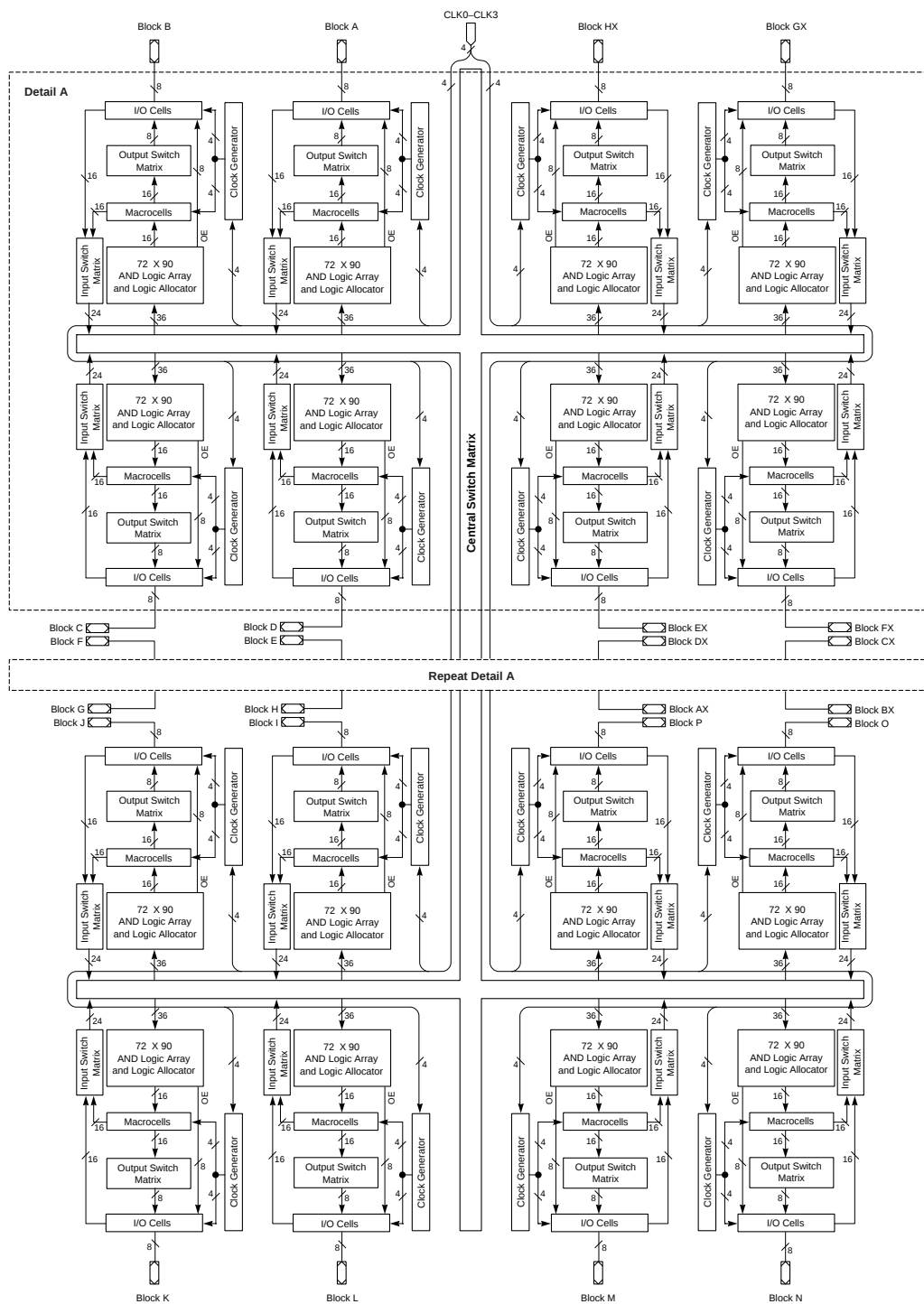
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BLOCK DIAGRAM – M4A(3,5)-256/128



17466G-024

BLOCK DIAGRAM – M4A3-384/160, M4A3-384/192



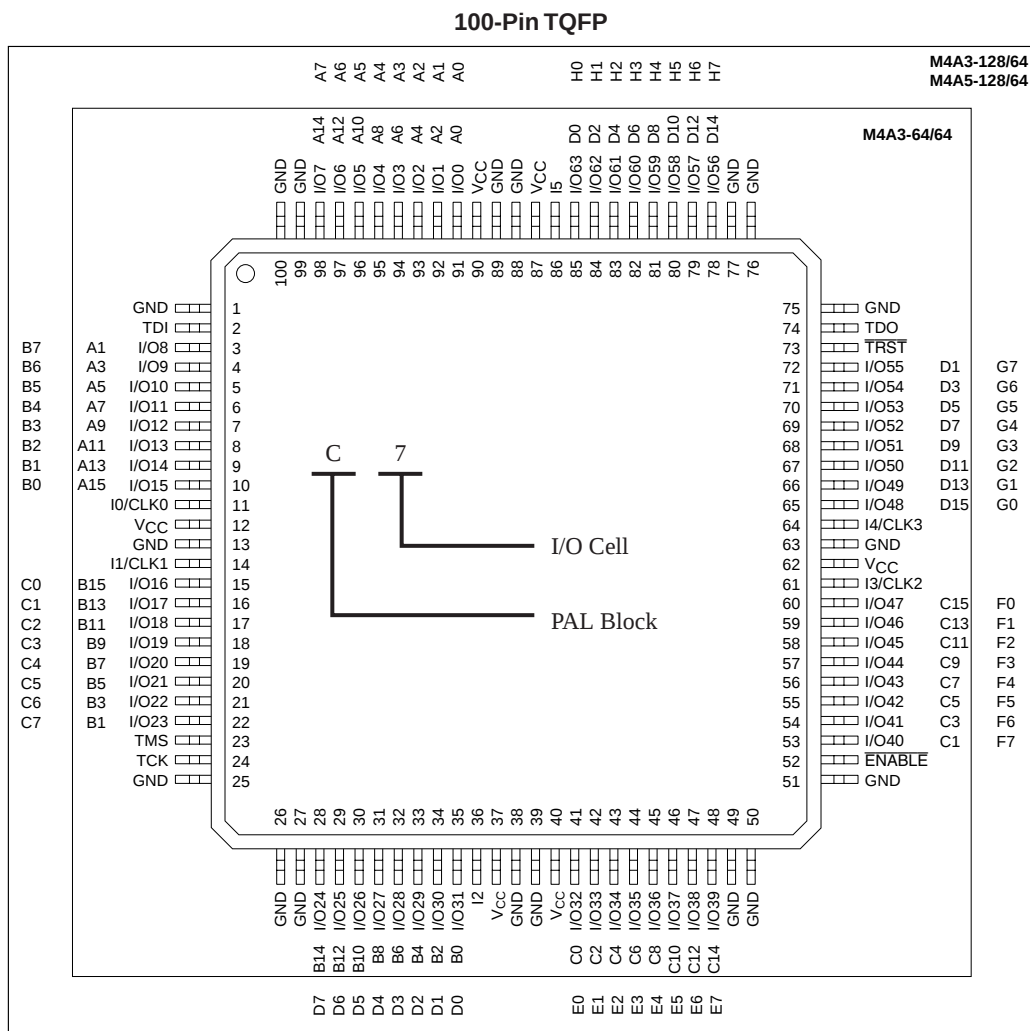
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ispMACH 4A TIMING PARAMETERS OVER OPERATING RANGES¹

		-5		-55		-6		-65		-7		-10		-12		-14		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Combinatorial Delay:																		
t _{PDi}	Internal combinatorial propagation delay		3.5		4.0		4.3		4.5		5.0		7.0		9.0		11.0	ns
t _{PD}	Combinatorial propagation delay		5.0		5.5		6.0		6.5		7.5		10.0		12.0		14.0	ns
Registered Delays:																		
t _{SS}	Synchronous clock setup time, D-type register	3.0		3.5		3.5		3.5		5.0		5.5		7.0		10.0		ns
t _{SST}	Synchronous clock setup time, T-type register	4.0		4.0		4.0		4.0		6.0		6.5		8.0		11.0		ns
t _{SA}	Asynchronous clock setup time, D-type register	2.5		2.5		2.5		3.0		3.5		4.0		5.0		8.0		ns
t _{SAT}	Asynchronous clock setup time, T-type register	3.0		3.0		3.0		3.5		4.5		5.0		6.0		9.0		ns
t _{HS}	Synchronous clock hold time	0.0		0.0		0.0		0.0		0.0		0.0		0.0		0.0		ns
t _{HA}	Asynchronous clock hold time	2.5		2.5		2.5		3.0		3.5		4.0		5.0		8.0		ns
t _{COsi}	Synchronous clock to internal output		2.5		2.5		2.8		3.0		3.0		3.0		3.5		3.5	ns
t _{COS}	Synchronous clock to output		4.0		4.0		4.5		5.0		5.5		6.0		6.5		6.5	ns
t _{COAi}	Asynchronous clock to internal output		5.0		5.0		5.0		5.0		6.0		8.0		10.0		12.0	ns
t _{COA}	Asynchronous clock to output		6.5		6.5		6.8		7.0		8.5		11.0		13.0		15.0	ns
Latched Delays:																		
t _{SSL}	Synchronous latch setup time	4.0		4.0		4.0		4.5		6.0		7.0		8.0		10.0		ns
t _{SAL}	Asynchronous latch setup time	3.0		3.0		3.5		3.5		4.0		4.0		5.0		8.0		ns
t _{HSL}	Synchronous latch hold time	0.0		0.0		0.0		0.0		0.0		0.0		0.0		0.0		ns
t _{HAL}	Asynchronous latch hold time	3.0		3.0		3.5		3.5		4.0		4.0		5.0		8.0		ns
t _{PDLi}	Transparent latch to internal output		5.5		5.5		5.8		6.0		7.5		9.0		11.0		12.0	ns
t _{PDL}	Propagation delay through transparent latch to output		7.0		7.0		7.5		8.0		10.0		12.0		14.0		15.0	ns
t _{GOSi}	Synchronous gate to internal output		3.0		3.0		3.0		3.0		3.5		4.5		7.0		8.0	ns
t _{GOS}	Synchronous gate to output		4.5		4.5		4.8		5.0		6.0		7.5		10.0		11.0	ns
t _{GOAi}	Asynchronous gate to internal output		6.0		6.0		6.0		6.0		8.5		10.0		13.0		15.0	ns
t _{GOA}	Asynchronous gate to output		7.5		7.5		7.8		8.0		11.0		13.0		16.0		18.0	ns
Input Register Delays:																		
t _{SIRS}	Input register setup time	1.5		1.5		2.0		2.0		2.0		2.0		2.0		2.0		ns
t _{HIRS}	Input register hold time	2.5		2.5		3.0		3.0		3.0		3.0		3.0		4.0		ns
t _{ICOSi}	Input register clock to internal feedback		3.0		3.0		3.0		3.0		3.5		4.5		6.0		6.0	ns
Input Latch Delays:																		
t _{SIL}	Input latch setup time	1.5		1.5		1.5		2.0		2.0		2.0		2.0		2.0		ns
t _{HIL}	Input latch hold time	2.5		2.5		2.5		3.0		3.0		3.0		3.0		4.0		ns
t _{IGOSi}	Input latch gate to internal feedback		3.5		3.5		3.8		4.0		4.0		4.0		4.0		5.0	ns
t _{PDILi}	Transparent input latch to internal feedback		1.5		1.5		1.5		1.5		2.0		2.0		2.0		2.0	ns

100-PIN TQFP CONNECTION DIAGRAM (M4A3-64/64 AND M4A(3,5)-128/64)

Top View



PIN DESIGNATIONS

CLK/I = Clock or Input

GND = Ground

I = Input

I/O = Input/Output

V_{CC} = Supply Voltage

TDI = Test Data In

TCK = Test Clock

TMS = Test Mode Select

TDO = Test Data Out

TRST = Test Reset

ENABLE = Program

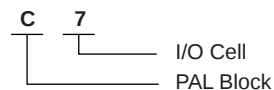
144-BALL FPBGA CONNECTION DIAGRAM (M4A3-192/96)

Bottom View

144-Ball fpBGA													
	12	11	10	9	8	7	6	5	4	3	2	1	
A	GND	I/O72 L7	I/O76 L3	I13	GBCLK3	I0	I/O82 A2	I/O86 A6	I/O88 B0	I/O93 B5	I/O95 B7	GND	A
B	GND	I/O73 L6	I/O77 L2	I/O79 L0	VCC	I1	I/O83 A3	I/O87 A7	I/O90 B2	I/O94 B6	I/O0 D7	TDI	B
C	GND	TD0	I/O74 L5	I14	GND	I/O80 A0	I/O84 A4	GND	I/O92 B4	I/O1 D6	I/O4 D3	I/O3 D4	C
D	I/O67 K4	I/O69 K2	I/O71 K0	I/O75 L4	GBCLK0	I/O81 A1	VCC	I/O91 B3	I/O2 D5	I2	I/O6 D1	I/O7 D0	D
E	I12	I/O64 K7	I/O66 K5	I/O70 K1	I/O78 L1	I/O85 A5	I/O89 B1	I/O5 D2	I/O8 C7	I4	GND	VCC	E
F	I10	I11	GND	I/O65 K6	I/O68 K3	I15	I3	GND	I/O12 C3	I/O11 C4	I/O10 C5	I/O9 C6	F
G	I/O60 J3	I/O61 J2	I/O62 J1	I/O63 J0	VCC	GND	I7	I/O20 E3	I/O17 E6	I/O15 C0	I/O14 C1	I/O13 C2	G
H	I/O56 J7	I/O57 J6	I/O58 J5	I/O59 J4	I/O53 I2	I/O41 H1	I/O37 G5	I/O30 F1	I/O22 E1	I/O18 E5	I/O16 E7	VCC	H
J	I/O55 I0	I/O54 I1	VCC	I/O50 I5	I/O43 H3	VCC	I/O33 G1	GBCLK2	I/O27 F4	I/O23 E0	I/O21 E2	I/O19 E4	J
K	I/O51 I4	I/O52 I3	I/O49 I6	I/O44 H4	GND	I/O36 G4	I/O32 G0	VCC	I6	I/O26 F5	TCK	TMS	K
L	GND	I/O48 I7	I/O46 H6	I/O42 H2	I/O39 G7	I/O35 G3	I9	GND	I/O31 F0	I/O29 F2	I/O25 F6	GND	L
M	GND	I/O47 H7	I/O45 H5	I/O40 H0	I/O38 G6	I/O34 G2	I8	GBCLK1	I5	I/O28 F3	I/O24 F7	GND	M
	12	11	10	9	8	7	6	5	4	3	2	1	

PIN DESIGNATIONS

CLK = Clock
 GND = Ground
 I = Input
 I/O = Input/Output
 N/C = No Connect
 VCC = Supply Voltage
 TDI = Test Data In
 TCK = Test Clock
 TMS = Test Mode Select
 TD0 = Test Data Out

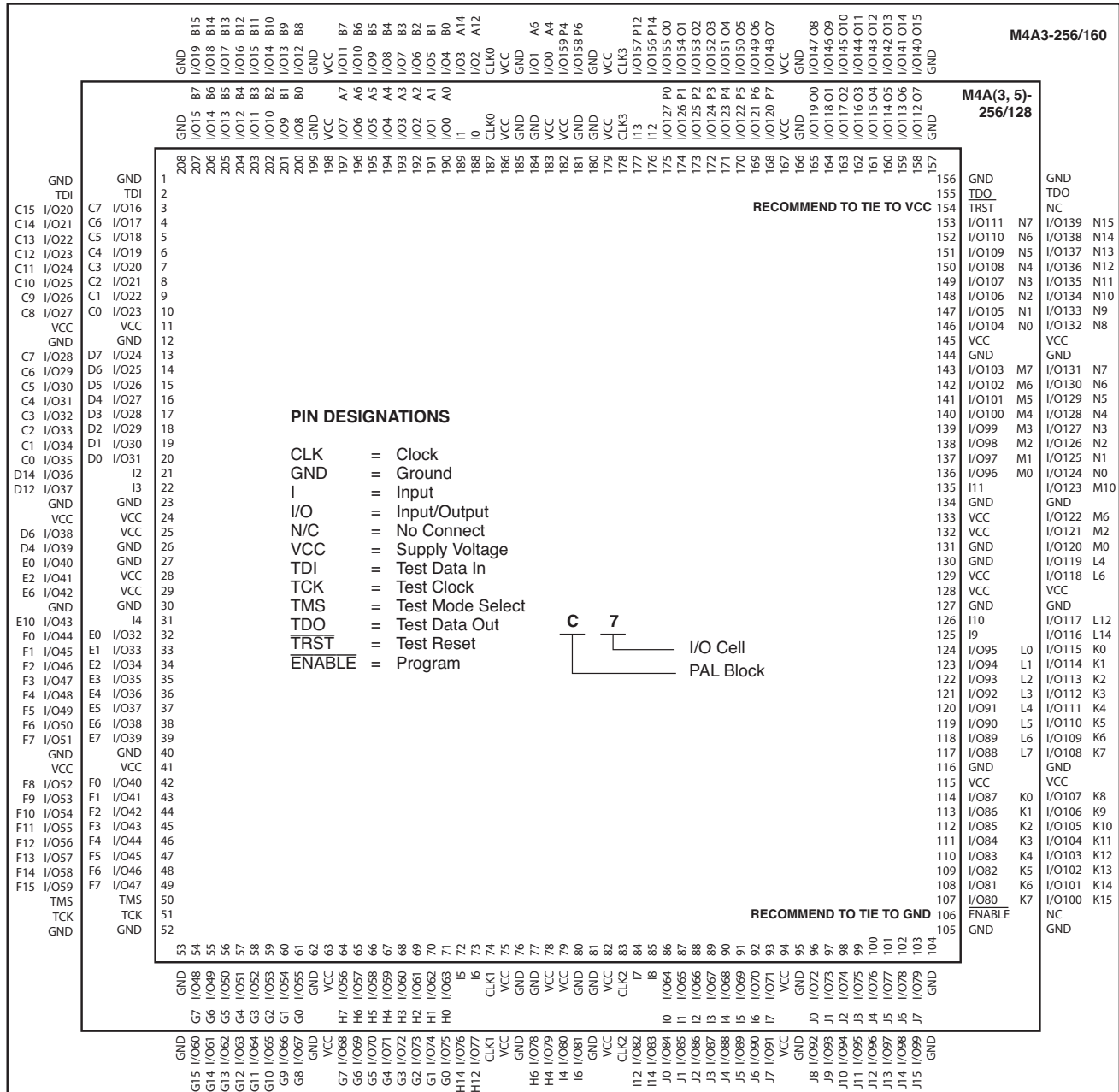


m4a3.192.96_144bga

208-PIN PQFP CONNECTION DIAGRAM (M4A(3,5)-256/128 AND M4A3-256/160)

Top View

208-Pin PQFP



17466G-044

256-BALL BGA CONNECTION DIAGRAM (M4A3-256/128)

Bottom View

256-Ball BGA

	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	GND	N/C	GND	I/O108 N4	I/O105 N1	GND	I/O100 M4	I/O96 M0	GND	GND	GND	GND	I/O95 L0	I/O91 L4	GND	I/O87 K0	N/C	GND	GND	GND	A
B	GND	I/O113 O6	N/C	I/O109 N5	I/O106 N2	I/O103 M7	I/O102 M6	I/O98 M2	N/C	I11	N/C	N/C	I/O93 L2	I/O89 L6	I/O88 L7	I/O85 K2	I/O83 K4	I/O82 K5	N/C	GND	B
C	I/O116 O3	N/C	VCC	TRST	I/O111 N7	I/O107 N3	I/O104 N0	I/O101 M5	I/O97 M1	N/C	I10	I/O94 L1	I/O90 L5	I/O86 K1	I/O84 K3	I/O80 K7	ENABLE	VCC	I/O78 J6	I/O74 J2	C
D	I/O120 P7	I/O117 O2	I/O112 O7	VCC	VCC	I/O110 N6	VCC	N/C	I/O99 M3	N/C	I9	I/O92 L3	N/C	VCC	I/O81 K6	VCC	VCC	I/O79 J7	I/O75 J3	I/O71 I7	D
E	I/O123 P4	I/O119 O0	I/O114 O5	TDI	PIN DESIGNATIONS CLK = Clock GND = Ground I = Input I/O = Input/Output N/C = No Connect VCC = Supply Voltage TDI = Test Data In TCK = Test Clock TMS = Test Mode Select TDO = Test Data Out TRST = Test Reset ENABLE = Program C7 I/O Cell PAL Block												TDO	I/O77 J5	I/O72 J0	I/O68 I4	E
F	GND	I/O122 P5	I/O118 O1	I/O115 O4													I/O76 J4	I/O73 J1	I/O69 I5	GND	F
G	I12	I/O125 P2	I/O121 P6	VCC													VCC	I/O70 I6	I/O65 I1	I8	G
H	GND	I/O127 P0	I/O126 P1	I/O124 P3													I/O67 I3	I/O66 I2	I/O64 I0	GND	H
J	N/C	N/C	N/C	I13													I7	N/C	N/C	N/C	J
K	GND	CLK3	N/C	N/C													N/C	N/C	CLK2	N/C	K
L	N/C	CLK0	N/C	N/C													N/C	N/C	CLK1	GND	L
M	N/C	N/C	N/C	I0													I6	N/C	I/O63 H0	I/O62 H1	M
N	GND	I/O0 A0	I/O2 A2	I/O3 A3													I/O60 H3	I/O61 H2	I/O59 H4	GND	N
P	I1	I/O1 A1	I/O6 A6	VCC													VCC	I/O57 H6	I/O58 H5	I5	P
R	GND	I/O5 A5	I/O9 B1	N/C	I/O51 G4	I/O54 G1	I/O56 H7	GND	R												
T	I/O4 A4	I/O8 B0	I/O12 B4	TCK	TMS	I/O50 G5	I/O55 G0	N/C	T												
U	I/O7 A7	I/O11 B3	I/O15 B7	VCC	VCC	I/O18 C5	VCC	I/O24 D7	I/O29 D2	I2	N/C	I/O35 E3	N/C	VCC	N/C	VCC	VCC	I/O48 G7	I/O53 G2	N/C	U
V	I/O10 B2	I/O13 B5	VCC	I/O16 C7	I/O17 C6	I/O21 C2	I/O23 C0	I/O27 D4	I/O31 D0	I3	N/C	I/O33 E1	I/O37 E5	I/O41 F1	I/O43 F3	I/O46 F6	I/O47 F7	VCC	I/O52 G3	N/C	V
W	GND	I/O14 B6	N/C	N/C	I/O19 C4	I/O22 C1	I/O25 D6	I/O28 D3	N/C	N/C	I4	N/C	I/O34 E2	I/O38 E6	I/O39 E7	I/O42 F2	I/O45 F5	N/C	I/O49 G6	GND	W
Y	GND	GND	GND	N/C	I/O20 C3	GND	I/O26 D5	I/O30 D1	GND	GND	GND	GND	I/O32 E0	I/O36 E4	GND	I/O40 F0	I/O44 F4	GND	N/C	GND	Y
	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

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256-BALL BGA CONNECTION DIAGRAM - (M4A3-384/192)

Bottom View

256-Ball BGA

	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1			
A	GND	I/O11 FX7	GND	I/O44 FX6	I/O58 CX6	GND	I/O70 CX2	I/O76 DX6	GND	GND	GND	GND	I/O108 AX5	I/O116 BX0	GND	I/O128 BX7	I/O134 O3	GND	GND	GND	A		
B	GND	I/O12 GX7	I/O28 FX5	I/O45 FX3	I/O59 CX7	I/O64 CX5	I/O71 CX3	I/O77 DX7	I/O84 DX5	I/O90 DX2	I/O96 AX0	I/O102 AX3	I/O109 AX6	I/O117 BX1	I/O122 BX4	I/O129 BX6	I/O135 O4	I/O148 O6	I/O164 O7	GND	B		
C	I/O0 GX6	I/O13 GX5	VCC	I/O46 FX4	I/O60 FX2	I/O65 FX1	I/O72 CX4	I/O78 CX0	I/O85 DX4	I/O91 DX1	I/O97 AX1	I/O103 AX4	I/O110 BX2	I/O118 BX5	I/O123 O0	I/O130 O1	I/O136 O5	VCC	I/O165 N7	I/O181 N6	C		
D	I/O1 EX7	I/O14 GX3	I/O29 GX4	VCC	VCC	I/O66 FX0	VCC	I/O79 CX1	I/O86 DX3	I/O92 DX0	I/O98 AX2	I/O104 AX7	I/O111 B3X	VCC	I/O124 O2	VCC	VCC	I/O149 N4	I/O166 N5	I/O182 P7	D		
E	I/O2 EX0	I/O15 GX0	I/O30 GX1	TDI	PIN DESIGNATIONS CLK = Clock GND = Ground I = Input I/O = Input/Output N/C = No Connect VCC = Supply Voltage TDI = Test Data In TCK = Test Clock TMS = Test Mode Select TDO = Test Data Out C7 I/O Cell PAL Block														TDO	I/O150 N2	I/O167 N3	I/O183 P6	E
F	GND	I/O16 EX1	I/O31 EX6	I/O47 GX2															I/O137 N1	I/O151 N0	I/O168 P5	GND	F
G	I/O3 HX6	I/O17 EX4	I/O32 EX5	VCC															VCC	I/O152 P4	I/O169 P3	I/O184 M7	G
H	GND	I/O18 HX5	I/O33 EX2	I/O48 EX3															I/O138 P2	I/O153 P1	I/O170 P0	GND	H
J	I/O4 HX0	I/O19 HX1	I/O34 HX4	I/O49 HX7															I/O139 M6	I/O154 M5	I/O171 M4	I/O185 M3	J
K	GND	CLK3	I/O35 HX2	I/O50 HX3															I/O140 M0	I/O155 M1	CLK2	I/O186 M2	K
L	I/O5 A2	CLK0	I/O36 A0	I/O51 A1															I/O141 L3	I/O156 L4	CLK1	GND	L
M	I/O6 A4	I/O20 A3	I/O37 A5	I/O52 A6															I/O142 L6	I/O157 L5	I/O172 L0	I/O187 L1	M
N	GND	I/O21 A7	I/O38 D0	I/O53 D1															I/O143 I5	I/O158 I0	I/O173 L7	GND	N
P	I/O7 D2	I/O22 D3	I/O39 D4	VCC															VCC	I/O159 I4	I/O174 I1	I/O188 L2	P
R	GND	I/O23 D5	I/O40 D6	I/O54 D7	I/O144 K5	I/O160 K0	I/O175 I3	GND	R														
T	I/O8 B3	I/O24 B0	I/O41 B7	TCK	TMS	I/O161 K4	I/O176 K1	I/O189 I2	T														
U	I/O9 B4	I/O25 B1	I/O42 B6	VCC	VCC	I/O67 C0	VCC	I/O80 F0	I/O87 E5	I/O93 E2	I/O99 H2	I/O105 H5	I/O112 G0	VCC	I/O125 J1	VCC	VCC	I/O162 K7	I/O177 K2	I/O190 I6	U		
V	I/O10 B5	I/O26 B2	VCC	I/O55 C5	I/O61 C2	I/O68 C1	I/O73 F4	I/O81 F1	I/O88 E4	I/O94 E1	I/O100 H1	I/O106 H4	I/O113 G1	I/O119 G4	I/O126 J0	I/O131 J2	I/O145 J5	VCC	I/O178 K3	I/O191 I7	V		
W	GND	I/O27 C7	I/O43 C6	I/O56 C3	I/O62 F7	I/O69 F5	I/O74 F3	I/O82 E7	I/O89 E3	I/O95 E0	I/O101 H0	I/O107 H3	I/O114 H7	I/O120 G3	I/O127 G5	I/O132 G7	I/O146 J4	I/O163 J6	I/O179 J7	GND	W		
Y	GND	GND	GND	I/O57 C4	I/O63 F6	GND	I/O75 F2	I/O83 E6	GND	GND	GND	GND	I/O115 H6	I/O121 G2	GND	I/O133 G6	I/O147 J3	GND	I/O180 K6	GND	Y		
	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1			

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