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Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details

Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	5 ns
Voltage Supply - Internal	3V ~ 3.6V
Number of Logic Elements/Blocks	-
Number of Macrocells	32
Number of Gates	-
Number of I/O	32
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.59x16.59)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/m4a3-32-32-5jc

The ispMACH 4A family offers 20 density-I/O combinations in Thin Quad Flat Pack (TQFP), Plastic Quad Flat Pack (PQFP), Plastic Leaded Chip Carrier (PLCC), Ball Grid Array (BGA), fine-pitch BGA (fpBGA), and chip-array BGA (caBGA) packages ranging from 44 to 388 pins (Table 3). It also offers I/O safety features for mixed-voltage designs so that the 3.3-V devices can accept 5-V inputs, and 5-V devices do not overdrive 3.3-V inputs. Additional features include Bus-Friendly inputs and I/Os, a programmable power-down mode for extra power savings and individual output slew rate control for the highest speed transition or for the lowest noise transition.

Table 3. ispMACH 4A Package and I/O Options (Number of I/Os and dedicated inputs in Table)

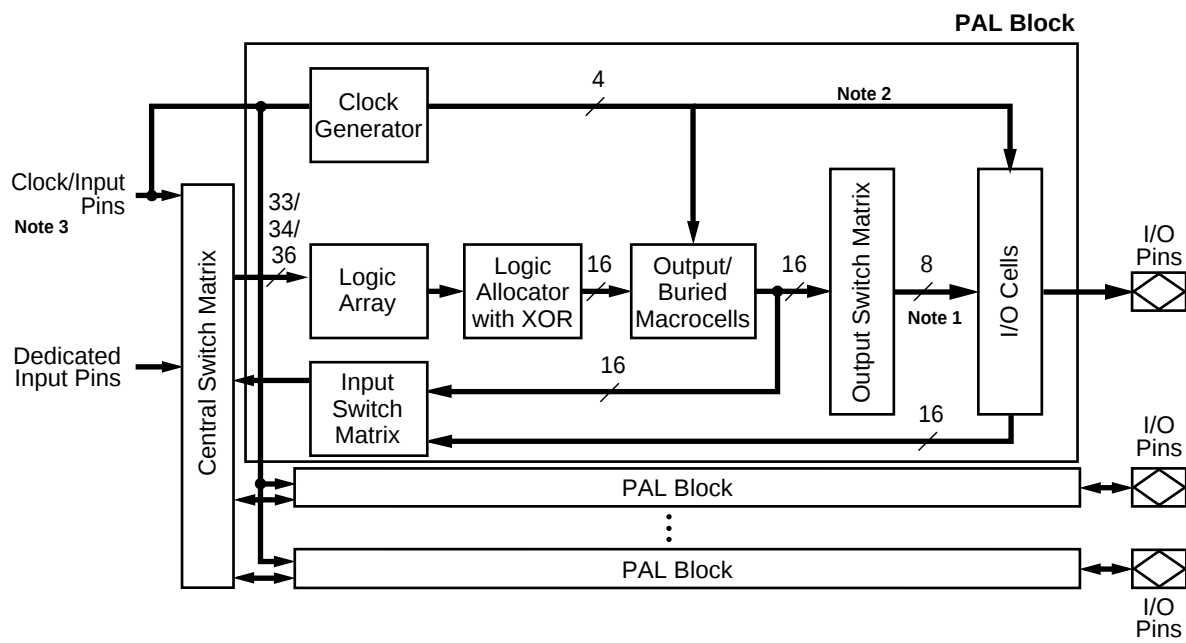
3.3 V Devices								
Package	M4A3-32	M4A3-64	M4A3-96	M4A3-128	M4A3-192	M4A3-256	M4A3-384	M4A3-512
44-pin PLCC	32+2	32+2						
44-pin TQFP	32+2	32+2						
48-pin TQFP	32+2	32+2						
100-pin TQFP		64+6	48+8	64+6				
100-pin PQFP				64+6				
100-ball caBGA				64+6				
144-pin TQFP					96+16			
144-ball fpBGA					96+16			
208-pin PQFP						128+14, 160	160	160
256-ball fpBGA						128+14, 192	192	192
256-ball BGA						128+14	192	
388-ball fpBGA								256

5 V Devices						
Package	M4A5-32	M4A5-64	M4A5-96	M4A5-128	M4A5-192	M4A5-256
44-pin PLCC	32+2	32+2				
44-pin TQFP	32+2	32+2				
48-pin TQFP	32+2	32+2				
100-pin TQFP			48+8	64+6		
100-pin PQFP				64+6		
144-pin TQFP					96+16	
208-pin PQFP						128+14

FUNCTIONAL DESCRIPTION

The fundamental architecture of ispMACH 4A devices (Figure 1) consists of multiple, optimized PAL[®] blocks interconnected by a central switch matrix. The central switch matrix allows communication between PAL blocks and routes inputs to the PAL blocks. Together, the PAL blocks and central switch matrix allow the logic designer to create large designs in a single device instead of having to use multiple devices.

The key to being able to make effective use of these devices lies in the interconnect schemes. In the ispMACH 4A architecture, the macrocells are flexibly coupled to the product terms through the logic allocator, and the I/O pins are flexibly coupled to the macrocells due to the output switch matrix. In addition, more input routing options are provided by the input switch matrix. These resources provide the flexibility needed to fit designs efficiently.



17466G-001

Figure 1. ispMACH 4A Block Diagram and PAL Block Structure

Notes:

1. 16 for ispMACH 4A devices with 1:1 macrocell-I/O cell ratio (see next page).
2. Block clocks do not go to I/O cells in M4A(3,5)-32/32.
3. M4A(3,5)-192, M4A(3,5)-256, M4A3-384, and M4A3-512 have dedicated clock pins which cannot be used as inputs and do not connect to the central switch matrix.

Table 4. Architectural Summary of ispMACH 4A devices

	ispMACH 4A Devices	
	M4A3-64/32, M4A5-64/32 M4A3-96/48, M4A5-96/48 M4A3-128/64, M4A5-128/64 M4A3-192/96, M4A5-192/96 M4A3-256/128, M4A5-256/128 M4A3-384 M4A3-512	M4A3-32/32 M4A5-32/32 M4A3-64/64 M4A3-256/160 M4A3-256/192
Macrocell-I/O Cell Ratio	2:1	1:1
Input Switch Matrix	Yes	Yes ¹
Input Registers	Yes	No
Central Switch Matrix	Yes	Yes
Output Switch Matrix	Yes	Yes

The Macrocell-I/O cell ratio is defined as the number of macrocells versus the number of I/O cells internally in a PAL block (Table 4).

The central switch matrix takes all dedicated inputs and signals from the input switch matrices and routes them as needed to the PAL blocks. Feedback signals that return to the same PAL block still must go through the central switch matrix. This mechanism ensures that PAL blocks in ispMACH 4A devices communicate with each other with consistent, predictable delays.

The central switch matrix makes a ispMACH 4A device more advanced than simply several PAL devices on a single chip. It allows the designer to think of the device not as a collection of blocks, but as a single programmable device; the software partitions the design into PAL blocks through the central switch matrix so that the designer does not have to be concerned with the internal architecture of the device.

Each PAL block consists of:

- ◆ Product-term array
- ◆ Logic allocator
- ◆ Macrocells
- ◆ Output switch matrix
- ◆ I/O cells
- ◆ Input switch matrix
- ◆ Clock generator

Notes:

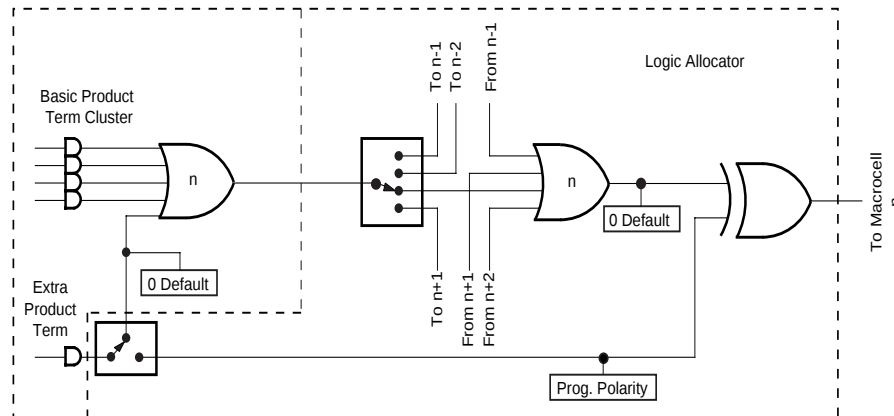
1. M4A3-64/64 internal switch matrix functionality embedded in central switch matrix.

Table 6. Logic Allocator for All ispMACH 4A Devices (except M4A(3,5)-32/32)

Output Macrocell	Available Clusters	Output Macrocell	Available Clusters
M ₀	C ₀ , C ₁ , C ₂	M ₈	C ₇ , C ₈ , C ₉ , C ₁₀
M ₁	C ₀ , C ₁ , C ₂ , C ₃	M ₉	C ₈ , C ₉ , C ₁₀ , C ₁₁
M ₂	C ₁ , C ₂ , C ₃ , C ₄	M ₁₀	C ₉ , C ₁₀ , C ₁₁ , C ₁₂
M ₃	C ₂ , C ₃ , C ₄ , C ₅	M ₁₁	C ₁₀ , C ₁₁ , C ₁₂ , C ₁₃
M ₄	C ₃ , C ₄ , C ₅ , C ₆	M ₁₂	C ₁₁ , C ₁₂ , C ₁₃ , C ₁₄
M ₅	C ₄ , C ₅ , C ₆ , C ₇	M ₁₃	C ₁₂ , C ₁₃ , C ₁₄ , C ₁₅
M ₆	C ₅ , C ₆ , C ₇ , C ₈	M ₁₄	C ₁₃ , C ₁₄ , C ₁₅
M ₇	C ₆ , C ₇ , C ₈ , C ₉	M ₁₅	C ₁₄ , C ₁₅

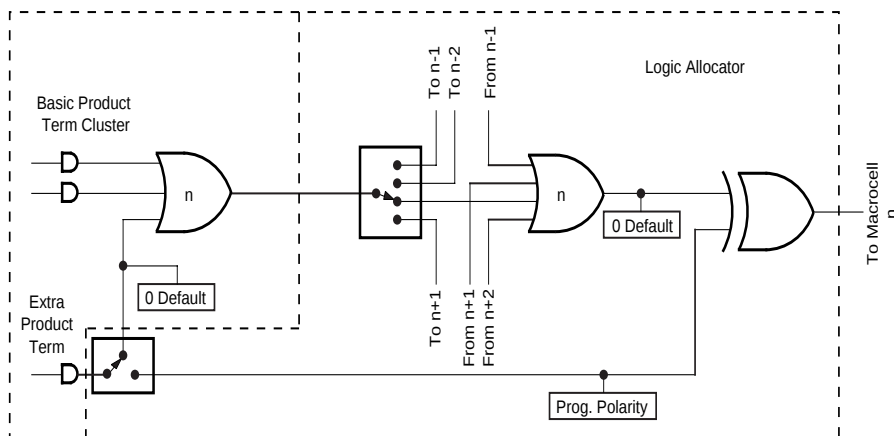
Table 7. Logic Allocator for M4A(3,5)-32/32

Output Macrocell	Available Clusters	Output Macrocell	Available Clusters
M ₀	C ₀ , C ₁ , C ₂	M ₈	C ₈ , C ₉ , C ₁₀
M ₁	C ₀ , C ₁ , C ₂ , C ₃	M ₉	C ₈ , C ₉ , C ₁₀ , C ₁₁
M ₂	C ₁ , C ₂ , C ₃ , C ₄	M ₁₀	C ₉ , C ₁₀ , C ₁₁ , C ₁₂
M ₃	C ₂ , C ₃ , C ₄ , C ₅	M ₁₁	C ₁₀ , C ₁₁ , C ₁₂ , C ₁₃
M ₄	C ₃ , C ₄ , C ₅ , C ₆	M ₁₂	C ₁₁ , C ₁₂ , C ₁₃ , C ₁₄
M ₅	C ₄ , C ₅ , C ₆ , C ₇	M ₁₃	C ₁₂ , C ₁₃ , C ₁₄ , C ₁₅
M ₆	C ₅ , C ₆ , C ₇	M ₁₄	C ₁₃ , C ₁₄ , C ₁₅
M ₇	C ₆ , C ₇	M ₁₅	C ₁₄ , C ₁₅



a. Synchronous Mode

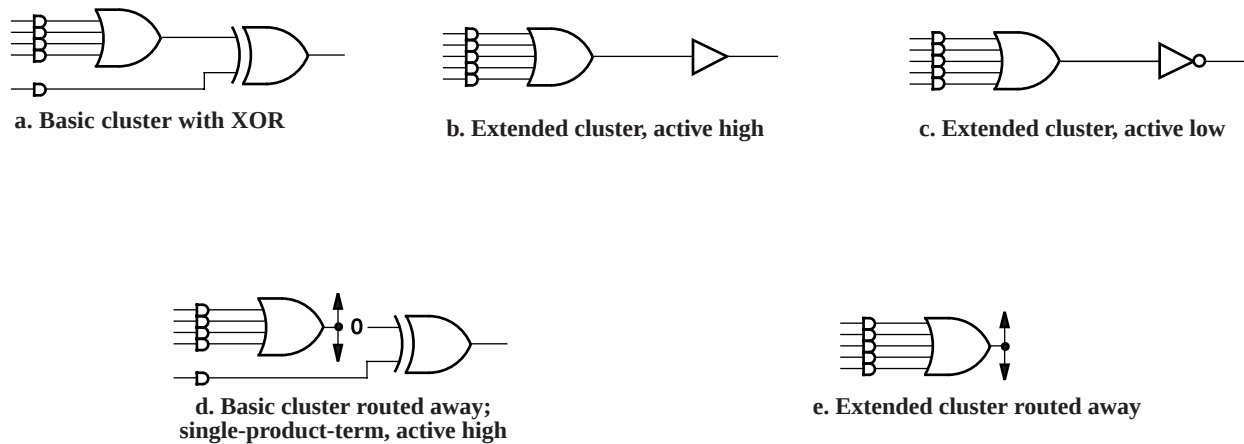
17466G-005



b. Asynchronous Mode

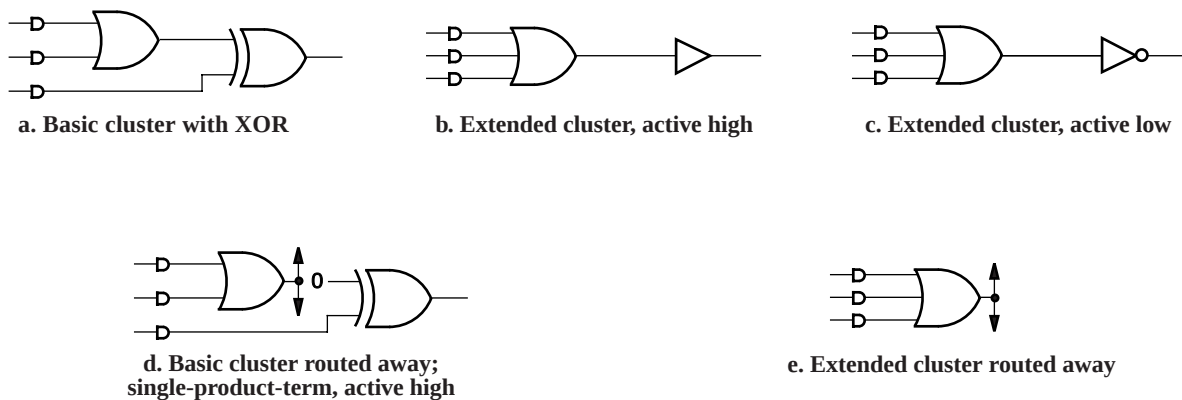
17466G-006

Figure 2. Logic Allocator: Configuration of Cluster “n” Set by Mode of Macrocell “n”



17466G-007

Figure 3. Logic Allocator Configurations: Synchronous Mode



17466G-008

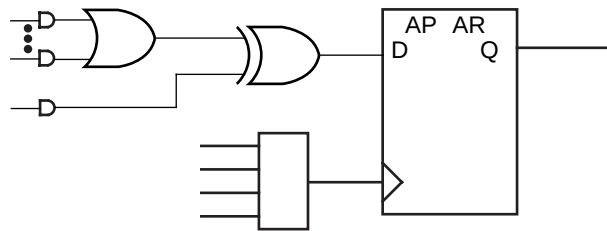
Figure 4. Logic Allocator Configurations: Asynchronous Mode

Note that the configuration of the logic allocator has absolutely no impact on the speed of the signal. All configurations have the same delay. This means that designers do not have to decide between optimizing resources or speed; both can be optimized.

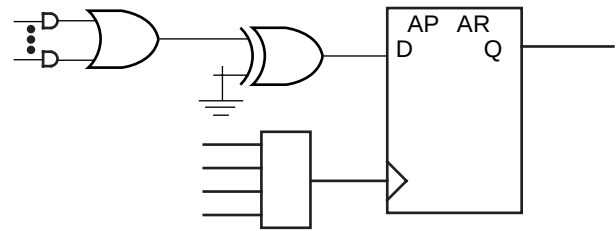
If not used in the cluster, the extra product term can act in conjunction with the basic cluster to provide XOR logic for such functions as data comparison, or it can work with the D-,T-type flip-flop to provide for J-K, and S-R register operation. In addition, if the basic cluster is routed to another macrocell, the extra product term is still available for logic. In this case, the first XOR input will be a logic 0. This circuit has the flexibility to route product terms elsewhere without giving up the use of the macrocell.

Product term clusters do not “wrap” around a PAL block. This means that the macrocells at the ends of the block have fewer product terms available.

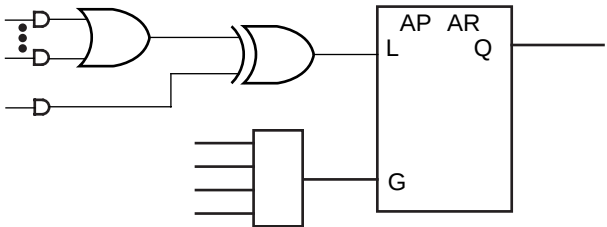
The flip-flop can be configured as a D-type or T-type latch. J-K or S-R registers can be synthesized. The primary flip-flop configurations are shown in Figure 6, although others are possible. Flip-flop functionality is defined in Table 8. Note that a J-K latch is inadvisable as it will cause oscillation if both J and K inputs are HIGH.



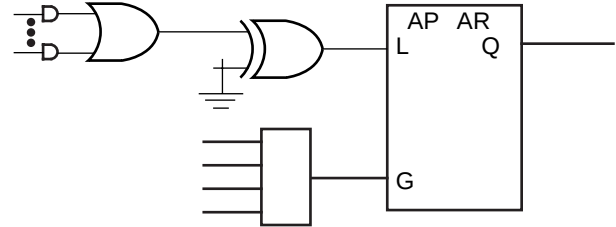
a. D-type with XOR



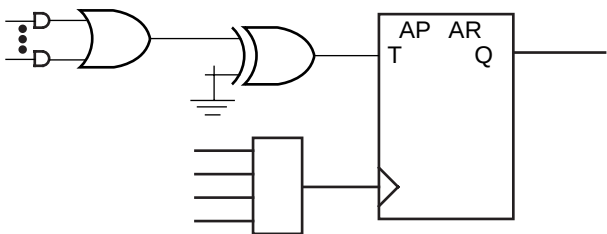
b. D-type with programmable D polarity



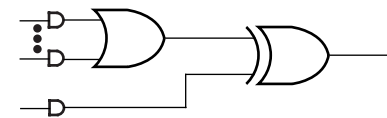
c. Latch with XOR



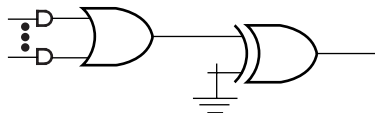
d. Latch with programmable D polarity



e. T-type with programmable T polarity



f. Combinatorial with XOR

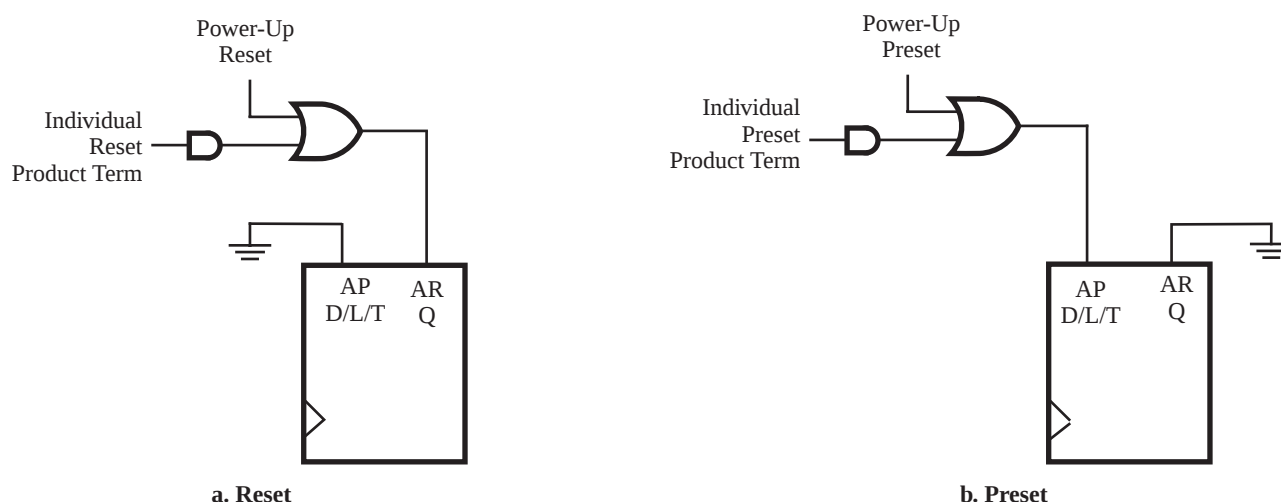


g. Combinatorial with programmable polarity

Figure 6. Primary Macrocell Configurations

17466G-011

A reset/preset swapping feature in each macrocell allows for reset and preset to be exchanged, providing flexibility. In asynchronous mode (Figure 8), a single individual product term is provided for initialization. It can be selected to control reset or preset.



17466G-014

17466G-015

Figure 8. Asynchronous Mode Initialization Configurations

Note that the reset/preset swapping selection feature effects power-up reset as well. The initialization functionality of the flip-flops is illustrated in Table 9. The macrocell sends its data to the output switch matrix and the input switch matrix. The output switch matrix can route this data to an output if so desired. The input switch matrix can send the signal back to the central switch matrix as feedback.

Table 9. Asynchronous Reset/Preset Operation

AR	AP	CLK/LE ¹	Q+
0	0	X	See Table 8
0	1	X	1
1	0	X	0
1	1	X	0

Note:

- Transparent latch is unaffected by AR, AP

Output Switch Matrix

The output switch matrix allows macrocells to be connected to any of several I/O cells within a PAL block. This provides high flexibility in determining pinout and allows design changes to occur without effecting pinout.

In ispMACH 4A devices with 2:1 Macrocell-I/O cell ratio, each PAL block has twice as many macrocells as I/O cells. The ispMACH 4A output switch matrix allows for half of the macrocells to drive I/O cells within a PAL block, in combinations according to Figure 9. Each I/O cell can choose from eight macrocells; each macrocell has a choice of four I/O cells. The ispMACH 4A devices with 1:1 Macrocell-I/O cell ratio allow each macrocell to drive one of eight I/O cells (Figure 9).

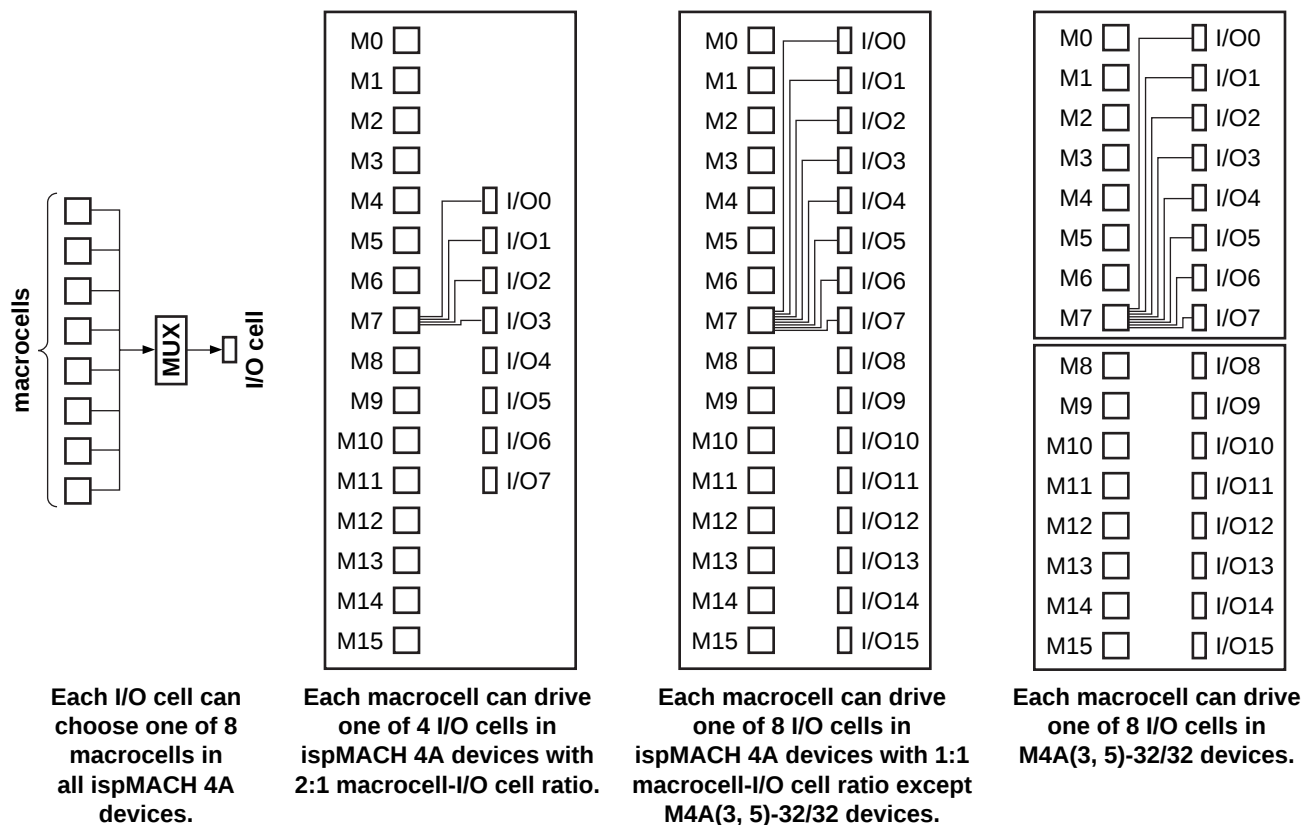


Figure 9. ispMACH 4A Output Switch Matrix

Table 10. Output Switch Matrix Combinations for ispMACH 4A Devices with 2:1 Macrocell-I/O Cell Ratio

Macrocell	Routeable to I/O Cells
M0, M1	I/O0, I/O5, I/O6, I/O7
M2, M3	I/O0, I/O1, I/O6, I/O7
M4, M5	I/O0, I/O1, I/O2, I/O7
M6, M7	I/O0, I/O1, I/O2, I/O3
M8, M9	I/O1, I/O2, I/O3, I/O4
M10, M11	I/O2, I/O3, I/O4, I/O5

Table 10. Output Switch Matrix Combinations for ispMACH 4A Devices with 2:1 Macrocell-I/O Cell Ratio

Macrocell	Routable to I/O Cells
M12, M13	I/O3, I/O4, I/O5, I/O6
M14, M15	I/O4, I/O5, I/O6, I/O7

I/O Cell	Available Macrocells
I/O0	M0, M1, M2, M3, M4, M5, M6, M7
I/O1	M2, M3, M4, M5, M6, M7, M8, M9
I/O2	M4, M5, M6, M7, M8, M9, M10, M11
I/O3	M6, M7, M8, M9, M10, M11, M12, M13
I/O4	M8, M9, M10, M11, M12, M13, M14, M15
I/O5	M0, M1, M10, M11, M12, M13, M14, M15
I/O6	M0, M1, M2, M3, M12, M13, M14, M15
I/O7	M0, M1, M2, M3, M4, M5, M14, M15

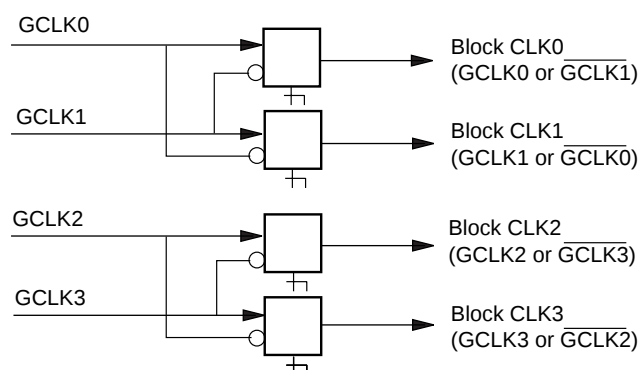
Table 11. Output Switch Matrix Combinations for M4A3-256/160 and M4A3-256/192

Macrocell	Routable to I/O Cells							
M0	I/O0	I/O1	I/O2	I/O3	I/O4	I/O5	I/O6	I/O7
M1	I/O0	I/O1	I/O2	I/O3	I/O4	I/O5	I/O6	I/O7
M2	I/O0	I/O1	I/O2	I/O3	I/O4	I/O5	I/O6	I/O7
M3	I/O0	I/O1	I/O2	I/O3	I/O4	I/O5	I/O6	I/O7
M4	I/O0	I/O1	I/O2	I/O3	I/O4	I/O5	I/O6	I/O7
M5	I/O0	I/O1	I/O2	I/O3	I/O4	I/O5	I/O6	I/O7
M6	I/O0	I/O1	I/O2	I/O3	I/O4	I/O5	I/O6	I/O7
M7	I/O0	I/O1	I/O2	I/O3	I/O4	I/O5	I/O6	I/O7
M8	I/O8	I/O9	I/O10	I/O11	I/O12	I/O13	I/O14	I/O15
M9	I/O8	I/O9	I/O10	I/O11	I/O12	I/O13	I/O14	I/O15
M10	I/O8	I/O9	I/O10	I/O11	I/O12	I/O13	I/O14	I/O15
M11	I/O8	I/O9	I/O10	I/O11	I/O12	I/O13	I/O14	I/O15
M12	I/O8	I/O9	I/O10	I/O11	I/O12	I/O13	I/O14	I/O15
M13	I/O8	I/O9	I/O10	I/O11	I/O12	I/O13	I/O14	I/O15
M14	I/O8	I/O9	I/O10	I/O11	I/O12	I/O13	I/O14	I/O15
M15	I/O8	I/O9	I/O10	I/O11	I/O12	I/O13	I/O14	I/O15

I/O Cell	Available Macrocells							
I/O0	M0	M1	M2	M3	M4	M5	M6	M7
I/O1	M0	M1	M2	M3	M4	M5	M6	M7
I/O2	M0	M1	M2	M3	M4	M5	M6	M7
I/O3	M0	M1	M2	M3	M4	M5	M6	M7
I/O4	M0	M1	M2	M3	M4	M5	M6	M7
I/O5	M0	M1	M2	M3	M4	M5	M6	M7
I/O6	M0	M1	M2	M3	M4	M5	M6	M7
I/O7	M0	M1	M2	M3	M4	M5	M6	M7

PAL Block Clock Generation

Each ispMACH 4A device has four clock pins that can also be used as inputs. These pins drive a clock generator in each PAL block (Figure 14). The clock generator provides four clock signals that can be used anywhere in the PAL block. These four PAL block clock signals can consist of a large number of combinations of the true and complement edges of the global clock signals. Table 14 lists the possible combinations.



17466G-004

Figure 14. PAL Block Clock Generator¹

1. M4A(3,5)-32/32 and M4A(3,5)-64/32 have only two clock pins, GCLK0 and GCLK1. GCLK2 is tied to GCLK0, and GCLK3 is tied to GCLK1.

Table 14. PAL Block Clock Combinations¹

Block CLK0	Block CLK1	Block CLK2	Block CLK3
GCLK0	GCLK1	X	X
$\overline{\text{GCLK1}}$	GCLK1	X	X
GCLK0	$\overline{\text{GCLK0}}$	X	X
$\overline{\text{GCLK1}}$	$\overline{\text{GCLK0}}$	X	X
X	X	GCLK2 (GCLK0)	GCLK3 (GCLK1)
X	X	$\overline{\text{GCLK3}}$ ($\overline{\text{GCLK1}}$)	GCLK3 (GCLK1)
X	X	GCLK2 (GCLK0)	$\overline{\text{GCLK2}}$ ($\overline{\text{GCLK0}}$)
X	X	$\overline{\text{GCLK3}}$ (GCLK1)	$\overline{\text{GCLK2}}$ ($\overline{\text{GCLK0}}$)

Note:

1. Values in parentheses are for the M4A(3,5)-32/32 and M4A(3,5)-64/32.

This feature provides high flexibility for partitioning state machines and dual-phase clocks. It also allows latches to be driven with either polarity of latch enable, and in a master-slave configuration.

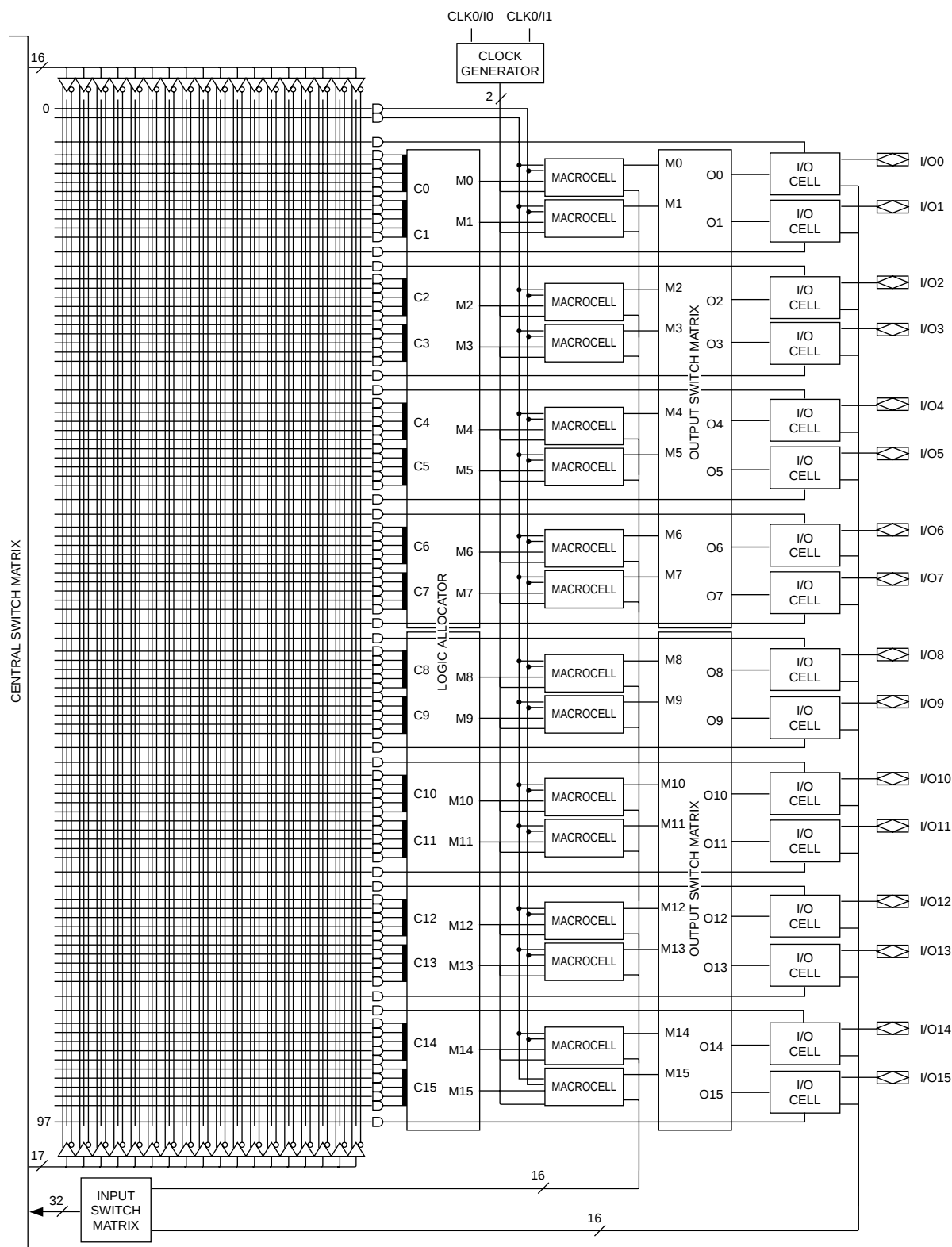
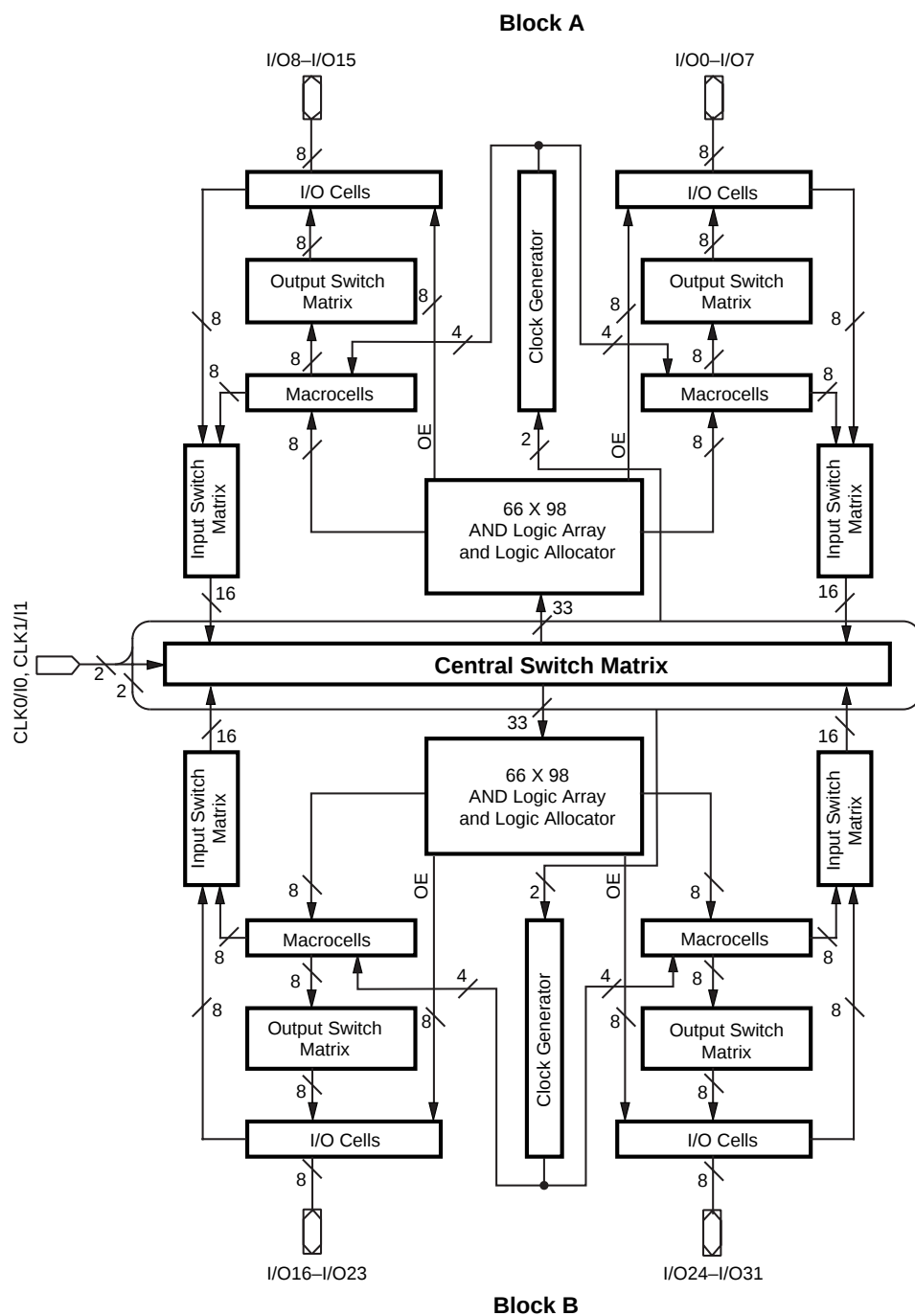


Figure 18. PAL Block for M4A (3,5)-32/32

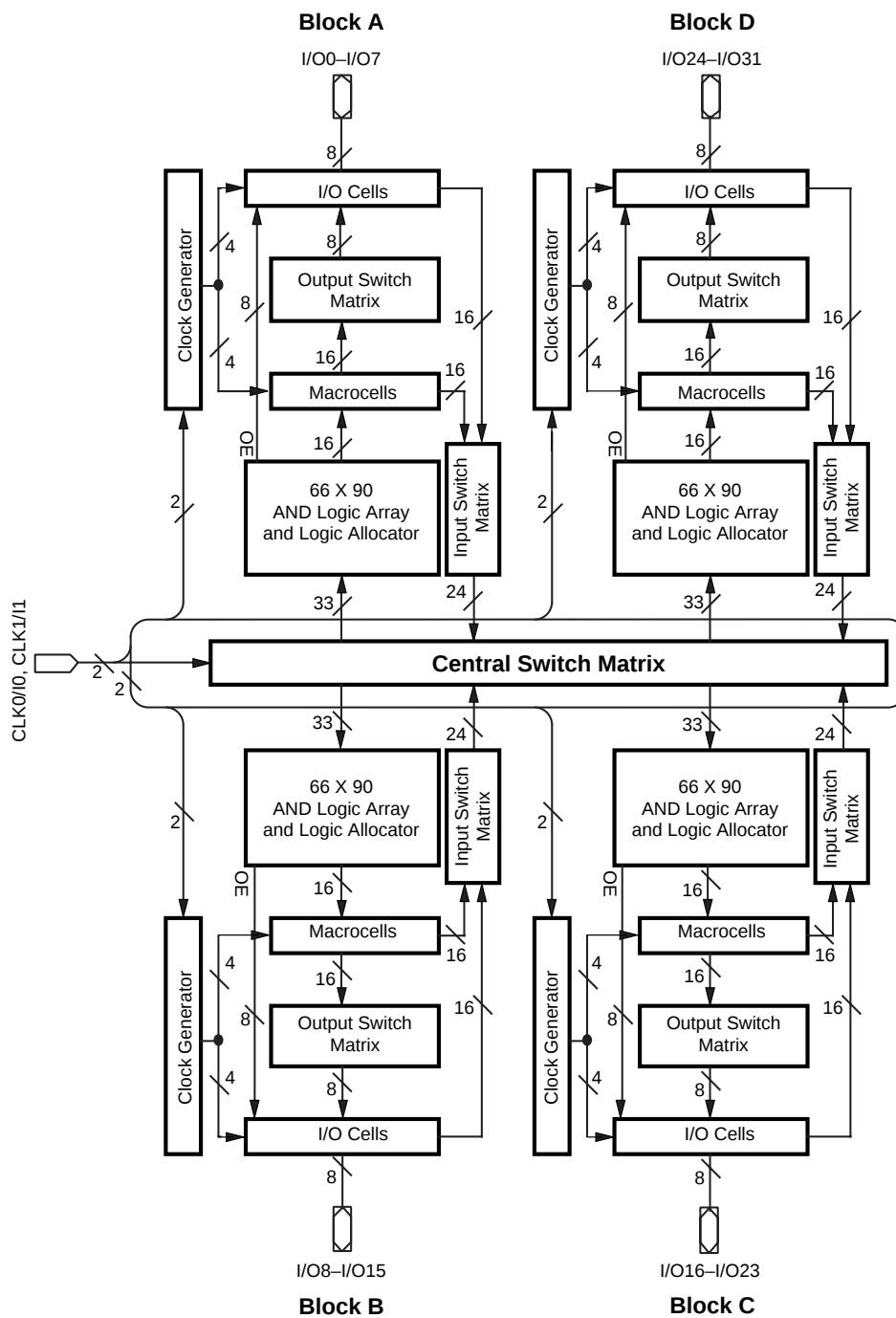
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BLOCK DIAGRAM – M4A(3,5)-32/32



17466H-019

BLOCK DIAGRAM – M4A(3,5)-64/32



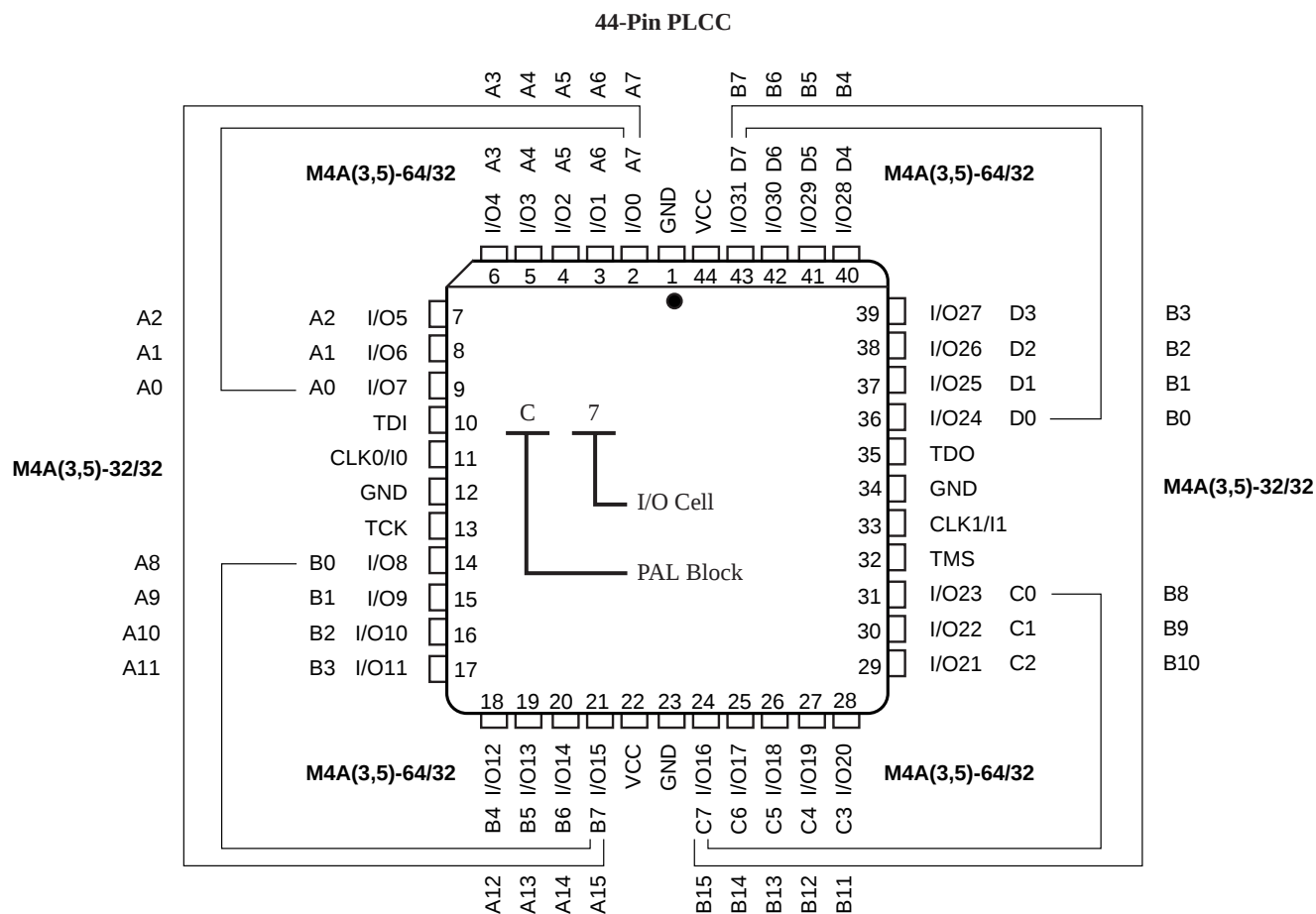
17466H-020

ispMACH 4A TIMING PARAMETERS OVER OPERATING RANGES¹

		-5		-55		-6		-65		-7		-10		-12		-14		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Combinatorial Delay:																		
t _{PDi}	Internal combinatorial propagation delay		3.5		4.0		4.3		4.5		5.0		7.0		9.0		11.0	ns
t _{PD}	Combinatorial propagation delay		5.0		5.5		6.0		6.5		7.5		10.0		12.0		14.0	ns
Registered Delays:																		
t _{SS}	Synchronous clock setup time, D-type register	3.0		3.5		3.5		3.5		5.0		5.5		7.0		10.0		ns
t _{SST}	Synchronous clock setup time, T-type register	4.0		4.0		4.0		4.0		6.0		6.5		8.0		11.0		ns
t _{SA}	Asynchronous clock setup time, D-type register	2.5		2.5		2.5		3.0		3.5		4.0		5.0		8.0		ns
t _{SAT}	Asynchronous clock setup time, T-type register	3.0		3.0		3.0		3.5		4.5		5.0		6.0		9.0		ns
t _{HS}	Synchronous clock hold time	0.0		0.0		0.0		0.0		0.0		0.0		0.0		0.0		ns
t _{HA}	Asynchronous clock hold time	2.5		2.5		2.5		3.0		3.5		4.0		5.0		8.0		ns
t _{COsi}	Synchronous clock to internal output		2.5		2.5		2.8		3.0		3.0		3.0		3.5		3.5	ns
t _{COS}	Synchronous clock to output		4.0		4.0		4.5		5.0		5.5		6.0		6.5		6.5	ns
t _{COAi}	Asynchronous clock to internal output		5.0		5.0		5.0		5.0		6.0		8.0		10.0		12.0	ns
t _{COA}	Asynchronous clock to output		6.5		6.5		6.8		7.0		8.5		11.0		13.0		15.0	ns
Latched Delays:																		
t _{SSL}	Synchronous latch setup time	4.0		4.0		4.0		4.5		6.0		7.0		8.0		10.0		ns
t _{SAL}	Asynchronous latch setup time	3.0		3.0		3.5		3.5		4.0		4.0		5.0		8.0		ns
t _{HSL}	Synchronous latch hold time	0.0		0.0		0.0		0.0		0.0		0.0		0.0		0.0		ns
t _{HAL}	Asynchronous latch hold time	3.0		3.0		3.5		3.5		4.0		4.0		5.0		8.0		ns
t _{PDLi}	Transparent latch to internal output		5.5		5.5		5.8		6.0		7.5		9.0		11.0		12.0	ns
t _{PDL}	Propagation delay through transparent latch to output		7.0		7.0		7.5		8.0		10.0		12.0		14.0		15.0	ns
t _{GOSi}	Synchronous gate to internal output		3.0		3.0		3.0		3.0		3.5		4.5		7.0		8.0	ns
t _{GOS}	Synchronous gate to output		4.5		4.5		4.8		5.0		6.0		7.5		10.0		11.0	ns
t _{GOAi}	Asynchronous gate to internal output		6.0		6.0		6.0		6.0		8.5		10.0		13.0		15.0	ns
t _{GOA}	Asynchronous gate to output		7.5		7.5		7.8		8.0		11.0		13.0		16.0		18.0	ns
Input Register Delays:																		
t _{SIRS}	Input register setup time	1.5		1.5		2.0		2.0		2.0		2.0		2.0		2.0		ns
t _{HIRS}	Input register hold time	2.5		2.5		3.0		3.0		3.0		3.0		3.0		4.0		ns
t _{ICOSi}	Input register clock to internal feedback		3.0		3.0		3.0		3.0		3.5		4.5		6.0		6.0	ns
Input Latch Delays:																		
t _{SIL}	Input latch setup time	1.5		1.5		1.5		2.0		2.0		2.0		2.0		2.0		ns
t _{HIL}	Input latch hold time	2.5		2.5		2.5		3.0		3.0		3.0		3.0		4.0		ns
t _{IGOSi}	Input latch gate to internal feedback		3.5		3.5		3.8		4.0		4.0		4.0		4.0		5.0	ns
t _{PDILi}	Transparent input latch to internal feedback		1.5		1.5		1.5		1.5		2.0		2.0		2.0		2.0	ns

44-PIN PLCC CONNECTION DIAGRAM (M4A(3,5)-32/32 AND M4A(3,5)-64/32)

Top View



17466G-026

PIN DESIGNATIONS

CLK/I = Clock or Input

GND = Ground

I/O = Input/Output

V_{CC} = Supply Voltage

TDI = Test Data In

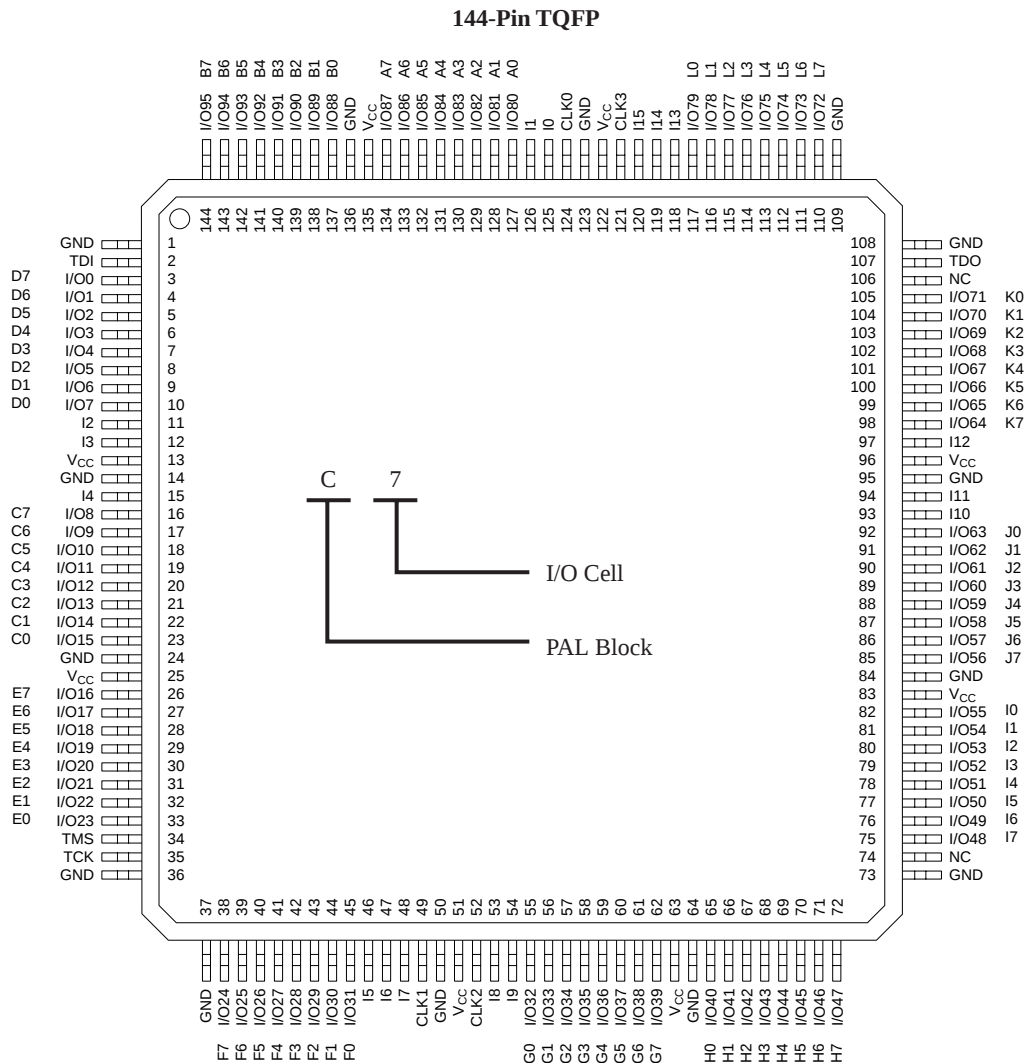
TCK = Test Clock

TMS = Test Mode Select

TDO = Test Data Out

144-PIN TQFP CONNECTION DIAGRAM (M4A(3,5)-192/96)

Top View



17466G-033

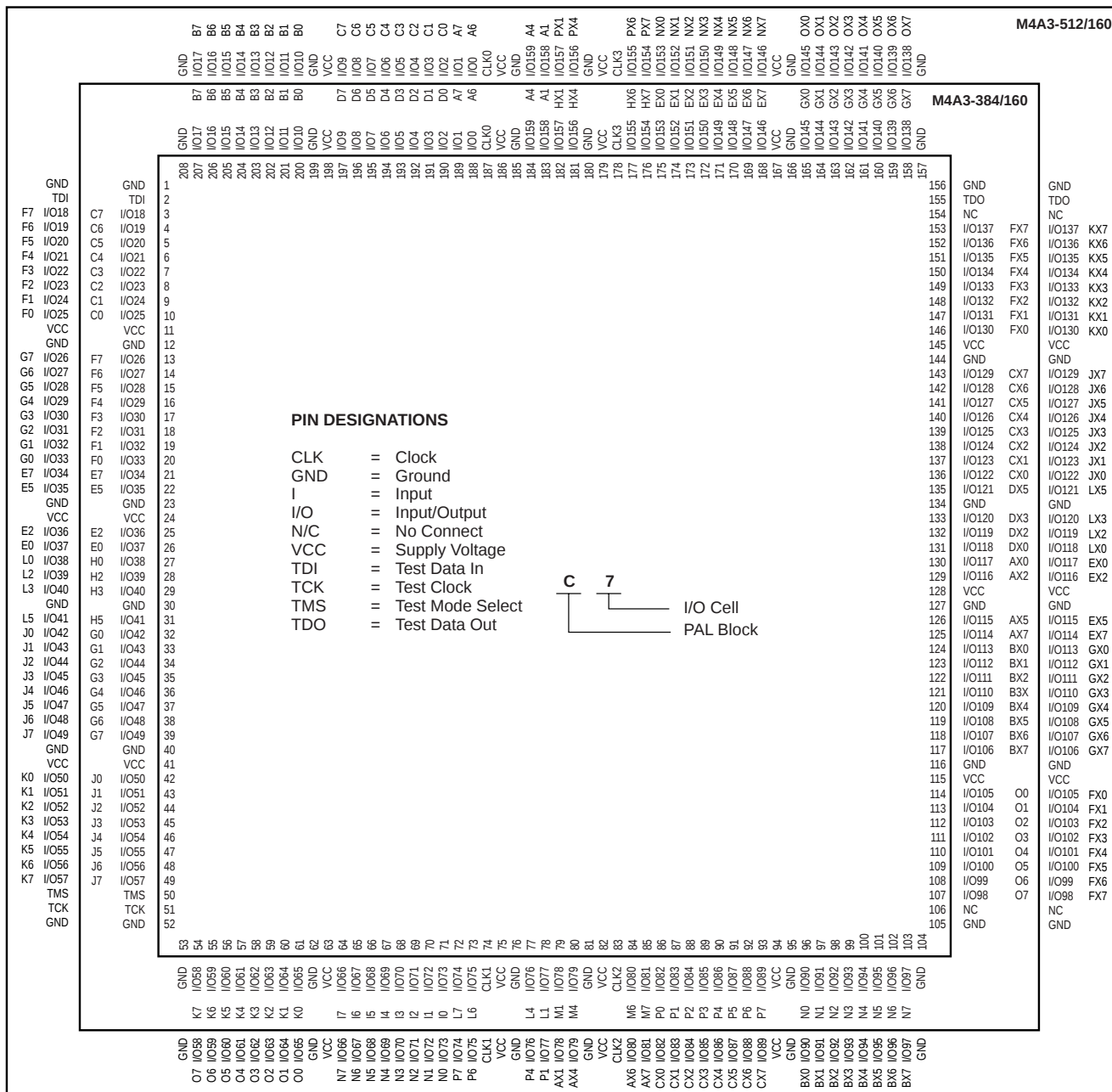
PIN DESIGNATIONS

- CLK = Clock
- GND = Ground
- I = Input
- I/O = Input/Output
- V_{CC} = Supply Voltage
- TDI = Test Data In
- TCK = Test Clock
- TMS = Test Mode Select
- TDO = Test Data Out

208-PIN PQFP CONNECTION DIAGRAM (M4A3-384/160 AND M4A3-512/160)

Top View

208-Pin PQFP



17466Ga-044

ispMACH 4A PRODUCT ORDERING INFORMATION

ispMACH 4A Devices Commercial and Industrial - 3.3V and 5V

Lattice programmable logic products are available with several ordering options. The order number (Valid Combination) is formed by a combination of:

M4A3- 256 / 128 -7 Y C		L48	
FAMILY TYPE		= 48-pin TQFP for M4A3-32/32 or M4A3-64/32 M4A5-32/32 or M4A5-64/32	
M4A3- = ispMACH 4A Family Low Voltage Advanced Feature (3.3-V V_{CC})		OPERATING CONDITIONS	
M4A5- = ispMACH 4A Family Advanced Feature (5-V V_{CC})		C = Commercial (0°C to +70°C)	
MACROCELL DENSITY		I = Industrial (-40°C to +85°C)	
32 = 32 Macrocells 192 = 192 Macrocells		PACKAGE TYPE	
64 = 64 Macrocells 256 = 256 Macrocells		SA = Ball Grid Array (BGA)	
96 = 96 Macrocells 384 = 384 Macrocells		J = Plastic Leaded Chip Carrier (PLCC)	
128 = 128 Macrocells 512 = 512 Macrocells		JN = Lead-free Plastic Leaded Chip Carrier (PLCC)	
I/Os		V = Thin Quad Flat Pack (TQFP)	
/32 = 32 I/Os in 44-pin PLCC, 44-pin TQFP or 48-pin TQFP		VN = Lead-free Thin Quad Flat Pack (TQFP)	
/48 = 48 I/Os in 100-pin TQFP		Y = Plastic Quad Flat Pack (PQFP)	
/64 = 64 I/Os in 100-pin TQFP, 100-pin PQFP, or 100-ball caBGA		YN = Lead-free Plastic Quad Flat Pack (PQFP)	
/96 = 96 I/Os in 144-pin TQFP or 144-ball fpBGA		FA = Fine-pitch Ball Grid Array (fpBGA)	
/128 = 128 I/Os in 208-pin PQFP, 256-ball BGA or 256-ball fpBGA		FAN = Lead-free Fine-pitch Ball Grid Array (fpBGA)	
/160 = 160 I/Os in 208-pin PQFP		CA = Chip-array Ball Grid Array (caBGA)	
/192 = 192 I/Os in 256-ball BGA or 256-ball fpBGA		SPEED	
/256 = 256 I/Os in 388-ball fpBGA		-5 = 5.0 ns t_{PD}	
		-55 = 5.5 ns t_{PD}	
		-6 = 6.0 ns t_{PD}	
		-65 = 6.5 ns t_{PD}	
		-7 = 7.5 ns t_{PD}	
		-10 = 10 ns t_{PD}	
		-12 = 12 ns t_{PD}	
		-14 = 14 ns t_{PD}	

*Package obsolete, contact factory.

Conventional Packaging

3.3V Commercial Combinations			3.3V Industrial Combinations		
M4A3-32/32	-5, -7, -10	JC, VC, VC48	M4A3-32/32	-7, -10, -12	JI, VI, VI48
M4A3-64/32	-55, -7, -10	JC, VC, VC48	M4A3-64/32		JI, VI, VI48
M4A3-64/64		VC	M4A3-64/64		VI
M4A3-96/48		VC	M4A3-96/48		VI
M4A3-128/64		YC, VC, CAC	M4A3-128/64		YI, VI, CAI
M4A3-192/96	-6, -7, -10	VC, FAC	M4A3-192/96		VI, FAI
M4A3-256/128	-55, -65 ¹ , -7, -10	YC, FAC, SAC	M4A3-256/128	-10, -12	YI, FAI, SAI
M4A3-256/160	-7, -10	YC	M4A3-256/160		YI
M4A3-256/192		FAC	M4A3-256/192	-10, -12, -14	FAI
M4A3-384/160	-65, -10, -12	YC	M4A3-384/160		YI
M4A3-384/192		SAC, FAC	M4A3-384/192		FAI
M4A3-512/160	-7, -10, -12	YC	M4A3-512/160		YI
M4A3-512/192		FAC	M4A3-512/192		FAI
M4A3-512/256		FAC	M4A3-512/256		FAI

1. Use 5.5ns for new designs.

Revision History

Date	Version	Change Summary
-	K	Previous Lattice release.
August 2006	L	Updated for lead-free package options.
September 2006	M	Revised M4A3-256/160 208-pin PQFP connection diagram.