



Welcome to [E-XFL.COM](http://E-XFL.COM)

### **Understanding Embedded - CPLDs (Complex Programmable Logic Devices)**

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

### **Applications of Embedded - CPLDs**

#### **Details**

Product Status	Not For New Designs
Programmable Type	In System Programmable
Delay Time tpd(1) Max	5 ns
Voltage Supply - Internal	3V ~ 3.6V
Number of Logic Elements/Blocks	-
Number of Macrocells	32
Number of Gates	-
Number of I/O	32
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/lattice-semiconductor/m4a3-32-32-5vnc">https://www.e-xfl.com/product-detail/lattice-semiconductor/m4a3-32-32-5vnc</a>

**Table 1. ispMACH 4A Device Features**

<b>3.3 V Devices</b>								
<b>Feature</b>	<b>M4A3-32</b>	<b>M4A3-64</b>	<b>M4A3-96</b>	<b>M4A3-128</b>	<b>M4A3-192</b>	<b>M4A3-256</b>	<b>M4A3-384</b>	<b>M4A3-512</b>
Macrocells	32	64	96	128	192	256	384	512
User I/O options	32	32/64	48	64	96	128/160/192	160/192	160/192/256
$t_{PD}$ (ns)	5.0	5.5	5.5	5.5	6.0	5.5	6.5	7.5
$f_{CNT}$ (MHz)	182	167	167	167	160	167	154	125
$t_{COS}$ (ns)	4.0	4.0	4.0	4.0	4.5	4.0	4.5	5.5
$t_{SS}$ (ns)	3.0	3.5	3.5	3.5	3.5	3.5	3.5	5.0
Static Power (mA)	20	25/52	40	55	85	110/150	149/155	179
JTAG Compliant	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
PCI Compliant	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes

<b>5 V Devices</b>						
<b>Feature</b>	<b>M4A5-32</b>	<b>M4A5-64</b>	<b>M4A5-96</b>	<b>M4A5-128</b>	<b>M4A5-192</b>	<b>M4A5-256</b>
Macrocells	32	64	96	128	192	256
User I/O options	32	32	48	64	96	128
$t_{PD}$ (ns)	5.0	5.5	5.5	5.5	6.0	6.5
$f_{CNT}$ (MHz)	182	167	167	167	160	154
$t_{COS}$ (ns)	4.0	4.0	4.0	4.0	4.5	5.0
$t_{SS}$ (ns)	3.0	3.5	3.5	3.5	3.5	3.5
Static Power (mA)	20	25	40	55	74	110
JTAG Compliant	Yes	Yes	Yes	Yes	Yes	Yes
PCI Compliant	Yes	Yes	Yes	Yes	Yes	Yes

**Table 4. Architectural Summary of ispMACH 4A devices**

	ispMACH 4A Devices	
		M4A3-64/32, M4A5-64/32 M4A3-96/48, M4A5-96/48 M4A3-128/64, M4A5-128/64 M4A3-192/96, M4A5-192/96 M4A3-256/128, M4A5-256/128 M4A3-384 M4A3-512
Macrocell-I/O Cell Ratio	2:1	1:1
Input Switch Matrix	Yes	Yes <sup>1</sup>
Input Registers	Yes	No
Central Switch Matrix	Yes	Yes
Output Switch Matrix	Yes	Yes

The Macrocell-I/O cell ratio is defined as the number of macrocells versus the number of I/O cells internally in a PAL block (Table 4).

The central switch matrix takes all dedicated inputs and signals from the input switch matrices and routes them as needed to the PAL blocks. Feedback signals that return to the same PAL block still must go through the central switch matrix. This mechanism ensures that PAL blocks in ispMACH 4A devices communicate with each other with consistent, predictable delays.

The central switch matrix makes a ispMACH 4A device more advanced than simply several PAL devices on a single chip. It allows the designer to think of the device not as a collection of blocks, but as a single programmable device; the software partitions the design into PAL blocks through the central switch matrix so that the designer does not have to be concerned with the internal architecture of the device.

Each PAL block consists of:

- ◆ Product-term array
- ◆ Logic allocator
- ◆ Macrocells
- ◆ Output switch matrix
- ◆ I/O cells
- ◆ Input switch matrix
- ◆ Clock generator

**Notes:**

1. M4A3-64/64 internal switch matrix functionality embedded in central switch matrix.

## Product-Term Array

The product-term array consists of a number of product terms that form the basis of the logic being implemented. The inputs to the AND gates come from the central switch matrix (Table 5), and are provided in both true and complement forms for efficient logic implementation.

**Table 5. PAL Block Inputs**

Device	Number of Inputs to PAL Block
M4A3-32/32 and M4A5-32/32	33
M4A3-64/32 and M4A5-64/32	33
M4A3-64/64	33
M4A3-96/48 and M4A5-96/48	33
M4A3-128/64 and M4A5-128/64	33
M4A3-192/96 and M4A5-192/96	34
M4A3-256/128 and M4A5-256/128	34
M4A3-256/160 and M4A3-256/192	36
M4A3-384	36
M4A3-512	36

## Logic Allocator

Within the logic allocator, product terms are allocated to macrocells in “product term clusters.” The availability and distribution of product term clusters are automatically considered by the software as it fits functions within a PAL block. The size of a product term cluster has been optimized to provide high utilization of product terms, making complex functions using many product terms possible. Yet when few product terms are used, there will be a minimal number of unused—or wasted—product terms left over. The product term clusters available to each macrocell within a PAL block are shown in Tables 6 and 7.

Each product term cluster is associated with a macrocell. The size of a cluster depends on the configuration of the associated macrocell. When the macrocell is used in synchronous mode (Figure 2a), the basic cluster has 4 product terms. When the associated macrocell is used in asynchronous mode (Figure 2b), the cluster has 2 product terms. Note that if the product term cluster is routed to a different macrocell, the allocator configuration is not determined by the mode of the macrocell actually being driven. The configuration is always set by the mode of the macrocell that the cluster will drive if not routed away, regardless of the actual routing.

In addition, there is an extra product term that can either join the basic cluster to give an extended cluster, or drive the second input of an exclusive-OR gate in the signal path. If included with the basic cluster, this provides for up to 20 product terms on a synchronous function that uses four extended 5-product-term clusters. A similar asynchronous function can have up to 18 product terms.

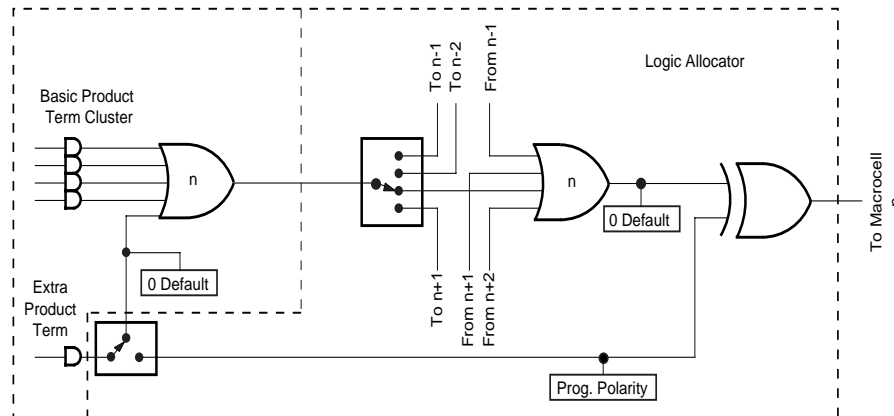
When the extra product term is used to extend the cluster, the value of the second XOR input can be programmed as a 0 or a 1, giving polarity control. The possible configurations of the logic allocator are shown in Figures 3 and 4.

**Table 6. Logic Allocator for All ispMACH 4A Devices (except M4A(3,5)-32/32)**

Output Macrocell	Available Clusters	Output Macrocell	Available Clusters
M <sub>0</sub>	C <sub>0</sub> , C <sub>1</sub> , C <sub>2</sub>	M <sub>8</sub>	C <sub>7</sub> , C <sub>8</sub> , C <sub>9</sub> , C <sub>10</sub>
M <sub>1</sub>	C <sub>0</sub> , C <sub>1</sub> , C <sub>2</sub> , C <sub>3</sub>	M <sub>9</sub>	C <sub>8</sub> , C <sub>9</sub> , C <sub>10</sub> , C <sub>11</sub>
M <sub>2</sub>	C <sub>1</sub> , C <sub>2</sub> , C <sub>3</sub> , C <sub>4</sub>	M <sub>10</sub>	C <sub>9</sub> , C <sub>10</sub> , C <sub>11</sub> , C <sub>12</sub>
M <sub>3</sub>	C <sub>2</sub> , C <sub>3</sub> , C <sub>4</sub> , C <sub>5</sub>	M <sub>11</sub>	C <sub>10</sub> , C <sub>11</sub> , C <sub>12</sub> , C <sub>13</sub>
M <sub>4</sub>	C <sub>3</sub> , C <sub>4</sub> , C <sub>5</sub> , C <sub>6</sub>	M <sub>12</sub>	C <sub>11</sub> , C <sub>12</sub> , C <sub>13</sub> , C <sub>14</sub>
M <sub>5</sub>	C <sub>4</sub> , C <sub>5</sub> , C <sub>6</sub> , C <sub>7</sub>	M <sub>13</sub>	C <sub>12</sub> , C <sub>13</sub> , C <sub>14</sub> , C <sub>15</sub>
M <sub>6</sub>	C <sub>5</sub> , C <sub>6</sub> , C <sub>7</sub> , C <sub>8</sub>	M <sub>14</sub>	C <sub>13</sub> , C <sub>14</sub> , C <sub>15</sub>
M <sub>7</sub>	C <sub>6</sub> , C <sub>7</sub> , C <sub>8</sub> , C <sub>9</sub>	M <sub>15</sub>	C <sub>14</sub> , C <sub>15</sub>

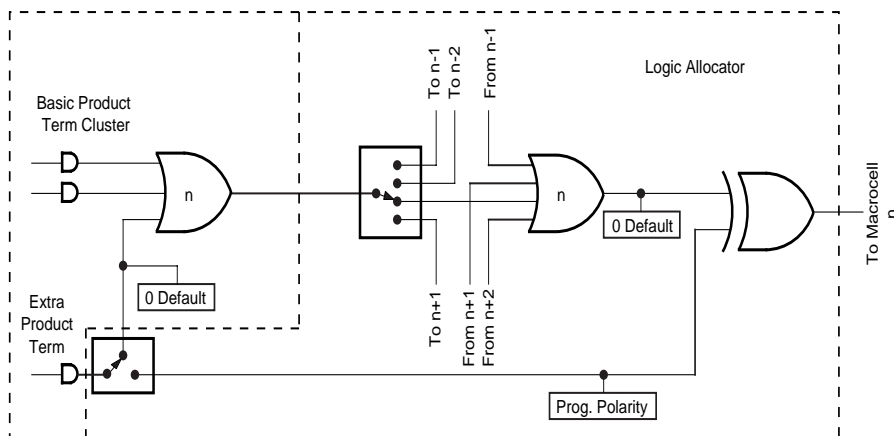
**Table 7. Logic Allocator for M4A(3,5)-32/32**

Output Macrocell	Available Clusters	Output Macrocell	Available Clusters
M <sub>0</sub>	C <sub>0</sub> , C <sub>1</sub> , C <sub>2</sub>	M <sub>8</sub>	C <sub>8</sub> , C <sub>9</sub> , C <sub>10</sub>
M <sub>1</sub>	C <sub>0</sub> , C <sub>1</sub> , C <sub>2</sub> , C <sub>3</sub>	M <sub>9</sub>	C <sub>8</sub> , C <sub>9</sub> , C <sub>10</sub> , C <sub>11</sub>
M <sub>2</sub>	C <sub>1</sub> , C <sub>2</sub> , C <sub>3</sub> , C <sub>4</sub>	M <sub>10</sub>	C <sub>9</sub> , C <sub>10</sub> , C <sub>11</sub> , C <sub>12</sub>
M <sub>3</sub>	C <sub>2</sub> , C <sub>3</sub> , C <sub>4</sub> , C <sub>5</sub>	M <sub>11</sub>	C <sub>10</sub> , C <sub>11</sub> , C <sub>12</sub> , C <sub>13</sub>
M <sub>4</sub>	C <sub>3</sub> , C <sub>4</sub> , C <sub>5</sub> , C <sub>6</sub>	M <sub>12</sub>	C <sub>11</sub> , C <sub>12</sub> , C <sub>13</sub> , C <sub>14</sub>
M <sub>5</sub>	C <sub>4</sub> , C <sub>5</sub> , C <sub>6</sub> , C <sub>7</sub>	M <sub>13</sub>	C <sub>12</sub> , C <sub>13</sub> , C <sub>14</sub> , C <sub>15</sub>
M <sub>6</sub>	C <sub>5</sub> , C <sub>6</sub> , C <sub>7</sub>	M <sub>14</sub>	C <sub>13</sub> , C <sub>14</sub> , C <sub>15</sub>
M <sub>7</sub>	C <sub>6</sub> , C <sub>7</sub>	M <sub>15</sub>	C <sub>14</sub> , C <sub>15</sub>



**a. Synchronous Mode**

17466G-005



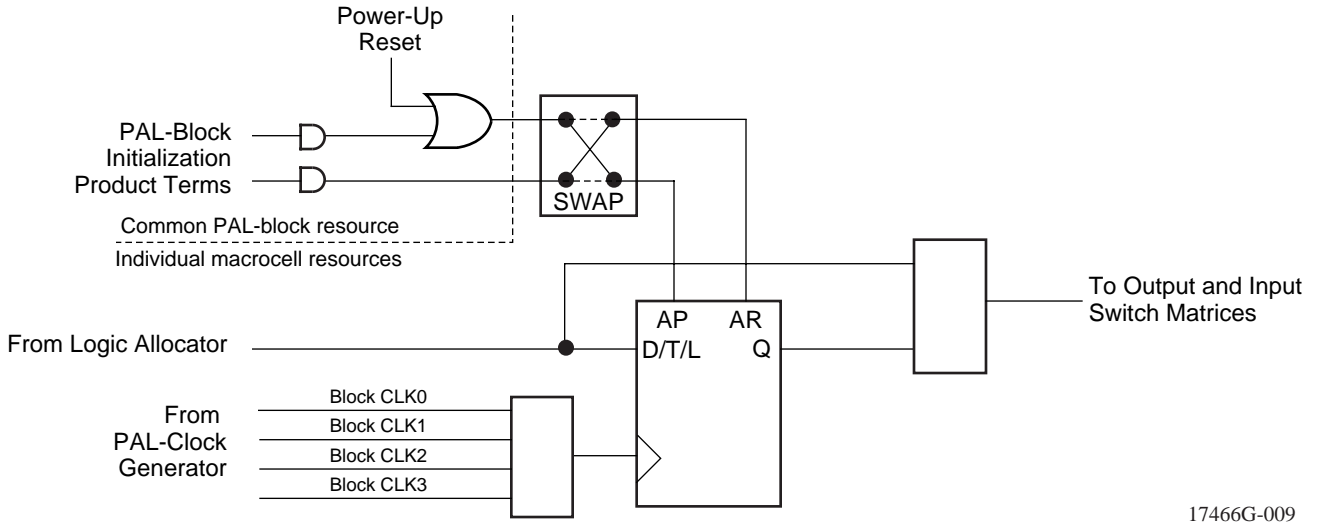
**b. Asynchronous Mode**

17466G-006

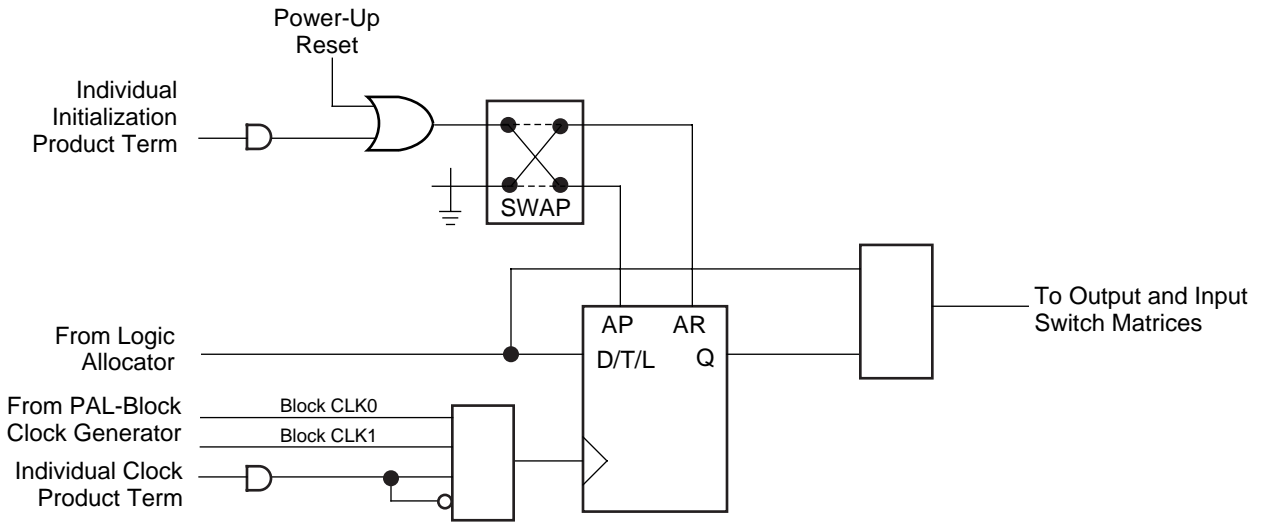
**Figure 2. Logic Allocator: Configuration of Cluster “n” Set by Mode of Macrocell “n”**

## Macrocell

The macrocell consists of a storage element, routing resources, a clock multiplexer, and initialization control. The macrocell has two fundamental modes: synchronous and asynchronous (Figure 5). The mode chosen only affects clocking and initialization in the macrocell.



**a. Synchronous mode**



**b. Asynchronous mode**

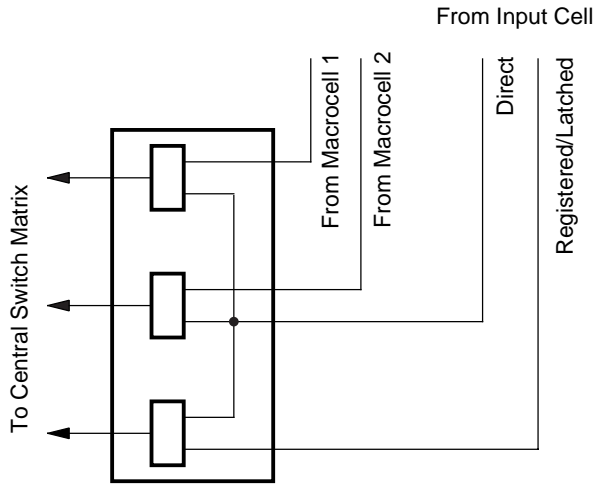
17466G-010

**Figure 5. Macrocell**

In either mode, a combinatorial path can be used. For combinatorial logic, the synchronous mode will generally be used, since it provides more product terms in the allocator.

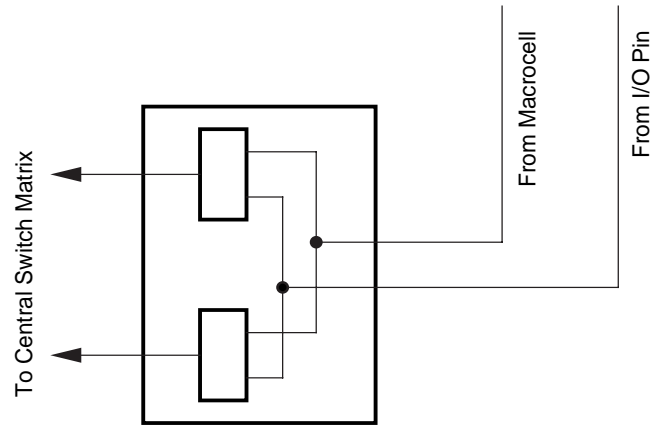
## Input Switch Matrix

The input switch matrix (Figures 12 and 13) optimizes routing of inputs to the central switch matrix. Without the input switch matrix, each input and feedback signal has only one way to enter the central switch matrix. The input switch matrix provides additional ways for these signals to enter the central switch matrix.



17466G-002

Figure 12. ispMACH 4A with 2:1 Macrocell-I/O Cell Ratio - Input Switch Matrix



17466G-003

Figure 13. ispMACH 4A with 1:1 Macrocell-I/O Cell Ratio - Input Switch Matrix



17466H-41

Figure 17. PAL Block for ispMACH 4A Devices with 1:1 Macrocell-I/O Cell Ratio (except M4A (3,5)-32/32)

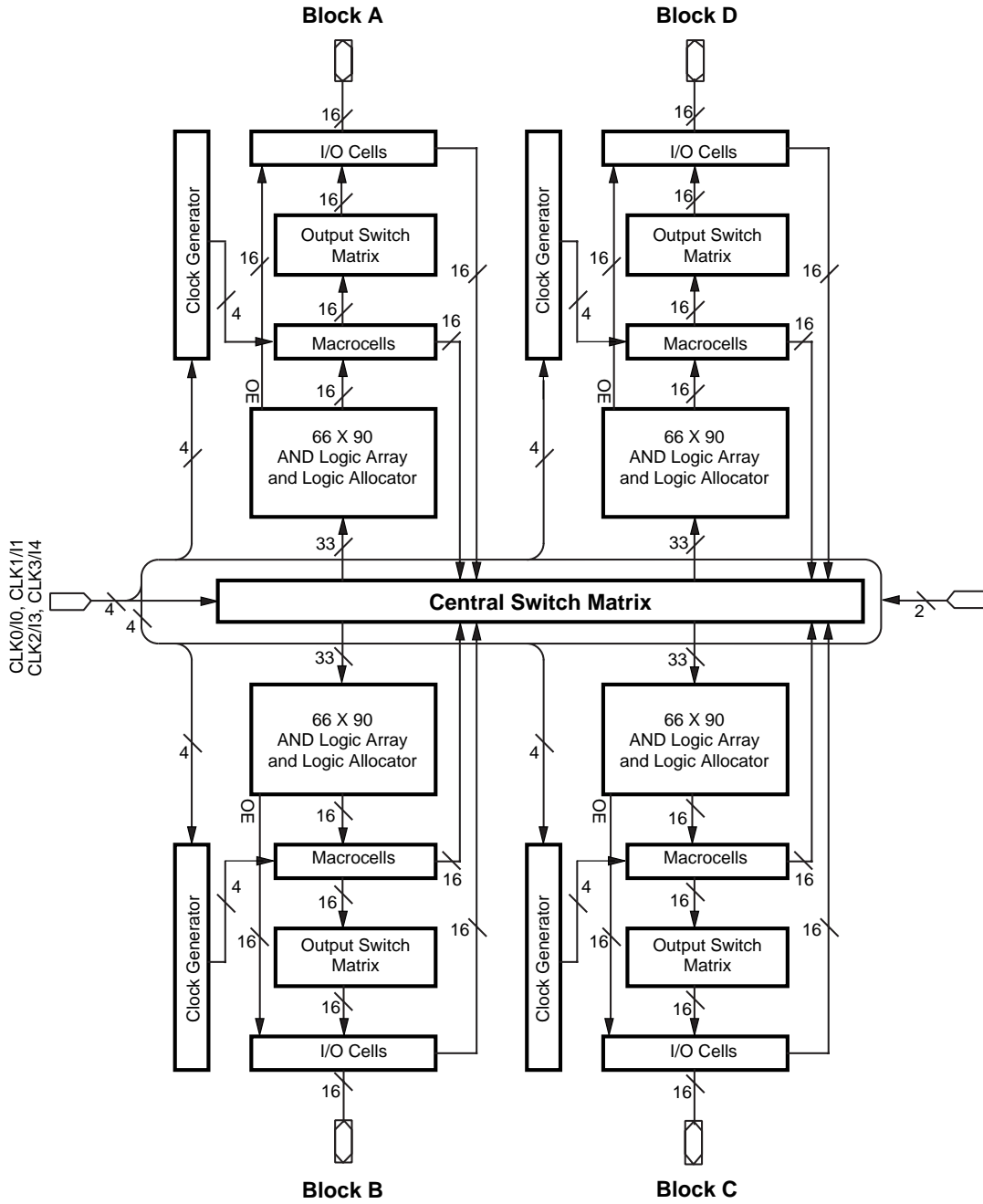




Figure 18. PAL Block for M4A (3,5)-32/32

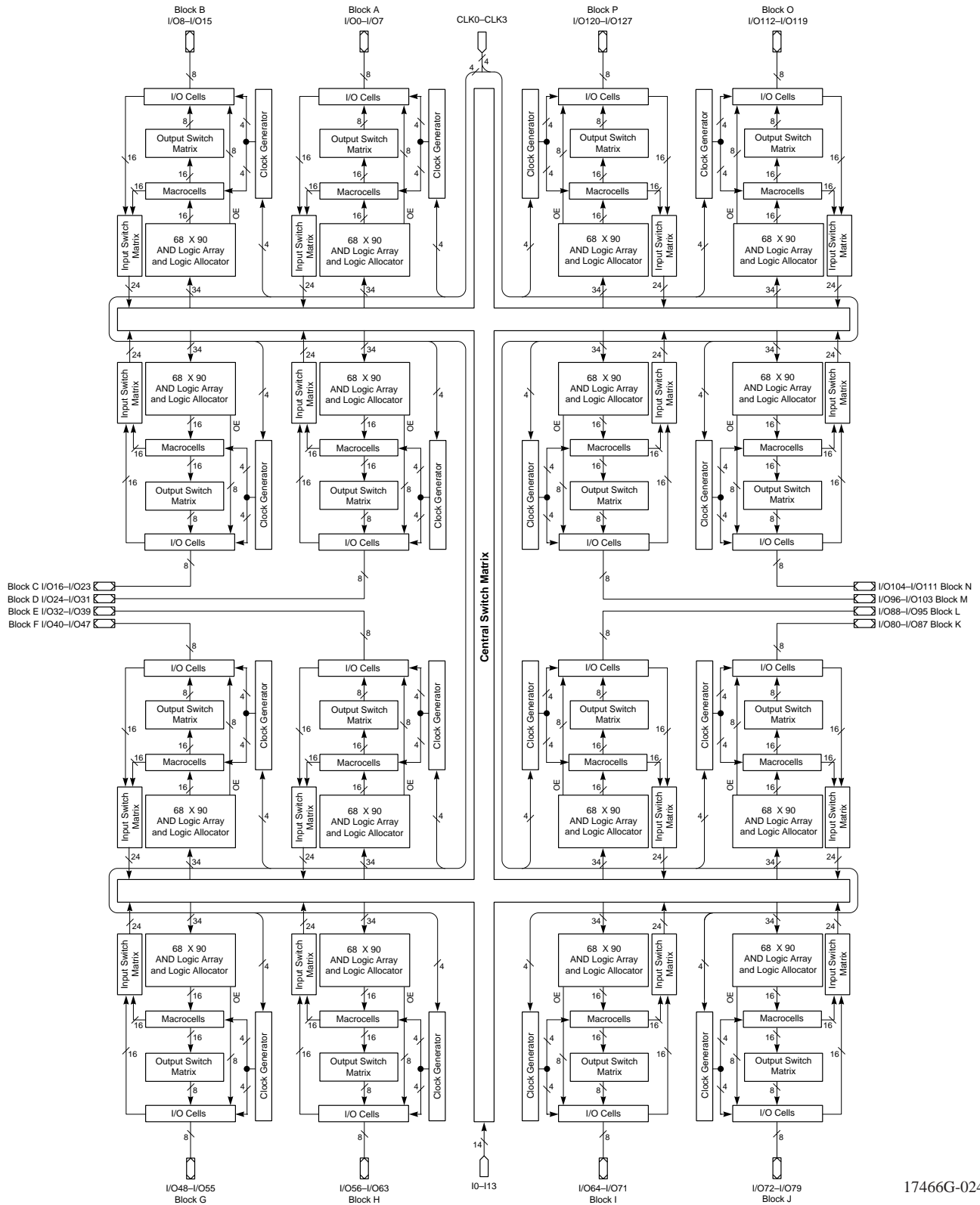
17466H-042

## BLOCK DIAGRAM – M4A3-64/64



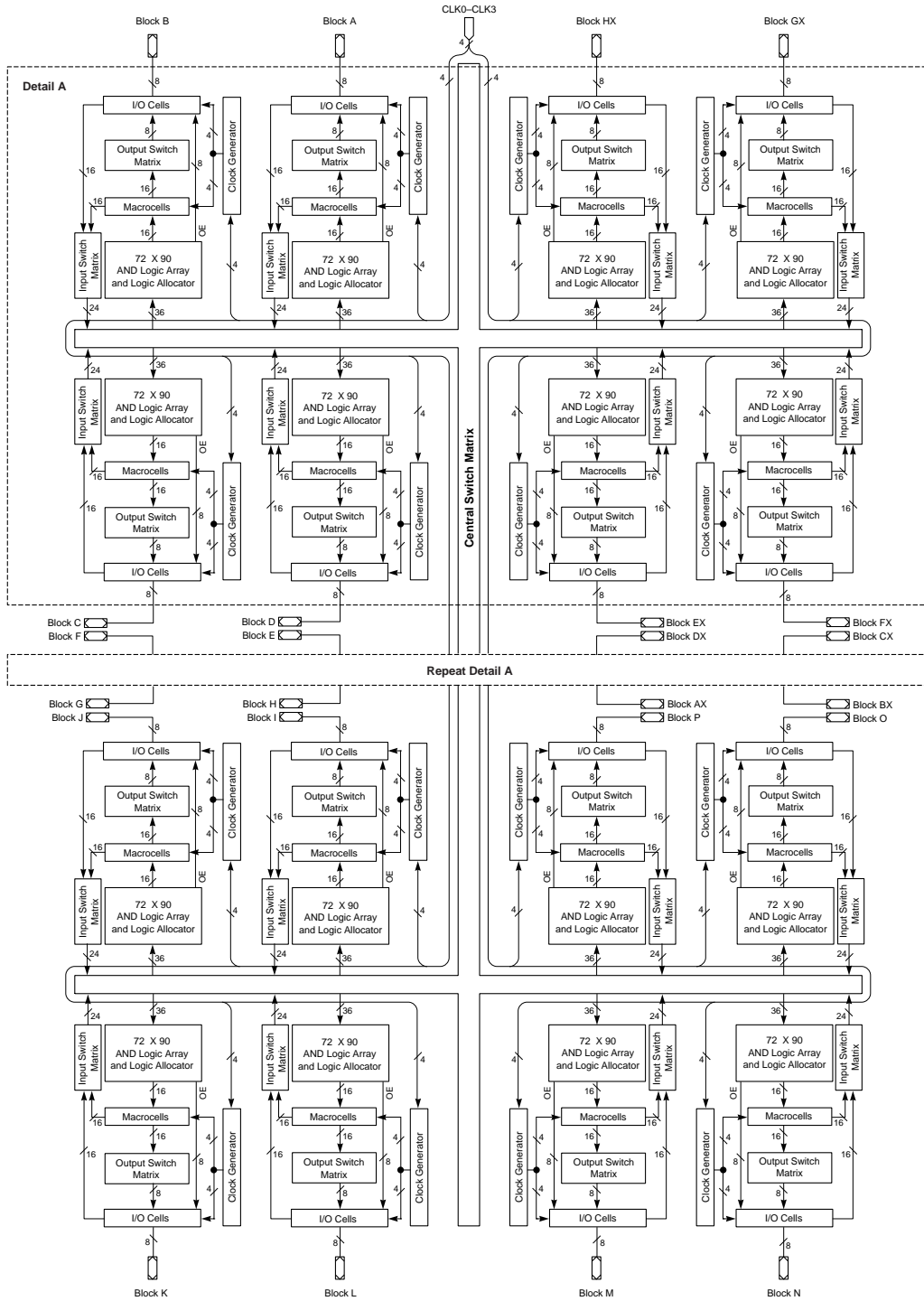
17466H-020A

# BLOCK DIAGRAM – M4A(3,5)-256/128



17466G-024

# BLOCK DIAGRAM – M4A3-384/160, M4A3-384/192



## ABSOLUTE MAXIMUM RATINGS

### M4A5

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-55°C to +100°C
Device Junction Temperature	+130°C
Supply Voltage with Respect to Ground	-0.5 V to +7.0 V
DC Input Voltage	-0.5 V to $V_{CC} + 0.5$ V
Static Discharge Voltage	2000 V
Latchup Current ( $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ )	200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

## OPERATING RANGES

### Commercial (C) Devices

Ambient Temperature ( $T_A$ ) Operating in Free Air	0°C to +70°C
Supply Voltage ( $V_{CC}$ ) with Respect to Ground	+4.75 V to +5.25 V

### Industrial (I) Devices

Ambient Temperature ( $T_A$ ) Operating in Free Air	-40°C to +85°C
Supply Voltage ( $V_{CC}$ ) with Respect to Ground	+4.50 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

## 5-V DC CHARACTERISTICS OVER OPERATING RANGES

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
$V_{OH}$	Output HIGH Voltage	$I_{OH} = -3.2$ mA, $V_{CC} = \text{Min}$ , $V_{IN} = V_{IH}$ or $V_{IL}$	2.4			V
		$I_{OH} = -100$ $\mu\text{A}$ , $V_{CC} = \text{Max}$ , $V_{IN} = V_{IH}$ or $V_{IL}$		3.3	3.6	V
$V_{OL}$	Output LOW Voltage	$I_{OL} = 24$ mA, $V_{CC} = \text{Min}$ , $V_{IN} = V_{IH}$ or $V_{IL}$ (Note 1)			0.5	V
$V_{IH}$	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 2)	2.0			V
$V_{IL}$	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 2)			0.8	V
$I_{IH}$	Input HIGH Leakage Current	$V_{IN} = 5.25$ V, $V_{CC} = \text{Max}$ (Note 3)			10	$\mu\text{A}$
$I_{IL}$	Input LOW Leakage Current	$V_{IN} = 0$ V, $V_{CC} = \text{Max}$ (Note 3)			-10	$\mu\text{A}$
$I_{OZH}$	Off-State Output Leakage Current HIGH	$V_{OUT} = 5.25$ V, $V_{CC} = \text{Max}$ , $V_{IN} = V_{IH}$ or $V_{IL}$ (Note 3)			10	$\mu\text{A}$
$I_{OZL}$	Off-State Output Leakage Current LOW	$V_{OUT} = 0$ V, $V_{CC} = \text{Max}$ , $V_{IN} = V_{IH}$ or $V_{IL}$ (Note 3)			-10	$\mu\text{A}$
$I_{SC}$	Output Short-Circuit Current	$V_{OUT} = 0.5$ V, $V_{CC} = \text{Max}$ (Note 4)	-30		-160	mA

### Notes:

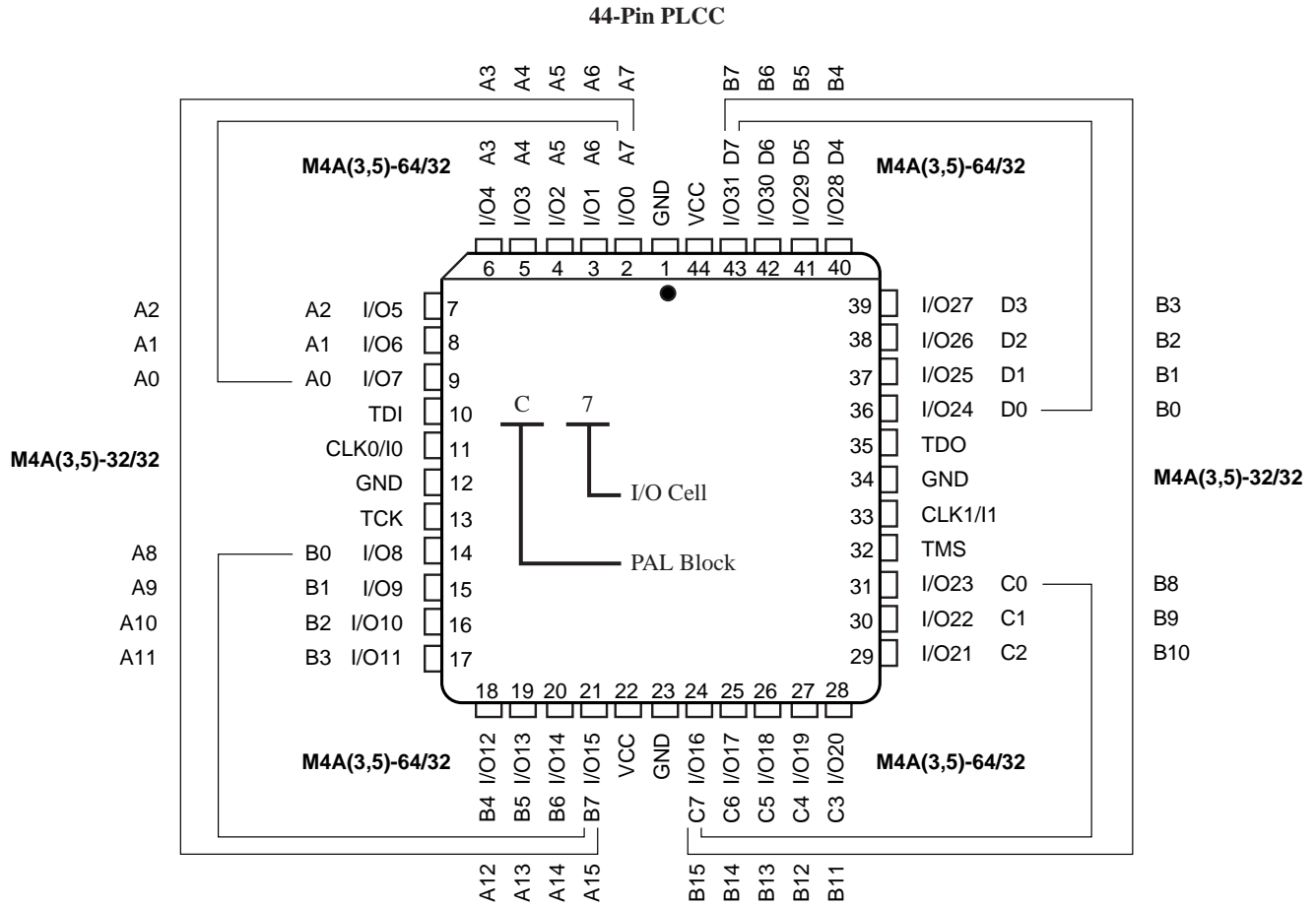
- Total  $I_{OL}$  for one PAL block should not exceed 64 mA.
- These are absolute values with respect to device ground, and all overshoots due to system or tester noise are included.
- I/O pin leakage is the worst case of  $I_{IL}$  and  $I_{OZL}$  (or  $I_{IH}$  and  $I_{OZH}$ ).
- Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.  $V_{OUT} = 0.5$  V has been chosen to avoid test problems caused by tester ground degradation.

## ispMACH 4A TIMING PARAMETERS OVER OPERATING RANGES<sup>1</sup>

		-5		-55		-6		-65		-7		-10		-12		-14		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
<b>Input Register Delays with ZHT Option:</b>																		
$t_{SIRZ}$	Input register setup time - ZHT	6.0		6.0		6.0		6.0		6.0		6.0		6.0		6.0		ns
$t_{HIRZ}$	Input register hold time - ZHT	0.0		0.0		0.0		0.0		0.0		0.0		0.0		0.0		ns
<b>Input Latch Delays with ZHT Option:</b>																		
$t_{SILZ}$	Input latch setup time - ZHT	6.0		6.0		6.0		6.0		6.0		6.0		6.0		6.0		ns
$t_{HILZ}$	Input latch hold time - ZHT	0.0		0.0		0.0		0.0		0.0		0.0		0.0		0.0		ns
$t_{PDIL}$ $Z_i$	Transparent input latch to internal feedback - ZHT		6.0		6.0		6.0		6.0		6.0		6.0		6.0		6.0	ns
<b>Output Delays:</b>																		
$t_{BUF}$	Output buffer delay		1.5		1.5		1.8		2.0		2.5		3.0		3.0		3.0	ns
$t_{SIW}$	Slow slew rate delay adder		2.5		2.5		2.5		2.5		2.5		2.5		2.5		2.5	ns
$t_{EA}$	Output enable time		7.5		7.5		8.5		8.5		9.5		10.0		12.0		15.0	ns
$t_{ER}$	Output disable time		7.5		7.5		8.5		8.5		9.5		10.0		12.0		15.0	ns
<b>Power Delay:</b>																		
$t_{PL}$	Power-down mode delay adder		2.5		2.5		2.5		2.5		2.5		2.5		2.5		2.5	ns
<b>Reset and Preset Delays:</b>																		
$t_{SRi}$	Asynchronous reset or preset to internal register output		7.5		7.7		8.0		8.0		9.5		11.0		13.0		16.0	ns
$t_{SR}$	Asynchronous reset or preset to register output		9.0		9.2		10.0		10.0		12.0		14.0		16.0		19.0	ns
$t_{SRR}$	Asynchronous reset and preset register recovery time	7.0		7.0		7.5		7.5		8.0		8.0		10.0		15.0		ns
$t_{SRW}$	Asynchronous reset or preset width	7.0		7.0		8.0		8.0		10.0		10.0		12.0		15.0		ns
<b>Clock/LE Width:</b>																		
$t_{WLS}$	Global clock width low	2.0		2.0		2.5		2.5		3.0		4.0		5.0		6.0		ns
$t_{WHS}$	Global clock width high	2.0		2.0		2.5		2.5		3.0		4.0		5.0		6.0		ns
$t_{WLA}$	Product term clock width low	3.0		3.0		3.5		3.5		4.0		5.0		8.0		9.0		ns
$t_{WHA}$	Product term clock width high	3.0		3.0		3.5		3.5		4.0		5.0		8.0		9.0		ns
$t_{GWS}$	Global gate width low (for low transparent) or high (for high transparent)	4.0		4.0		4.5		4.5		5.0		5.0		6.0		6.0		ns
$t_{GWA}$	Product term gate width low (for low transparent) or high (for high transparent)	4.0		4.0		4.5		4.5		5.0		5.0		6.0		9.0		ns
$t_{WIRL}$	Input register clock width low	3.0		3.0		3.5		3.5		4.0		5.0		6.0		6.0		ns
$t_{WIRH}$	Input register clock width high	3.0		3.0		3.5		3.5		4.0		5.0		6.0		6.0		ns
$t_{WIL}$	Input latch gate width	4.0		4.0		4.5		4.5		5.0		5.0		6.0		6.0		ns

## 44-PIN PLCC CONNECTION DIAGRAM (M4A(3,5)-32/32 AND M4A(3,5)-64/32)

### Top View



## PIN DESIGNATIONS

CLK/I = Clock or Input

GND = Ground

I/O = Input/Output

V<sub>CC</sub> = Supply Voltage

TDI = Test Data In

TCK = Test Clock

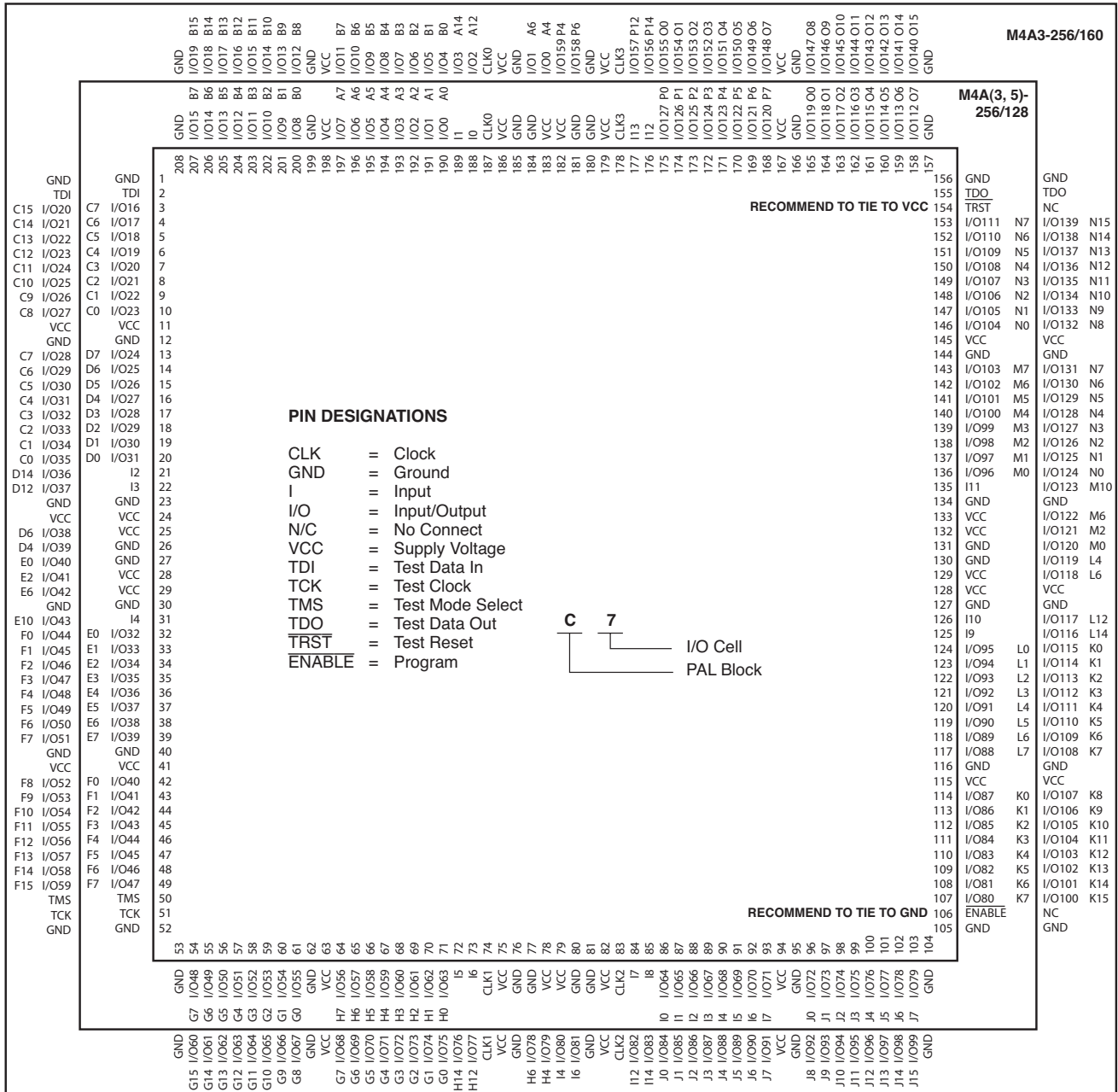
TMS = Test Mode Select

TDO = Test Data Out

# 208-PIN PQFP CONNECTION DIAGRAM (M4A(3,5)-256/128 AND M4A3-256/160)

## Top View

### 208-Pin PQFP



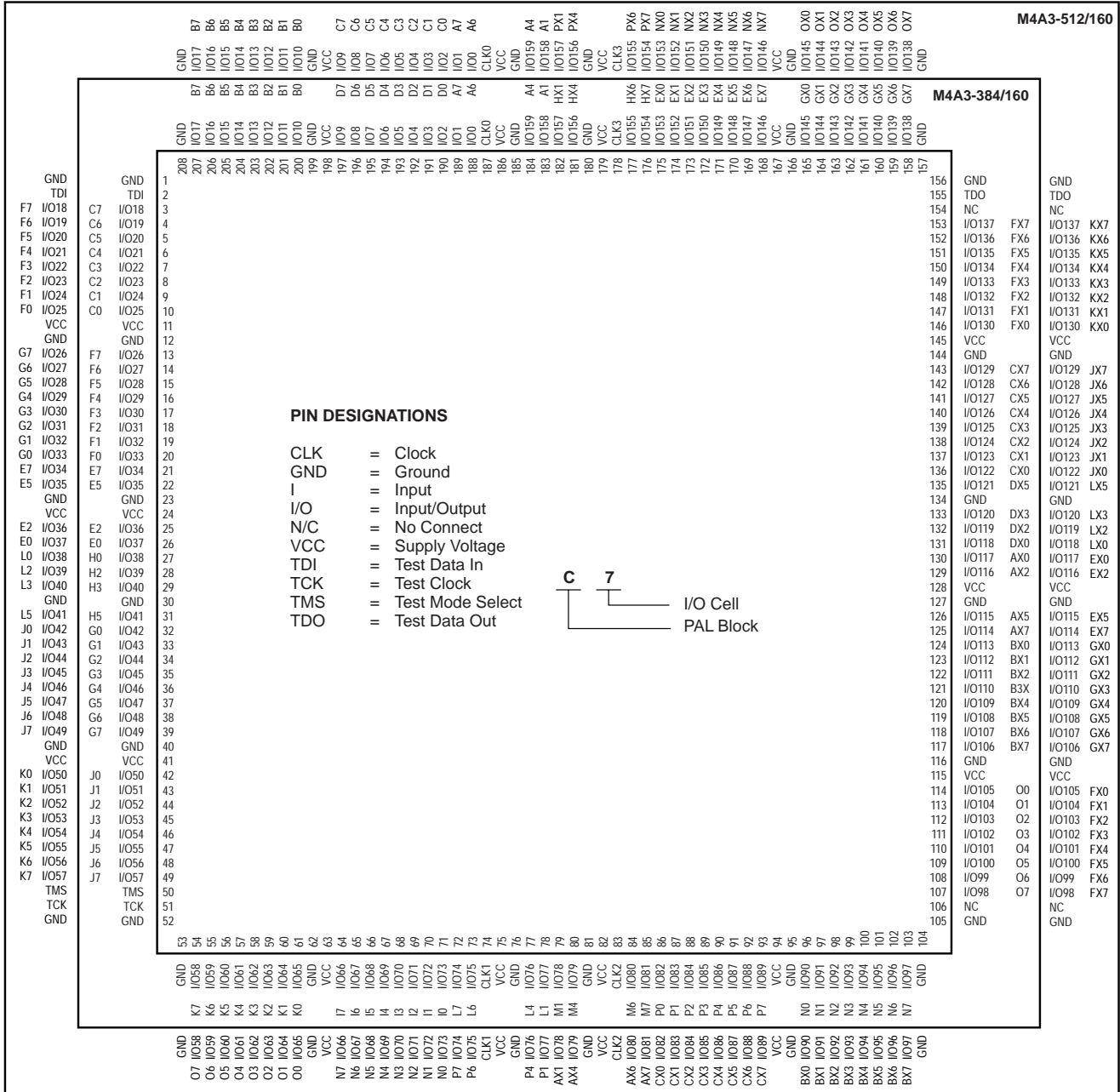
17466G-044



# 208-PIN PQFP CONNECTION DIAGRAM (M4A3-384/160 AND M4A3-512/160)

Top View

## 208-Pin PQFP



17466Ga-044

# 256-BALL BGA CONNECTION DIAGRAM (M4A3-256/128)

## Bottom View

### 256-Ball BGA

	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	GND	N/C	GND	I/O108 N4	I/O105 N1	GND	I/O100 M4	I/O96 M0	GND	GND	GND	GND	I/O95 L0	I/O91 L4	GND	I/O87 K0	N/C	GND	GND	GND	A
B	GND	I/O113 O6	N/C	I/O109 N5	I/O106 N2	I/O103 M7	I/O102 M6	I/O98 M2	N/C	I11	N/C	N/C	I/O93 L2	I/O89 L6	I/O88 L7	I/O85 K2	I/O83 K4	I/O82 K5	N/C	GND	B
C	I/O116 O3	N/C	VCC	TRST	I/O111 N7	I/O107 N3	I/O104 N0	I/O101 M5	I/O97 M1	N/C	I10	I/O94 L1	I/O90 L5	I/O86 K1	I/O84 K3	I/O80 K7	ENABLE	VCC	I/O78 J6	I/O74 J2	C
D	I/O120 P7	I/O117 O2	I/O112 O7	VCC	VCC	I/O110 N6	VCC	N/C	I/O99 M3	N/C	I9	I/O92 L3	N/C	VCC	I/O81 K6	VCC	VCC	I/O79 J7	I/O75 J3	I/O71 I7	D
E	I/O123 P4	I/O119 O0	I/O114 O5	TDI	<p style="text-align: center;"><b>PIN DESIGNATIONS</b></p> <p>           CLK = Clock            GND = Ground            I = Input            I/O = Input/Output            N/C = No Connect            VCC = Supply Voltage            TDI = Test Data In            TCK = Test Clock            TMS = Test Mode Select            TDO = Test Data Out            TRST = Test Reset            ENABLE = Program         </p>												TDO	I/O77 J5	I/O72 J0	I/O68 I4	E
F	GND	I/O122 P5	I/O118 O1	I/O115 O4													I/O76 J4	I/O73 J1	I/O69 I5	GND	F
G	I12	I/O125 P2	I/O121 P6	VCC													VCC	I/O70 I6	I/O65 I1	I8	G
H	GND	I/O127 P0	I/O126 P1	I/O124 P3													I/O67 I3	I/O66 I2	I/O64 I0	GND	H
J	N/C	N/C	N/C	I13													I7	N/C	N/C	N/C	J
K	GND	CLK3	N/C	N/C													N/C	N/C	CLK2	N/C	K
L	N/C	CLK0	N/C	N/C													N/C	N/C	CLK1	GND	L
M	N/C	N/C	N/C	I0													I6	N/C	I/O63 H0	I/O62 H1	M
N	GND	I/O0 A0	I/O2 A2	I/O3 A3													I/O60 H3	I/O61 H2	I/O59 H4	GND	N
P	I1	I/O1 A1	I/O6 A6	VCC													VCC	I/O57 H6	I/O58 H5	I5	P
R	GND	I/O5 A5	I/O9 B1	N/C	I/O51 G4	I/O54 G1	I/O56 H7	GND	R												
T	I/O4 A4	I/O8 B0	I/O12 B4	TCK	TMS	I/O50 G5	I/O55 G0	N/C	T												
U	I/O7 A7	I/O11 B3	I/O15 B7	VCC	VCC	I/O18 C5	VCC	I/O24 D7	I/O29 D2	I2	N/C	I/O35 E3	N/C	VCC	N/C	VCC	VCC	I/O48 G7	I/O53 G2	N/C	U
V	I/O10 B2	I/O13 B5	VCC	I/O16 C7	I/O17 C6	I/O21 C2	I/O23 C0	I/O27 D4	I/O31 D0	I3	N/C	I/O33 E1	I/O37 E5	I/O41 F1	I/O43 F3	I/O46 F6	I/O47 F7	VCC	I/O52 G3	N/C	V
W	GND	I/O14 B6	N/C	N/C	I/O19 C4	I/O22 C1	I/O25 D6	I/O28 D3	N/C	N/C	I4	N/C	I/O34 E2	I/O38 E6	I/O39 E7	I/O42 F2	I/O45 F5	N/C	I/O49 G6	GND	W
Y	GND	GND	GND	N/C	I/O20 C3	GND	I/O26 D5	I/O30 D1	GND	GND	GND	GND	I/O32 E0	I/O36 E4	GND	I/O40 F0	I/O44 F4	GND	N/C	GND	Y
	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

17466G-045

# 256-BALL fpBGA CONNECTION DIAGRAM (M4A3-512/192)

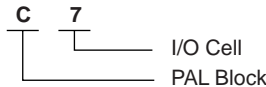
## Bottom View

### 256-Ball fpBGA

	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	I/O159 KX7	I/O181 OX5	I/O180 OX4	I/O177 OX1	I/O174 NX6	I/O172 NX4	I/O191 PX7	I/O186 PX2	I/O1 A1	I/O3 A3	CLK0	I/O17 C1	I/O21 C5	I/O23 C7	I/O10 B2	I/O12 B4	A
B	I/O157 KX5	I/O158 KX6	I/O182 OX6	I/O179 OX3	I/O175 NX7	I/O173 NX5	I/O168 NX0	I/O187 PX3	I/O0 A0	I/O5 A5	I/O7 A7	I/O18 C2	I/O8 B0	I/O11 B3	I/O13 B5	N/C	B
C	I/O155 KX3	I/O156 KX4	N/C	I/O183 OX7	I/O178 OX2	I/O170 NX2	I/O171 NX3	I/O189 PX5	I/O184 PX0	I/O6 A6	I/O20 C4	I/O22 C6	I/O15 B7	I/O14 B6	TDI	I/O39 F7	C
D	I/O150 JX6	I/O151 JX7	TDO	GND	GND	VCC	GND	VCC	GND	GND	VCC	GND	VCC	I/O9 B1	I/O38 F6	I/O37 F5	D
E	I/O148 JX4	N/C	I/O154 KX2	VCC	I/O152 KX0	I/O153 KX1	I/O190 PX6	CLK3	I/O188 PX4	I/O2 A2	I/O16 C0	N/C	GND	I/O36 F4	I/O35 F3	I/O47 G7	E
F	I/O144 JX0	I/O149 JX5	I/O147 JX3	GND	I/O146 JX2	I/O145 JX1	I/O176 OX0	I/O169 NX1	I/O185 PX1	I/O4 A4	I/O19 C3	I/O34 F2	VCC	I/O32 F0	I/O46 G6	I/O45 G5	F
G	I/O163 LX3	I/O166 LX6	I/O165 LX5	VCC	I/O164 LX4	I/O167 LX7	VCC	GND	GND	VCC	I/O33 F1	I/O44 G4	GND	I/O42 G2	I/O41 G1	I/O31 E7	G
H	I/O160 LX0	I/O162 LX2	I/O161 LX1	GND	I/O120 EX0	I/O121 EX1	GND	VCC	VCC	GND	I/O43 G3	I/O40 G0	VCC	I/O28 E4	I/O27 E3	I/O26 E2	H
J	I/O122 EX2	I/O123 EX3	I/O124 EX4	GND	I/O126 EX6	I/O125 EX5	GND	VCC	VCC	GND	I/O30 E6	I/O29 E5	GND	I/O65 L1	I/O64 L0	I/O66 L2	J
K	I/O127 EX7	I/O136 GX0	I/O137 GX1	VCC	I/O139 GX3	I/O138 GX2	VCC	GND	GND	VCC	I/O25 E1	I/O24 E0	VCC	I/O71 L7	I/O70 L6	I/O48 J0	K
L	I/O140 GX4	I/O141 GX5	I/O143 GX7	GND	I/O130 FX2	I/O142 GX6	I/O98 AX2	I/O91 P3	I/O75 N3	I/O77 N5	I/O68 L4	I/O67 L3	GND	I/O51 J3	I/O52 J4	I/O49 J1	L
M	I/O128 FX0	I/O129 FX1	I/O131 FX3	GND	I/O115 CX3	I/O113 CX1	I/O100 AX4	I/O90 P2	I/O74 N2	I/O80 O0	I/O83 O3	I/O69 L5	VCC	I/O60 K4	I/O55 J7	I/O50 J2	M
N	I/O132 FX4	I/O133 FX5	I/O135 FX7	VCC	GND	VCC	GND	VCC	GND	GND	VCC	GND	GND	TCK	I/O56 K0	I/O53 J5	N
P	I/O134 FX6	I/O109 BX5	I/O110 BX6	I/O111 BX7	I/O116 CX4	I/O114 CX2	I/O101 AX5	I/O89 P1	I/O93 P5	I/O94 P6	I/O79 N7	I/O84 O4	I/O87 O7	TMS	I/O57 K1	I/O54 J6	P
R	I/O108 BX4	I/O107 BX3	I/O104 BX0	I/O119 CX7	I/O112 CX0	I/O102 AX6	I/O99 AX3	I/O96 AX0	I/O92 P4	I/O72 N0	I/O76 N4	I/O81 O1	I/O85 O5	I/O63 K7	I/O59 K3	I/O58 K2	R
T	I/O106 BX2	I/O105 BX1	I/O118 CX6	I/O117 CX5	I/O103 AX7	CLK2	I/O97 AX1	I/O88 P0	CLK1	I/O95 P7	I/O73 N1	I/O78 N6	I/O82 O2	I/O86 O6	I/O62 K6	I/O61 K5	T

#### PIN DESIGNATIONS

- CLK = Clock
- GND = Ground
- I = Input
- I/O = Input/Output
- N/C = No Connect
- VCC = Supply Voltage
- TDI = Test Data In
- TCK = Test Clock
- TMS = Test Mode Select
- TDO = Test Data Out



5V Commercial Combinations		
M4A5-32/32	-5, -7, -10,	JC, VC, VC48
M4A5-64/32	-55, -7, -10	JC, VC, VC48
M4A5-96/48		VC
M4A5-128/64		YC, VC
M4A5-192/96	-6, -7, -10	VC
M4A5-256/128	-65, -7, -10	YC

5V Industrial Combinations		
M4A5-32/32	-7, -10, -12	JJ, VI, VI48
M4A5-64/32	-7, -10, -12	JJ, VI, VI48
M4A5-96/48		VI
M4A5-128/64		YI, VI
M4A5-192/96	-7, -10, -12	VI
M4A5-256/128	-10, -12	YI

## Lead-free Packaging

3.3V Commercial Combinations		
M4A3-32/32	-5, -7, -10	VNC, VNC48, JNC
M4A3-64/32	-55, -7, -10	VNC, VNC48, JNC
M4A3-64/64		VNC
M4A3-128/64		VNC
M4A3-192/96	-6, -7, -10	VNC
M4A3-256/128	-55, -7, -10	FANC, YNC
M4A3-256/160	-7, -10	YNC
M4A3-256/192		FANC
M4A3-384/192	-65, -10, -12	FANC
M4A3-512/192	-7, -10, -12	FANC

3.3V Industrial Combinations		
M4A3-32/32	-7, -10, -12	VNI, VNI48, JNI
M4A3-64/32		VNI, VNI48, JNI
M4A3-64/64		VNI
M4A3-128/64		VNI
M4A3-192/96	-10, -12	VNI
M4A3-256/128		FANI, YNI
M4A3-256/160		YNI
M4A3-256/192	-10, -12, -14	FANI
M4A3-384/192		FANI
M4A3-512/192		FANI

5V Commercial Combinations		
M4A5-32/32	-5, -7, -10	VNC, VNC48, JNC
M4A5-64/32	-55, -7, -10	VNC, VNC48, JNC
M4A5-96/48		VNC
M4A5-128/64		VNC, YNC
M4A5-192/96	-6, -7, -10	VNC
M4A5-256/128	-65, -7, -10	YNC

5V Industrial Combinations		
M4A5-32/32	-7, -10, -12	VNI, VNI48, JNI
M4A5-64/32		VNI, VNI48, JNI
M4A5-96/48		VNI
M4A5-128/64		VNI, YNI
M4A5-192/96		VNI
M4A5-256/128		YNI

Most ispMACH devices are dual-marked with both Commercial and Industrial grades. The Industrial speed grade is slower, i.e., M4A3-256/128-7YC-10YI

### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local Lattice sales office to confirm availability of specific valid combinations and to check on newly released combinations.

---

## Revision History

Date	Version	Change Summary
-	K	Previous Lattice release.
August 2006	L	Updated for lead-free package options.
September 2006	M	Revised M4A3-256/160 208-pin PQFP connection diagram.