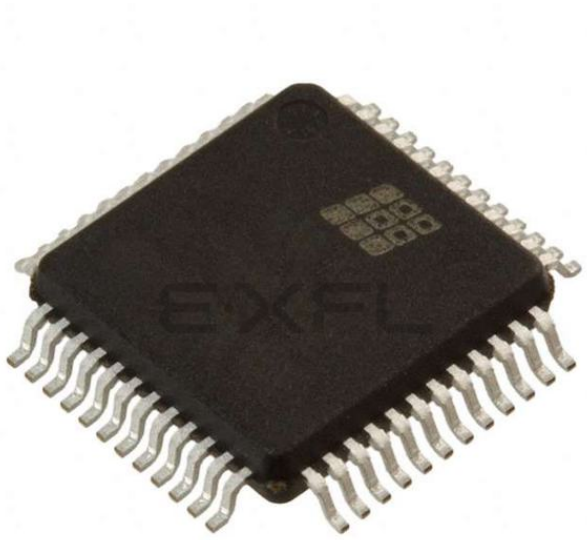
Lattice Semiconductor Corporation - M4A3-32/32-7VC48 Datasheet



Welcome to E-XFL.COM

Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	7.5 ns
Voltage Supply - Internal	3V ~ 3.6V
Number of Logic Elements/Blocks	-
Number of Macrocells	32
Number of Gates	-
Number of I/O	32
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-TQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/m4a3-32-32-7vc48

Table 1. ispMACH 4A Device Features

3.3 V Devices								
Feature	**M4A3-32**	**M4A3-64**	**M4A3-96**	**M4A3-128**	**M4A3-192**	**M4A3-256**	**M4A3-384**	**M4A3-512**
Macrocells	32	64	96	128	192	256	384	512
User I/O options	32	32/64	48	64	96	128/160/192	160/192	160/192/256
t_{PD} (ns)	5.0	5.5	5.5	5.5	6.0	5.5	6.5	7.5
f_{CNT} (MHz)	182	167	167	167	160	167	154	125
t_{COS} (ns)	4.0	4.0	4.0	4.0	4.5	4.0	4.5	5.5
t_{SS} (ns)	3.0	3.5	3.5	3.5	3.5	3.5	3.5	5.0
Static Power (mA)	20	25/52	40	55	85	110/150	149/155	179
JTAG Compliant	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
PCI Compliant	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes

5 V Devices						
Feature	**M4A5-32**	**M4A5-64**	**M4A5-96**	**M4A5-128**	**M4A5-192**	**M4A5-256**
Macrocells	32	64	96	128	192	256
User I/O options	32	32	48	64	96	128
t_{PD} (ns)	5.0	5.5	5.5	5.5	6.0	6.5
f_{CNT} (MHz)	182	167	167	167	160	154
t_{COS} (ns)	4.0	4.0	4.0	4.0	4.5	5.0
t_{SS} (ns)	3.0	3.5	3.5	3.5	3.5	3.5
Static Power (mA)	20	25	40	55	74	110
JTAG Compliant	Yes	Yes	Yes	Yes	Yes	Yes
PCI Compliant	Yes	Yes	Yes	Yes	Yes	Yes

FUNCTIONAL DESCRIPTION

The fundamental architecture of ispMACH 4A devices (Figure 1) consists of multiple, optimized PAL® blocks interconnected by a central switch matrix. The central switch matrix allows communication between PAL blocks and routes inputs to the PAL blocks. Together, the PAL blocks and central switch matrix allow the logic designer to create large designs in a single device instead of having to use multiple devices.

The key to being able to make effective use of these devices lies in the interconnect schemes. In the ispMACH 4A architecture, the macrocells are flexibly coupled to the product terms through the logic allocator, and the I/O pins are flexibly coupled to the macrocells due to the output switch matrix. In addition, more input routing options are provided by the input switch matrix. These resources provide the flexibility needed to fit designs efficiently.

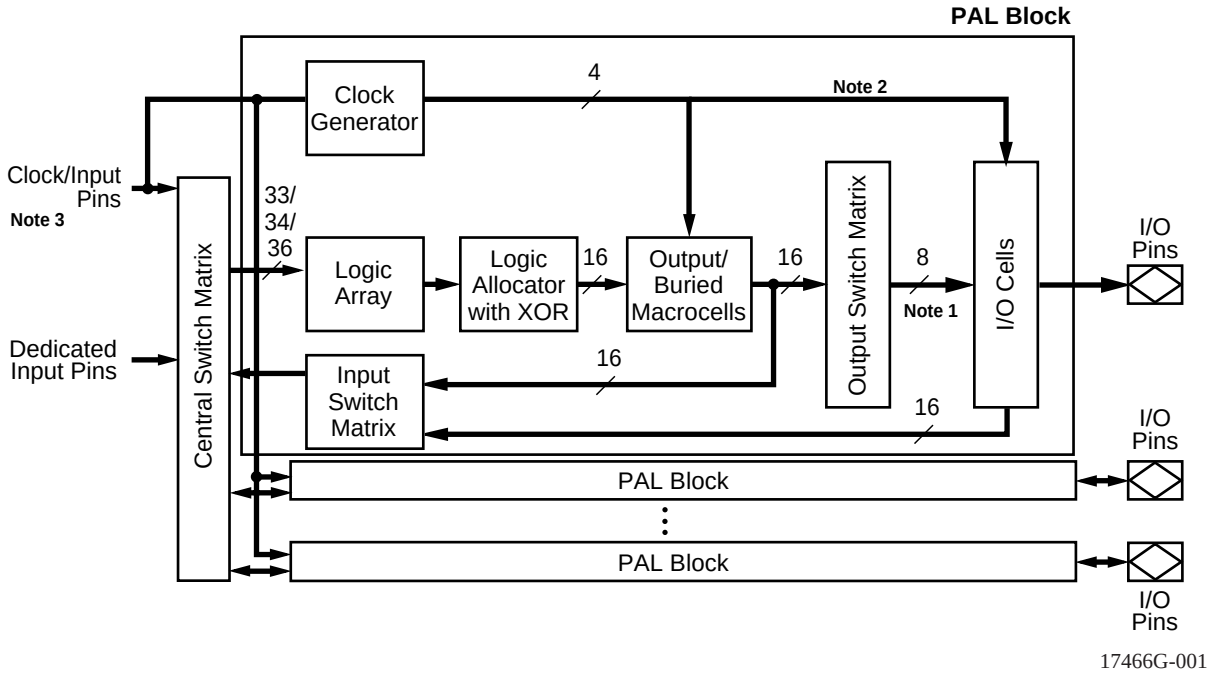
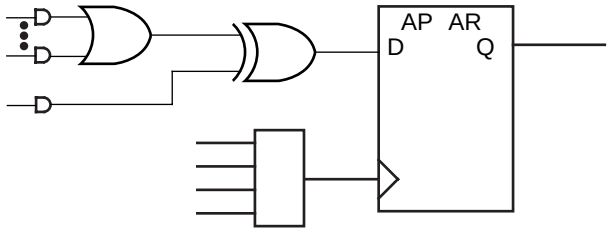


Figure 1. ispMACH 4A Block Diagram and PAL Block Structure

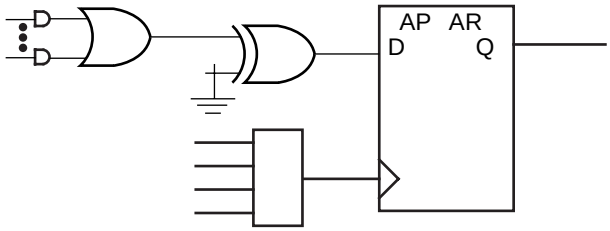
Notes:

1. *16 for ispMACH 4A devices with 1:1 macrocell-I/O cell ratio (see next page).*
2. *Block clocks do not go to I/O cells in M4A(3,5)-32/32.*
3. *M4A(3,5)-192, M4A(3,5)-256, M4A3-384, and M4A3-512 have dedicated clock pins which cannot be used as inputs and do not connect to the central switch matrix.*

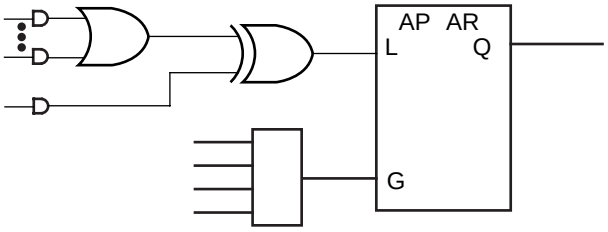
The flip-flop can be configured as a D-type or T-type latch. J-K or S-R registers can be synthesized. The primary flip-flop configurations are shown in Figure 6, although others are possible. Flip-flop functionality is defined in Table 8. Note that a J-K latch is inadvisable as it will cause oscillation if both J and K inputs are HIGH.



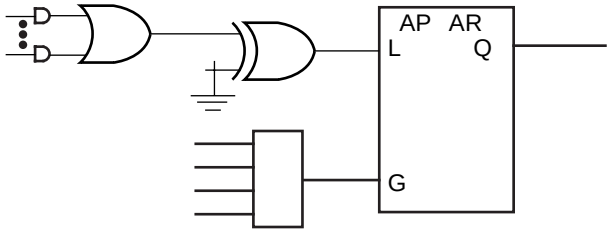
a. D-type with XOR



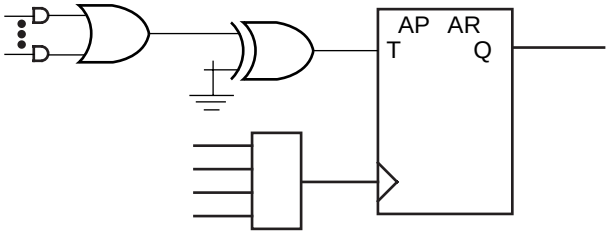
b. D-type with programmable D polarity



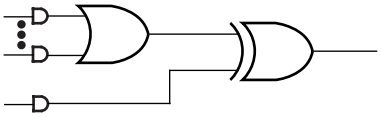
c. Latch with XOR



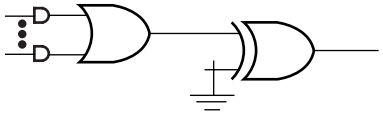
d. Latch with programmable D polarity



e. T-type with programmable T polarity



f. Combinatorial with XOR



g. Combinatorial with programmable polarity

17466G-011

Figure 6. Primary Macrocell Configurations

Table 8. Register/Latch Operation

Configuration	Input(s)	CLK/LE [1]	Q+
D-type Register	D=X	0, 1, ↓ (↑)	Q
	D=0	↑ (↓)	0
	D=1	↑ (↓)	1
T-type Register	T=X	0, 1, ↓ (↑)	Q
	T=0	↑ (↓)	Q
	T=1	↑ (↓)	$\overline{Q}$
D-type Latch	D=X	1(0)	Q
	D=0	0(1)	0
	D=1	0(1)	1

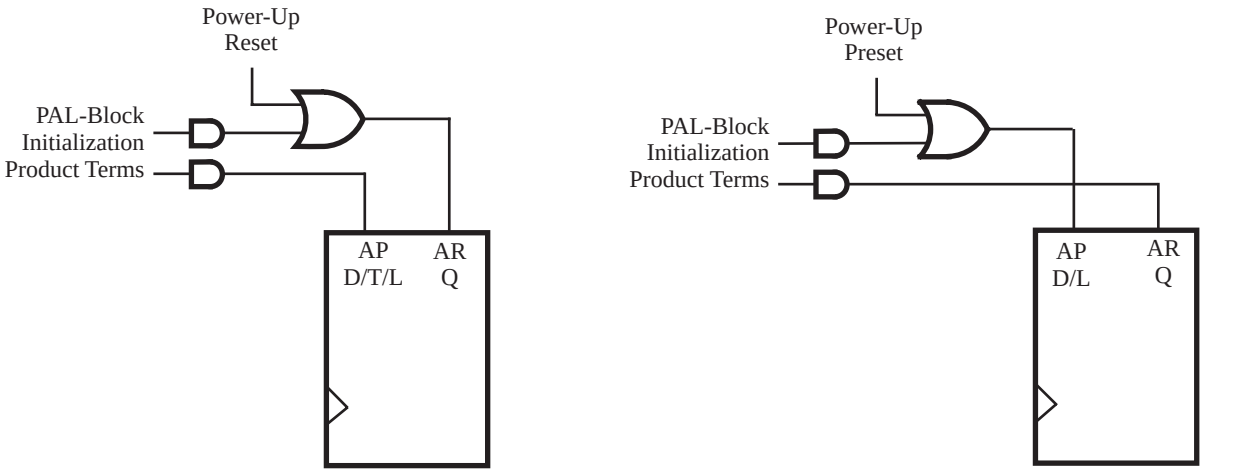
Note:

1. Polarity of CLK/LE can be programmed

Although the macrocell shows only one input to the register, the XOR gate in the logic allocator allows the D-, T-type register to emulate J-K, and S-R behavior. In this case, the available product terms are divided between J and K (or S and R). When configured as J-K, S-R, or T-type, the extra product term must be used on the XOR gate input for flip-flop emulation. In any register type, the polarity of the inputs can be programmed.

The clock input to the flip-flop can select any of the four PAL block clocks in synchronous mode, with the additional choice of either polarity of an individual product term clock in the asynchronous mode.

The initialization circuit depends on the mode. In synchronous mode (Figure 7), asynchronous reset and preset are provided, each driven by a product term common to the entire PAL block.



a. Power-up reset **b. Power-up preset**

17466G-012 17466G-013

Figure 7. Synchronous Mode Initialization Configurations

Output Switch Matrix

The output switch matrix allows macrocells to be connected to any of several I/O cells within a PAL block. This provides high flexibility in determining pinout and allows design changes to occur without effecting pinout.

In ispMACH 4A devices with 2:1 Macrocell-I/O cell ratio, each PAL block has twice as many macrocells as I/O cells. The ispMACH 4A output switch matrix allows for half of the macrocells to drive I/O cells within a PAL block, in combinations according to Figure 9. Each I/O cell can choose from eight macrocells; each macrocell has a choice of four I/O cells. The ispMACH 4A devices with 1:1 Macrocell-I/O cell ratio allow each macrocell to drive one of eight I/O cells (Figure 9).

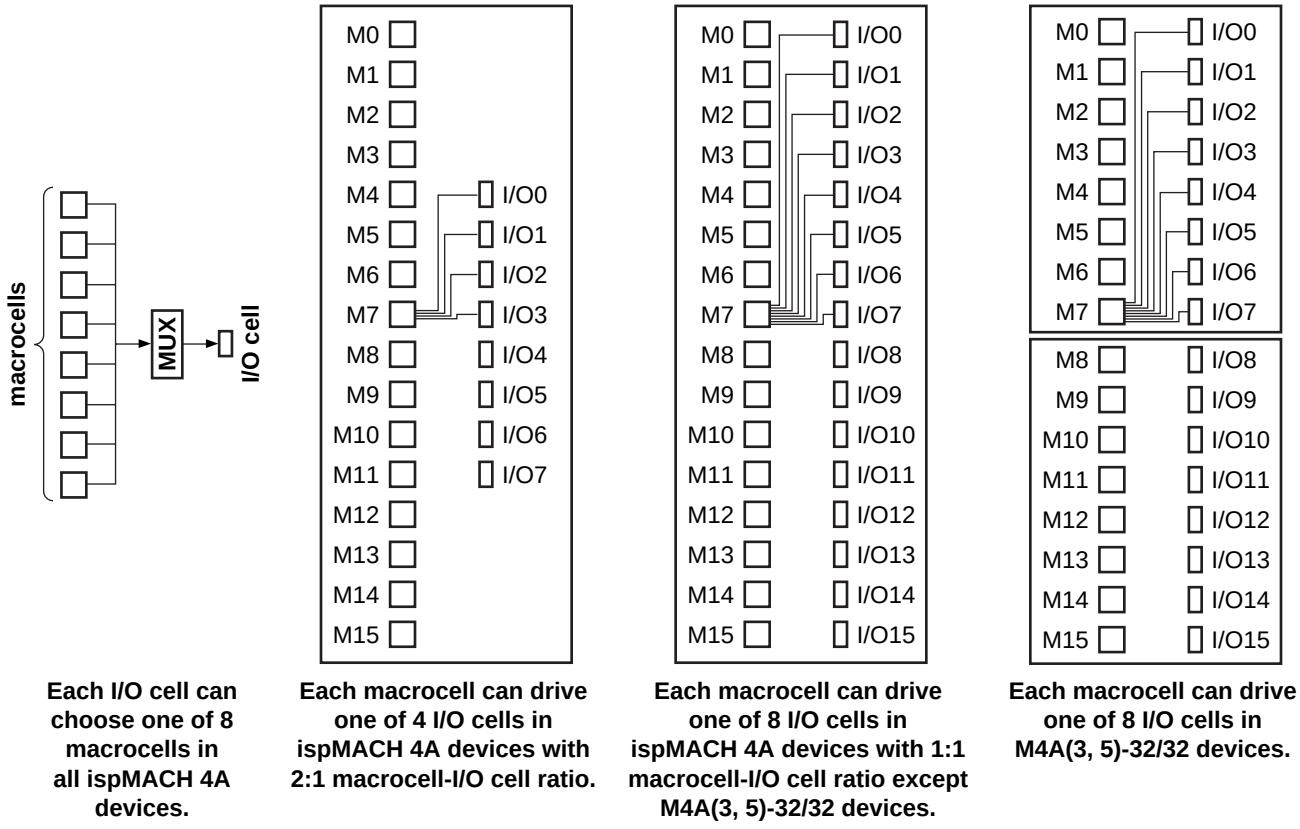


Figure 9. ispMACH 4A Output Switch Matrix

Table 10. Output Switch Matrix Combinations for ispMACH 4A Devices with 2:1 Macrocell-I/O Cell Ratio

Macrocell	Routable to I/O Cells
M0, M1	I/O0, I/O5, I/O6, I/O7
M2, M3	I/O0, I/O1, I/O6, I/O7
M4, M5	I/O0, I/O1, I/O2, I/O7
M6, M7	I/O0, I/O1, I/O2, I/O3
M8, M9	I/O1, I/O2, I/O3, I/O4
M10, M11	I/O2, I/O3, I/O4, I/O5

Input Switch Matrix

The input switch matrix (Figures 12 and 13) optimizes routing of inputs to the central switch matrix. Without the input switch matrix, each input and feedback signal has only one way to enter the central switch matrix. The input switch matrix provides additional ways for these signals to enter the central switch matrix.

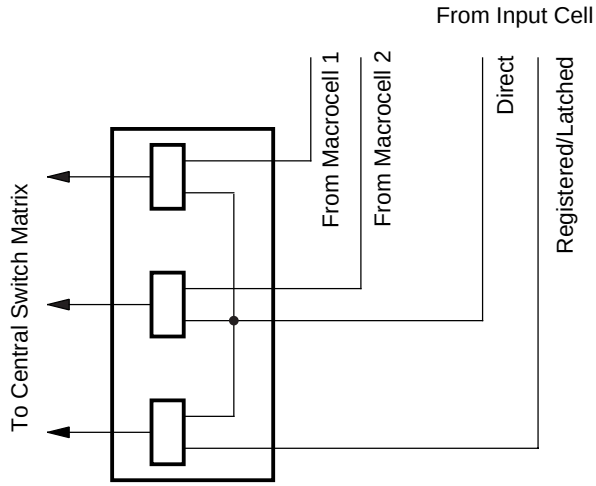


Figure 12. ispMACH 4A with 2:1 Macrocell-I/O Cell Ratio - Input Switch Matrix

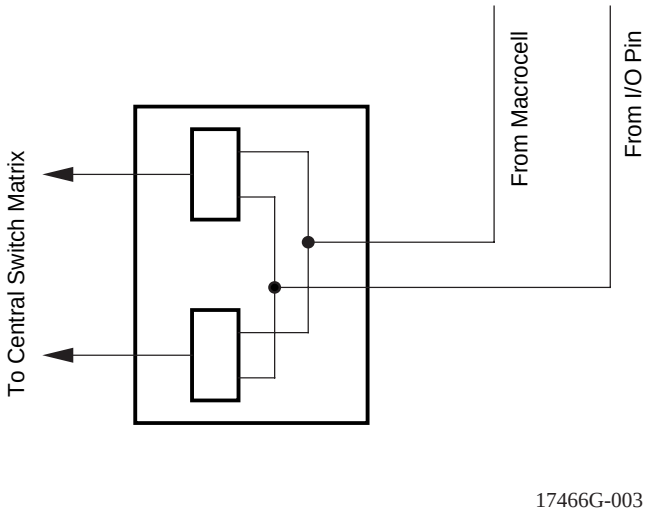
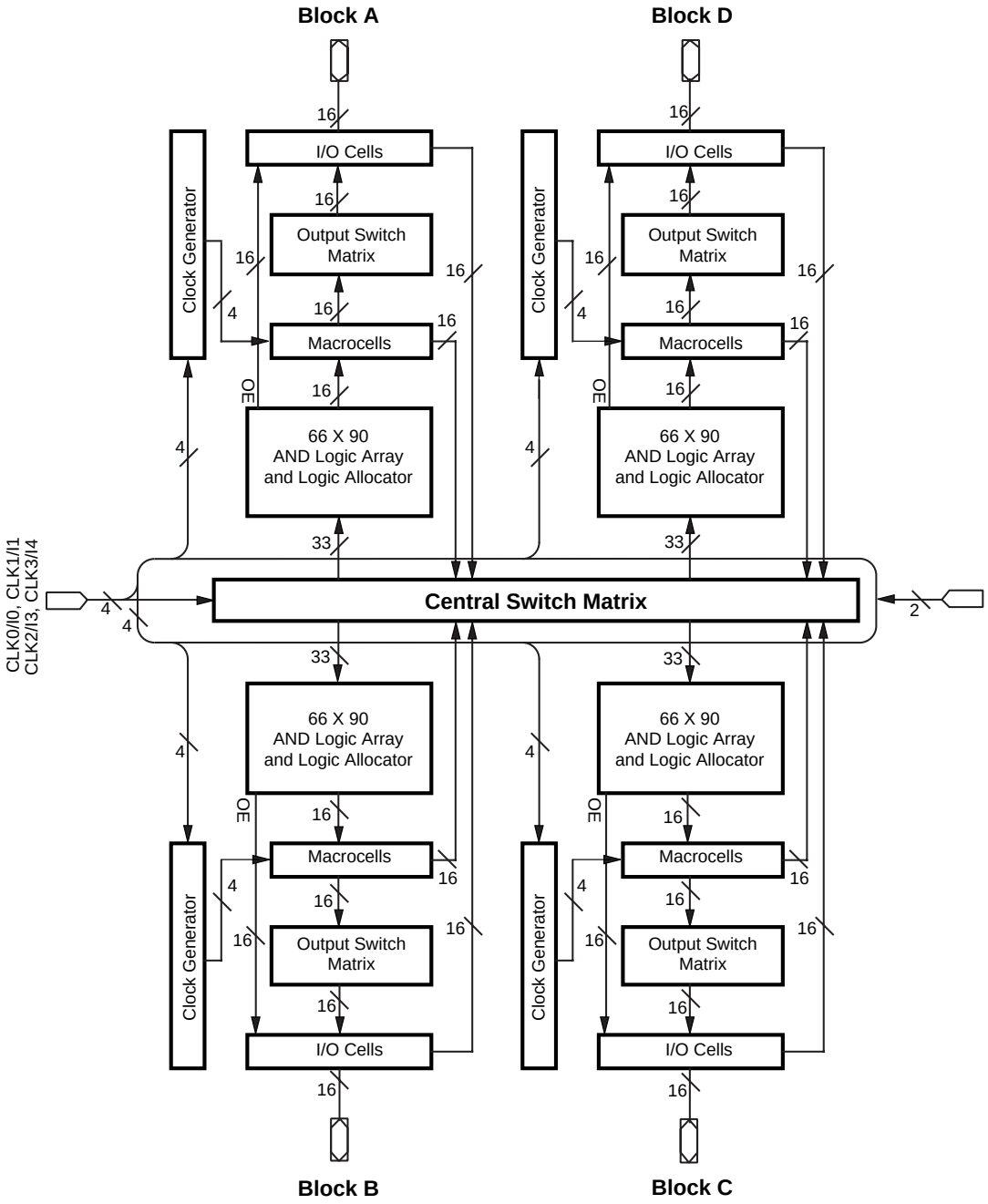


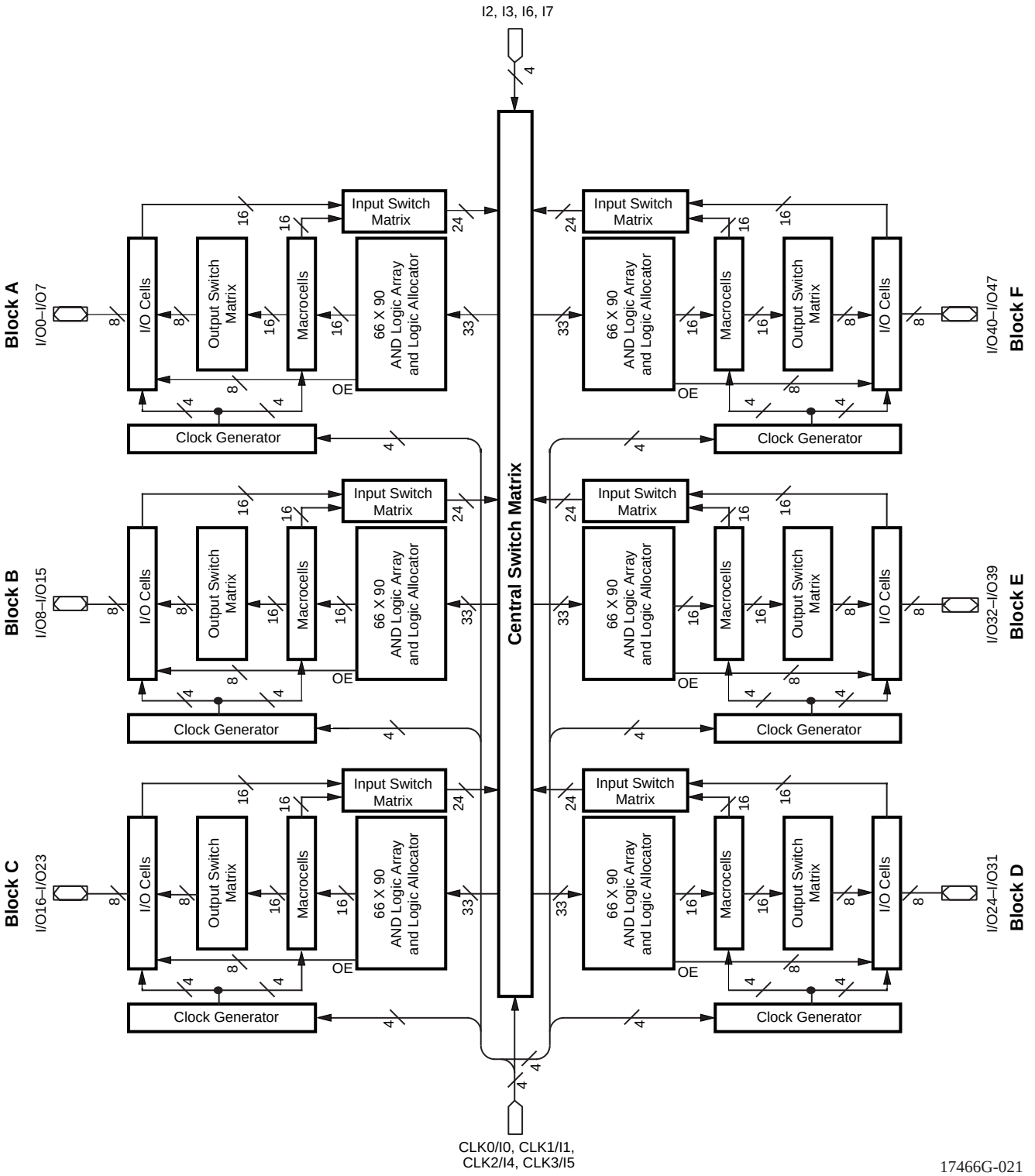
Figure 13. ispMACH 4A with 1:1 Macrocell-I/O Cell Ratio - Input Switch Matrix

BLOCK DIAGRAM – M4A3-64/64



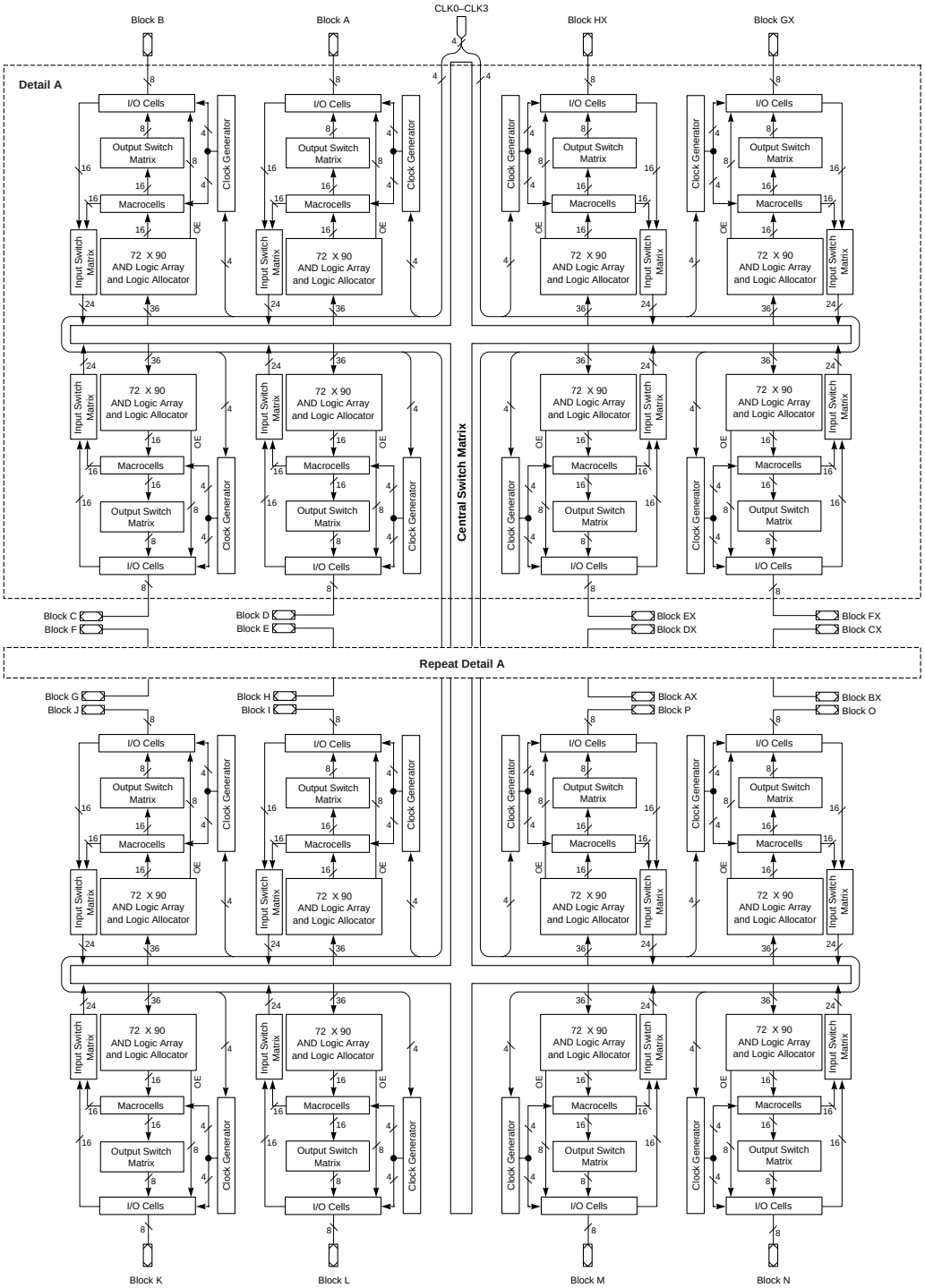
17466H-020A

BLOCK DIAGRAM – M4A(3,5)-96/48



17466G-021

BLOCK DIAGRAM – M4A3-384/160, M4A3-384/192



17466G-067

ABSOLUTE MAXIMUM RATINGS

M4A5

Storage Temperature . . . . . -65°C to +150°C

Ambient Temperature
with Power Applied. . . . . -55°C to +100°C

Device Junction Temperature. . . . . +130°C

Supply Voltage
with Respect to Ground . . . . . -0.5 V to +7.0 V

DC Input Voltage . . . . . -0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage . . . . . 2000 V

Latchup Current (T_A = -40°C to +85°C) . . . . . 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)
Operating in Free Air . . . . . 0°C to +70°C

Supply Voltage (V_{CC})
with Respect to Ground. . . . . +4.75 V to +5.25 V

Industrial (I) Devices

Ambient Temperature (T_A)
Operating in Free Air . . . . . -40°C to +85°C

Supply Voltage (V_{CC})
with Respect to Ground. . . . . +4.50 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

5-V DC CHARACTERISTICS OVER OPERATING RANGES

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA, V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	2.4			V
		I_{OH} = -100 µA, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL}		3.3	3.6	V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA, V_{CC} = Min, V_{IN} = V_{IH} or V_{IL} (Note 1)			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 2)	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 2)			0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 3)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 3)			–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 3)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max , V_{IN} = V_{IH} or V_{IL} (Note 3)			–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 4)	–30		–160	mA

Notes:

1. *Total I_{OL} for one PAL block should not exceed 64 mA.*
2. *These are absolute values with respect to device ground, and all overshoots due to system or tester noise are included.*
3. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
4. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

ABSOLUTE MAXIMUM RATINGS

M4A3

Storage Temperature . . . . . -65°C to +150°C

Ambient Temperature
with Power Applied. . . . . -55°C to +100°C

Device Junction Temperature. . . . . +130°C

Supply Voltage
with Respect to Ground . . . . . -0.5 V to +4.5 V

DC Input Voltage . . . . . -0.5 V to 6.0 V

Static Discharge Voltage . . . . . 2000 V

Latchup Current (T_A = -40°C to +85°C) . . . . . 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)
Operating in Free Air . . . . . 0°C to +70°C

Supply Voltage (V_{CC})
with Respect to Ground. . . . . +3.0 V to +3.6 V

Industrial (I) Devices

Ambient Temperature (T_A)
Operating in Free Air . . . . . -40°C to +85°C

Supply Voltage (V_{CC})
with Respect to Ground. . . . . +3.0 V to +3.6 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

3.3-V DC CHARACTERISTICS OVER OPERATING RANGES

Parameter Symbol	Parameter Description	Test Conditions		Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = –100 µA	V_{CC} – 0.2			V
			I_{OH} = –3.2 mA	2.4			V
V_{OL}	Output LOW Voltage	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL} (Note 1)	I_{OL} = 100 µA			0.2	V
			I_{OL} = 24 mA			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs		2.0		5.5	V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs		–0.3		0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 3.6 V, V_{CC} = Max (Note 2)				5	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)				–5	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 3.6 V, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 2)				5	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 2)				–5	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)		–15		–160	mA

Notes:

1. *Total I_{OL} for one PAL block should not exceed 64 mA.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.*

Notes:

1. *See "MACH Switching Test Circuit" document on the Literature Download page of the Lattice web site.*
2. *This parameter does not apply to flip-flops in the emulated mode since the feedback path is required for emulation.*

ispMACH 4A TIMING PARAMETERS OVER OPERATING RANGES[1]

		-5		-55		-6		-65		-7		-10		-12		-14		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit
Combinatorial Delay:																		
t_{PDi}	Internal combinatorial propagation delay		3.5		4.0		4.3		4.5		5.0		7.0		9.0		11.0	ns
t_{PD}	Combinatorial propagation delay		5.0		5.5		6.0		6.5		7.5		10.0		12.0		14.0	ns
Registered Delays:																		
t_{SS}	Synchronous clock setup time, D-type register	3.0		3.5		3.5		3.5		5.0		5.5		7.0		10.0		ns
t_{SST}	Synchronous clock setup time, T-type register	4.0		4.0		4.0		4.0		6.0		6.5		8.0		11.0		ns
t_{SA}	Asynchronous clock setup time, D-type register	2.5		2.5		2.5		3.0		3.5		4.0		5.0		8.0		ns
t_{SAT}	Asynchronous clock setup time, T-type register	3.0		3.0		3.0		3.5		4.5		5.0		6.0		9.0		ns
t_{HS}	Synchronous clock hold time	0.0		0.0		0.0		0.0		0.0		0.0		0.0		0.0		ns
t_{HA}	Asynchronous clock hold time	2.5		2.5		2.5		3.0		3.5		4.0		5.0		8.0		ns
t_{COSi}	Synchronous clock to internal output		2.5		2.5		2.8		3.0		3.0		3.0		3.5		3.5	ns
t_{COS}	Synchronous clock to output		4.0		4.0		4.5		5.0		5.5		6.0		6.5		6.5	ns
t_{COAi}	Asynchronous clock to internal output		5.0		5.0		5.0		5.0		6.0		8.0		10.0		12.0	ns
t_{COA}	Asynchronous clock to output		6.5		6.5		6.8		7.0		8.5		11.0		13.0		15.0	ns
Latched Delays:																		
t_{SSL}	Synchronous latch setup time	4.0		4.0		4.0		4.5		6.0		7.0		8.0		10.0		ns
t_{SAL}	Asynchronous latch setup time	3.0		3.0		3.5		3.5		4.0		4.0		5.0		8.0		ns
t_{HSL}	Synchronous latch hold time	0.0		0.0		0.0		0.0		0.0		0.0		0.0		0.0		ns
t_{HAL}	Asynchronous latch hold time	3.0		3.0		3.5		3.5		4.0		4.0		5.0		8.0		ns
t_{PDLi}	Transparent latch to internal output		5.5		5.5		5.8		6.0		7.5		9.0		11.0		12.0	ns
t_{PDL}	Propagation delay through transparent latch to output		7.0		7.0		7.5		8.0		10.0		12.0		14.0		15.0	ns
t_{GOSi}	Synchronous gate to internal output		3.0		3.0		3.0		3.0		3.5		4.5		7.0		8.0	ns
t_{GOS}	Synchronous gate to output		4.5		4.5		4.8		5.0		6.0		7.5		10.0		11.0	ns
t_{GOAi}	Asynchronous gate to internal output		6.0		6.0		6.0		6.0		8.5		10.0		13.0		15.0	ns
t_{GOA}	Asynchronous gate to output		7.5		7.5		7.8		8.0		11.0		13.0		16.0		18.0	ns
Input Register Delays:																		
t_{SIRS}	Input register setup time	1.5		1.5		2.0		2.0		2.0		2.0		2.0		2.0		ns
t_{HIRS}	Input register hold time	2.5		2.5		3.0		3.0		3.0		3.0		3.0		4.0		ns
t_{ICOSi}	Input register clock to internal feedback		3.0		3.0		3.0		3.0		3.5		4.5		6.0		6.0	ns
Input Latch Delays:																		
t_{SIL}	Input latch setup time	1.5		1.5		1.5		2.0		2.0		2.0		2.0		2.0		ns
t_{HIL}	Input latch hold time	2.5		2.5		2.5		3.0		3.0		3.0		3.0		4.0		ns
t_{IGOSi}	Input latch gate to internal feedback		3.5		3.5		3.8		4.0		4.0		4.0		4.0		5.0	ns
t_{PDILi}	Transparent input latch to internal feedback		1.5		1.5		1.5		1.5		2.0		2.0		2.0		2.0	ns

ispMACH 4A TIMING PARAMETERS OVER OPERATING RANGES[1]

		-5		-55		-6		-65		-7		-10		-12		-14		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit
Input Register Delays with ZHT Option:																		
t_{SIRZ}	Input register setup time - ZHT	6.0		6.0		6.0		6.0		6.0		6.0		6.0		6.0		ns
t_{HIRZ}	Input register hold time - ZHT	0.0		0.0		0.0		0.0		0.0		0.0		0.0		0.0		ns
Input Latch Delays with ZHT Option:																		
t_{SILZ}	Input latch setup time - ZHT	6.0		6.0		6.0		6.0		6.0		6.0		6.0		6.0		ns
t_{HILZ}	Input latch hold time - ZHT	0.0		0.0		0.0		0.0		0.0		0.0		0.0		0.0		ns
t_{PDILZi}	Transparent input latch to internal feedback - ZHT		6.0		6.0		6.0		6.0		6.0		6.0		6.0		6.0	ns
Output Delays:																		
t_{BUF}	Output buffer delay		1.5		1.5		1.8		2.0		2.5		3.0		3.0		3.0	ns
t_{SLW}	Slow slew rate delay adder		2.5		2.5		2.5		2.5		2.5		2.5		2.5		2.5	ns
t_{EA}	Output enable time		7.5		7.5		8.5		8.5		9.5		10.0		12.0		15.0	ns
t_{ER}	Output disable time		7.5		7.5		8.5		8.5		9.5		10.0		12.0		15.0	ns
Power Delay:																		
t_{PL}	Power-down mode delay adder		2.5		2.5		2.5		2.5		2.5		2.5		2.5		2.5	ns
Reset and Preset Delays:																		
t_{SRi}	Asynchronous reset or preset to internal register output		7.5		7.7		8.0		8.0		9.5		11.0		13.0		16.0	ns
t_{SR}	Asynchronous reset or preset to register output		9.0		9.2		10.0		10.0		12.0		14.0		16.0		19.0	ns
t_{SRR}	Asynchronous reset and preset register recovery time	7.0		7.0		7.5		7.5		8.0		8.0		10.0		15.0		ns
t_{SRW}	Asynchronous reset or preset width	7.0		7.0		8.0		8.0		10.0		10.0		12.0		15.0		ns
Clock/LE Width:																		
t_{WLS}	Global clock width low	2.0		2.0		2.5		2.5		3.0		4.0		5.0		6.0		ns
t_{WHS}	Global clock width high	2.0		2.0		2.5		2.5		3.0		4.0		5.0		6.0		ns
t_{WLA}	Product term clock width low	3.0		3.0		3.5		3.5		4.0		5.0		8.0		9.0		ns
t_{WHA}	Product term clock width high	3.0		3.0		3.5		3.5		4.0		5.0		8.0		9.0		ns
t_{GWS}	Global gate width low (for low transparent) or high (for high transparent)	4.0		4.0		4.5		4.5		5.0		5.0		6.0		6.0		ns
t_{GWA}	Product term gate width low (for low transparent) or high (for high transparent)	4.0		4.0		4.5		4.5		5.0		5.0		6.0		9.0		ns
t_{WIRL}	Input register clock width low	3.0		3.0		3.5		3.5		4.0		5.0		6.0		6.0		ns
t_{WIRH}	Input register clock width high	3.0		3.0		3.5		3.5		4.0		5.0		6.0		6.0		ns
t_{WIL}	Input latch gate width	4.0		4.0		4.5		4.5		5.0		5.0		6.0		6.0		ns

ispMACH 4A TIMING PARAMETERS OVER OPERATING RANGES[1]

		-5		-55		-6		-65		-7		-10		-12		-14		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Frequency:																		
f_{MAXS}	External feedback, D-type, Min of $1/(t_{WLS} + t_{WHS})$ or $1/(t_{SS} + t_{COS})$	143		133		125		118		95.2		87.0		74.1		60.6		MHz
	External feedback, T-type, Min of $1/(t_{WLS} + t_{WHS})$ or $1/(t_{SST} + t_{COS})$	125		125		118		111		87.0		80.0		69.0		57.1		MHz
	Internal feedback (f_{CNT}), D-type, Min of $1/(t_{WLS} + t_{WHS})$ or $1/(t_{SS} + t_{COSi})$	182		167		160		154		125		118		95.0		74.1		MHz
	Internal feedback (f_{CNT}), T-type, Min of $1/(t_{WLS} + t_{WHS})$ or $1/(t_{SST} + t_{COSi})$	154		154		148		143		111		105		87.0		69.0		MHz
	No feedback[2], Min of $1/(t_{WLS} + t_{WHS})$, $1/(t_{SS} + t_{HS})$ or $1/(t_{SST} + t_{HS})$	250		250		200		200		154		125		100		83.3		MHz
f_{MAXA}	External feedback, D-type, Min of $1/(t_{WLA} + t_{WHA})$ or $1/(t_{SA} + t_{COA})$	111		111		108		100		83.3		66.7		55.6		43.5		MHz
	External feedback, T-type, Min of $1/(t_{WLA} + t_{WHA})$ or $1/(t_{SAT} + t_{COA})$	105		105		102		95.2		76.9		62.5		52.6		41.7		MHz
	Internal feedback (f_{CNTA}), D-type, Min of $1/(t_{WLA} + t_{WHA})$ or $1/(t_{SA} + t_{COAi})$	133		133		125		125		105		83.3		66.7		50.0		MHz
	Internal feedback (f_{CNTA}), T-type, Min of $1/(t_{WLA} + t_{WHA})$ or $1/(t_{SAT} + t_{COAi})$	125		125		125		118		95.2		76.9		62.5		47.6		MHz
	No feedback[2], Min of $1/(t_{WLA} + t_{WHA})$, $1/(t_{SA} + t_{HA})$ or $1/(t_{SAT} + t_{HA})$	167		167		143		143		125		100		62.5		55.6		MHz
f_{MAXI}	Maximum input register frequency, Min of $1/(t_{WIRH} + t_{WIRL})$ or $1/(t_{SIRS} + t_{HIRS})$	167		167		143		143		125		100		83.3		83.3		MHz

Notes:

1. *See "Switching Test Circuit" document on the Literature Download page of the Lattice web site.*
2. *This parameter does not apply to flip-flops in the emulated mode since the feedback path is required for emulation.*

CAPACITANCE [1]

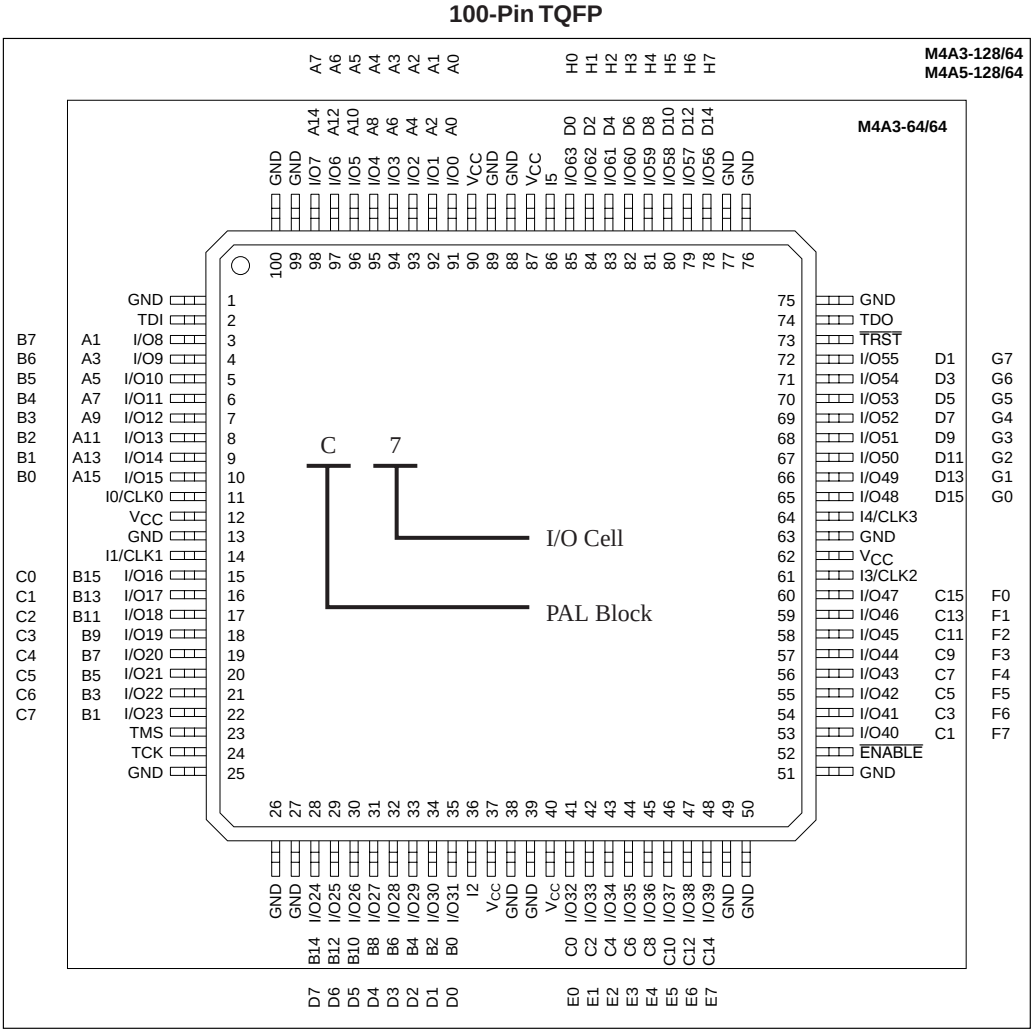
Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input capacitance	V_{IN}=2.0 V	3.3 V or 5 V, 25°C, 1 MHz	6	pF
$C_{I/O}$	Output capacitance	V_{OUT}=2.0V	3.3 V or 5 V, 25°C, 1 MHz	8	pF

Note:

1. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where this parameter may be affected.*

100-PIN TQFP CONNECTION DIAGRAM (M4A3-64/64 AND M4A(3,5)-128/64)

Top View



17466G-032a

PIN DESIGNATIONS

CLK/I = Clock or Input

GND = Ground

I = Input

I/O = Input/Output

V_{CC} = Supply Voltage

TDI = Test Data In

TCK = Test Clock

TMS = Test Mode Select

TDO = Test Data Out

$\overline{TRST}$ = Test Reset

$\overline{ENABLE}$ = Program

100-BALL caBGA CONNECTION DIAGRAM (M4A3-128/64)

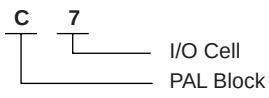
Bottom View

100-Ball caBGA

	10	9	8	7	6	5	4	3	2	1	
A	GND	I/O63 H7	I/O60 H4	I/O57 H1	GND	GND	I/O1 A1	I/O4 A4	I/O7 A7	GND	**A**
B	$\overline{\text{TRST}}$	GND	I/O61 H5	I5	VCC	I/O0 A0	I/O6 A6	GND	TDI	I/O15 B7	**B**
C	I/O53 G5	TDO	I/O62 H6	I/O58 H2	I/O56 H0	I/O2 A2	GND	I/O14 B6	I/O13 B5	I/O12 B4	**C**
D	I/O50 G2	I/O55 G7	GND	I/O59 H3	I/O3 A3	I/O5 A5	I/O11 B3	I/O10 B2	CLK0/I0	I/O9 B1	**D**
E	CLK3/I4	I/O49 G1	I/O51 G3	I/O54 G6	VCC	I/O16 C0	I/O20 C4	I/O8 B0	VCC	GND	**E**
F	GND	VCC	I/O40 F0	I/O52 G4	I/O48 G0	VCC	I/O22 C6	I/O19 C3	I/O17 C1	CLK1/I1	**F**
G	I/O41 F1	CLK2/I3	I/O42 F2	I/O43 F3	I/O37 E5	I/O35 E3	I/O27 D3	GND	I/O23 C7	I/O18 C2	**G**
H	I/O44 F4	I/O45 F5	I/O46 F6	GND	I/O34 E2	I/O24 D0	I/O26 D2	I/O30 D6	TCK	I/O21 C5	**H**
J	I/O47 F7	$\overline{\text{ENABLE}}$	GND	I/O38 E6	I/O32 E0	VCC	I2	I/O29 D5	GND	TMS	**J**
K	GND	I/O39 E7	I/O36 E4	I/O33 E1	GND	GND	I/O25 D1	I/O28 D4	I/O31 D7	GND	**K**
	10	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	

PIN DESIGNATIONS

CLK	=	Clock
GND	=	Ground
I	=	Input
I/O	=	Input/Output
N/C	=	No Connect
VCC	=	Supply Voltage
TDI	=	Test Data In
TCK	=	Test Clock
TMS	=	Test Mode Select
TDO	=	Test Data Out
$\overline{\text{TRST}}$	=	Test Reset
$\overline{\text{ENABLE}}$	=	Program

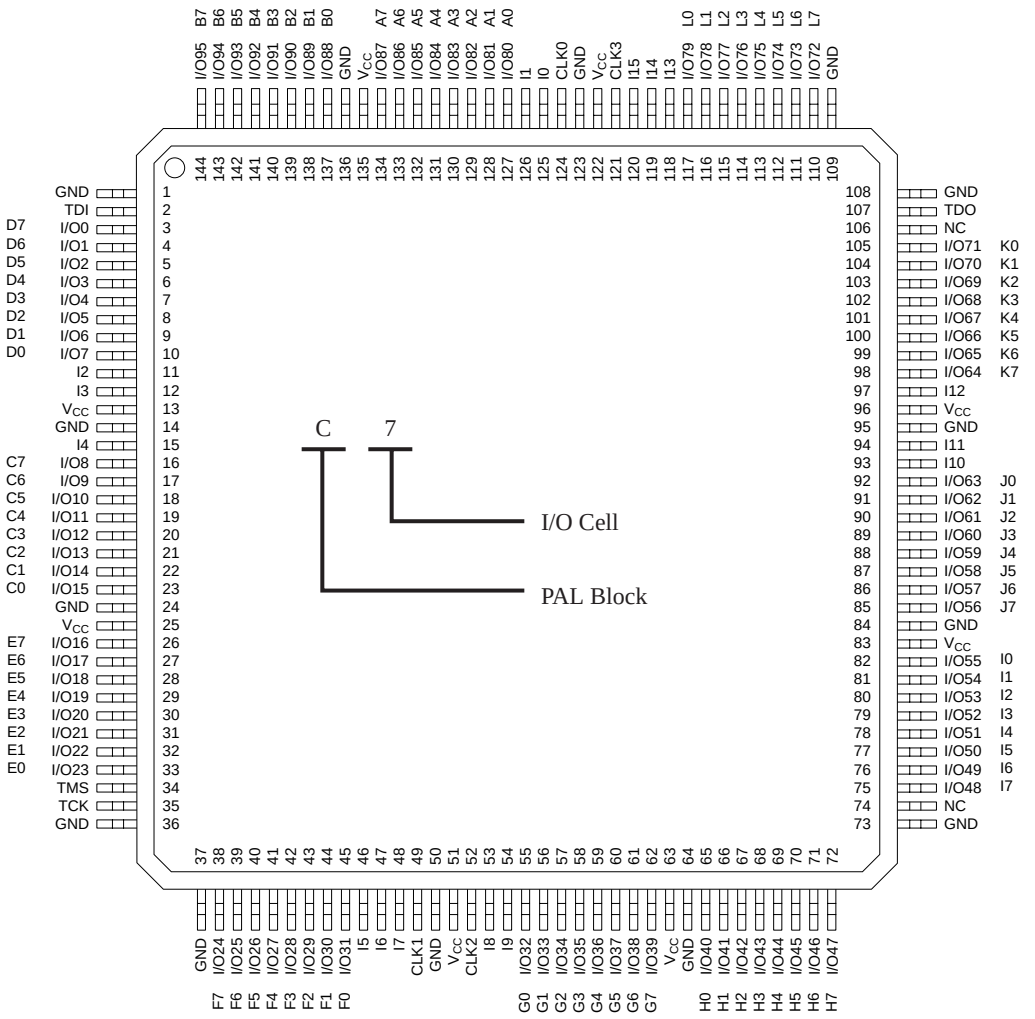


17466G-100cabga

144-PIN TQFP CONNECTION DIAGRAM (M4A(3,5)-192/96)

Top View

144-Pin TQFP



17466G-033

PIN DESIGNATIONS

CLK = Clock

GND = Ground

I = Input

I/O = Input/Output

V_{CC} = Supply Voltage

TDI = Test Data In

TCK = Test Clock

TMS = Test Mode Select

TDO = Test Data Out

256-BALL fpBGA CONNECTION DIAGRAM (M4A3-256/192)

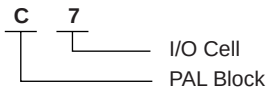
Bottom View

256-Ball fpBGA

	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	I/O167 N15	I/O181 O13	I/O180 O12	I/O177 O9	I/O174 O6	I/O172 O4	I/O191 P14	I/O186 P4	I/O1 A2	I/O3 A6	GCLK0	I/O9 B1	I/O13 B5	I/O15 B7	I/O18 B10	I/O20 B12	A
B	I/O165 N13	I/O166 N14	I/O182 O14	I/O179 O11	I/O175 O7	I/O173 O5	I/O168 O0	I/O187 P6	I/O0 A0	I/O5 A10	I/O7 A14	I/O10 B2	I/O16 B8	I/O19 B11	I/O21 B13	NC	B
C	I/O163 N11	I/O164 N12	NC	I/O183 O15	I/O178 O10	I/O170 O2	I/O171 O3	I/O189 P10	I/O184 P0	I/O6 A12	I/O12 B4	I/O14 B6	I/O23 B15	I/O22 B14	TDI	I/O39 C15	C
D	I/O158 N6	I/O159 N7	TDO	GND	GND	VCC	GND	VCC	GND	GND	VCC	GND	VCC	I/O17 B9	I/O38 C14	I/O37 C13	D
E	I/O156 N4	NC	I/O162 N10	VCC	I/O160 N8	I/O161 N9	I/O190 P12	GCLK3	I/O188 P8	I/O2 A4	I/O8 B0	NC	GND	I/O36 C12	I/O35 C11	I/O31 C7	E
F	I/O152 N0	I/O157 N5	I/O155 N3	GND	I/O154 N2	I/O153 N1	I/O176 O8	I/O169 O1	I/O185 P2	I/O4 A8	I/O11 B3	I/O34 C10	VCC	I/O32 C8	I/O30 C6	I/O29 C5	F
G	I/O147 M6	I/O150 M12	I/O149 M10	VCC	I/O148 M8	I/O151 M14	VCC	GND	GND	VCC	I/O33 C9	I/O28 C4	GND	I/O26 C2	I/O25 C1	I/O47 D14	G
H	I/O144 M0	I/O146 M4	I/145 OM2	GND	I/O136 L0	I/O137 L2	GND	VCC	VCC	GND	I/O27 C3	I/O24 C0	VCC	I/O44 D8	I/O43 D6	I/O42 D4	H
J	I/O138 L4	I/O139 L6	I/O140 L8	GND	I/O142 L12	I/O141 L10	GND	VCC	VCC	GND	I/O46 D12	I/O45 D10	GND	I/O49 E2	I/O48 E0	I/O50 E4	J
K	I/O143 L14	I/O120 K0	I/O121 K1	VCC	I/O123 K3	I/O122 K2	VCC	GND	GND	VCC	I/O41 D2	I/O40 D0	VCC	I/O55 E14	I/O54 E12	I/O56 F0	K
L	I/O124 K4	I/O125 K5	I/O127 K7	GND	I/O130 K10	I/O126 K6	I/O98 I4	I/O91 H6	I/O75 G3	I/O77 G5	I/O52 E8	I/O51 E6	GND	I/O59 F3	I/O60 F4	I/O57 F1	L
M	I/O128 K8	I/O129 K9	I/O131 K11	GND	I/O107 J3	I/O105 J1	I/O100 I8	I/O90 H4	I/O74 G2	I/O80 G8	I/O83 G11	I/O53 E10	VCC	I/O68 F12	I/O63 F7	I/O58 F2	M
N	I/O132 K12	I/O133 K13	I/O135 K15	VCC	GND	VCC	GND	VCC	GND	GND	VCC	GND	GND	TCK	I/O64 F8	I/O61 F5	N
P	I/O134 K14	I/O117 J13	I/O118 J14	I/O119 J15	I/O108 J4	I/O106 J2	I/O101 I10	I/O89 H2	I/O93 H10	I/O94 H12	I/O79 G7	I/O84 G12	I/O87 G15	TMS	I/O65 F9	I/O62 F6	P
R	I/O116 J12	I/O115 J11	I/O112 J8	I/O111 J7	I/O104 J0	I/O102 I12	I/O99 I6	I/O96 I0	I/O92 H8	I/O72 G0	I/O76 G4	I/O81 G9	I/O85 G13	I/O71 F15	I/O67 F11	I/O66 F10	R
T	I/O114 J10	I/O113 J9	I/O110 J6	I/O109 J5	I/O103 I14	GCLK2	I/O97 I2	I/O88 H0	GCLK1	I/O95 H14	I/O73 G1	I/O78 G6	I/O82 G10	I/O86 G14	I/O70 F14	I/O69 F13	T
	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

PIN DESIGNATIONS

CLK = Clock
GND = Ground
I = Input
I/O = Input/Output
N/C = No Connect
VCC = Supply Voltage
TDI = Test Data In
TCK = Test Clock
TMS = Test Mode Select
TDO = Test Data Out



17466G-047

256-BALL fpBGA CONNECTION DIAGRAM (M4A3-256/128)

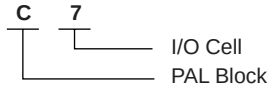
Bottom View

256-Ball fpBGA

	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	$\overline{\text{TRST}}$	I/O117 O5	I/O116 O4	I/O113 O1	I/O126 P6	I/O124 P4	I12	NC	NC	NC	CLK0	I/O1 A1	I/O5 A5	I/O7 A7	I/O10 B2	I/O12 B4	**A**
B	I/O110 N6	I/O111 N7	I/O118 O6	I/O115 O3	I/O127 P7	I/O125 P5	I/O120 P0	NC	NC	NC	I1	I/O2 A2	I/O8 B0	I/O11 B3	I/O13 B5	NC	**B**
C	I/O108 N4	I/O109 N5	NC	I/O119 O7	I/O114 O2	I/O122 P2	I/O123 P3	NC	NC	I0	I/O4 A4	I/O6 A6	I/O15 B7	I/O14 B6	TDI	I/O23 C7	**C**
D	NC	I/O104 N0	TDO	GND	GND	VCC	GND	VCC	GND	GND	VCC	GND	VCC	I/O9 B1	I/O22 C6	I/O21 C5	**D**
E	I/O102 M6	NC	I/O107 N3	VCC	I/O105 N1	I/O106 N2	I13	CLK3	NC	NC	I/O0 A0	NC	GND	I/O20 C4	I/O19 C3	I/O31 D7	**E**
F	I/O98 M2	I/O103 M7	I/O101 M5	GND	I/O100 M4	I/O99 M3	I/O112 O0	I/O121 P1	NC	NC	I/O3 A3	I/O18 C2	VCC	I/O16 C0	I/O30 D6	I/O29 D5	**F**
G	NC	I/O96 M0	I11	VCC	NC	I/O97 M1	VCC	GND	GND	VCC	I/O17 C1	I/O28 D4	GND	I/O26 D2	I/O25 D1	I2	**G**
H	I/O88 L0	I10	I9	GND	I/O89 L1	I/O90 L2	GND	VCC	VCC	GND	I/O27 D3	I/O24 D0	VCC	NC	NC	NC	**H**
J	I/O91 L3	I/O92 L4	I/O93 L5	GND	I/O95 L7	I/O94 L6	GND	VCC	VCC	GND	I3	NC	GND	NC	NC	NC	**J**
K	NC	NC	NC	VCC	NC	NC	VCC	GND	GND	VCC	NC	NC	VCC	I4	NC	I/O32 E0	**K**
L	NC	NC	I/O80 K0	GND	I/O83 K3	NC	NC	NC	I/O59 H3	I/O61 H5	NC	NC	GND	I/O35 E3	I/O36 E4	I/O33 E1	**L**
M	I/O81 K1	I/O82 K2	I/O84 K4	GND	I/O67 I3	I/O65 I1	NC	NC	I/O58 H2	I/O48 G0	I/O51 G3	NC	VCC	I/O44 F4	I/O39 E7	I/O34 E2	**M**
N	I/O85 K5	I/O86 K6	$\overline{\text{ENABLE}}$	VCC	GND	VCC	GND	VCC	GND	GND	VCC	GND	GND	TCK	I/O40 F0	I/O37 E5	**N**
P	I/O87 K7	I/O77 J5	I/O78 J6	I/O79 J7	I/O68 I4	I/O66 I2	NC	NC	NC	I6	I/O63 H7	I/O52 G4	I/O55 G7	TMS	I/O41 F1	I/O38 E6	**P**
R	I/O76 J4	I/O75 J3	I/O72 J0	I/O71 I7	I/O64 I0	I7	NC	NC	NC	I/O56 H0	I/O60 H4	I/O49 G1	I/O53 G5	I/O47 F7	I/O43 F3	I/O42 F2	**R**
T	I/O74 J2	I/O73 J1	I/O70 I6	I/O69 I5	I8	CLK2	NC	NC	CLK1	I5	I/O57 H1	I/O62 H6	I/O50 G2	I/O54 G6	I/O46 F6	I/O45 F5	**T**
	16	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	

PIN DESIGNATIONS

CLK = Clock
GND = Ground
I = Input
I/O = Input/Output
N/C = No Connect
VCC = Supply Voltage
TDI = Test Data In
TCK = Test Clock
TMS = Test Mode Select
$\overline{\text{TDO}}$ = Test Data Out
$\overline{\text{TRST}}$ = Test Reset
$\overline{\text{ENABLE}}$ = Program



m4a3.256.128_256bga

388-BALL fpBGA CONNECTION DIAGRAM (M4A3-512/256)

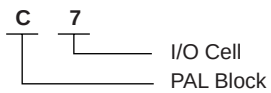
Bottom View

388-Ball fpBGA

	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	GND	I/O243 OX3	I/O240 OX0	I/O241 OX1	I/O236 NX4	I/O231 MX7	I/O228 MX4	I/O226 MX2	I/O255 PX7	I/O251 PX3	I/O248 PX0	I/O0 A0	I/O5 A5	I/O6 A6	I/O27 D3	I/O30 D6	I/O17 C1	I/O22 C6	I/O8 B0	I/O10 B2	N/C	GND	**A**
B	N/C	GND	I/O245 OX5	I/O242 OX2	I/O238 NX6	I/O234 NX2	I/O232 NX0	I/O229 MX5	I/O224 MX0	I/O253 PX5	I/O249 PX1	I/O2 A2	CLK0	I/O26 D2	I/O29 D5	I/O31 D7	I/O20 C4	I/O9 B1	I/O12 B4	I/O13 B5	GND	TDI	**B**
C	I/O213 KX5	TDO	GND	I/O247 OX7	I/O244 OX4	I/O239 NX7	I/O235 NX3	I/O230 MX6	I/O227 MX3	CLK3	I/O250 PX2	I/O1 A1	I/O7 A7	I/O25 D1	I/O16 C0	I/O18 C2	I/O23 C7	I/O11 B3	I/O15 B7	GND	I/O47 F7	I/O44 F4	**C**
D	I/O210 KX2	I/O212 KX4	I/O215 KX7	GND	I/O246 OX6	VCC	I/O237 NX5	I/O233 NX1	VCC	I/O254 PX6	VCC	I/O3 A3	I/O24 D0	VCC	I/O19 C3	I/O21 C5	VCC	I/O14 B6	GND	I/O46 F6	I/O43 F3	I/O41 F1	**D**
E	I/O207 JX7	I/O209 KX1	I/O211 KX3	I/O214 KX6															I/O45 F5	I/O42 F2	I/O40 F0	I/O54 G6	**E**
F	I/O203 JX3	I/O205 JX5	I/O208 KX0	VCC															VCC	I/O55 G7	I/O52 G4	I/O50 G2	**F**
G	I/O200 JX0	I/O202 JX2	I/O204 JX4	I/O206 JX6			VCC	VCC	N/C	I/O225 MX1	I/O252 PX4	I/O4 A4	I/O28 D4	N/C	VCC	VCC			I/O53 G5	I/O51 G3	I/O49 G1	I/O39 E7	**G**
H	I/O221 LX5	I/O222 LX6	I/O223 LX7	I/O201 JX1			VCC	N/C	GND	GND	GND	GND	GND	GND	N/C	VCC			I/O48 G0	I/O38 E6	I/O37 E5	I/O36 E4	**H**
J	I/O218 LX2	I/O219 LX3	I/O220 LX4	VCC			N/C	GND	GND	GND	GND	GND	GND	GND	GND	N/C			VCC	I/O35 E3	I/O34 E2	I/O32 E0	**J**
K	I/O197 IX5	I/O198 IX6	I/O199 IX7	I/O216 LX0			I/O217 LX1	GND	GND	GND	GND	GND	GND	GND	GND	I/O33 E1			I/O63 H7	I/O62 H6	I/O61 H5	I/O60 H4	**K**
L	I/O192 IX0	I/O194 IX2	I/O195 IX3	I/O196 IX4			I/O193 IX1	GND	GND	GND	GND	GND	GND	GND	GND	I/O58 H2			VCC	I/O59 H3	I/O57 H1	I/O56 H0	**L**
M	I/O184 HX0	I/O185 HX1	I/O187 HX3	VCC			I/O186 HX2	GND	GND	GND	GND	GND	GND	GND	GND	I/O69 I5			I/O67 I3	I/O65 I1	I/O66 I2	I/O64 I0	**M**
N	I/O188 HX4	I/O189 HX5	I/O191 HX7	I/O190 HX6			I/O162 EX2	GND	GND	GND	GND	GND	GND	GND	GND	I/O89 L1			I/O88 L0	I/O71 I7	I/O70 I6	I/O68 I4	**N**
P	I/O160 EX0	I/O161 EX1	I/O163 EX3	VCC			N/C	GND	GND	GND	GND	GND	GND	GND	GND	N/C			VCC	I/O92 L4	I/O91 L3	I/O90 L2	**P**
R	I/O164 EX4	I/O165 EX5	I/O166 EX6	I/O177 GX1			VCC	N/C	GND	GND	GND	GND	GND	GND	N/C	VCC			I/O74 J2	I/O95 L7	I/O94 L6	I/O93 L5	**R**
T	I/O167 EX7	I/O176 GX0	I/O179 GX3	I/O181 GX5			VCC	VCC	N/C	I/O152 DX0	I/O131 AX3	I/O122 P2	I/O98 M2	N/C	VCC	VCC			I/O78 J6	I/O76 J4	I/O73 J1	I/O72 J0	**T**
U	I/O178 GX2	I/O180 GX4	I/O183 GX7	VCC															VCC	I/O80 K0	I/O77 J5	I/O75 J3	**U**
V	I/O182 GX6	N/C	I/O169 FX1	I/O172 FX4															I/O86 K6	I/O83 K3	I/O81 K1	I/O79 J7	**V**
W	I/O168 FX0	I/O170 FX2	I/O173 FX5	GND	I/O143 BX7	VCC	I/O150 CX6	I/O145 CX1	VCC	I/O153 DX1	I/O123 P3	VCC	I/O96 M0	VCC	I/O104 N0	I/O111 N7	VCC	I/O119 O7	GND	I/O87 K7	I/O84 K4	I/O82 K2	**W**
Y	I/O171 FX3	I/O174 FX6	GND	I/O141 BX5	I/O138 BX2	I/O136 BX0	I/O147 CX3	I/O158 DX6	I/O156 DX4	CLK2	I/O132 AX4	I/O121 P1	I/O125 P5	I/O99 M3	I/O101 M5	I/O106 N2	I/O110 N6	I/O115 O3	I/O118 O6	GND	TMS	I/O85 K5	**Y**
AA	I/O175 FX7	GND	I/O142 BX6	I/O140 BX4	I/O151 CX7	I/O149 CX5	I/O144 CX0	I/O157 DX5	I/O154 DX2	I/O134 AX6	I/O130 AX2	I/O128 AX0	CLK1	I/O127 P7	I/O100 M4	I/O103 M7	I/O108 N4	I/O109 N5	I/O113 O1	I/O116 O4	GND	TCK	**AA**
AB	GND	N/C	I/O139 BX3	I/O137 BX1	I/O148 CX4	I/O146 CX2	I/O159 DX7	I/O155 DX3	I/O135 AX7	I/O133 AX5	I/O129 AX1	I/O120 P0	I/O124 P4	I/O126 P6	I/O97 M1	I/O102 M6	I/O105 N1	I/O107 N3	I/O112 O0	I/O114 O2	I/O117 O5	GND	**AB**
	22	**21**	**20**	**19**	**18**	**17**	**16**	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	

PIN DESIGNATIONS

CLK	=	Clock
GND	=	Ground
I	=	Input
I/O	=	Input/Output
N/C	=	No Connect
VCC	=	Supply Voltage
TDI	=	Test Data In
TCK	=	Test Clock
TMS	=	Test Mode Select
TDO	=	Test Data Out



m4a3.512.256_388bga