Lattice Semiconductor Corporation - M4A3-384/160-14YI Datasheet

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Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	14 ns
Voltage Supply - Internal	3V ~ 3.6V
Number of Logic Elements/Blocks	-
Number of Macrocells	384
Number of Gates	-
Number of I/O	160
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/m4a3-384-160-14yi

The ispMACH 4A family offers 20 density-I/O combinations in Thin Quad Flat Pack (TQFP), Plastic Quad Flat Pack (PQFP), Plastic Leaded Chip Carrier (PLCC), Ball Grid Array (BGA), fine-pitch BGA (fpBGA), and chip-array BGA (caBGA) packages ranging from 44 to 388 pins (Table 3). It also offers I/O safety features for mixed-voltage designs so that the 3.3-V devices can accept 5-V inputs, and 5-V devices do not overdrive 3.3-V inputs. Additional features include Bus-Friendly inputs and I/Os, a programmable power-down mode for extra power savings and individual output slew rate control for the highest speed transition or for the lowest noise transition.

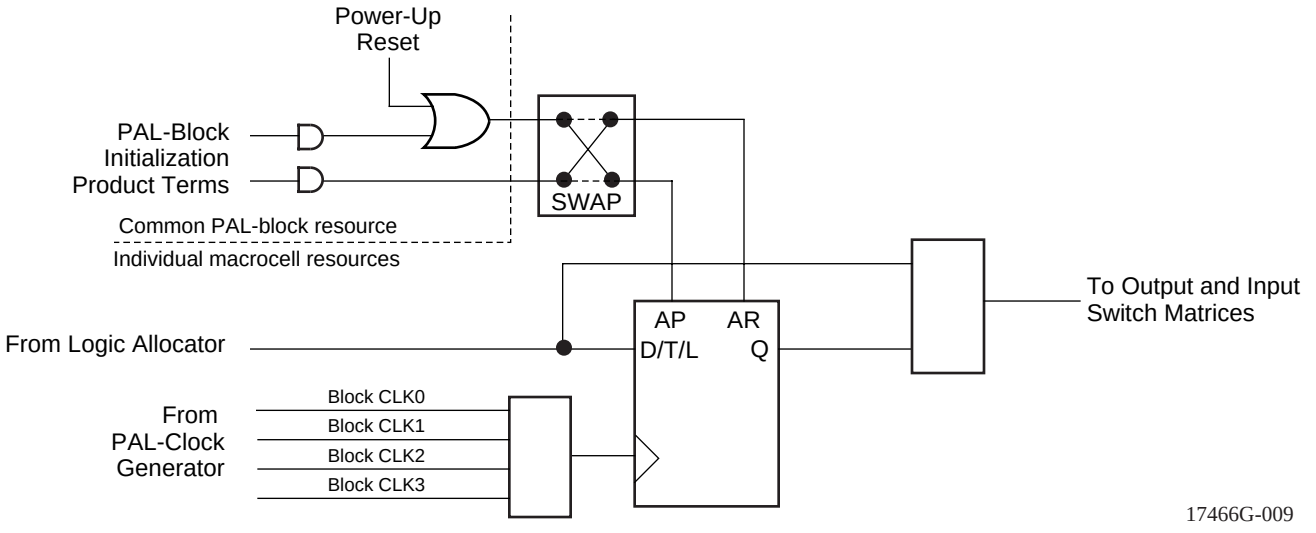
Table 3. ispMACH 4A Package and I/O Options (Number of I/Os and dedicated inputs in Table)

3.3 V Devices								
Package	**M4A3-32**	**M4A3-64**	**M4A3-96**	**M4A3-128**	**M4A3-192**	**M4A3-256**	**M4A3-384**	**M4A3-512**
44-pin PLCC	32+2	32+2						
44-pin TQFP	32+2	32+2						
48-pin TQFP	32+2	32+2						
100-pin TQFP		64+6	48+8	64+6				
100-pin PQFP				64+6				
100-ball caBGA				64+6				
144-pin TQFP					96+16			
144-ball fpBGA					96+16			
208-pin PQFP						128+14, 160	160	160
256-ball fpBGA						128+14, 192	192	192
256-ball BGA						128+14	192	
388-ball fpBGA								256

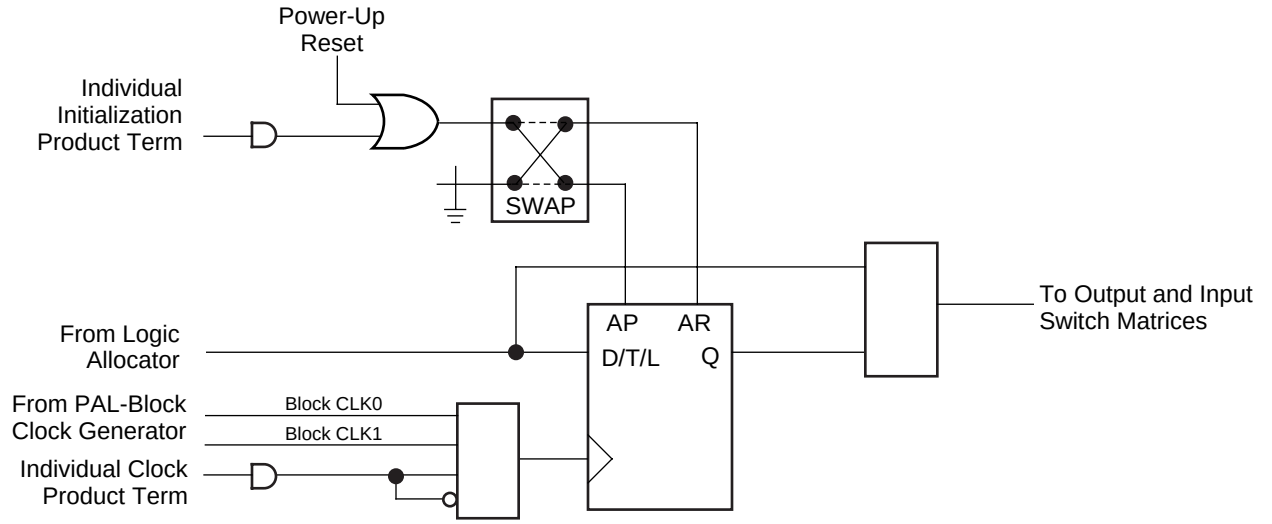
5 V Devices						
Package	**M4A5-32**	**M4A5-64**	**M4A5-96**	**M4A5-128**	**M4A5-192**	**M4A5-256**
44-pin PLCC	32+2	32+2				
44-pin TQFP	32+2	32+2				
48-pin TQFP	32+2	32+2				
100-pin TQFP			48+8	64+6		
100-pin PQFP				64+6		
144-pin TQFP					96+16	
208-pin PQFP						128+14

Macrocell

The macrocell consists of a storage element, routing resources, a clock multiplexer, and initialization control. The macrocell has two fundamental modes: synchronous and asynchronous (Figure 5). The mode chosen only affects clocking and initialization in the macrocell.



a. Synchronous mode

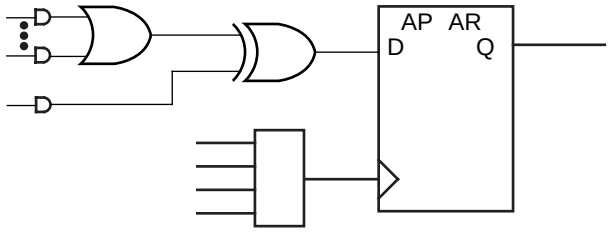


b. Asynchronous mode

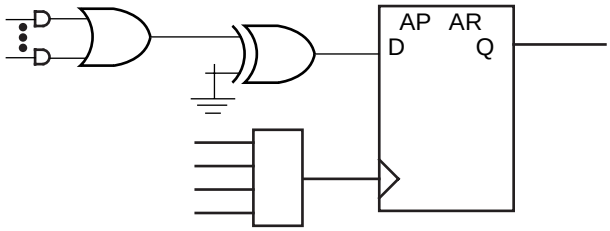
Figure 5. Macrocell

In either mode, a combinatorial path can be used. For combinatorial logic, the synchronous mode will generally be used, since it provides more product terms in the allocator.

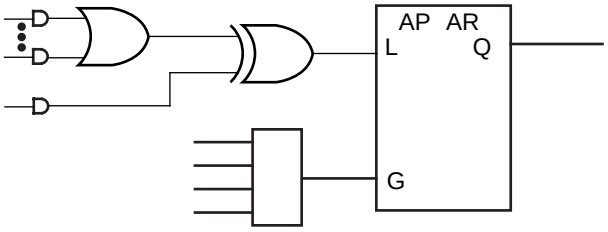
The flip-flop can be configured as a D-type or T-type latch. J-K or S-R registers can be synthesized. The primary flip-flop configurations are shown in Figure 6, although others are possible. Flip-flop functionality is defined in Table 8. Note that a J-K latch is inadvisable as it will cause oscillation if both J and K inputs are HIGH.



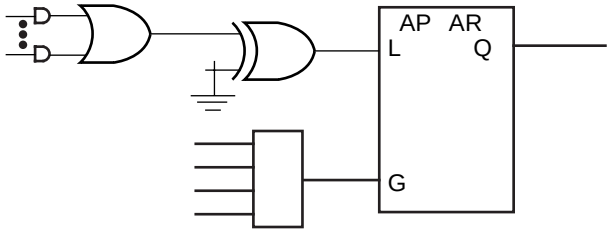
a. D-type with XOR



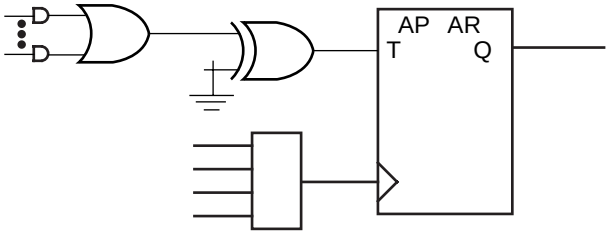
b. D-type with programmable D polarity



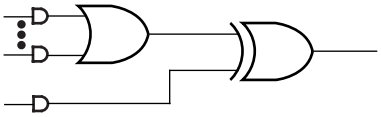
c. Latch with XOR



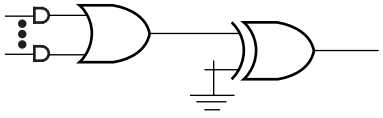
d. Latch with programmable D polarity



e. T-type with programmable T polarity



f. Combinatorial with XOR



g. Combinatorial with programmable polarity

17466G-011

Figure 6. Primary Macrocell Configurations

A reset/preset swapping feature in each macrocell allows for reset and preset to be exchanged, providing flexibility. In asynchronous mode (Figure 8), a single individual product term is provided for initialization. It can be selected to control reset or preset.

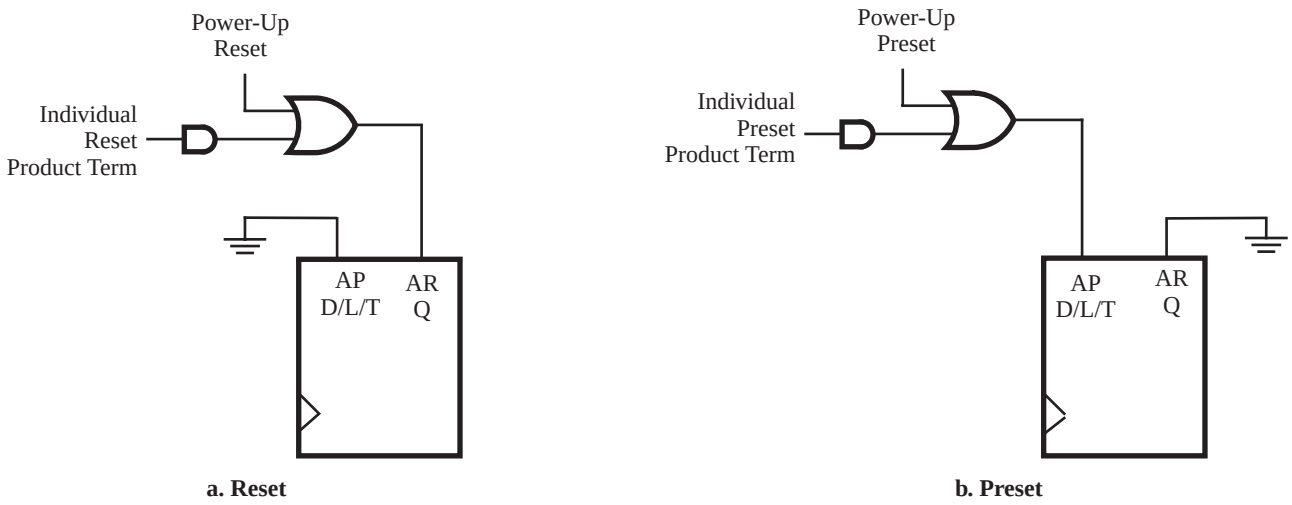


Figure 8. Asynchronous Mode Initialization Configurations

Note that the reset/preset swapping selection feature effects power-up reset as well. The initialization functionality of the flip-flops is illustrated in Table 9. The macrocell sends its data to the output switch matrix and the input switch matrix. The output switch matrix can route this data to an output if so desired. The input switch matrix can send the signal back to the central switch matrix as feedback.

Table 9. Asynchronous Reset/Preset Operation

AR	AP	CLK/LE[1]	Q+
0	0	X	See Table 8
0	1	X	1
1	0	X	0
1	1	X	0

Note:

1. Transparent latch is unaffected by AR, AP

weakly pulled up. For the circuit diagram, please refer to the document entitled *MACH Endurance Characteristics* on the Lattice Data Book CD-ROM or Lattice web site.

POWER MANAGEMENT

Each individual PAL block in ispMACH 4A devices features a programmable low-power mode, which results in power savings of up to 50%. The signal speed paths in the low-power PAL block will be slower than those in the non-low-power PAL block. This feature allows speed critical paths to run at maximum frequency while the rest of the signal paths operate in the low-power mode.

PROGRAMMABLE SLEW RATE

Each ispMACH 4A device I/O has an individually programmable output slew rate control bit. Each output can be individually configured for the higher speed transition (3 V/ns) or for the lower noise transition (1 V/ns). For high-speed designs with long, unterminated traces, the slow-slew rate will introduce fewer reflections, less noise, and keep ground bounce to a minimum. For designs with short traces or well terminated lines, the fast slew rate can be used to achieve the highest speed. The slew rate is adjusted independent of power.

POWER-UP RESET/SET

All flip-flops power up to a known state for predictable system initialization. If a macrocell is configured to SET on a signal from the control generator, then that macrocell will be SET during device power-up. If a macrocell is configured to RESET on a signal from the control generator or is not configured for set/reset, then that macrocell will RESET on power-up. To guarantee initialization values, the V_{CC} rise must be monotonic, and the clock must be inactive until the reset delay time has elapsed.

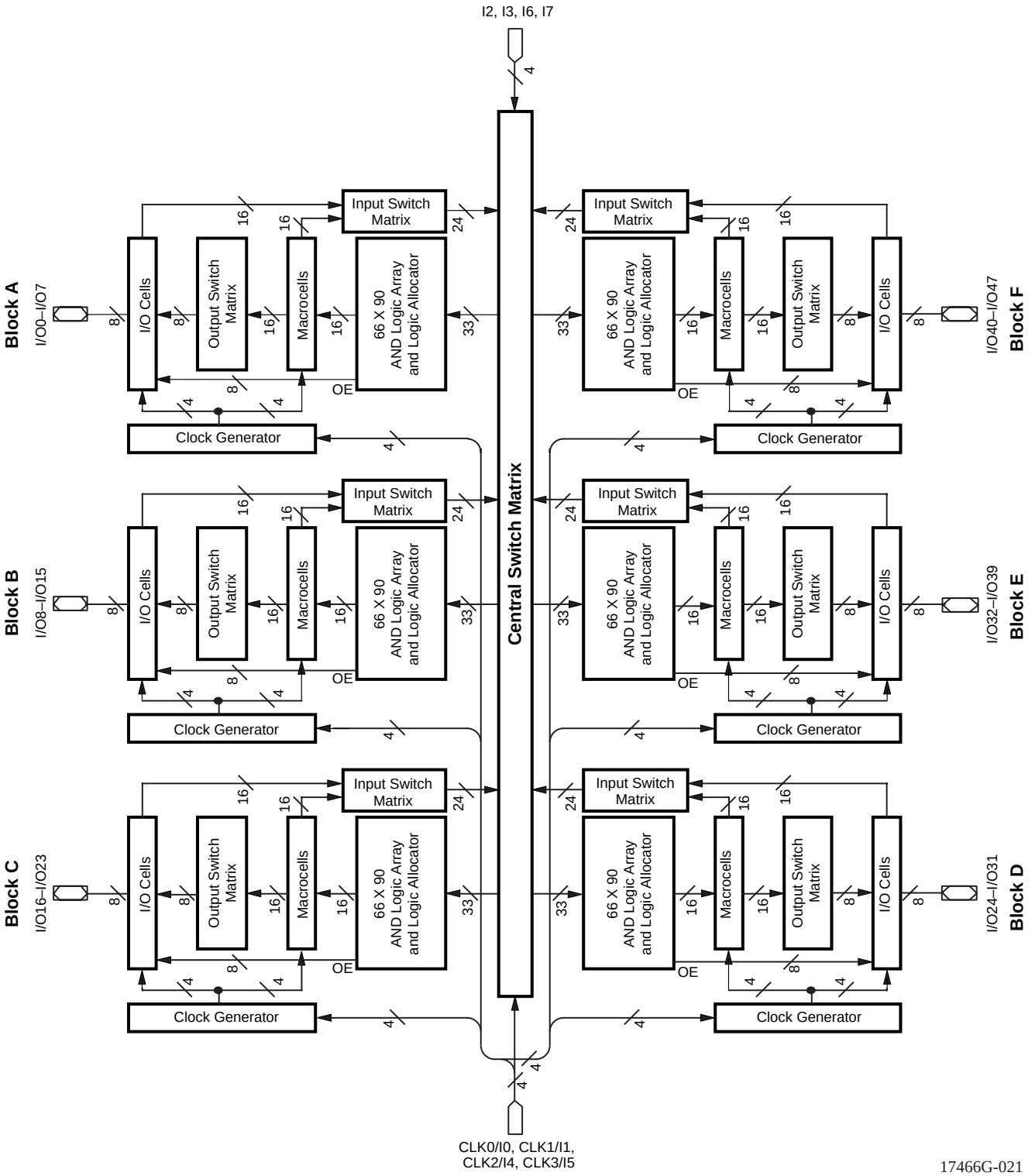
SECURITY BIT

A programmable security bit is provided on the ispMACH 4A devices as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, this bit defeats readback of the programmed pattern by a device programmer, securing proprietary designs from competitors. Programming and verification are also defeated by the security bit. The bit can only be reset by erasing the entire device.

HOT SOCKETING

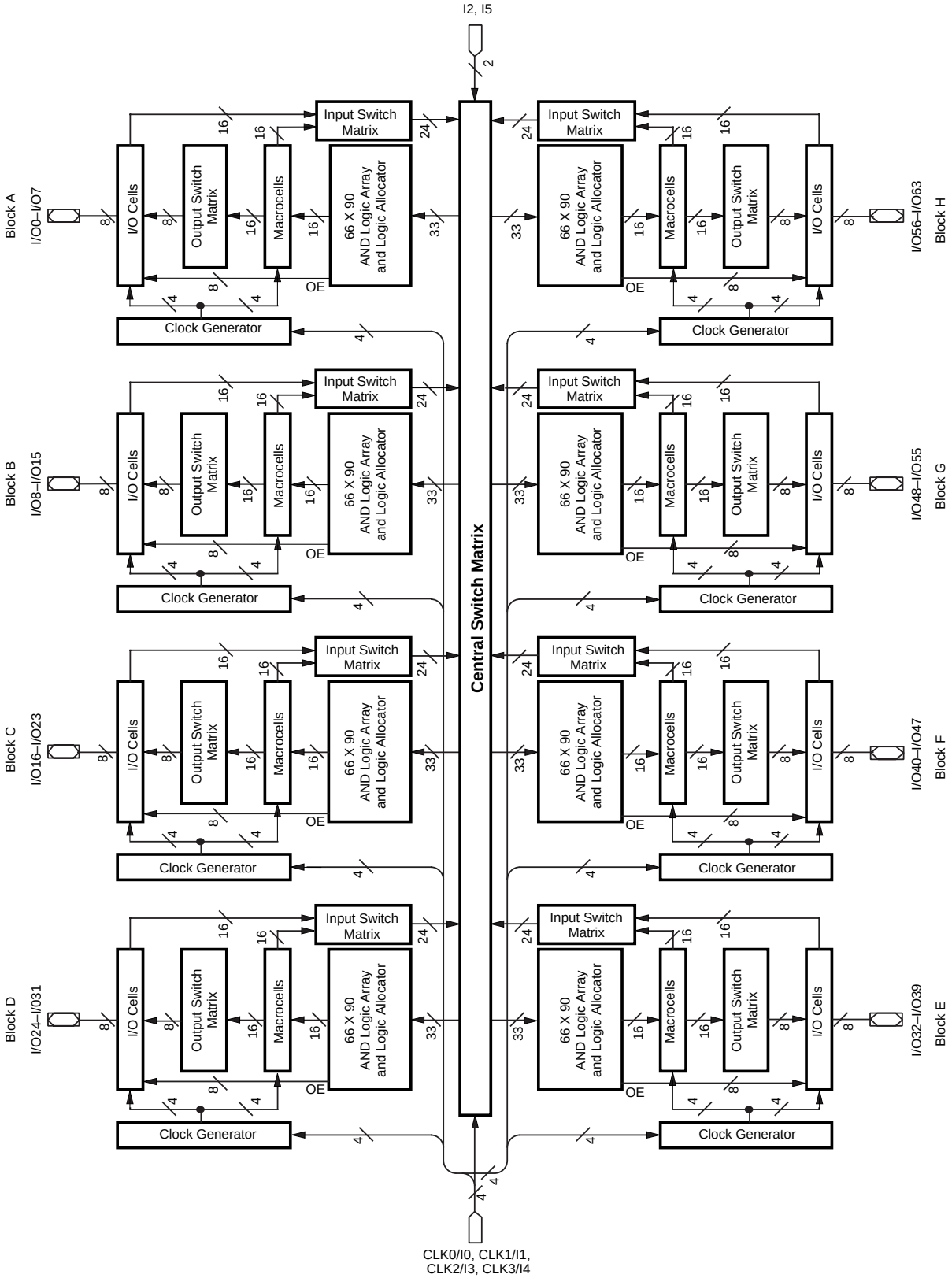
ispMACH 4A devices are well-suited for those applications that require hot socketing capability. Hot socketing a device requires that the device, when powered down, can tolerate active signals on the I/Os and inputs without being damaged. Additionally, it requires that the effects of the powered-down MACH devices be minimal on active signals.

BLOCK DIAGRAM – M4A(3,5)-96/48



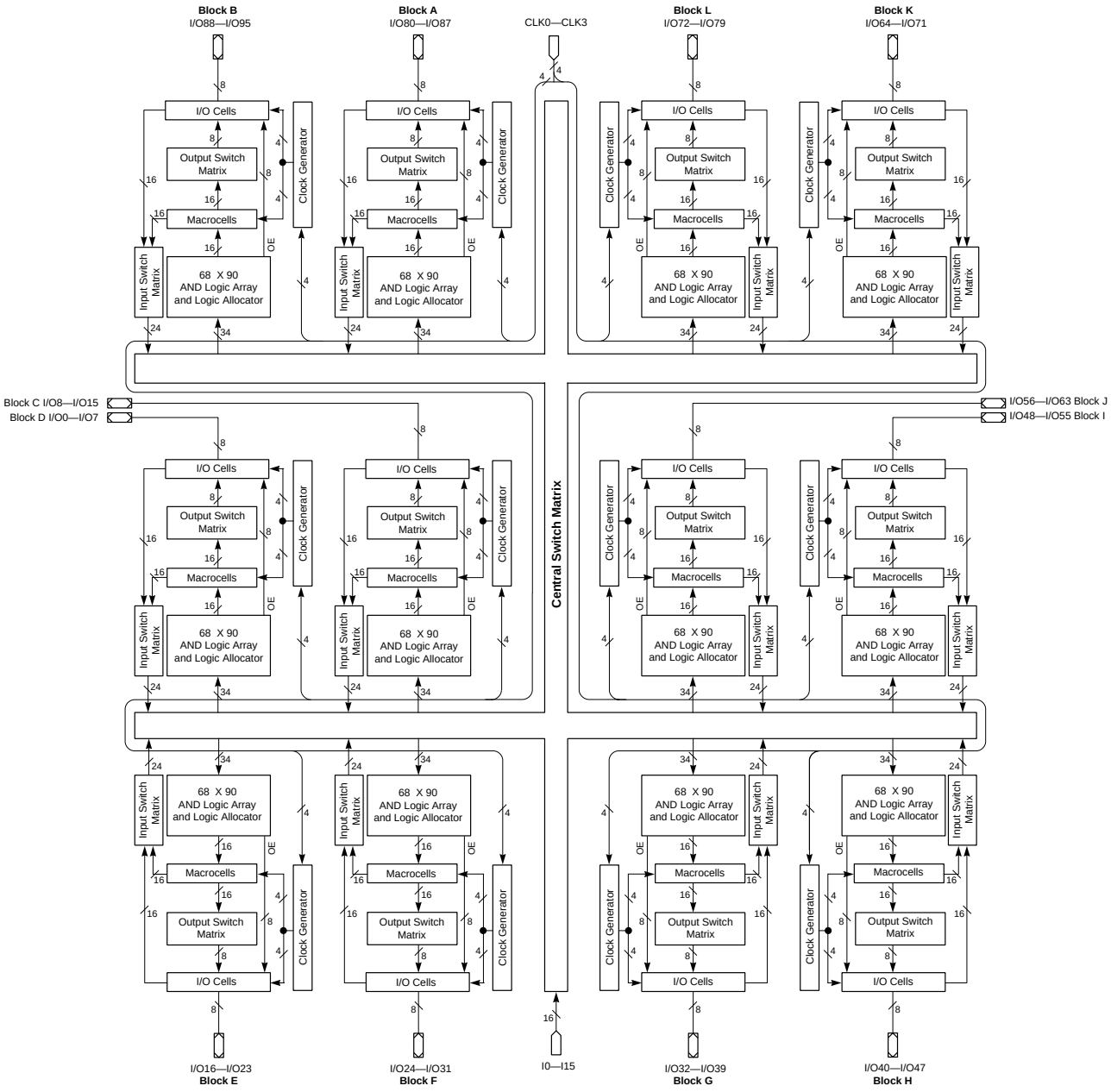
17466G-021

BLOCK DIAGRAM – M4A(3,5)-128/64



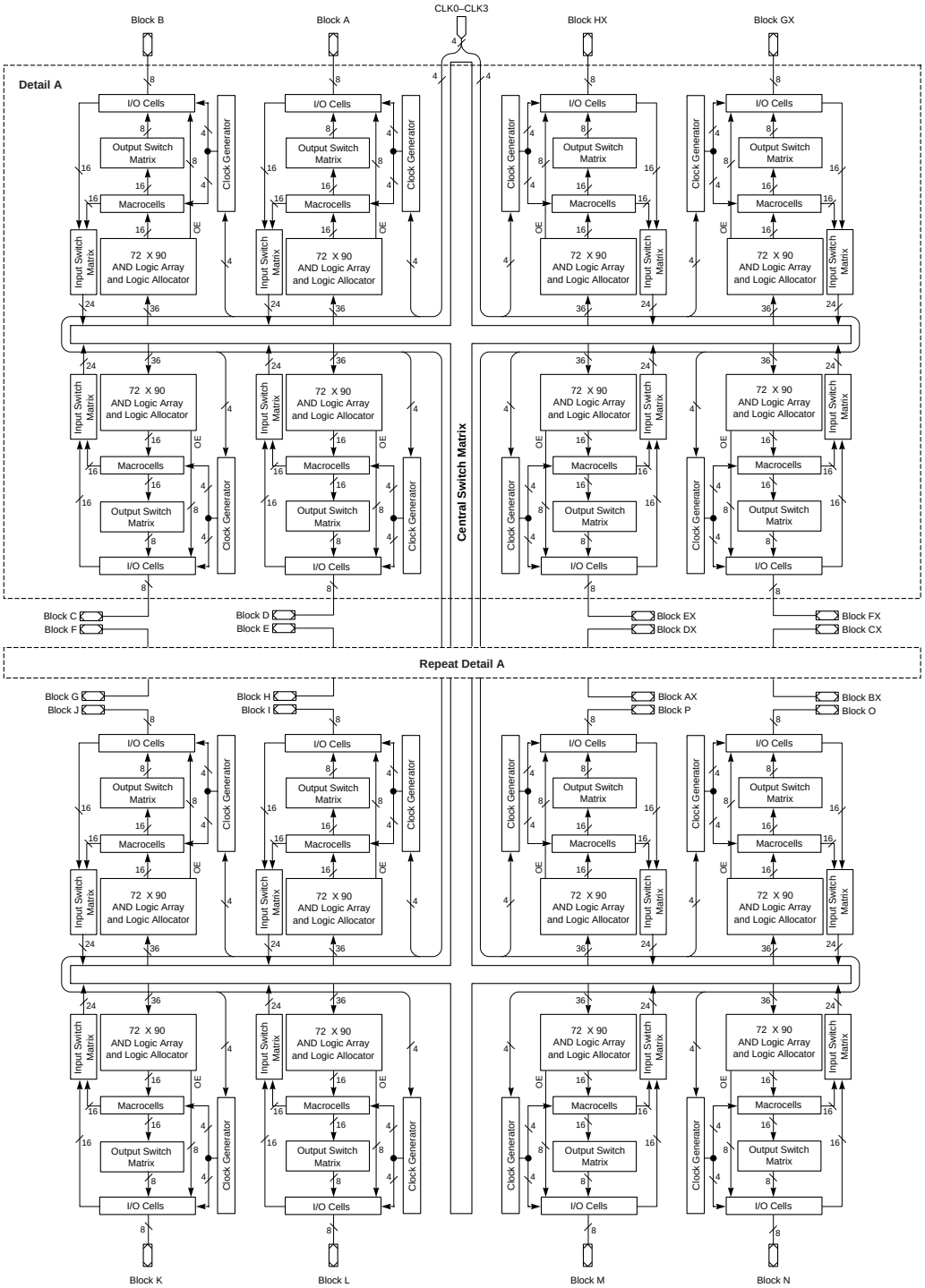
17466H-022

BLOCK DIAGRAM – M4A(3,5)-192/96



17466G-067

BLOCK DIAGRAM – M4A3-384/160, M4A3-384/192



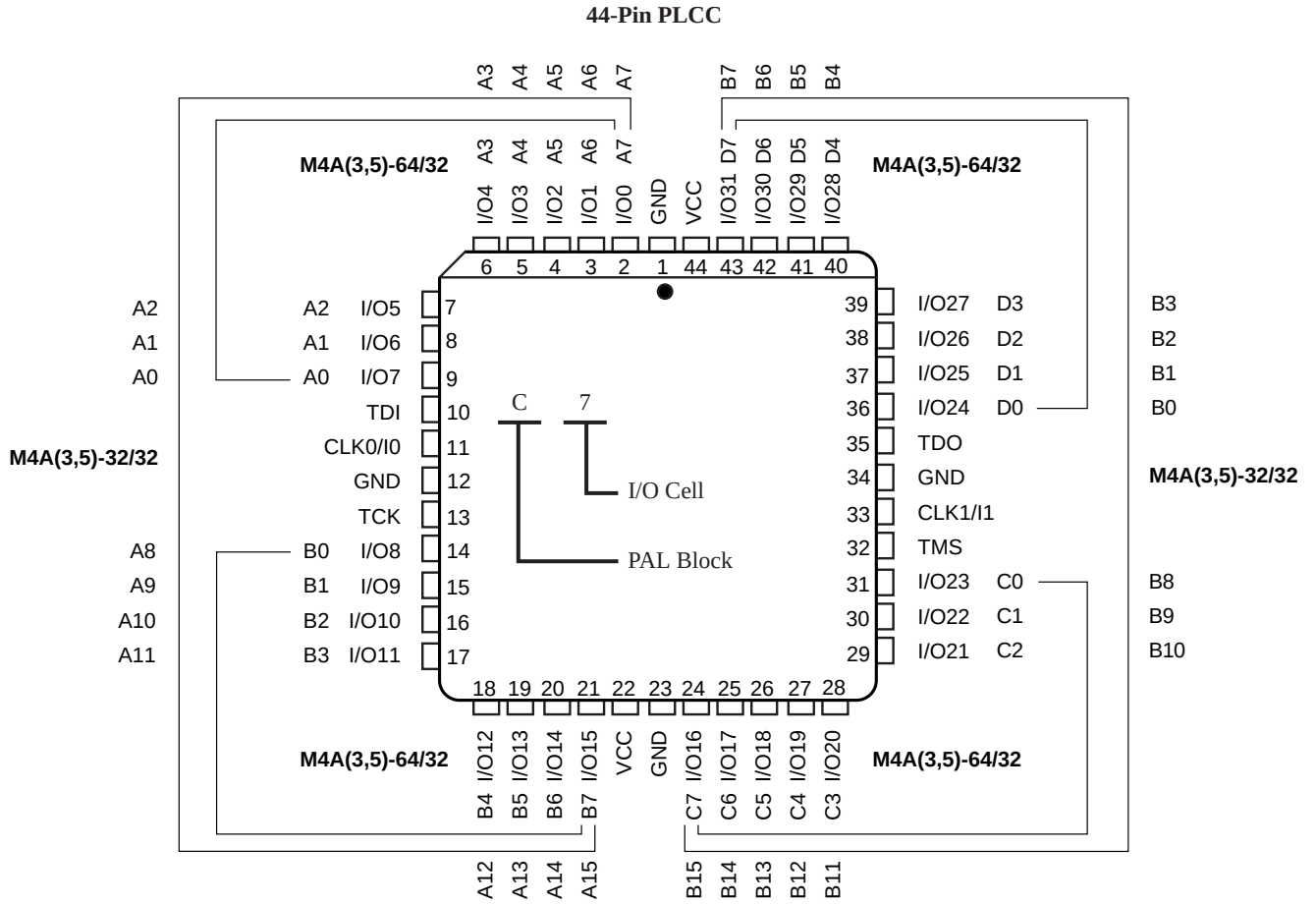
17466G-067

ispMACH 4A TIMING PARAMETERS OVER OPERATING RANGES[1]

		-5		-55		-6		-65		-7		-10		-12		-14		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit
Input Register Delays with ZHT Option:																		
t_{SIRZ}	Input register setup time - ZHT	6.0		6.0		6.0		6.0		6.0		6.0		6.0		6.0		ns
t_{HIRZ}	Input register hold time - ZHT	0.0		0.0		0.0		0.0		0.0		0.0		0.0		0.0		ns
Input Latch Delays with ZHT Option:																		
t_{SILZ}	Input latch setup time - ZHT	6.0		6.0		6.0		6.0		6.0		6.0		6.0		6.0		ns
t_{HILZ}	Input latch hold time - ZHT	0.0		0.0		0.0		0.0		0.0		0.0		0.0		0.0		ns
t_{PDILZi}	Transparent input latch to internal feedback - ZHT		6.0		6.0		6.0		6.0		6.0		6.0		6.0		6.0	ns
Output Delays:																		
t_{BUF}	Output buffer delay		1.5		1.5		1.8		2.0		2.5		3.0		3.0		3.0	ns
t_{SLW}	Slow slew rate delay adder		2.5		2.5		2.5		2.5		2.5		2.5		2.5		2.5	ns
t_{EA}	Output enable time		7.5		7.5		8.5		8.5		9.5		10.0		12.0		15.0	ns
t_{ER}	Output disable time		7.5		7.5		8.5		8.5		9.5		10.0		12.0		15.0	ns
Power Delay:																		
t_{PL}	Power-down mode delay adder		2.5		2.5		2.5		2.5		2.5		2.5		2.5		2.5	ns
Reset and Preset Delays:																		
t_{SRi}	Asynchronous reset or preset to internal register output		7.5		7.7		8.0		8.0		9.5		11.0		13.0		16.0	ns
t_{SR}	Asynchronous reset or preset to register output		9.0		9.2		10.0		10.0		12.0		14.0		16.0		19.0	ns
t_{SRR}	Asynchronous reset and preset register recovery time	7.0		7.0		7.5		7.5		8.0		8.0		10.0		15.0		ns
t_{SRW}	Asynchronous reset or preset width	7.0		7.0		8.0		8.0		10.0		10.0		12.0		15.0		ns
Clock/LE Width:																		
t_{WLS}	Global clock width low	2.0		2.0		2.5		2.5		3.0		4.0		5.0		6.0		ns
t_{WHS}	Global clock width high	2.0		2.0		2.5		2.5		3.0		4.0		5.0		6.0		ns
t_{WLA}	Product term clock width low	3.0		3.0		3.5		3.5		4.0		5.0		8.0		9.0		ns
t_{WHA}	Product term clock width high	3.0		3.0		3.5		3.5		4.0		5.0		8.0		9.0		ns
t_{GWS}	Global gate width low (for low transparent) or high (for high transparent)	4.0		4.0		4.5		4.5		5.0		5.0		6.0		6.0		ns
t_{GWA}	Product term gate width low (for low transparent) or high (for high transparent)	4.0		4.0		4.5		4.5		5.0		5.0		6.0		9.0		ns
t_{WIRL}	Input register clock width low	3.0		3.0		3.5		3.5		4.0		5.0		6.0		6.0		ns
t_{WIRH}	Input register clock width high	3.0		3.0		3.5		3.5		4.0		5.0		6.0		6.0		ns
t_{WIL}	Input latch gate width	4.0		4.0		4.5		4.5		5.0		5.0		6.0		6.0		ns

44-PIN PLCC CONNECTION DIAGRAM (M4A(3,5)-32/32 AND M4A(3,5)-64/32)

Top View



17466G-026

PIN DESIGNATIONS

CLK/I = Clock or Input

GND = Ground

I/O = Input/Output

V_{CC} = Supply Voltage

TDI = Test Data In

TCK = Test Clock

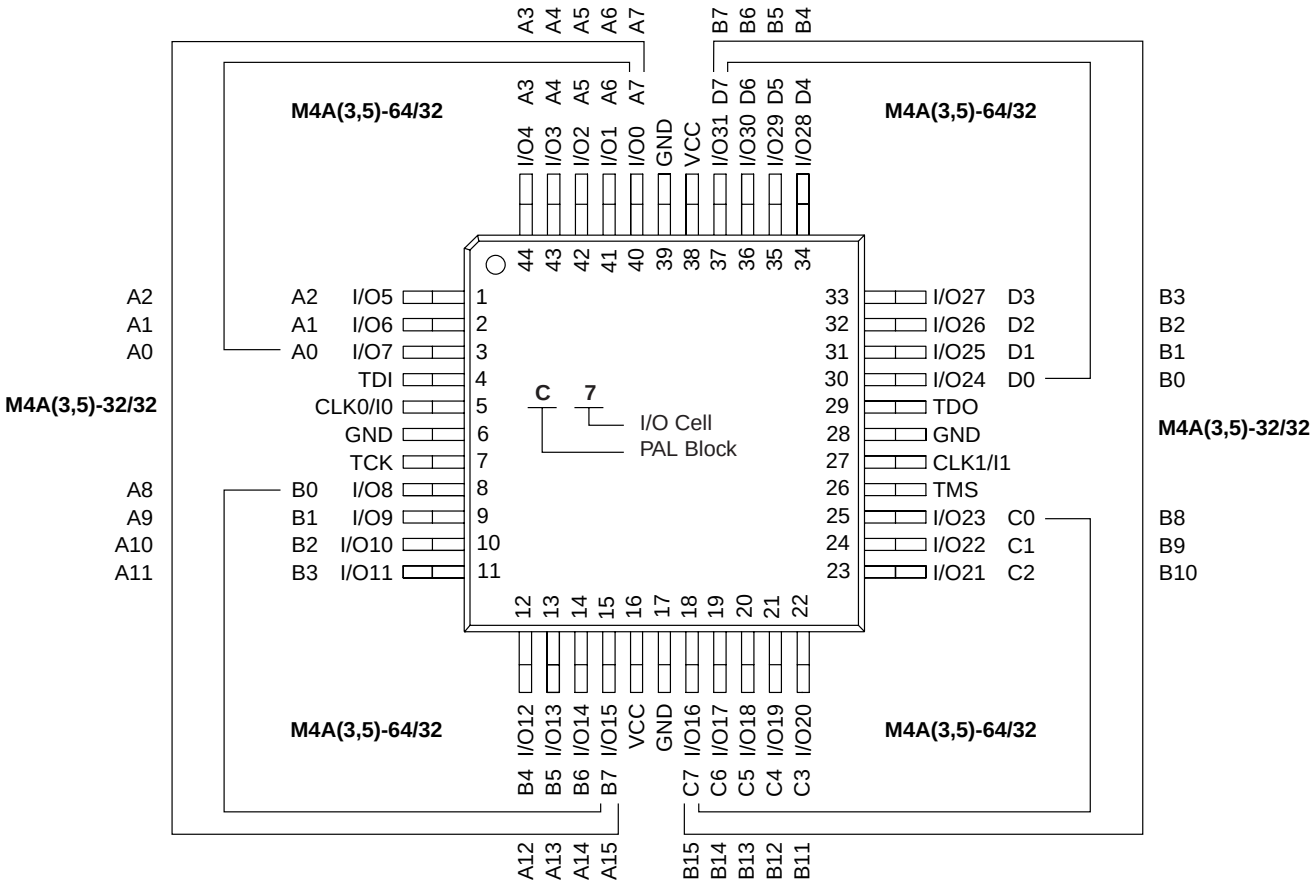
TMS = Test Mode Select

TDO = Test Data Out

44-PIN TQFP CONNECTION DIAGRAM (M4A(3,5)-32/32 AND M4A(3,5)-64/32)

Top View

44-Pin TQFP (1.0mm Thickness)



PIN DESIGNATIONS

CLK/I = Clock or Input

GND = Ground

I/O = Input/Output

V_{CC} = Supply Voltage

TDI = Test Data In

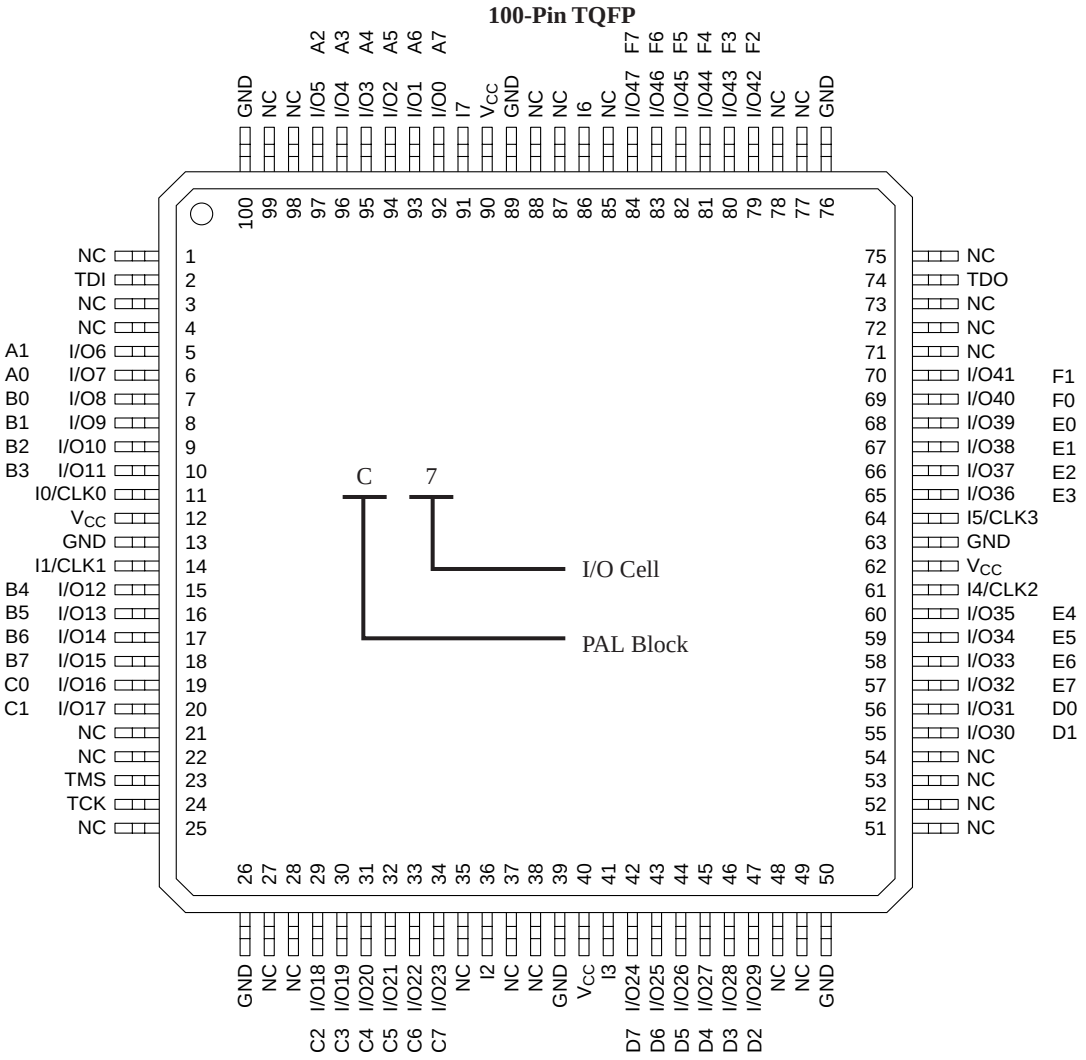
TCK = Test Clock

TMS = Test Mode Select

TDO = Test Data Out

100-PIN TQFP CONNECTION DIAGRAM (M4A(3,5)-96/48)

Top View



17466G-029

PIN DESIGNATIONS

CLK/I = Clock or Input

GND = Ground

I = Input

I/O = Input/Output

V_{CC} = Supply Voltage

NC = No Connect

TDI = Test Data In

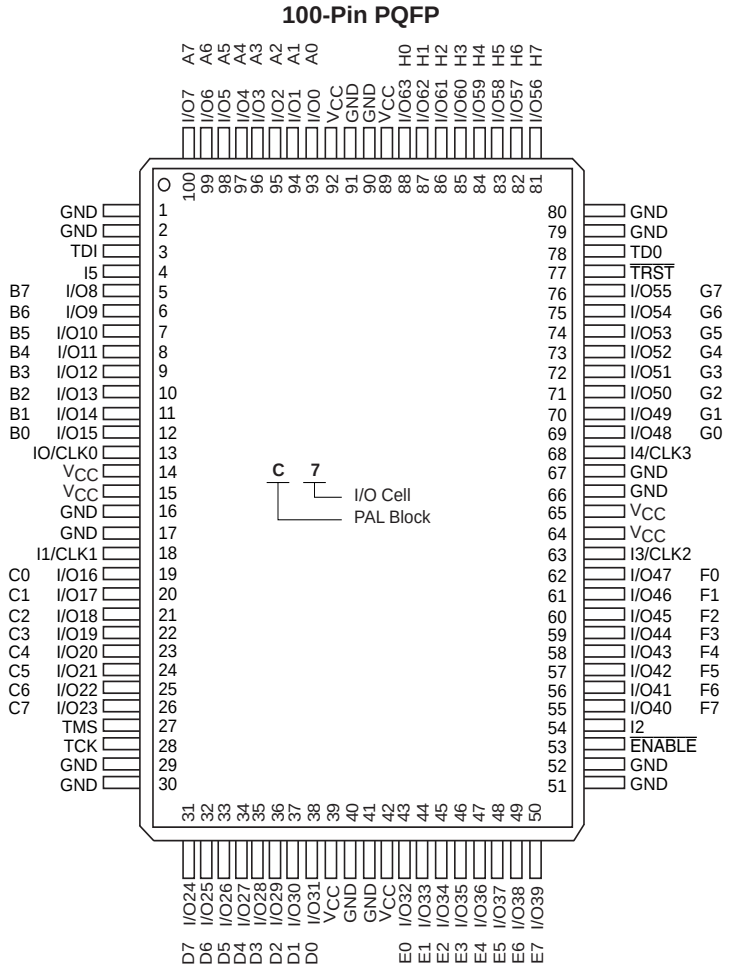
TCK = Test Clock

TMS = Test Mode Select

TDO = Test Data Out

100-PIN PQFP CONNECTION DIAGRAM (M4A(3,5)-128/64)

Top View



PIN DESIGNATIONS

I/CLK = Input or Clock

GND = Ground

I = Input

I/O = Input/Output

V_{CC} = Supply Voltage

TDI = Test Data In

TCK = Test Clock

TMS = Test Mode Select

TDO = Test Data Out

$\overline{TRST}$ = Test Reset

$\overline{ENABLE}$ = Program

256-BALL fpBGA CONNECTION DIAGRAM (M4A3-256/192)

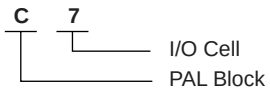
Bottom View

256-Ball fpBGA

	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	I/O167 N15	I/O181 O13	I/O180 O12	I/O177 O9	I/O174 O6	I/O172 O4	I/O191 P14	I/O186 P4	I/O1 A2	I/O3 A6	GCLK0	I/O9 B1	I/O13 B5	I/O15 B7	I/O18 B10	I/O20 B12	A
B	I/O165 N13	I/O166 N14	I/O182 O14	I/O179 O11	I/O175 O7	I/O173 O5	I/O168 O0	I/O187 P6	I/O0 A0	I/O5 A10	I/O7 A14	I/O10 B2	I/O16 B8	I/O19 B11	I/O21 B13	NC	B
C	I/O163 N11	I/O164 N12	NC	I/O183 O15	I/O178 O10	I/O170 O2	I/O171 O3	I/O189 P10	I/O184 P0	I/O6 A12	I/O12 B4	I/O14 B6	I/O23 B15	I/O22 B14	TDI	I/O39 C15	C
D	I/O158 N6	I/O159 N7	TDO	GND	GND	VCC	GND	VCC	GND	GND	VCC	GND	VCC	I/O17 B9	I/O38 C14	I/O37 C13	D
E	I/O156 N4	NC	I/O162 N10	VCC	I/O160 N8	I/O161 N9	I/O190 P12	GCLK3	I/O188 P8	I/O2 A4	I/O8 B0	NC	GND	I/O36 C12	I/O35 C11	I/O31 C7	E
F	I/O152 N0	I/O157 N5	I/O155 N3	GND	I/O154 N2	I/O153 N1	I/O176 O8	I/O169 O1	I/O185 P2	I/O4 A8	I/O11 B3	I/O34 C10	VCC	I/O32 C8	I/O30 C6	I/O29 C5	F
G	I/O147 M6	I/O150 M12	I/O149 M10	VCC	I/O148 M8	I/O151 M14	VCC	GND	GND	VCC	I/O33 C9	I/O28 C4	GND	I/O26 C2	I/O25 C1	I/O47 D14	G
H	I/O144 M0	I/O146 M4	I/145 OM2	GND	I/O136 L0	I/O137 L2	GND	VCC	VCC	GND	I/O27 C3	I/O24 C0	VCC	I/O44 D8	I/O43 D6	I/O42 D4	H
J	I/O138 L4	I/O139 L6	I/O140 L8	GND	I/O142 L12	I/O141 L10	GND	VCC	VCC	GND	I/O46 D12	I/O45 D10	GND	I/O49 E2	I/O48 E0	I/O50 E4	J
K	I/O143 L14	I/O120 K0	I/O121 K1	VCC	I/O123 K3	I/O122 K2	VCC	GND	GND	VCC	I/O41 D2	I/O40 D0	VCC	I/O55 E14	I/O54 E12	I/O56 F0	K
L	I/O124 K4	I/O125 K5	I/O127 K7	GND	I/O130 K10	I/O126 K6	I/O98 I4	I/O91 H6	I/O75 G3	I/O77 G5	I/O52 E8	I/O51 E6	GND	I/O59 F3	I/O60 F4	I/O57 F1	L
M	I/O128 K8	I/O129 K9	I/O131 K11	GND	I/O107 J3	I/O105 J1	I/O100 I8	I/O90 H4	I/O74 G2	I/O80 G8	I/O83 G11	I/O53 E10	VCC	I/O68 F12	I/O63 F7	I/O58 F2	M
N	I/O132 K12	I/O133 K13	I/O135 K15	VCC	GND	VCC	GND	VCC	GND	GND	VCC	GND	GND	TCK	I/O64 F8	I/O61 F5	N
P	I/O134 K14	I/O117 J13	I/O118 J14	I/O119 J15	I/O108 J4	I/O106 J2	I/O101 I10	I/O89 H2	I/O93 H10	I/O94 H12	I/O79 G7	I/O84 G12	I/O87 G15	TMS	I/O65 F9	I/O62 F6	P
R	I/O116 J12	I/O115 J11	I/O112 J8	I/O111 J7	I/O104 J0	I/O102 I12	I/O99 I6	I/O96 I0	I/O92 H8	I/O72 G0	I/O76 G4	I/O81 G9	I/O85 G13	I/O71 F15	I/O67 F11	I/O66 F10	R
T	I/O114 J10	I/O113 J9	I/O110 J6	I/O109 J5	I/O103 I14	GCLK2	I/O97 I2	I/O88 H0	GCLK1	I/O95 H14	I/O73 G1	I/O78 G6	I/O82 G10	I/O86 G14	I/O70 F14	I/O69 F13	T
	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

PIN DESIGNATIONS

CLK = Clock
GND = Ground
I = Input
I/O = Input/Output
N/C = No Connect
VCC = Supply Voltage
TDI = Test Data In
TCK = Test Clock
TMS = Test Mode Select
TDO = Test Data Out



17466G-047

256-BALL BGA CONNECTION DIAGRAM - (M4A3-384/192)

Bottom View

256-Ball BGA

	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	GND	I/O11 FX7	GND	I/O44 FX6	I/O58 CX6	GND	I/O70 CX2	I/O76 DX6	GND	GND	GND	GND	I/O108 AX5	I/O116 BX0	GND	I/O128 BX7	I/O134 O3	GND	GND	GND	A
B	GND	I/O12 GX7	I/O28 FX5	I/O45 FX3	I/O59 CX7	I/O64 CX5	I/O71 CX3	I/O77 DX7	I/O84 DX5	I/O90 DX2	I/O96 AX0	I/O102 AX3	I/O109 AX6	I/O117 BX1	I/O122 BX4	I/O129 BX6	I/O135 O4	I/O148 O6	I/O164 O7	GND	B
C	I/O0 GX6	I/O13 GX5	VCC	I/O46 FX4	I/O60 FX2	I/O65 FX1	I/O72 CX4	I/O78 CX0	I/O85 DX4	I/O91 DX1	I/O97 AX1	I/O103 AX4	I/O110 BX2	I/O118 BX5	I/O123 O0	I/O130 O1	I/O136 O5	VCC	I/O165 N7	I/O181 N6	C
D	I/O1 EX7	I/O14 GX3	I/O29 GX4	VCC	VCC	I/O66 FX0	VCC	I/O79 CX1	I/O86 DX3	I/O92 DX0	I/O98 AX2	I/O104 AX7	I/O111 B3X	VCC	I/O124 O2	VCC	VCC	I/O149 N4	I/O166 N5	I/O182 P7	D
E	I/O2 EX0	I/O15 GX0	I/O30 GX1	TDI													TDO	I/O150 N2	I/O167 N3	I/O183 P6	E
F	GND	I/O16 EX1	I/O31 EX6	I/O47 GX2													I/O137 N1	I/O151 N0	I/O168 P5	GND	F
G	I/O3 HX6	I/O17 EX4	I/O32 EX5	VCC													VCC	I/O152 P4	I/O169 P3	I/O184 M7	G
H	GND	I/O18 HX5	I/O33 EX2	I/O48 EX3													I/O138 P2	I/O153 P1	I/O170 P0	GND	H
J	I/O4 HX0	I/O19 HX1	I/O34 HX4	I/O49 HX7													I/O139 M6	I/O154 M5	I/O171 M4	I/O185 M3	J
K	GND	CLK3	I/O35 HX2	I/O50 HX3													I/O140 M0	I/O155 M1	CLK2	I/O186 M2	K
L	I/O5 A2	CLK0	I/O36 A0	I/O51 A1													I/O141 L3	I/O156 L4	CLK1	GND	L
M	I/O6 A4	I/O20 A3	I/O37 A5	I/O52 A6													I/O142 L6	I/O157 L5	I/O172 L0	I/O187 L1	M
N	GND	I/O21 A7	I/O38 D0	I/O53 D1													I/O143 I5	I/O158 I0	I/O173 L7	GND	N
P	I/O7 D2	I/O22 D3	I/O39 D4	VCC													VCC	I/O159 I4	I/O174 I1	I/O188 L2	P
R	GND	I/O23 D5	I/O40 D6	I/O54 D7													I/O144 K5	I/O160 K0	I/O175 I3	GND	R
T	I/O8 B3	I/O24 B0	I/O41 B7	TCK													TMS	I/O161 K4	I/O176 K1	I/O189 I2	T
U	I/O9 B4	I/O25 B1	I/O42 B6	VCC	VCC	I/O67 C0	VCC	I/O80 F0	I/O87 E5	I/O93 E2	I/O99 H2	I/O105 H5	I/O112 G0	VCC	I/O125 J1	VCC	VCC	I/O162 K7	I/O177 K2	I/O190 I6	U
V	I/O10 B5	I/O26 B2	VCC	I/O55 C5	I/O61 C2	I/O68 C1	I/O73 F4	I/O81 F1	I/O88 E4	I/O94 E1	I/O100 H1	I/O106 H4	I/O113 G1	I/O119 G4	I/O126 J0	I/O131 J2	I/O145 J5	VCC	I/O178 K3	I/O191 I7	V
W	GND	I/O27 C7	I/O43 C6	I/O56 C3	I/O62 F7	I/O69 F5	I/O74 F3	I/O82 E7	I/O89 E3	I/O95 E0	I/O101 H0	I/O107 H3	I/O114 H7	I/O120 G3	I/O127 G5	I/O132 G7	I/O146 J4	I/O163 J6	I/O179 J7	GND	W
Y	GND	GND	GND	I/O57 C4	I/O63 F6	GND	I/O75 F2	I/O83 E6	GND	GND	GND	GND	I/O115 H6	I/O121 G2	GND	I/O133 G6	I/O147 J3	GND	I/O180 K6	GND	Y
	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

PIN DESIGNATIONS

CLK	=	Clock
GND	=	Ground
I	=	Input
I/O	=	Input/Output
N/C	=	No Connect
VCC	=	Supply Voltage
TDI	=	Test Data In
TCK	=	Test Clock
TMS	=	Test Mode Select
TDO	=	Test Data Out

C 7
I/O Cell
PAL Block

17466G-046

256-BALL fpBGA CONNECTION DIAGRAM (M4A3-256/128)

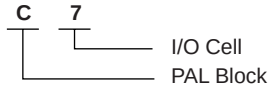
Bottom View

256-Ball fpBGA

	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	$\overline{\text{TRST}}$	I/O117 O5	I/O116 O4	I/O113 O1	I/O126 P6	I/O124 P4	I12	NC	NC	NC	CLK0	I/O1 A1	I/O5 A5	I/O7 A7	I/O10 B2	I/O12 B4	**A**
B	I/O110 N6	I/O111 N7	I/O118 O6	I/O115 O3	I/O127 P7	I/O125 P5	I/O120 P0	NC	NC	NC	I1	I/O2 A2	I/O8 B0	I/O11 B3	I/O13 B5	NC	**B**
C	I/O108 N4	I/O109 N5	NC	I/O119 O7	I/O114 O2	I/O122 P2	I/O123 P3	NC	NC	I0	I/O4 A4	I/O6 A6	I/O15 B7	I/O14 B6	TDI	I/O23 C7	**C**
D	NC	I/O104 N0	TDO	GND	GND	VCC	GND	VCC	GND	GND	VCC	GND	VCC	I/O9 B1	I/O22 C6	I/O21 C5	**D**
E	I/O102 M6	NC	I/O107 N3	VCC	I/O105 N1	I/O106 N2	I13	CLK3	NC	NC	I/O0 A0	NC	GND	I/O20 C4	I/O19 C3	I/O31 D7	**E**
F	I/O98 M2	I/O103 M7	I/O101 M5	GND	I/O100 M4	I/O99 M3	I/O112 O0	I/O121 P1	NC	NC	I/O3 A3	I/O18 C2	VCC	I/O16 C0	I/O30 D6	I/O29 D5	**F**
G	NC	I/O96 M0	I11	VCC	NC	I/O97 M1	VCC	GND	GND	VCC	I/O17 C1	I/O28 D4	GND	I/O26 D2	I/O25 D1	I2	**G**
H	I/O88 L0	I10	I9	GND	I/O89 L1	I/O90 L2	GND	VCC	VCC	GND	I/O27 D3	I/O24 D0	VCC	NC	NC	NC	**H**
J	I/O91 L3	I/O92 L4	I/O93 L5	GND	I/O95 L7	I/O94 L6	GND	VCC	VCC	GND	I3	NC	GND	NC	NC	NC	**J**
K	NC	NC	NC	VCC	NC	NC	VCC	GND	GND	VCC	NC	NC	VCC	I4	NC	I/O32 E0	**K**
L	NC	NC	I/O80 K0	GND	I/O83 K3	NC	NC	NC	I/O59 H3	I/O61 H5	NC	NC	GND	I/O35 E3	I/O36 E4	I/O33 E1	**L**
M	I/O81 K1	I/O82 K2	I/O84 K4	GND	I/O67 I3	I/O65 I1	NC	NC	I/O58 H2	I/O48 G0	I/O51 G3	NC	VCC	I/O44 F4	I/O39 E7	I/O34 E2	**M**
N	I/O85 K5	I/O86 K6	$\overline{\text{ENABLE}}$	VCC	GND	VCC	GND	VCC	GND	GND	VCC	GND	GND	TCK	I/O40 F0	I/O37 E5	**N**
P	I/O87 K7	I/O77 J5	I/O78 J6	I/O79 J7	I/O68 I4	I/O66 I2	NC	NC	NC	I6	I/O63 H7	I/O52 G4	I/O55 G7	TMS	I/O41 F1	I/O38 E6	**P**
R	I/O76 J4	I/O75 J3	I/O72 J0	I/O71 I7	I/O64 I0	I7	NC	NC	NC	I/O56 H0	I/O60 H4	I/O49 G1	I/O53 G5	I/O47 F7	I/O43 F3	I/O42 F2	**R**
T	I/O74 J2	I/O73 J1	I/O70 I6	I/O69 I5	I8	CLK2	NC	NC	CLK1	I5	I/O57 H1	I/O62 H6	I/O50 G2	I/O54 G6	I/O46 F6	I/O45 F5	**T**
	16	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	

PIN DESIGNATIONS

CLK = Clock
GND = Ground
I = Input
I/O = Input/Output
N/C = No Connect
VCC = Supply Voltage
TDI = Test Data In
TCK = Test Clock
TMS = Test Mode Select
$\overline{\text{TDO}}$ = Test Data Out
$\overline{\text{TRST}}$ = Test Reset
$\overline{\text{ENABLE}}$ = Program



m4a3.256.128_256bga

256-BALL fpBGA CONNECTION DIAGRAM (M4A3-512/192)

Bottom View

256-Ball fpBGA

	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	I/O159 KX7	I/O181 OX5	I/O180 OX4	I/O177 OX1	I/O174 NX6	I/O172 NX4	I/O191 PX7	I/O186 PX2	I/O1 A1	I/O3 A3	CLK0	I/O17 C1	I/O21 C5	I/O23 C7	I/O10 B2	I/O12 B4	**A**
B	I/O157 KX5	I/O158 KX6	I/O182 OX6	I/O179 OX3	I/O175 NX7	I/O173 NX5	I/O168 NX0	I/O187 PX3	I/O0 A0	I/O5 A5	I/O7 A7	I/O18 C2	I/O8 B0	I/O11 B3	I/O13 B5	N/C	**B**
C	I/O155 KX3	I/O156 KX4	N/C	I/O183 OX7	I/O178 OX2	I/O170 NX2	I/O171 NX3	I/O189 PX5	I/O184 PX0	I/O6 A6	I/O20 C4	I/O22 C6	I/O15 B7	I/O14 B6	TDI	I/O39 F7	**C**
D	I/O150 JX6	I/O151 JX7	TDO	GND	GND	VCC	GND	VCC	GND	GND	VCC	GND	VCC	I/O9 B1	I/O38 F6	I/O37 F5	**D**
E	I/O148 JX4	N/C	I/O154 KX2	VCC	I/O152 KX0	I/O153 KX1	I/O190 PX6	CLK3	I/O188 PX4	I/O2 A2	I/O16 C0	N/C	GND	I/O36 F4	I/O35 F3	I/O47 G7	**E**
F	I/O144 JX0	I/O149 JX5	I/O147 JX3	GND	I/O146 JX2	I/O145 JX1	I/O176 OX0	I/O169 NX1	I/O185 PX1	I/O4 A4	I/O19 C3	I/O34 F2	VCC	I/O32 F0	I/O46 G6	I/O45 G5	**F**
G	I/O163 LX3	I/O166 LX6	I/O165 LX5	VCC	I/O164 LX4	I/O167 LX7	VCC	GND	GND	VCC	I/O33 F1	I/O44 G4	GND	I/O42 G2	I/O41 G1	I/O31 E7	**G**
H	I/O160 LX0	I/O162 LX2	I/O161 LX1	GND	I/O120 EX0	I/O121 EX1	GND	VCC	VCC	GND	I/O43 G3	I/O40 G0	VCC	I/O28 E4	I/O27 E3	I/O26 E2	**H**
J	I/O122 EX2	I/O123 EX3	I/O124 EX4	GND	I/O126 EX6	I/O125 EX5	GND	VCC	VCC	GND	I/O30 E6	I/O29 E5	GND	I/O65 L1	I/O64 L0	I/O66 L2	**J**
K	I/O127 EX7	I/O136 GX0	I/O137 GX1	VCC	I/O139 GX3	I/O138 GX2	VCC	GND	GND	VCC	I/O25 E1	I/O24 E0	VCC	I/O71 L7	I/O70 L6	I/O48 J0	**K**
L	I/O140 GX4	I/O141 GX5	I/O143 GX7	GND	I/O130 FX2	I/O142 GX6	I/O98 AX2	I/O91 P3	I/O75 N3	I/O77 N5	I/O68 L4	I/O67 L3	GND	I/O51 J3	I/O52 J4	I/O49 J1	**L**
M	I/O128 FX0	I/O129 FX1	I/O131 FX3	GND	I/O115 CX3	I/O113 CX1	I/O100 AX4	I/O90 P2	I/O74 N2	I/O80 O0	I/O83 O3	I/O69 L5	VCC	I/O60 K4	I/O55 J7	I/O50 J2	**M**
N	I/O132 FX4	I/O133 FX5	I/O135 FX7	VCC	GND	VCC	GND	VCC	GND	GND	VCC	GND	GND	TCK	I/O56 K0	I/O53 J5	**N**
P	I/O134 FX6	I/O109 BX5	I/O110 BX6	I/O111 BX7	I/O116 CX4	I/O114 CX2	I/O101 AX5	I/O89 P1	I/O93 P5	I/O94 P6	I/O79 N7	I/O84 O4	I/O87 O7	TMS	I/O57 K1	I/O54 J6	**P**
R	I/O108 BX4	I/O107 BX3	I/O104 BX0	I/O119 CX7	I/O112 CX0	I/O102 AX6	I/O99 AX3	I/O96 AX0	I/O92 P4	I/O72 N0	I/O76 N4	I/O81 O1	I/O85 O5	I/O63 K7	I/O59 K3	I/O58 K2	**R**
T	I/O106 BX2	I/O105 BX1	I/O118 CX6	I/O117 CX5	I/O103 AX7	CLK2	I/O97 AX1	I/O88 P0	CLK1	I/O95 P7	I/O73 N1	I/O78 N6	I/O82 O2	I/O86 O6	I/O62 K6	I/O61 K5	**T**
	16	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	

PIN DESIGNATIONS

CLK = Clock
GND = Ground
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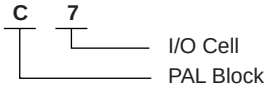

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388-BALL fpBGA CONNECTION DIAGRAM (M4A3-512/256)

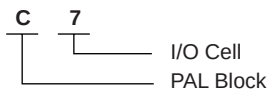
Bottom View

388-Ball fpBGA

	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	GND	I/O243 OX3	I/O240 OX0	I/O241 OX1	I/O236 NX4	I/O231 MX7	I/O228 MX4	I/O226 MX2	I/O255 PX7	I/O251 PX3	I/O248 PX0	I/O0 A0	I/O5 A5	I/O6 A6	I/O27 D3	I/O30 D6	I/O17 C1	I/O22 C6	I/O8 B0	I/O10 B2	N/C	GND	**A**
B	N/C	GND	I/O245 OX5	I/O242 OX2	I/O238 NX6	I/O234 NX2	I/O232 NX0	I/O229 MX5	I/O224 MX0	I/O253 PX5	I/O249 PX1	I/O2 A2	CLK0	I/O26 D2	I/O29 D5	I/O31 D7	I/O20 C4	I/O9 B1	I/O12 B4	I/O13 B5	GND	TDI	**B**
C	I/O213 KX5	TDO	GND	I/O247 OX7	I/O244 OX4	I/O239 NX7	I/O235 NX3	I/O230 MX6	I/O227 MX3	CLK3	I/O250 PX2	I/O1 A1	I/O7 A7	I/O25 D1	I/O16 C0	I/O18 C2	I/O23 C7	I/O11 B3	I/O15 B7	GND	I/O47 F7	I/O44 F4	**C**
D	I/O210 KX2	I/O212 KX4	I/O215 KX7	GND	I/O246 OX6	VCC	I/O237 NX5	I/O233 NX1	VCC	I/O254 PX6	VCC	I/O3 A3	I/O24 D0	VCC	I/O19 C3	I/O21 C5	VCC	I/O14 B6	GND	I/O46 F6	I/O43 F3	I/O41 F1	**D**
E	I/O207 JX7	I/O209 KX1	I/O211 KX3	I/O214 KX6															I/O45 F5	I/O42 F2	I/O40 F0	I/O54 G6	**E**
F	I/O203 JX3	I/O205 JX5	I/O208 KX0	VCC															VCC	I/O55 G7	I/O52 G4	I/O50 G2	**F**
G	I/O200 JX0	I/O202 JX2	I/O204 JX4	I/O206 JX6			VCC	VCC	N/C	I/O225 MX1	I/O252 PX4	I/O4 A4	I/O28 D4	N/C	VCC	VCC			I/O53 G5	I/O51 G3	I/O49 G1	I/O39 E7	**G**
H	I/O221 LX5	I/O222 LX6	I/O223 LX7	I/O201 JX1			VCC	N/C	GND	GND	GND	GND	GND	GND	N/C	VCC			I/O48 G0	I/O38 E6	I/O37 E5	I/O36 E4	**H**
J	I/O218 LX2	I/O219 LX3	I/O220 LX4	VCC			N/C	GND	GND	GND	GND	GND	GND	GND	GND	N/C			VCC	I/O35 E3	I/O34 E2	I/O32 E0	**J**
K	I/O197 IX5	I/O198 IX6	I/O199 IX7	I/O216 LX0			I/O217 LX1	GND	GND	GND	GND	GND	GND	GND	GND	I/O33 E1			I/O63 H7	I/O62 H6	I/O61 H5	I/O60 H4	**K**
L	I/O192 IX0	I/O194 IX2	I/O195 IX3	I/O196 IX4			I/O193 IX1	GND	GND	GND	GND	GND	GND	GND	GND	I/O58 H2			VCC	I/O59 H3	I/O57 H1	I/O56 H0	**L**
M	I/O184 HX0	I/O185 HX1	I/O187 HX3	VCC			I/O186 HX2	GND	GND	GND	GND	GND	GND	GND	GND	I/O69 I5			I/O67 I3	I/O65 I1	I/O66 I2	I/O64 I0	**M**
N	I/O188 HX4	I/O189 HX5	I/O191 HX7	I/O190 HX6			I/O162 EX2	GND	GND	GND	GND	GND	GND	GND	GND	I/O89 L1			I/O88 L0	I/O71 I7	I/O70 I6	I/O68 I4	**N**
P	I/O160 EX0	I/O161 EX1	I/O163 EX3	VCC			N/C	GND	GND	GND	GND	GND	GND	GND	GND	N/C			VCC	I/O92 L4	I/O91 L3	I/O90 L2	**P**
R	I/O164 EX4	I/O165 EX5	I/O166 EX6	I/O177 GX1			VCC	N/C	GND	GND	GND	GND	GND	GND	N/C	VCC			I/O74 J2	I/O95 L7	I/O94 L6	I/O93 L5	**R**
T	I/O167 EX7	I/O176 GX0	I/O179 GX3	I/O181 GX5			VCC	VCC	N/C	I/O152 DX0	I/O131 AX3	I/O122 P2	I/O98 M2	N/C	VCC	VCC			I/O78 J6	I/O76 J4	I/O73 J1	I/O72 J0	**T**
U	I/O178 GX2	I/O180 GX4	I/O183 GX7	VCC															VCC	I/O80 K0	I/O77 J5	I/O75 J3	**U**
V	I/O182 GX6	N/C	I/O169 FX1	I/O172 FX4															I/O86 K6	I/O83 K3	I/O81 K1	I/O79 J7	**V**
W	I/O168 FX0	I/O170 FX2	I/O173 FX5	GND	I/O143 BX7	VCC	I/O150 CX6	I/O145 CX1	VCC	I/O153 DX1	I/O123 P3	VCC	I/O96 M0	VCC	I/O104 N0	I/O111 N7	VCC	I/O119 O7	GND	I/O87 K7	I/O84 K4	I/O82 K2	**W**
Y	I/O171 FX3	I/O174 FX6	GND	I/O141 BX5	I/O138 BX2	I/O136 BX0	I/O147 CX3	I/O158 DX6	I/O156 DX4	CLK2	I/O132 AX4	I/O121 P1	I/O125 P5	I/O99 M3	I/O101 M5	I/O106 N2	I/O110 N6	I/O115 O3	I/O118 O6	GND	TMS	I/O85 K5	**Y**
AA	I/O175 FX7	GND	I/O142 BX6	I/O140 BX4	I/O151 CX7	I/O149 CX5	I/O144 CX0	I/O157 DX5	I/O154 DX2	I/O134 AX6	I/O130 AX2	I/O128 AX0	CLK1	I/O127 P7	I/O100 M4	I/O103 M7	I/O108 N4	I/O109 N5	I/O113 O1	I/O116 O4	GND	TCK	**AA**
AB	GND	N/C	I/O139 BX3	I/O137 BX1	I/O148 CX4	I/O146 CX2	I/O159 DX7	I/O155 DX3	I/O135 AX7	I/O133 AX5	I/O129 AX1	I/O120 P0	I/O124 P4	I/O126 P6	I/O97 M1	I/O102 M6	I/O105 N1	I/O107 N3	I/O112 O0	I/O114 O2	I/O117 O5	GND	**AB**
	22	**21**	**20**	**19**	**18**	**17**	**16**	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	

PIN DESIGNATIONS

CLK	=	Clock
GND	=	Ground
I	=	Input
I/O	=	Input/Output
N/C	=	No Connect
VCC	=	Supply Voltage
TDI	=	Test Data In
TCK	=	Test Clock
TMS	=	Test Mode Select
TDO	=	Test Data Out



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Revision History

Date	Version	Change Summary
-	K	Previous Lattice release.
August 2006	L	Updated for lead-free package options.
September 2006	M	Revised M4A3-256/160 208-pin PQFP connection diagram.