



Welcome to [E-XFL.COM](https://www.e-xfl.com)

## Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

## Applications of Embedded - CPLDs

### Details

|                                 |                                                                                                                                                                           |
|---------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Product Status                  | Obsolete                                                                                                                                                                  |
| Programmable Type               | In System Programmable                                                                                                                                                    |
| Delay Time tpd(1) Max           | 14 ns                                                                                                                                                                     |
| Voltage Supply - Internal       | 3V ~ 3.6V                                                                                                                                                                 |
| Number of Logic Elements/Blocks | -                                                                                                                                                                         |
| Number of Macrocells            | 384                                                                                                                                                                       |
| Number of Gates                 | -                                                                                                                                                                         |
| Number of I/O                   | 192                                                                                                                                                                       |
| Operating Temperature           | -40°C ~ 85°C (TA)                                                                                                                                                         |
| Mounting Type                   | Surface Mount                                                                                                                                                             |
| Package / Case                  | 256-LBGA                                                                                                                                                                  |
| Supplier Device Package         | 256-SBGA (27x27)                                                                                                                                                          |
| Purchase URL                    | <a href="https://www.e-xfl.com/product-detail/lattice-semiconductor/m4a3-384-192-14sai">https://www.e-xfl.com/product-detail/lattice-semiconductor/m4a3-384-192-14sai</a> |

The ispMACH 4A family offers 20 density-I/O combinations in Thin Quad Flat Pack (TQFP), Plastic Quad Flat Pack (PQFP), Plastic Leaded Chip Carrier (PLCC), Ball Grid Array (BGA), fine-pitch BGA (fpBGA), and chip-array BGA (caBGA) packages ranging from 44 to 388 pins (Table 3). It also offers I/O safety features for mixed-voltage designs so that the 3.3-V devices can accept 5-V inputs, and 5-V devices do not overdrive 3.3-V inputs. Additional features include Bus-Friendly inputs and I/Os, a programmable power-down mode for extra power savings and individual output slew rate control for the highest speed transition or for the lowest noise transition.

**Table 3. ispMACH 4A Package and I/O Options (Number of I/Os and dedicated inputs in Table)**

| 3.3 V Devices  |         |         |         |          |          |             |          |          |
|----------------|---------|---------|---------|----------|----------|-------------|----------|----------|
| Package        | M4A3-32 | M4A3-64 | M4A3-96 | M4A3-128 | M4A3-192 | M4A3-256    | M4A3-384 | M4A3-512 |
| 44-pin PLCC    | 32+2    | 32+2    |         |          |          |             |          |          |
| 44-pin TQFP    | 32+2    | 32+2    |         |          |          |             |          |          |
| 48-pin TQFP    | 32+2    | 32+2    |         |          |          |             |          |          |
| 100-pin TQFP   |         | 64+6    | 48+8    | 64+6     |          |             |          |          |
| 100-pin PQFP   |         |         |         | 64+6     |          |             |          |          |
| 100-ball caBGA |         |         |         | 64+6     |          |             |          |          |
| 144-pin TQFP   |         |         |         |          | 96+16    |             |          |          |
| 144-ball fpBGA |         |         |         |          | 96+16    |             |          |          |
| 208-pin PQFP   |         |         |         |          |          | 128+14, 160 | 160      | 160      |
| 256-ball fpBGA |         |         |         |          |          | 128+14, 192 | 192      | 192      |
| 256-ball BGA   |         |         |         |          |          | 128+14      | 192      |          |
| 388-ball fpBGA |         |         |         |          |          |             |          | 256      |

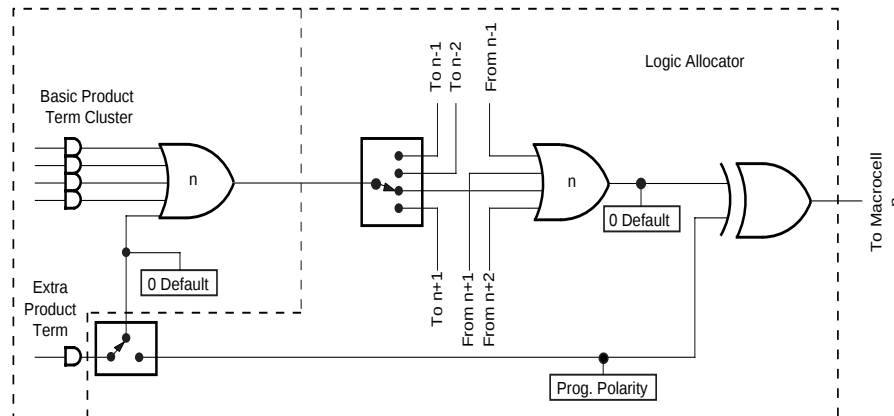
| 5 V Devices  |         |         |         |          |          |          |
|--------------|---------|---------|---------|----------|----------|----------|
| Package      | M4A5-32 | M4A5-64 | M4A5-96 | M4A5-128 | M4A5-192 | M4A5-256 |
| 44-pin PLCC  | 32+2    | 32+2    |         |          |          |          |
| 44-pin TQFP  | 32+2    | 32+2    |         |          |          |          |
| 48-pin TQFP  | 32+2    | 32+2    |         |          |          |          |
| 100-pin TQFP |         |         | 48+8    | 64+6     |          |          |
| 100-pin PQFP |         |         |         | 64+6     |          |          |
| 144-pin TQFP |         |         |         |          | 96+16    |          |
| 208-pin PQFP |         |         |         |          |          | 128+14   |

**Table 6. Logic Allocator for All ispMACH 4A Devices (except M4A(3,5)-32/32)**

| Output Macrocell | Available Clusters                                                | Output Macrocell | Available Clusters                                                    |
|------------------|-------------------------------------------------------------------|------------------|-----------------------------------------------------------------------|
| M <sub>0</sub>   | C <sub>0</sub> , C <sub>1</sub> , C <sub>2</sub>                  | M <sub>8</sub>   | C <sub>7</sub> , C <sub>8</sub> , C <sub>9</sub> , C <sub>10</sub>    |
| M <sub>1</sub>   | C <sub>0</sub> , C <sub>1</sub> , C <sub>2</sub> , C <sub>3</sub> | M <sub>9</sub>   | C <sub>8</sub> , C <sub>9</sub> , C <sub>10</sub> , C <sub>11</sub>   |
| M <sub>2</sub>   | C <sub>1</sub> , C <sub>2</sub> , C <sub>3</sub> , C <sub>4</sub> | M <sub>10</sub>  | C <sub>9</sub> , C <sub>10</sub> , C <sub>11</sub> , C <sub>12</sub>  |
| M <sub>3</sub>   | C <sub>2</sub> , C <sub>3</sub> , C <sub>4</sub> , C <sub>5</sub> | M <sub>11</sub>  | C <sub>10</sub> , C <sub>11</sub> , C <sub>12</sub> , C <sub>13</sub> |
| M <sub>4</sub>   | C <sub>3</sub> , C <sub>4</sub> , C <sub>5</sub> , C <sub>6</sub> | M <sub>12</sub>  | C <sub>11</sub> , C <sub>12</sub> , C <sub>13</sub> , C <sub>14</sub> |
| M <sub>5</sub>   | C <sub>4</sub> , C <sub>5</sub> , C <sub>6</sub> , C <sub>7</sub> | M <sub>13</sub>  | C <sub>12</sub> , C <sub>13</sub> , C <sub>14</sub> , C <sub>15</sub> |
| M <sub>6</sub>   | C <sub>5</sub> , C <sub>6</sub> , C <sub>7</sub> , C <sub>8</sub> | M <sub>14</sub>  | C <sub>13</sub> , C <sub>14</sub> , C <sub>15</sub>                   |
| M <sub>7</sub>   | C <sub>6</sub> , C <sub>7</sub> , C <sub>8</sub> , C <sub>9</sub> | M <sub>15</sub>  | C <sub>14</sub> , C <sub>15</sub>                                     |

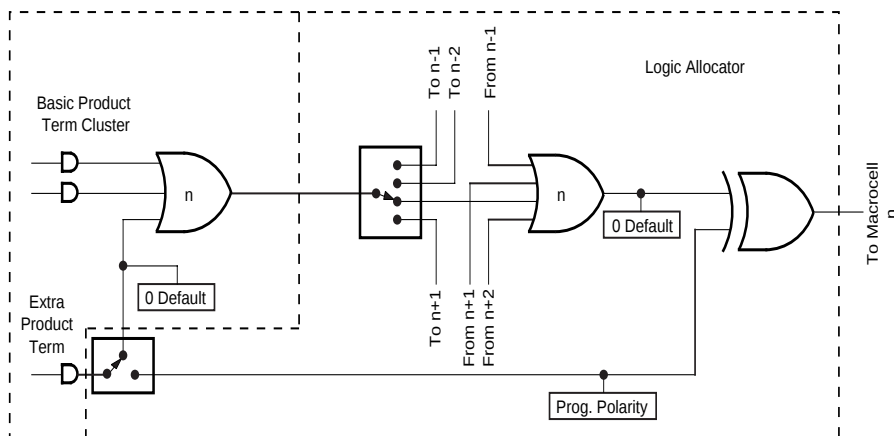
**Table 7. Logic Allocator for M4A(3,5)-32/32**

| Output Macrocell | Available Clusters                                                | Output Macrocell | Available Clusters                                                    |
|------------------|-------------------------------------------------------------------|------------------|-----------------------------------------------------------------------|
| M <sub>0</sub>   | C <sub>0</sub> , C <sub>1</sub> , C <sub>2</sub>                  | M <sub>8</sub>   | C <sub>8</sub> , C <sub>9</sub> , C <sub>10</sub>                     |
| M <sub>1</sub>   | C <sub>0</sub> , C <sub>1</sub> , C <sub>2</sub> , C <sub>3</sub> | M <sub>9</sub>   | C <sub>8</sub> , C <sub>9</sub> , C <sub>10</sub> , C <sub>11</sub>   |
| M <sub>2</sub>   | C <sub>1</sub> , C <sub>2</sub> , C <sub>3</sub> , C <sub>4</sub> | M <sub>10</sub>  | C <sub>9</sub> , C <sub>10</sub> , C <sub>11</sub> , C <sub>12</sub>  |
| M <sub>3</sub>   | C <sub>2</sub> , C <sub>3</sub> , C <sub>4</sub> , C <sub>5</sub> | M <sub>11</sub>  | C <sub>10</sub> , C <sub>11</sub> , C <sub>12</sub> , C <sub>13</sub> |
| M <sub>4</sub>   | C <sub>3</sub> , C <sub>4</sub> , C <sub>5</sub> , C <sub>6</sub> | M <sub>12</sub>  | C <sub>11</sub> , C <sub>12</sub> , C <sub>13</sub> , C <sub>14</sub> |
| M <sub>5</sub>   | C <sub>4</sub> , C <sub>5</sub> , C <sub>6</sub> , C <sub>7</sub> | M <sub>13</sub>  | C <sub>12</sub> , C <sub>13</sub> , C <sub>14</sub> , C <sub>15</sub> |
| M <sub>6</sub>   | C <sub>5</sub> , C <sub>6</sub> , C <sub>7</sub>                  | M <sub>14</sub>  | C <sub>13</sub> , C <sub>14</sub> , C <sub>15</sub>                   |
| M <sub>7</sub>   | C <sub>6</sub> , C <sub>7</sub>                                   | M <sub>15</sub>  | C <sub>14</sub> , C <sub>15</sub>                                     |



**a. Synchronous Mode**

17466G-005



**b. Asynchronous Mode**

17466G-006

**Figure 2. Logic Allocator: Configuration of Cluster “n” Set by Mode of Macrocell “n”**



weakly pulled up. For the circuit diagram, please refer to the document entitled *MACH Endurance Characteristics* on the Lattice Data Book CD-ROM or Lattice web site.

## **POWER MANAGEMENT**

Each individual PAL block in ispMACH 4A devices features a programmable low-power mode, which results in power savings of up to 50%. The signal speed paths in the low-power PAL block will be slower than those in the non-low-power PAL block. This feature allows speed critical paths to run at maximum frequency while the rest of the signal paths operate in the low-power mode.

## **PROGRAMMABLE SLEW RATE**

Each ispMACH 4A device I/O has an individually programmable output slew rate control bit. Each output can be individually configured for the higher speed transition (3 V/ns) or for the lower noise transition (1 V/ns). For high-speed designs with long, unterminated traces, the slow-slew rate will introduce fewer reflections, less noise, and keep ground bounce to a minimum. For designs with short traces or well terminated lines, the fast slew rate can be used to achieve the highest speed. The slew rate is adjusted independent of power.

## **POWER-UP RESET/SET**

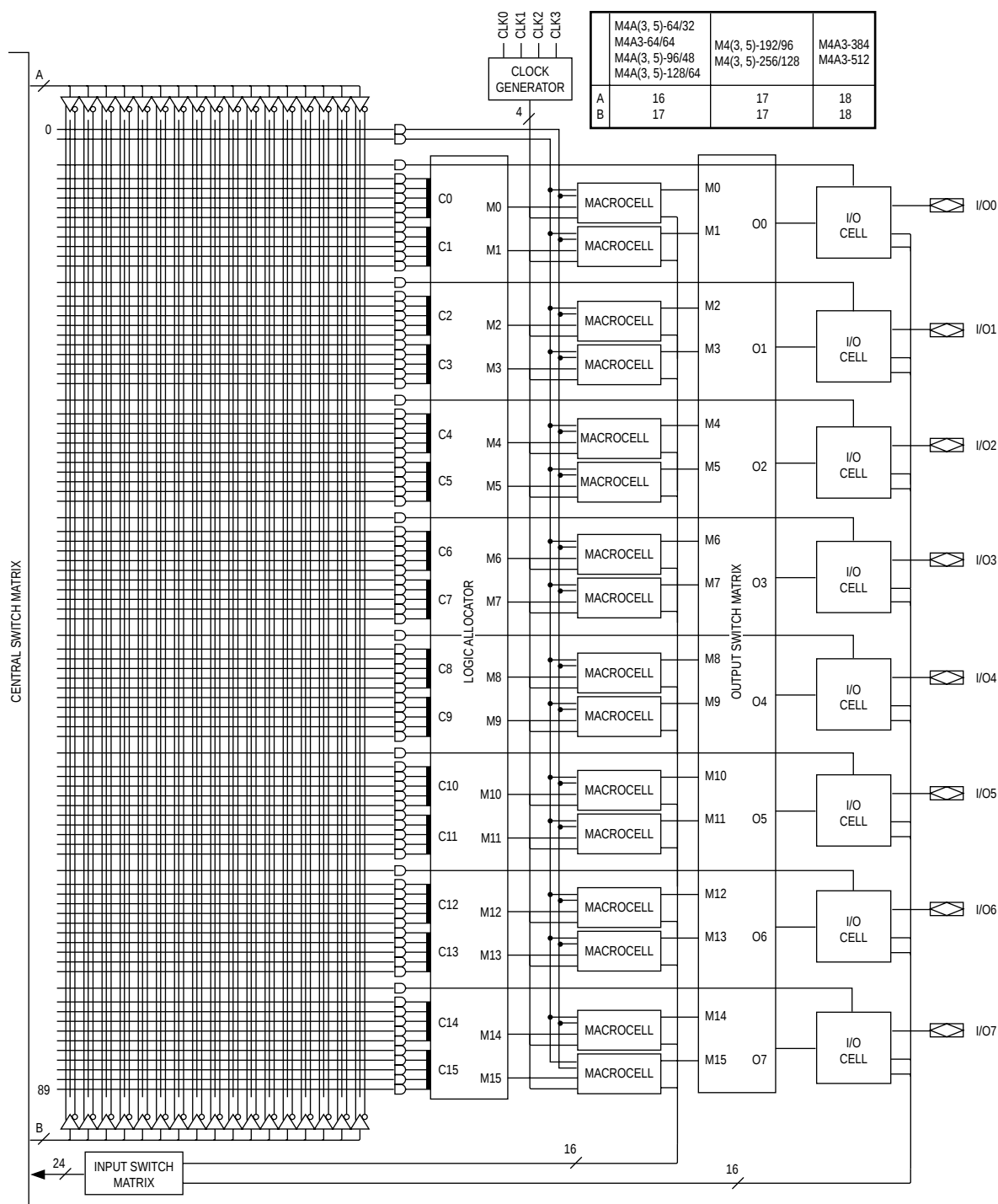
All flip-flops power up to a known state for predictable system initialization. If a macrocell is configured to SET on a signal from the control generator, then that macrocell will be SET during device power-up. If a macrocell is configured to RESET on a signal from the control generator or is not configured for set/reset, then that macrocell will RESET on power-up. To guarantee initialization values, the  $V_{CC}$  rise must be monotonic, and the clock must be inactive until the reset delay time has elapsed.

## **SECURITY BIT**

A programmable security bit is provided on the ispMACH 4A devices as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, this bit defeats readback of the programmed pattern by a device programmer, securing proprietary designs from competitors. Programming and verification are also defeated by the security bit. The bit can only be reset by erasing the entire device.

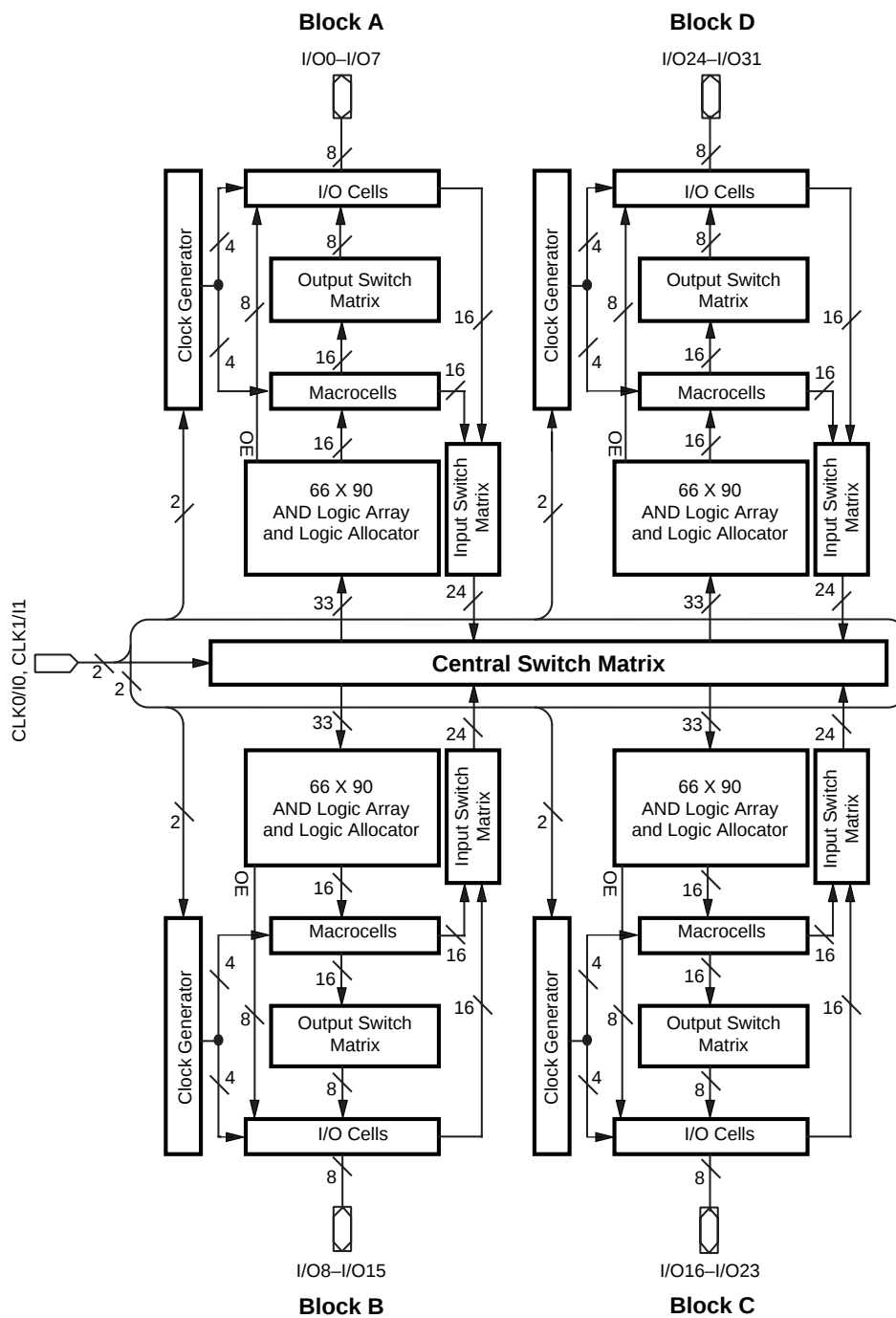
## **HOT SOCKETING**

ispMACH 4A devices are well-suited for those applications that require hot socketing capability. Hot socketing a device requires that the device, when powered down, can tolerate active signals on the I/Os and inputs without being damaged. Additionally, it requires that the effects of the powered-down MACH devices be minimal on active signals.



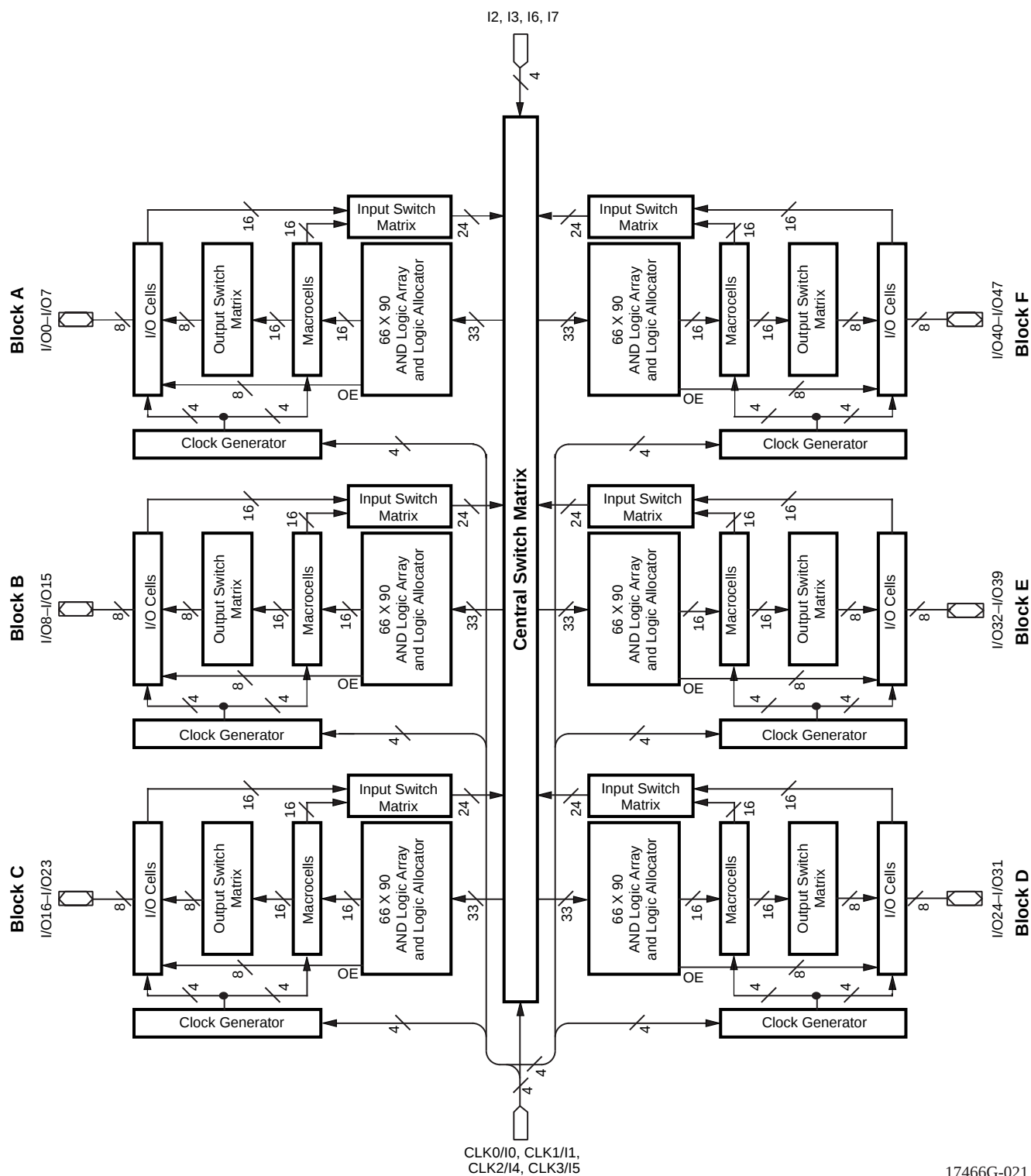
**Figure 16. PAL Block for ispMACH 4A with 2:1 Macrocell - I/O Cell Ratio**

## BLOCK DIAGRAM – M4A(3,5)-64/32



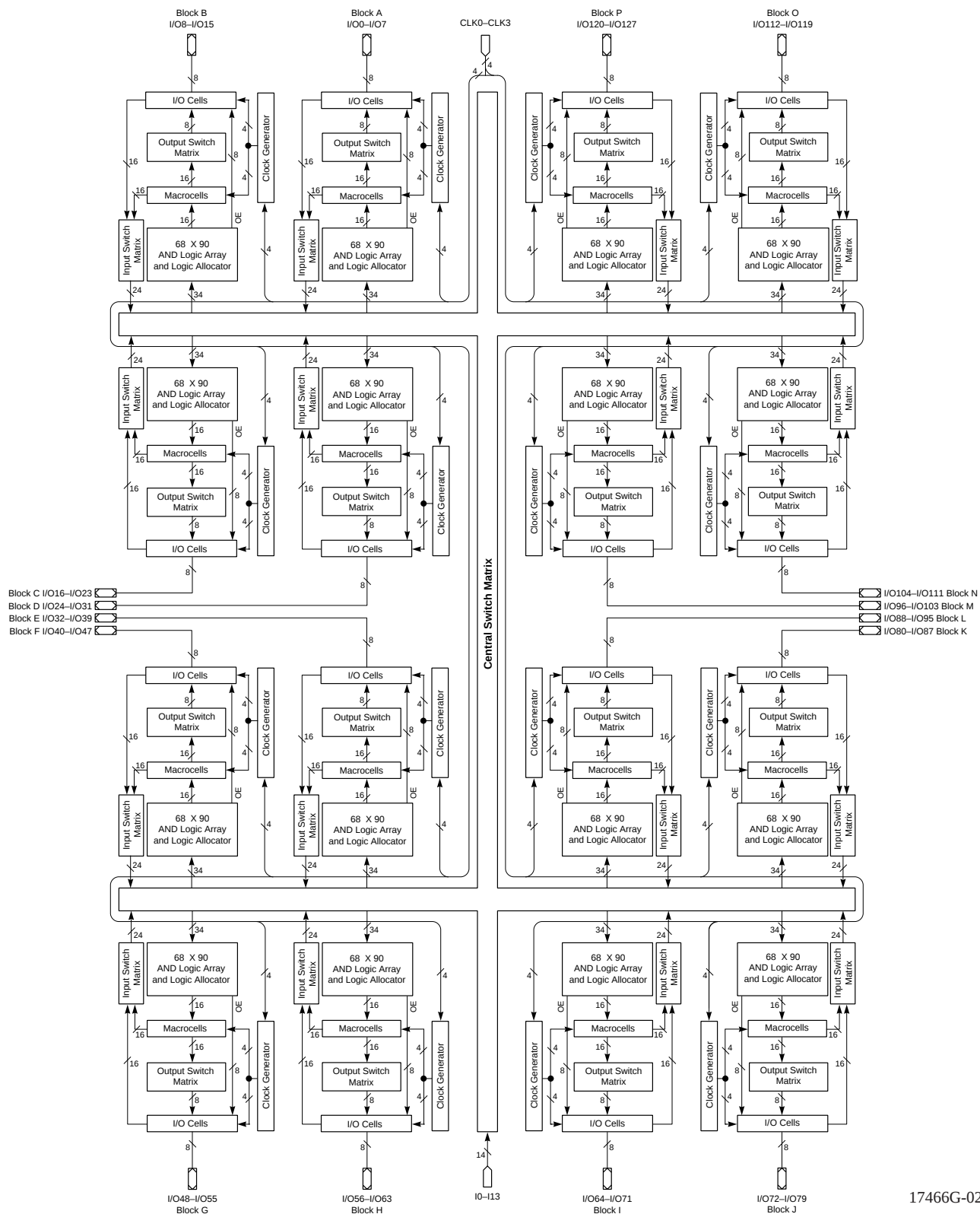
17466H-020

## BLOCK DIAGRAM – M4A(3,5)-96/48



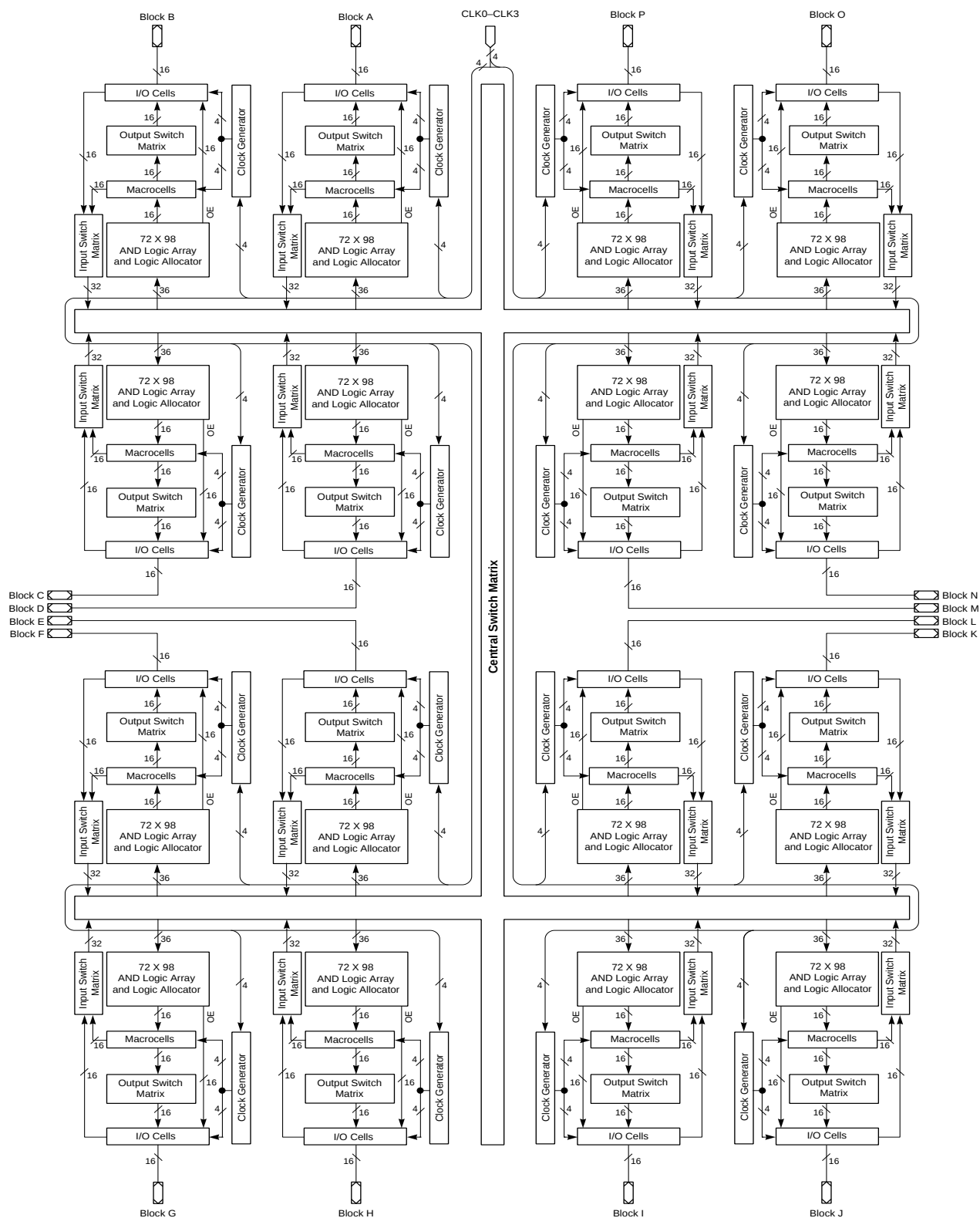
17466G-021

## BLOCK DIAGRAM – M4A(3,5)-256/128



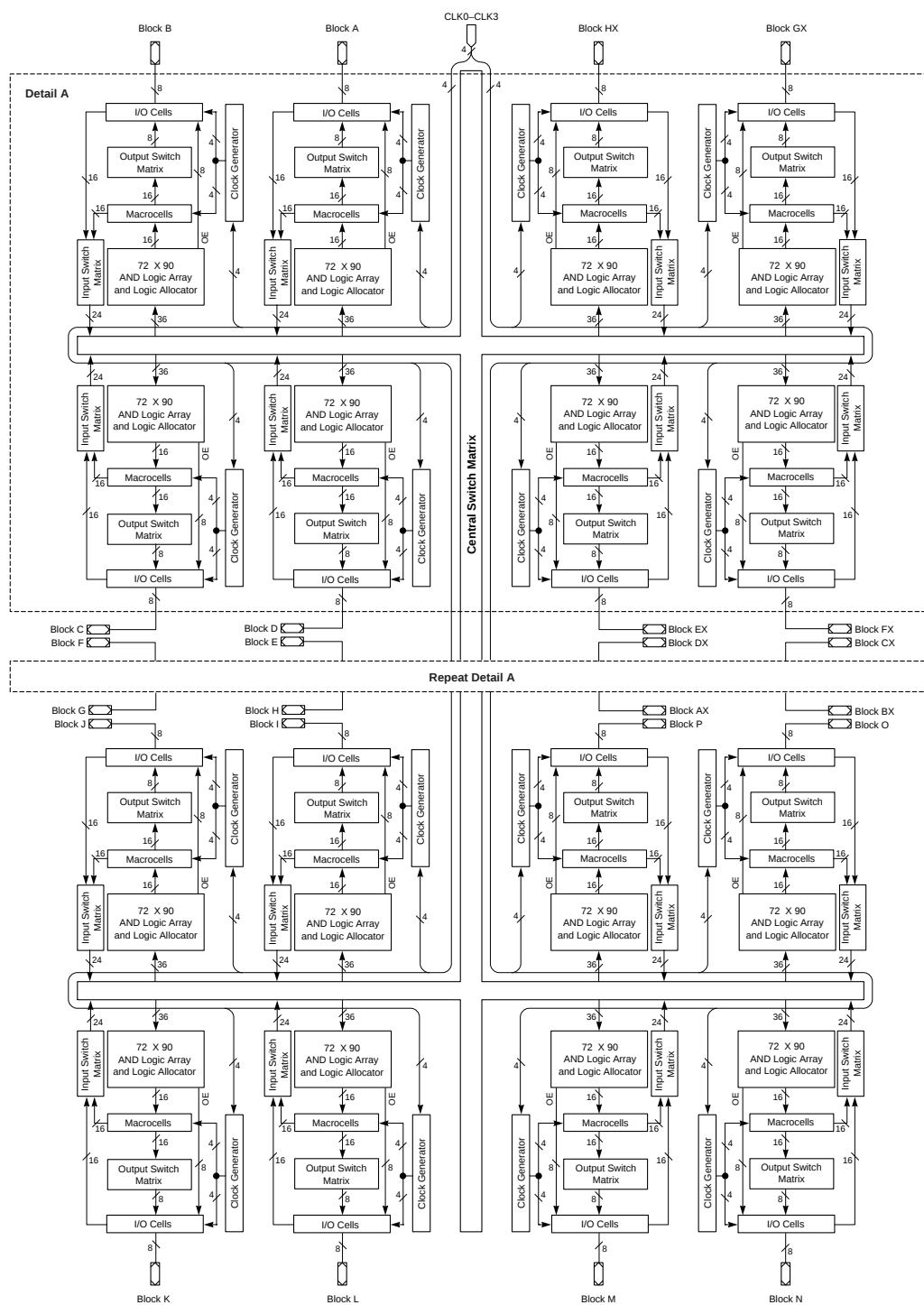
17466G-024

## BLOCK DIAGRAM – M4A3-256/160, M4A3-256/192



17466G-050

## BLOCK DIAGRAM – M4A3-384/160, M4A3-384/192



17466G-067

## ABSOLUTE MAXIMUM RATINGS

### M4A5

Storage Temperature. . . . . -65°C to +150°C  
 Ambient Temperature  
 with Power Applied. . . . . -55°C to +100°C  
 Device Junction Temperature. . . . . +130°C  
 Supply Voltage  
 with Respect to Ground . . . . . -0.5 V to +7.0 V  
 DC Input Voltage . . . . . -0.5 V to  $V_{CC} + 0.5$  V  
 Static Discharge Voltage . . . . . 2000 V  
 Latchup Current ( $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ) . . . . . 200 mA

*Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.*

## OPERATING RANGES

### Commercial (C) Devices

Ambient Temperature ( $T_A$ )  
 Operating in Free Air. . . . .  $0^\circ\text{C}$  to  $+70^\circ\text{C}$   
 Supply Voltage ( $V_{CC}$ )  
 with Respect to Ground. . . . . +4.75 V to +5.25 V

### Industrial (I) Devices

Ambient Temperature ( $T_A$ )  
 Operating in Free Air. . . . .  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$   
 Supply Voltage ( $V_{CC}$ )  
 with Respect to Ground. . . . . +4.50 V to +5.5 V  
*Operating ranges define those limits between which the functionality of the device is guaranteed.*

## 5-V DC CHARACTERISTICS OVER OPERATING RANGES

| Parameter Symbol | Parameter Description                 | Test Conditions                                                                       | Min | Typ | Max  | Unit          |
|------------------|---------------------------------------|---------------------------------------------------------------------------------------|-----|-----|------|---------------|
| $V_{OH}$         | Output HIGH Voltage                   | $I_{OH} = -3.2$ mA, $V_{CC} = \text{Min}$ , $V_{IN} = V_{IH}$ or $V_{IL}$             | 2.4 |     |      | V             |
|                  |                                       | $I_{OH} = -100$ $\mu\text{A}$ , $V_{CC} = \text{Max}$ , $V_{IN} = V_{IH}$ or $V_{IL}$ |     | 3.3 | 3.6  | V             |
| $V_{OL}$         | Output LOW Voltage                    | $I_{OL} = 24$ mA, $V_{CC} = \text{Min}$ , $V_{IN} = V_{IH}$ or $V_{IL}$ (Note 1)      |     |     | 0.5  | V             |
| $V_{IH}$         | Input HIGH Voltage                    | Guaranteed Input Logical HIGH Voltage for all Inputs (Note 2)                         | 2.0 |     |      | V             |
| $V_{IL}$         | Input LOW Voltage                     | Guaranteed Input Logical LOW Voltage for all Inputs (Note 2)                          |     |     | 0.8  | V             |
| $I_{IH}$         | Input HIGH Leakage Current            | $V_{IN} = 5.25$ V, $V_{CC} = \text{Max}$ (Note 3)                                     |     |     | 10   | $\mu\text{A}$ |
| $I_{IL}$         | Input LOW Leakage Current             | $V_{IN} = 0$ V, $V_{CC} = \text{Max}$ (Note 3)                                        |     |     | -10  | $\mu\text{A}$ |
| $I_{OZH}$        | Off-State Output Leakage Current HIGH | $V_{OUT} = 5.25$ V, $V_{CC} = \text{Max}$ , $V_{IN} = V_{IH}$ or $V_{IL}$ (Note 3)    |     |     | 10   | $\mu\text{A}$ |
| $I_{OZL}$        | Off-State Output Leakage Current LOW  | $V_{OUT} = 0$ V, $V_{CC} = \text{Max}$ , $V_{IN} = V_{IH}$ or $V_{IL}$ (Note 3)       |     |     | -10  | $\mu\text{A}$ |
| $I_{SC}$         | Output Short-Circuit Current          | $V_{OUT} = 0.5$ V, $V_{CC} = \text{Max}$ (Note 4)                                     | -30 |     | -160 | mA            |

### Notes:

1. Total  $I_{OL}$  for one PAL block should not exceed 64 mA.
2. These are absolute values with respect to device ground, and all overshoots due to system or tester noise are included.
3. I/O pin leakage is the worst case of  $I_{IL}$  and  $I_{OZL}$  (or  $I_{IH}$  and  $I_{OZH}$ ).
4. Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.  
 $V_{OUT} = 0.5$  V has been chosen to avoid test problems caused by tester ground degradation.

## ABSOLUTE MAXIMUM RATINGS

### M4A3

Storage Temperature. . . . . -65°C to +150°C  
 Ambient Temperature  
 with Power Applied. . . . . -55°C to +100°C  
 Device Junction Temperature. . . . . +130°C  
 Supply Voltage  
 with Respect to Ground. . . . . -0.5 V to +4.5 V  
 DC Input Voltage. . . . . -0.5 V to 6.0 V  
 Static Discharge Voltage. . . . . 2000 V  
 Latchup Current ( $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ) . . . . . 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

## OPERATING RANGES

### Commercial (C) Devices

Ambient Temperature ( $T_A$ )  
 Operating in Free Air. . . . .  $0^{\circ}\text{C}$  to  $+70^{\circ}\text{C}$   
 Supply Voltage ( $V_{CC}$ )  
 with Respect to Ground. . . . . +3.0 V to +3.6 V

### Industrial (I) Devices

Ambient Temperature ( $T_A$ )  
 Operating in Free Air. . . . .  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
 Supply Voltage ( $V_{CC}$ )  
 with Respect to Ground. . . . . +3.0 V to +3.6 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

## 3.3-V DC CHARACTERISTICS OVER OPERATING RANGES

| Parameter Symbol | Parameter Description                 | Test Conditions                                                                             |                              | Min            | Typ | Max  | Unit          |
|------------------|---------------------------------------|---------------------------------------------------------------------------------------------|------------------------------|----------------|-----|------|---------------|
| $V_{OH}$         | Output HIGH Voltage                   | $V_{CC} = \text{Min}$<br>$V_{IN} = V_{IH}$ or $V_{IL}$                                      | $I_{OH} = -100\ \mu\text{A}$ | $V_{CC} - 0.2$ |     |      | V             |
|                  |                                       |                                                                                             | $I_{OH} = -3.2\ \text{mA}$   | 2.4            |     |      | V             |
| $V_{OL}$         | Output LOW Voltage                    | $V_{CC} = \text{Min}$<br>$V_{IN} = V_{IH}$ or $V_{IL}$<br>(Note 1)                          | $I_{OL} = 100\ \mu\text{A}$  |                |     | 0.2  | V             |
|                  |                                       |                                                                                             | $I_{OL} = 24\ \text{mA}$     |                |     | 0.5  | V             |
| $V_{IH}$         | Input HIGH Voltage                    | Guaranteed Input Logical HIGH Voltage for all Inputs                                        |                              | 2.0            |     | 5.5  | V             |
| $V_{IL}$         | Input LOW Voltage                     | Guaranteed Input Logical LOW Voltage for all Inputs                                         |                              | -0.3           |     | 0.8  | V             |
| $I_{IH}$         | Input HIGH Leakage Current            | $V_{IN} = 3.6\ \text{V}$ , $V_{CC} = \text{Max}$ (Note 2)                                   |                              |                |     | 5    | $\mu\text{A}$ |
| $I_{IL}$         | Input LOW Leakage Current             | $V_{IN} = 0\ \text{V}$ , $V_{CC} = \text{Max}$ (Note 2)                                     |                              |                |     | -5   | $\mu\text{A}$ |
| $I_{OZH}$        | Off-State Output Leakage Current HIGH | $V_{OUT} = 3.6\ \text{V}$ , $V_{CC} = \text{Max}$<br>$V_{IN} = V_{IH}$ or $V_{IL}$ (Note 2) |                              |                |     | 5    | $\mu\text{A}$ |
| $I_{OZL}$        | Off-State Output Leakage Current LOW  | $V_{OUT} = 0\ \text{V}$ , $V_{CC} = \text{Max}$<br>$V_{IN} = V_{IH}$ or $V_{IL}$ (Note 2)   |                              |                |     | -5   | $\mu\text{A}$ |
| $I_{SC}$         | Output Short-Circuit Current          | $V_{OUT} = 0.5\ \text{V}$ , $V_{CC} = \text{Max}$ (Note 3)                                  |                              | -15            |     | -160 | mA            |

### Notes:

1. Total  $I_{OL}$  for one PAL block should not exceed 64 mA.
2. I/O pin leakage is the worst case of  $I_{IL}$  and  $I_{OZL}$  (or  $I_{IH}$  and  $I_{OZH}$ ).
3. Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

### Notes:

1. See "MACH Switching Test Circuit" document on the Literature Download page of the Lattice web site.
2. This parameter does not apply to flip-flops in the emulated mode since the feedback path is required for emulation.

## ispMACH 4A TIMING PARAMETERS OVER OPERATING RANGES<sup>1</sup>

|                                        |                                                                                  | -5  |     | -55 |     | -6  |      | -65 |      | -7   |      | -10  |      | -12  |      | -14  |      | Unit |
|----------------------------------------|----------------------------------------------------------------------------------|-----|-----|-----|-----|-----|------|-----|------|------|------|------|------|------|------|------|------|------|
|                                        |                                                                                  | Min | Max | Min | Max | Min | Max  | Min | Max  | Min  | Max  | Min  | Max  | Min  | Max  | Min  | Max  |      |
| Input Register Delays with ZHT Option: |                                                                                  |     |     |     |     |     |      |     |      |      |      |      |      |      |      |      |      |      |
| t <sub>SIRZ</sub>                      | Input register setup time - ZHT                                                  | 6.0 |     | 6.0 |     | 6.0 |      | 6.0 |      | 6.0  |      | 6.0  |      | 6.0  |      | 6.0  |      | ns   |
| t <sub>HIRZ</sub>                      | Input register hold time - ZHT                                                   | 0.0 |     | 0.0 |     | 0.0 |      | 0.0 |      | 0.0  |      | 0.0  |      | 0.0  |      | 0.0  |      | ns   |
| Input Latch Delays with ZHT Option:    |                                                                                  |     |     |     |     |     |      |     |      |      |      |      |      |      |      |      |      |      |
| t <sub>SILZ</sub>                      | Input latch setup time - ZHT                                                     | 6.0 |     | 6.0 |     | 6.0 |      | 6.0 |      | 6.0  |      | 6.0  |      | 6.0  |      | 6.0  |      | ns   |
| t <sub>HILZ</sub>                      | Input latch hold time - ZHT                                                      | 0.0 |     | 0.0 |     | 0.0 |      | 0.0 |      | 0.0  |      | 0.0  |      | 0.0  |      | 0.0  |      | ns   |
| t <sub>PDIL</sub><br>Z <sub>i</sub>    | Transparent input latch to internal feedback - ZHT                               |     | 6.0 |     | 6.0 |     | 6.0  |     | 6.0  |      | 6.0  |      | 6.0  |      | 6.0  |      | 6.0  | ns   |
| Output Delays:                         |                                                                                  |     |     |     |     |     |      |     |      |      |      |      |      |      |      |      |      |      |
| t <sub>BUF</sub>                       | Output buffer delay                                                              |     | 1.5 |     | 1.5 |     | 1.8  |     | 2.0  |      | 2.5  |      | 3.0  |      | 3.0  |      | 3.0  | ns   |
| t <sub>SLW</sub>                       | Slow slew rate delay adder                                                       |     | 2.5 |     | 2.5 |     | 2.5  |     | 2.5  |      | 2.5  |      | 2.5  |      | 2.5  |      | 2.5  | ns   |
| t <sub>EA</sub>                        | Output enable time                                                               |     | 7.5 |     | 7.5 |     | 8.5  |     | 8.5  |      | 9.5  |      | 10.0 |      | 12.0 |      | 15.0 | ns   |
| t <sub>ER</sub>                        | Output disable time                                                              |     | 7.5 |     | 7.5 |     | 8.5  |     | 8.5  |      | 9.5  |      | 10.0 |      | 12.0 |      | 15.0 | ns   |
| Power Delay:                           |                                                                                  |     |     |     |     |     |      |     |      |      |      |      |      |      |      |      |      |      |
| t <sub>PL</sub>                        | Power-down mode delay adder                                                      |     | 2.5 |     | 2.5 |     | 2.5  |     | 2.5  |      | 2.5  |      | 2.5  |      | 2.5  |      | 2.5  | ns   |
| Reset and Preset Delays:               |                                                                                  |     |     |     |     |     |      |     |      |      |      |      |      |      |      |      |      |      |
| t <sub>SRI</sub>                       | Asynchronous reset or preset to internal register output                         |     | 7.5 |     | 7.7 |     | 8.0  |     | 8.0  |      | 9.5  |      | 11.0 |      | 13.0 |      | 16.0 | ns   |
| t <sub>SR</sub>                        | Asynchronous reset or preset to register output                                  |     | 9.0 |     | 9.2 |     | 10.0 |     | 10.0 |      | 12.0 |      | 14.0 |      | 16.0 |      | 19.0 | ns   |
| t <sub>SRR</sub>                       | Asynchronous reset and preset register recovery time                             | 7.0 |     | 7.0 |     | 7.5 |      | 7.5 |      | 8.0  |      | 8.0  |      | 10.0 |      | 15.0 |      | ns   |
| t <sub>SRW</sub>                       | Asynchronous reset or preset width                                               | 7.0 |     | 7.0 |     | 8.0 |      | 8.0 |      | 10.0 |      | 10.0 |      | 12.0 |      | 15.0 |      | ns   |
| Clock/LE Width:                        |                                                                                  |     |     |     |     |     |      |     |      |      |      |      |      |      |      |      |      |      |
| t <sub>WLS</sub>                       | Global clock width low                                                           | 2.0 |     | 2.0 |     | 2.5 |      | 2.5 |      | 3.0  |      | 4.0  |      | 5.0  |      | 6.0  |      | ns   |
| t <sub>WHS</sub>                       | Global clock width high                                                          | 2.0 |     | 2.0 |     | 2.5 |      | 2.5 |      | 3.0  |      | 4.0  |      | 5.0  |      | 6.0  |      | ns   |
| t <sub>WLA</sub>                       | Product term clock width low                                                     | 3.0 |     | 3.0 |     | 3.5 |      | 3.5 |      | 4.0  |      | 5.0  |      | 8.0  |      | 9.0  |      | ns   |
| t <sub>WHA</sub>                       | Product term clock width high                                                    | 3.0 |     | 3.0 |     | 3.5 |      | 3.5 |      | 4.0  |      | 5.0  |      | 8.0  |      | 9.0  |      | ns   |
| t <sub>GWS</sub>                       | Global gate width low (for low transparent) or high (for high transparent)       | 4.0 |     | 4.0 |     | 4.5 |      | 4.5 |      | 5.0  |      | 5.0  |      | 6.0  |      | 6.0  |      | ns   |
| t <sub>GWA</sub>                       | Product term gate width low (for low transparent) or high (for high transparent) | 4.0 |     | 4.0 |     | 4.5 |      | 4.5 |      | 5.0  |      | 5.0  |      | 6.0  |      | 9.0  |      | ns   |
| t <sub>WIRL</sub>                      | Input register clock width low                                                   | 3.0 |     | 3.0 |     | 3.5 |      | 3.5 |      | 4.0  |      | 5.0  |      | 6.0  |      | 6.0  |      | ns   |
| t <sub>WIRH</sub>                      | Input register clock width high                                                  | 3.0 |     | 3.0 |     | 3.5 |      | 3.5 |      | 4.0  |      | 5.0  |      | 6.0  |      | 6.0  |      | ns   |
| t <sub>WIL</sub>                       | Input latch gate width                                                           | 4.0 |     | 4.0 |     | 4.5 |      | 4.5 |      | 5.0  |      | 5.0  |      | 6.0  |      | 6.0  |      | ns   |

## ispMACH 4A TIMING PARAMETERS OVER OPERATING RANGES<sup>1</sup>

|                   |                                                                                                                                                               | -5  |     | -55 |     | -6  |     | -65  |     | -7   |     | -10  |     | -12  |     | -14  |     | Unit |
|-------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-----|-----|-----|-----|-----|------|-----|------|-----|------|-----|------|-----|------|-----|------|
|                   |                                                                                                                                                               | Min | Max | Min | Max | Min | Max | Min  | Max | Min  | Max | Min  | Max | Min  | Max | Min  | Max |      |
| Frequency:        |                                                                                                                                                               |     |     |     |     |     |     |      |     |      |     |      |     |      |     |      |     |      |
| f <sub>MAXS</sub> | External feedback, D-type, Min of 1/(t <sub>WLS</sub> + t <sub>WHS</sub> ) or 1/(t <sub>SS</sub> + t <sub>COS</sub> )                                         | 143 |     | 133 |     | 125 |     | 118  |     | 95.2 |     | 87.0 |     | 74.1 |     | 60.6 |     | MHz  |
|                   | External feedback, T-type, Min of 1/(t <sub>WLS</sub> + t <sub>WHS</sub> ) or 1/(t <sub>SST</sub> + t <sub>COS</sub> )                                        | 125 |     | 125 |     | 118 |     | 111  |     | 87.0 |     | 80.0 |     | 69.0 |     | 57.1 |     | MHz  |
|                   | Internal feedback (f <sub>CNT</sub> ), D-type, Min of 1/(t <sub>WLS</sub> + t <sub>WHS</sub> ) or 1/(t <sub>SS</sub> + t <sub>COSi</sub> )                    | 182 |     | 167 |     | 160 |     | 154  |     | 125  |     | 118  |     | 95.0 |     | 74.1 |     | MHz  |
|                   | Internal feedback (f <sub>CNT</sub> ), T-type, Min of 1/(t <sub>WLS</sub> + t <sub>WHS</sub> ) or 1/(t <sub>SST</sub> + t <sub>COSi</sub> )                   | 154 |     | 154 |     | 148 |     | 143  |     | 111  |     | 105  |     | 87.0 |     | 69.0 |     | MHz  |
|                   | No feedback <sup>2</sup> , Min of 1/(t <sub>WLS</sub> + t <sub>WHS</sub> ), 1/(t <sub>SS</sub> + t <sub>HS</sub> ) or 1/(t <sub>SST</sub> + t <sub>HS</sub> ) | 250 |     | 250 |     | 200 |     | 200  |     | 154  |     | 125  |     | 100  |     | 83.3 |     | MHz  |
| f <sub>MAXA</sub> | External feedback, D-type, Min of 1/(t <sub>WLA</sub> + t <sub>WHA</sub> ) or 1/(t <sub>SA</sub> + t <sub>COA</sub> )                                         | 111 |     | 111 |     | 108 |     | 100  |     | 83.3 |     | 66.7 |     | 55.6 |     | 43.5 |     | MHz  |
|                   | External feedback, T-type, Min of 1/(t <sub>WLA</sub> + t <sub>WHA</sub> ) or 1/(t <sub>SAT</sub> + t <sub>COA</sub> )                                        | 105 |     | 105 |     | 102 |     | 95.2 |     | 76.9 |     | 62.5 |     | 52.6 |     | 41.7 |     | MHz  |
|                   | Internal feedback (f <sub>CNTA</sub> ), D-type, Min of 1/(t <sub>WLA</sub> + t <sub>WHA</sub> ) or 1/(t <sub>SA</sub> + t <sub>COAi</sub> )                   | 133 |     | 133 |     | 125 |     | 125  |     | 105  |     | 83.3 |     | 66.7 |     | 50.0 |     | MHz  |
|                   | Internal feedback (f <sub>CNTA</sub> ), T-type, Min of 1/(t <sub>WLA</sub> + t <sub>WHA</sub> ) or 1/(t <sub>SAT</sub> + t <sub>COAi</sub> )                  | 125 |     | 125 |     | 125 |     | 118  |     | 95.2 |     | 76.9 |     | 62.5 |     | 47.6 |     | MHz  |
|                   | No feedback <sup>2</sup> , Min of 1/(t <sub>WLA</sub> + t <sub>WHA</sub> ), 1/(t <sub>SA</sub> + t <sub>HA</sub> ) or 1/(t <sub>SAT</sub> + t <sub>HA</sub> ) | 167 |     | 167 |     | 143 |     | 143  |     | 125  |     | 100  |     | 62.5 |     | 55.6 |     | MHz  |
| f <sub>MAXI</sub> | Maximum input register frequency, Min of 1/(t <sub>WIRH</sub> + t <sub>WIRL</sub> ) or 1/(t <sub>SIRS</sub> + t <sub>HIRS</sub> )                             | 167 |     | 167 |     | 143 |     | 143  |     | 125  |     | 100  |     | 83.3 |     | 83.3 |     | MHz  |

### Notes:

1. See "Switching Test Circuit" document on the Literature Download page of the Lattice web site.
2. This parameter does not apply to flip-flops in the emulated mode since the feedback path is required for emulation.

## CAPACITANCE<sup>1</sup>

| Parameter Symbol | Parameter Description | Test Conditions        |                           | Typ | Unit |
|------------------|-----------------------|------------------------|---------------------------|-----|------|
| $C_{IN}$         | Input capacitance     | $V_{IN}=2.0\text{ V}$  | 3.3 V or 5 V, 25°C, 1 MHz | 6   | pF   |
| $C_{I/O}$        | Output capacitance    | $V_{OUT}=2.0\text{ V}$ | 3.3 V or 5 V, 25°C, 1 MHz | 8   | pF   |

### Note:

1. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where this parameter may be affected.

## 100-BALL caBGA CONNECTION DIAGRAM (M4A3-128/64)

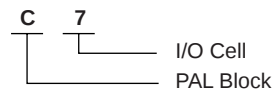
### Bottom View

100-Ball caBGA

|   | 10          | 9           | 8           | 7           | 6           | 5           | 4           | 3           | 2           | 1           |   |
|---|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|---|
| A | GND         | I/O63<br>H7 | I/O60<br>H4 | I/O57<br>H1 | GND         | GND         | I/O1<br>A1  | I/O4<br>A4  | I/O7<br>A7  | GND         | A |
| B | TRST        | GND         | I/O61<br>H5 | I5          | VCC         | I/O0<br>A0  | I/O6<br>A6  | GND         | TDI         | I/O15<br>B7 | B |
| C | I/O53<br>G5 | TDO         | I/O62<br>H6 | I/O58<br>H2 | I/O56<br>H0 | I/O2<br>A2  | GND         | I/O14<br>B6 | I/O13<br>B5 | I/O12<br>B4 | C |
| D | I/O50<br>G2 | I/O55<br>G7 | GND         | I/O59<br>H3 | I/O3<br>A3  | I/O5<br>A5  | I/O11<br>B3 | I/O10<br>B2 | CLK0/I0     | I/O9<br>B1  | D |
| E | CLK3/I4     | I/O49<br>G1 | I/O51<br>G3 | I/O54<br>G6 | VCC         | I/O16<br>C0 | I/O20<br>C4 | I/O8<br>B0  | VCC         | GND         | E |
| F | GND         | VCC         | I/O40<br>F0 | I/O52<br>G4 | I/O48<br>G0 | VCC         | I/O22<br>C6 | I/O19<br>C3 | I/O17<br>C1 | CLK1/I1     | F |
| G | I/O41<br>F1 | CLK2/I3     | I/O42<br>F2 | I/O43<br>F3 | I/O37<br>E5 | I/O35<br>E3 | I/O27<br>D3 | GND         | I/O23<br>C7 | I/O18<br>C2 | G |
| H | I/O44<br>F4 | I/O45<br>F5 | I/O46<br>F6 | GND         | I/O34<br>E2 | I/O24<br>D0 | I/O26<br>D2 | I/O30<br>D6 | TCK         | I/O21<br>C5 | H |
| J | I/O47<br>F7 | ENABLE      | GND         | I/O38<br>E6 | I/O32<br>E0 | VCC         | I2          | I/O29<br>D5 | GND         | TMS         | J |
| K | GND         | I/O39<br>E7 | I/O36<br>E4 | I/O33<br>E1 | GND         | GND         | I/O25<br>D1 | I/O28<br>D4 | I/O31<br>D7 | GND         | K |
|   | 10          | 9           | 8           | 7           | 6           | 5           | 4           | 3           | 2           | 1           |   |

#### PIN DESIGNATIONS

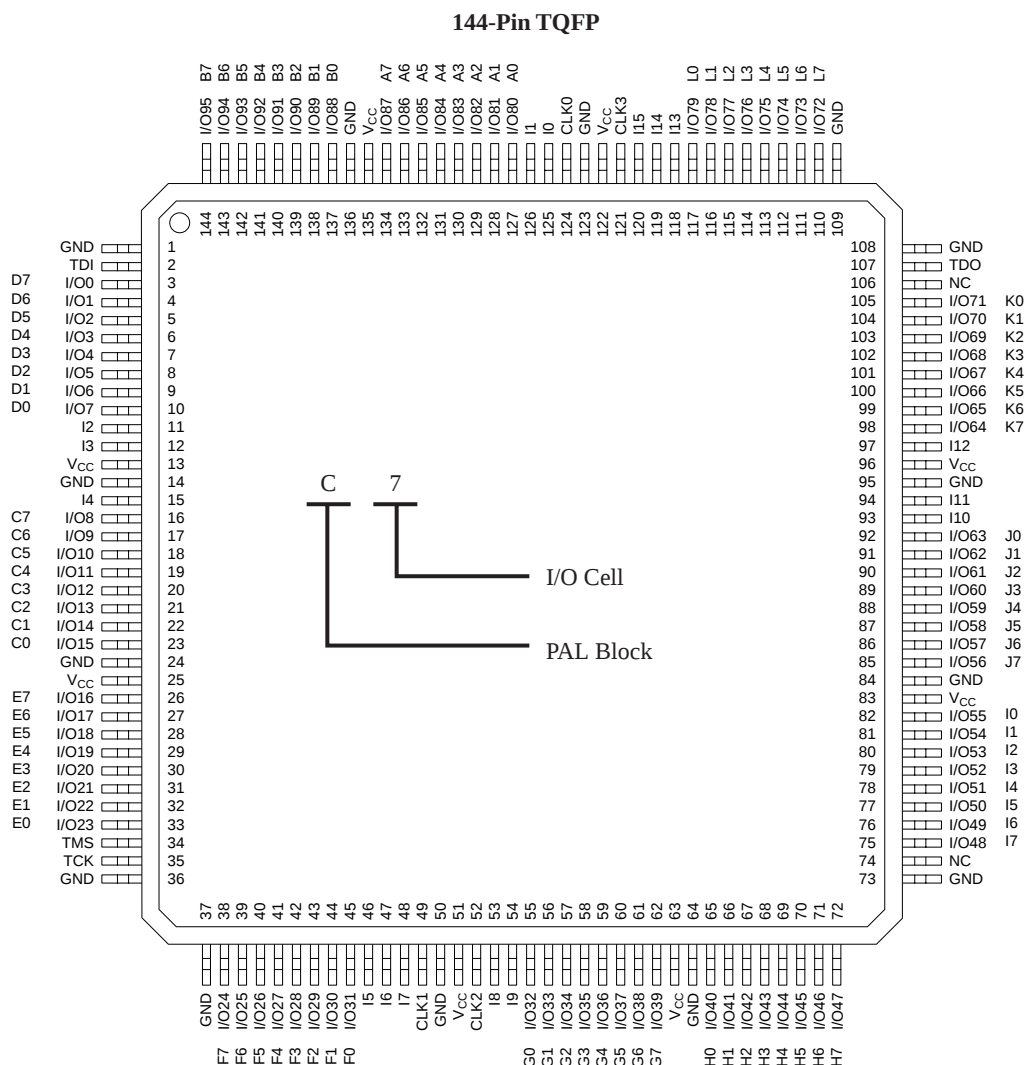
CLK = Clock  
 GND = Ground  
 I = Input  
 I/O = Input/Output  
 N/C = No Connect  
 VCC = Supply Voltage  
 TDI = Test Data In  
 TCK = Test Clock  
 TMS = Test Mode Select  
 TDO = Test Data Out  
 TRST = Test Reset  
 ENABLE = Program



17466G-100cabga

## 144-PIN TQFP CONNECTION DIAGRAM (M4A(3,5)-192/96)

### Top View



## PIN DESIGNATIONS

- CLK = Clock
- GND = Ground
- I = Input
- I/O = Input/Output
- V<sub>CC</sub> = Supply Voltage
- TDI = Test Data In
- TCK = Test Clock
- TMS = Test Mode Select
- TDO = Test Data Out

# 256-BALL BGA CONNECTION DIAGRAM (M4A3-256/128)

## Bottom View

### 256-Ball BGA

|   | 20           | 19           | 18           | 17           | 16                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | 15           | 14           | 13           | 12          | 11  | 10  | 9           | 8           | 7           | 6           | 5           | 4           | 3           | 2           | 1           |   |
|---|--------------|--------------|--------------|--------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------|--------------|--------------|-------------|-----|-----|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|---|
| A | GND          | N/C          | GND          | I/O108<br>N4 | I/O105<br>N1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | GND          | I/O100<br>M4 | I/O96<br>M0  | GND         | GND | GND | GND         | I/O95<br>L0 | I/O91<br>L4 | GND         | I/O87<br>K0 | N/C         | GND         | GND         | GND         | A |
| B | GND          | I/O113<br>O6 | N/C          | I/O109<br>N5 | I/O106<br>N2                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | I/O103<br>M7 | I/O102<br>M6 | I/O98<br>M2  | N/C         | I11 | N/C | N/C         | I/O93<br>L2 | I/O89<br>L6 | I/O88<br>L7 | I/O85<br>K2 | I/O83<br>K4 | I/O82<br>K5 | N/C         | GND         | B |
| C | I/O116<br>O3 | N/C          | VCC          | TRST         | I/O111<br>N7                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | I/O107<br>N3 | I/O104<br>N0 | I/O101<br>M5 | I/O97<br>M1 | N/C | I10 | I/O94<br>L1 | I/O90<br>L5 | I/O86<br>K1 | I/O84<br>K3 | I/O80<br>K7 | ENABLE      | VCC         | I/O78<br>J6 | I/O74<br>J2 | C |
| D | I/O120<br>P7 | I/O117<br>O2 | I/O112<br>O7 | VCC          | VCC                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | I/O110<br>N6 | VCC          | N/C          | I/O99<br>M3 | N/C | I9  | I/O92<br>L3 | N/C         | VCC         | I/O81<br>K6 | VCC         | VCC         | I/O79<br>J7 | I/O75<br>J3 | I/O71<br>I7 | D |
| E | I/O123<br>P4 | I/O119<br>O0 | I/O114<br>O5 | TDI          | <div><div>PIN DESIGNATIONS</div><div>CLK = Clock</div><div>GND = Ground</div><div>I = Input</div><div>I/O = Input/Output</div><div>N/C = No Connect</div><div>VCC = Supply Voltage</div><div>TDI = Test Data In</div><div>TCK = Test Clock</div><div>TMS = Test Mode Select</div><div>TDO = Test Data Out</div><div>TRST = Test Reset</div><div>ENABLE = Program</div><div><div>C7</div><div>I/O Cell</div><div>PAL Block</div></div></div> <td>TDO</td> <td>I/O77<br/>J5</td> <td>I/O72<br/>J0</td> <td>I/O68<br/>I4</td> <td>E</td> |              |              |              |             |     |     |             |             |             |             |             | TDO         | I/O77<br>J5 | I/O72<br>J0 | I/O68<br>I4 | E |
| F | GND          | I/O122<br>P5 | I/O118<br>O1 | I/O115<br>O4 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |              |              |              |             |     |     |             |             |             |             |             | I/O76<br>J4 | I/O73<br>J1 | I/O69<br>I5 | GND         | F |
| G | I12          | I/O125<br>P2 | I/O121<br>P6 | VCC          |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |              |              |              |             |     |     |             |             |             |             |             | VCC         | I/O70<br>I6 | I/O65<br>I1 | I8          | G |
| H | GND          | I/O127<br>P0 | I/O126<br>P1 | I/O124<br>P3 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |              |              |              |             |     |     |             |             |             |             |             | I/O67<br>I3 | I/O66<br>I2 | I/O64<br>I0 | GND         | H |
| J | N/C          | N/C          | N/C          | I13          |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |              |              |              |             |     |     |             |             |             |             |             | I7          | N/C         | N/C         | N/C         | J |
| K | GND          | CLK3         | N/C          | N/C          |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |              |              |              |             |     |     |             |             |             |             |             | N/C         | N/C         | CLK2        | N/C         | K |
| L | N/C          | CLK0         | N/C          | N/C          |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |              |              |              |             |     |     |             |             |             |             |             | N/C         | N/C         | CLK1        | GND         | L |
| M | N/C          | N/C          | N/C          | I0           |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |              |              |              |             |     |     |             |             |             |             |             | I6          | N/C         | I/O63<br>H0 | I/O62<br>H1 | M |
| N | GND          | I/O0<br>A0   | I/O2<br>A2   | I/O3<br>A3   |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |              |              |              |             |     |     |             |             |             |             |             | I/O60<br>H3 | I/O61<br>H2 | I/O59<br>H4 | GND         | N |
| P | I1           | I/O1<br>A1   | I/O6<br>A6   | VCC          | VCC                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | I/O57<br>H6  | I/O58<br>H5  | I5           | P           |     |     |             |             |             |             |             |             |             |             |             |   |
| R | GND          | I/O5<br>A5   | I/O9<br>B1   | N/C          | I/O51<br>G4                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | I/O54<br>G1  | I/O56<br>H7  | GND          | R           |     |     |             |             |             |             |             |             |             |             |             |   |
| T | I/O4<br>A4   | I/O8<br>B0   | I/O12<br>B4  | TCK          | TMS                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | I/O50<br>G5  | I/O55<br>G0  | N/C          | T           |     |     |             |             |             |             |             |             |             |             |             |   |
| U | I/O7<br>A7   | I/O11<br>B3  | I/O15<br>B7  | VCC          | VCC                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | I/O18<br>C5  | VCC          | I/O24<br>D7  | I/O29<br>D2 | I2  | N/C | I/O35<br>E3 | N/C         | VCC         | N/C         | VCC         | VCC         | I/O48<br>G7 | I/O53<br>G2 | N/C         | U |
| V | I/O10<br>B2  | I/O13<br>B5  | VCC          | I/O16<br>C7  | I/O17<br>C6                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | I/O21<br>C2  | I/O23<br>C0  | I/O27<br>D4  | I/O31<br>D0 | I3  | N/C | I/O33<br>E1 | I/O37<br>E5 | I/O41<br>F1 | I/O43<br>F3 | I/O46<br>F6 | I/O47<br>F7 | VCC         | I/O52<br>G3 | N/C         | V |
| W | GND          | I/O14<br>B6  | N/C          | N/C          | I/O19<br>C4                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | I/O22<br>C1  | I/O25<br>D6  | I/O28<br>D3  | N/C         | N/C | I4  | N/C         | I/O34<br>E2 | I/O38<br>E6 | I/O39<br>E7 | I/O42<br>F2 | I/O45<br>F5 | N/C         | I/O49<br>G6 | GND         | W |
| Y | GND          | GND          | GND          | N/C          | I/O20<br>C3                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | GND          | I/O26<br>D5  | I/O30<br>D1  | GND         | GND | GND | GND         | I/O32<br>E0 | I/O36<br>E4 | GND         | I/O40<br>F0 | I/O44<br>F4 | GND         | N/C         | GND         | Y |
|   | 20           | 19           | 18           | 17           | 16                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | 15           | 14           | 13           | 12          | 11  | 10  | 9           | 8           | 7           | 6           | 5           | 4           | 3           | 2           | 1           |   |

17466G-045

## 256-BALL fpBGA CONNECTION DIAGRAM (M4A3-256/192)

### Bottom View

256-Ball fpBGA

|   | 16            | 15            | 14            | 13            | 12            | 11            | 10            | 9             | 8            | 7            | 6            | 5            | 4            | 3            | 2            | 1            |   |
|---|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|---|
| A | I/O167<br>N15 | I/O181<br>O13 | I/O180<br>O12 | I/O177<br>O9  | I/O174<br>O6  | I/O172<br>O4  | I/O191<br>P14 | I/O186<br>P4  | I/O1<br>A2   | I/O3<br>A6   | GCLK0        | I/O9<br>B1   | I/O13<br>B5  | I/O15<br>B7  | I/O18<br>B10 | I/O20<br>B12 | A |
| B | I/O165<br>N13 | I/O166<br>N14 | I/O182<br>O14 | I/O179<br>O11 | I/O175<br>O7  | I/O173<br>O5  | I/O168<br>O0  | I/O187<br>P6  | I/O0<br>A0   | I/O5<br>A10  | I/O7<br>A14  | I/O10<br>B2  | I/O16<br>B8  | I/O19<br>B11 | I/O21<br>B13 | NC           | B |
| C | I/O163<br>N11 | I/O164<br>N12 | NC            | I/O183<br>O15 | I/O178<br>O10 | I/O170<br>O2  | I/O171<br>O3  | I/O189<br>P10 | I/O184<br>P0 | I/O6<br>A12  | I/O12<br>B4  | I/O14<br>B6  | I/O23<br>B15 | I/O22<br>B14 | TDI          | I/O39<br>C15 | C |
| D | I/O158<br>N6  | I/O159<br>N7  | TDO           | GND           | GND           | VCC           | GND           | VCC           | GND          | GND          | VCC          | GND          | VCC          | I/O17<br>B9  | I/O38<br>C14 | I/O37<br>C13 | D |
| E | I/O156<br>N4  | NC            | I/O162<br>N10 | VCC           | I/O160<br>N8  | I/O161<br>N9  | I/O190<br>P12 | GCLK3         | I/O188<br>P8 | I/O2<br>A4   | I/O8<br>B0   | NC           | GND          | I/O36<br>C12 | I/O35<br>C11 | I/O31<br>C7  | E |
| F | I/O152<br>N0  | I/O157<br>N5  | I/O155<br>N3  | GND           | I/O154<br>N2  | I/O153<br>N1  | I/O176<br>O8  | I/O169<br>O1  | I/O185<br>P2 | I/O4<br>A8   | I/O11<br>B3  | I/O34<br>C10 | VCC          | I/O32<br>C8  | I/O30<br>C6  | I/O29<br>C5  | F |
| G | I/O147<br>M6  | I/O150<br>M12 | I/O149<br>M10 | VCC           | I/O148<br>M8  | I/O151<br>M14 | VCC           | GND           | GND          | VCC          | I/O33<br>C9  | I/O28<br>C4  | GND          | I/O26<br>C2  | I/O25<br>C1  | I/O47<br>D14 | G |
| H | I/O144<br>M0  | I/O146<br>M4  | I/O145<br>OM2 | GND           | I/O136<br>L0  | I/O137<br>L2  | GND           | VCC           | VCC          | GND          | I/O27<br>C3  | I/O24<br>C0  | VCC          | I/O44<br>D8  | I/O43<br>D6  | I/O42<br>D4  | H |
| J | I/O138<br>L4  | I/O139<br>L6  | I/O140<br>L8  | GND           | I/O142<br>L12 | I/O141<br>L10 | GND           | VCC           | VCC          | GND          | I/O46<br>D12 | I/O45<br>D10 | GND          | I/O49<br>E2  | I/O48<br>E0  | I/O50<br>E4  | J |
| K | I/O143<br>L14 | I/O120<br>K0  | I/O121<br>K1  | VCC           | I/O123<br>K3  | I/O122<br>K2  | VCC           | GND           | GND          | VCC          | I/O41<br>D2  | I/O40<br>D0  | VCC          | I/O55<br>E14 | I/O54<br>E12 | I/O56<br>F0  | K |
| L | I/O124<br>K4  | I/O125<br>K5  | I/O127<br>K7  | GND           | I/O130<br>K10 | I/O126<br>K6  | I/O98<br>I4   | I/O91<br>H6   | I/O75<br>G3  | I/O77<br>G5  | I/O52<br>E8  | I/O51<br>E6  | GND          | I/O59<br>F3  | I/O60<br>F4  | I/O57<br>F1  | L |
| M | I/O128<br>K8  | I/O129<br>K9  | I/O131<br>K11 | GND           | I/O107<br>J3  | I/O105<br>J1  | I/O100<br>I8  | I/O90<br>H4   | I/O74<br>G2  | I/O80<br>G8  | I/O83<br>G11 | I/O53<br>E10 | VCC          | I/O68<br>F12 | I/O63<br>F7  | I/O58<br>F2  | M |
| N | I/O132<br>K12 | I/O133<br>K13 | I/O135<br>K15 | VCC           | GND           | VCC           | GND           | VCC           | GND          | GND          | VCC          | GND          | GND          | TCK          | I/O64<br>F8  | I/O61<br>F5  | N |
| P | I/O134<br>K14 | I/O117<br>J13 | I/O118<br>J14 | I/O119<br>J15 | I/O108<br>J4  | I/O106<br>J2  | I/O101<br>I10 | I/O89<br>H2   | I/O93<br>H10 | I/O94<br>H12 | I/O79<br>G7  | I/O84<br>G12 | I/O87<br>G15 | TMS          | I/O65<br>F9  | I/O62<br>F6  | P |
| R | I/O116<br>J12 | I/O115<br>J11 | I/O112<br>J8  | I/O111<br>J7  | I/O104<br>J0  | I/O102<br>I12 | I/O99<br>I6   | I/O96<br>I0   | I/O92<br>H8  | I/O72<br>G0  | I/O76<br>G4  | I/O81<br>G9  | I/O85<br>G13 | I/O71<br>F15 | I/O67<br>F11 | I/O66<br>F10 | R |
| T | I/O114<br>J10 | I/O113<br>J9  | I/O110<br>J6  | I/O109<br>J5  | I/O103<br>I14 | GCLK2         | I/O97<br>I2   | I/O88<br>H0   | GCLK1        | I/O95<br>H14 | I/O73<br>G1  | I/O78<br>G6  | I/O82<br>G10 | I/O86<br>G14 | I/O70<br>F14 | I/O69<br>F13 | T |
|   | 16            | 15            | 14            | 13            | 12            | 11            | 10            | 9             | 8            | 7            | 6            | 5            | 4            | 3            | 2            | 1            |   |

#### PIN DESIGNATIONS

CLK = Clock  
 GND = Ground  
 I = Input  
 I/O = Input/Output  
 N/C = No Connect  
 VCC = Supply Voltage  
 TDI = Test Data In  
 TCK = Test Clock  
 TMS = Test Mode Select  
 TDO = Test Data Out



17466G-047

## 256-BALL fpBGA CONNECTION DIAGRAM (M4A3-512/192)

### Bottom View

#### 256-Ball fpBGA

|   | 16            | 15            | 14            | 13            | 12            | 11            | 10            | 9             | 8             | 7           | 6           | 5           | 4           | 3           | 2           | 1           |   |
|---|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|---|
| A | I/O159<br>KX7 | I/O181<br>OX5 | I/O180<br>OX4 | I/O177<br>OX1 | I/O174<br>NX6 | I/O172<br>NX4 | I/O191<br>PX7 | I/O186<br>PX2 | I/O1<br>A1    | I/O3<br>A3  | CLK0        | I/O17<br>C1 | I/O21<br>C5 | I/O23<br>C7 | I/O10<br>B2 | I/O12<br>B4 | A |
| B | I/O157<br>KX5 | I/O158<br>KX6 | I/O182<br>OX6 | I/O179<br>OX3 | I/O175<br>NX7 | I/O173<br>NX5 | I/O168<br>NX0 | I/O187<br>PX3 | I/O0<br>A0    | I/O5<br>A5  | I/O7<br>A7  | I/O18<br>C2 | I/O8<br>B0  | I/O11<br>B3 | I/O13<br>B5 | N/C         | B |
| C | I/O155<br>KX3 | I/O156<br>KX4 | N/C           | I/O183<br>OX7 | I/O178<br>OX2 | I/O170<br>NX2 | I/O171<br>NX3 | I/O189<br>PX5 | I/O184<br>PX0 | I/O6<br>A6  | I/O20<br>C4 | I/O22<br>C6 | I/O15<br>B7 | I/O14<br>B6 | TDI         | I/O39<br>F7 | C |
| D | I/O150<br>JX6 | I/O151<br>JX7 | TDO           | GND           | GND           | VCC           | GND           | VCC           | GND           | GND         | VCC         | GND         | VCC         | I/O9<br>B1  | I/O38<br>F6 | I/O37<br>F5 | D |
| E | I/O148<br>JX4 | N/C           | I/O154<br>KX2 | VCC           | I/O152<br>KX0 | I/O153<br>KX1 | I/O190<br>PX6 | CLK3          | I/O188<br>PX4 | I/O2<br>A2  | I/O16<br>C0 | N/C         | GND         | I/O36<br>F4 | I/O35<br>F3 | I/O47<br>G7 | E |
| F | I/O144<br>JX0 | I/O149<br>JX5 | I/O147<br>JX3 | GND           | I/O146<br>JX2 | I/O145<br>JX1 | I/O176<br>OX0 | I/O169<br>NX1 | I/O185<br>PX1 | I/O4<br>A4  | I/O19<br>C3 | I/O34<br>F2 | VCC         | I/O32<br>F0 | I/O46<br>G6 | I/O45<br>G5 | F |
| G | I/O163<br>LX3 | I/O166<br>LX6 | I/O165<br>LX5 | VCC           | I/O164<br>LX4 | I/O167<br>LX7 | VCC           | GND           | GND           | VCC         | I/O33<br>F1 | I/O44<br>G4 | GND         | I/O42<br>G2 | I/O41<br>G1 | I/O31<br>E7 | G |
| H | I/O160<br>LX0 | I/O162<br>LX2 | I/O161<br>LX1 | GND           | I/O120<br>EX0 | I/O121<br>EX1 | GND           | VCC           | VCC           | GND         | I/O43<br>G3 | I/O40<br>G0 | VCC         | I/O28<br>E4 | I/O27<br>E3 | I/O26<br>E2 | H |
| J | I/O122<br>EX2 | I/O123<br>EX3 | I/O124<br>EX4 | GND           | I/O126<br>EX6 | I/O125<br>EX5 | GND           | VCC           | VCC           | GND         | I/O30<br>E6 | I/O29<br>E5 | GND         | I/O65<br>L1 | I/O64<br>L0 | I/O66<br>L2 | J |
| K | I/O127<br>EX7 | I/O136<br>GX0 | I/O137<br>GX1 | VCC           | I/O139<br>GX3 | I/O138<br>GX2 | VCC           | GND           | GND           | VCC         | I/O25<br>E1 | I/O24<br>E0 | VCC         | I/O71<br>L7 | I/O70<br>L6 | I/O48<br>J0 | K |
| L | I/O140<br>GX4 | I/O141<br>GX5 | I/O143<br>GX7 | GND           | I/O130<br>FX2 | I/O142<br>GX6 | I/O98<br>AX2  | I/O91<br>P3   | I/O75<br>N3   | I/O77<br>N5 | I/O68<br>L4 | I/O67<br>L3 | GND         | I/O51<br>J3 | I/O52<br>J4 | I/O49<br>J1 | L |
| M | I/O128<br>FX0 | I/O129<br>FX1 | I/O131<br>FX3 | GND           | I/O115<br>CX3 | I/O113<br>CX1 | I/O100<br>AX4 | I/O90<br>P2   | I/O74<br>N2   | I/O80<br>O0 | I/O83<br>O3 | I/O69<br>L5 | VCC         | I/O60<br>K4 | I/O55<br>J7 | I/O50<br>J2 | M |
| N | I/O132<br>FX4 | I/O133<br>FX5 | I/O135<br>FX7 | VCC           | GND           | VCC           | GND           | VCC           | GND           | GND         | VCC         | GND         | GND         | TCK         | I/O56<br>K0 | I/O53<br>J5 | N |
| P | I/O134<br>FX6 | I/O109<br>BX5 | I/O110<br>BX6 | I/O111<br>BX7 | I/O116<br>CX4 | I/O114<br>CX2 | I/O101<br>AX5 | I/O89<br>P1   | I/O93<br>P5   | I/O94<br>P6 | I/O79<br>N7 | I/O84<br>O4 | I/O87<br>O7 | TMS         | I/O57<br>K1 | I/O54<br>J6 | P |
| R | I/O108<br>BX4 | I/O107<br>BX3 | I/O104<br>BX0 | I/O119<br>CX7 | I/O112<br>CX0 | I/O102<br>AX6 | I/O99<br>AX3  | I/O96<br>AX0  | I/O92<br>P4   | I/O72<br>N0 | I/O76<br>N4 | I/O81<br>O1 | I/O85<br>O5 | I/O63<br>K7 | I/O59<br>K3 | I/O58<br>K2 | R |
| T | I/O106<br>BX2 | I/O105<br>BX1 | I/O118<br>CX6 | I/O117<br>CX5 | I/O103<br>AX7 | CLK2          | I/O97<br>AX1  | I/O88<br>P0   | CLK1          | I/O95<br>P7 | I/O73<br>N1 | I/O78<br>N6 | I/O82<br>O2 | I/O86<br>O6 | I/O62<br>K6 | I/O61<br>K5 | T |
|   | 16            | 15            | 14            | 13            | 12            | 11            | 10            | 9             | 8             | 7           | 6           | 5           | 4           | 3           | 2           | 1           |   |

#### PIN DESIGNATIONS

CLK = Clock  
 GND = Ground  
 I = Input  
 I/O = Input/Output  
 N/C = No Connect  
 VCC = Supply Voltage  
 TDI = Test Data In  
 TCK = Test Clock  
 TMS = Test Mode Select  
 TDO = Test Data Out



m4a3.512.192\_256bga

| 5V Commercial Combinations |              |              |
|----------------------------|--------------|--------------|
| M4A5-32/32                 | -5, -7, -10, | JC, VC, VC48 |
| M4A5-64/32                 | -55, -7, -10 | JC, VC, VC48 |
| M4A5-96/48                 |              | VC           |
| M4A5-128/64                |              | YC, VC       |
| M4A5-192/96                | -6, -7, -10  | VC           |
| M4A5-256/128               | -65, -7, -10 | YC           |

| 5V Industrial Combinations |              |              |
|----------------------------|--------------|--------------|
| M4A5-32/32                 | -7, -10, -12 | JJ, VI, VI48 |
| M4A5-64/32                 | -7, -10, -12 | JJ, VI, VI48 |
| M4A5-96/48                 |              | VI           |
| M4A5-128/64                |              | YI, VI       |
| M4A5-192/96                | -7, -10, -12 | VI           |
| M4A5-256/128               | -10, -12     | YI           |

## Lead-free Packaging

| 3.3V Commercial Combinations |               |                 |
|------------------------------|---------------|-----------------|
| M4A3-32/32                   | -5, -7, -10   | VNC, VNC48, JNC |
| M4A3-64/32                   | -55, -7, -10  | VNC, VNC48, JNC |
| M4A3-64/64                   |               | VNC             |
| M4A3-128/64                  |               | VNC             |
| M4A3-192/96                  | -6, -7, -10   | VNC             |
| M4A3-256/128                 | -55, -7, -10  | FANC, YNC       |
| M4A3-256/160                 | -7, -10       | YNC             |
| M4A3-256/192                 |               | FANC            |
| M4A3-384/192                 | -65, -10, -12 | FANC            |
| M4A3-512/192                 | -7, -10, -12  | FANC            |

| 3.3V Industrial Combinations |               |                 |
|------------------------------|---------------|-----------------|
| M4A3-32/32                   | -7, -10, -12  | VNI, VNI48, JNI |
| M4A3-64/32                   |               | VNI, VNI48, JNI |
| M4A3-64/64                   |               | VNI             |
| M4A3-128/64                  |               | VNI             |
| M4A3-192/96                  | -10, -12      | VNI             |
| M4A3-256/128                 |               | FANI, YNI       |
| M4A3-256/160                 |               | YNI             |
| M4A3-256/192                 | -10, -12, -14 | FANI            |
| M4A3-384/192                 |               | FANI            |
| M4A3-512/192                 |               | FANI            |

| 5V Commercial Combinations |              |                 |
|----------------------------|--------------|-----------------|
| M4A5-32/32                 | -5, -7, -10  | VNC, VNC48, JNC |
| M4A5-64/32                 | -55, -7, -10 | VNC, VNC48, JNC |
| M4A5-96/48                 |              | VNC             |
| M4A5-128/64                |              | VNC, YNC        |
| M4A5-192/96                | -6, -7, -10  | VNC             |
| M4A5-256/128               | -65, -7, -10 | YNC             |

| 5V Industrial Combinations |              |                 |
|----------------------------|--------------|-----------------|
| M4A5-32/32                 | -7, -10, -12 | VNI, VNI48, JNI |
| M4A5-64/32                 |              | VNI, VNI48, JNI |
| M4A5-96/48                 |              | VNI             |
| M4A5-128/64                |              | VNI, YNI        |
| M4A5-192/96                |              | VNI             |
| M4A5-256/128               |              | YNI             |

Most ispMACH devices are dual-marked with both Commercial and Industrial grades. The Industrial speed grade is slower, i.e., M4A3-256/128-7YC-10YI

### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local Lattice sales office to confirm availability of specific valid combinations and to check on newly released combinations.