Lattice Semiconductor Corporation - M4A3-64/32-12VI48 Datasheet

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Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	12 ns
Voltage Supply - Internal	3V ~ 3.6V
Number of Logic Elements/Blocks	-
Number of Macrocells	64
Number of Gates	-
Number of I/O	32
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-TQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/m4a3-64-32-12vi48

Table 1. ispMACH 4A Device Features

3.3 V Devices								
Feature	**M4A3-32**	**M4A3-64**	**M4A3-96**	**M4A3-128**	**M4A3-192**	**M4A3-256**	**M4A3-384**	**M4A3-512**
Macrocells	32	64	96	128	192	256	384	512
User I/O options	32	32/64	48	64	96	128/160/192	160/192	160/192/256
t_{PD} (ns)	5.0	5.5	5.5	5.5	6.0	5.5	6.5	7.5
f_{CNT} (MHz)	182	167	167	167	160	167	154	125
t_{COS} (ns)	4.0	4.0	4.0	4.0	4.5	4.0	4.5	5.5
t_{SS} (ns)	3.0	3.5	3.5	3.5	3.5	3.5	3.5	5.0
Static Power (mA)	20	25/52	40	55	85	110/150	149/155	179
JTAG Compliant	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
PCI Compliant	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes

5 V Devices						
Feature	**M4A5-32**	**M4A5-64**	**M4A5-96**	**M4A5-128**	**M4A5-192**	**M4A5-256**
Macrocells	32	64	96	128	192	256
User I/O options	32	32	48	64	96	128
t_{PD} (ns)	5.0	5.5	5.5	5.5	6.0	6.5
f_{CNT} (MHz)	182	167	167	167	160	154
t_{COS} (ns)	4.0	4.0	4.0	4.0	4.5	5.0
t_{SS} (ns)	3.0	3.5	3.5	3.5	3.5	3.5
Static Power (mA)	20	25	40	55	74	110
JTAG Compliant	Yes	Yes	Yes	Yes	Yes	Yes
PCI Compliant	Yes	Yes	Yes	Yes	Yes	Yes

I/O Cell

The I/O cell (Figures 10 and 11) simply consists of a programmable output enable, a feedback path, and flip-flop (except ispMACH 4A devices with 1:1 macrocell-I/O cell ratio). An individual output enable product term is provided for each I/O cell. The feedback signal drives the input switch matrix.

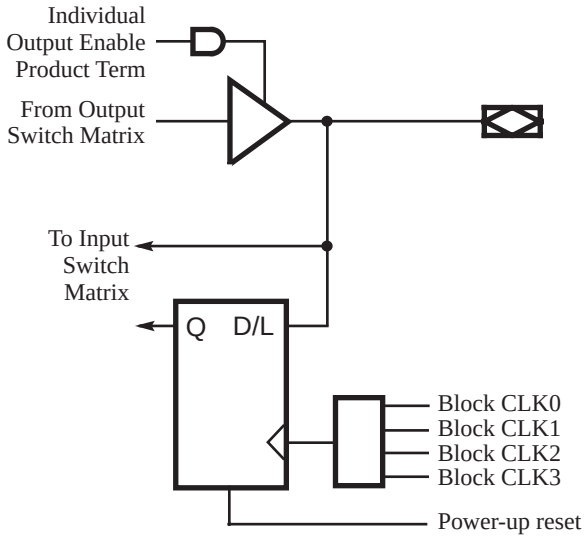

Figure 10. I/O Cell for ispMACH 4A Devices with 2:1 Macrocell-I/O Cell Ratio

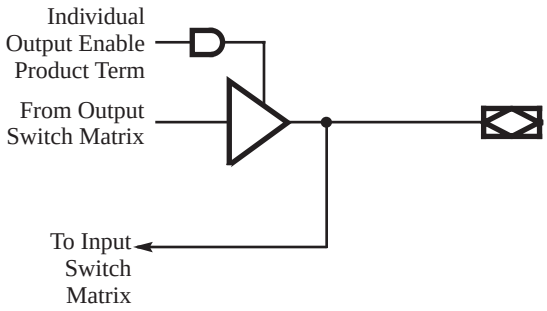

Figure 11. I/O Cell for ispMACH 4A Devices with 1:1 Macrocell-I/O Cell Ratio

The I/O cell (Figure 10) contains a flip-flop, which provides the capability for storing the input in a D-type register or latch. The clock can be any of the PAL block clocks. Both the direct and registered versions of the input are sent to the input switch matrix. This allows for such functions as "time-domain-multiplexed" data comparison, where the first data value is stored, and then the second data value is put on the I/O pin and compared with the previous stored value.

Note that the flip-flop used in the ispMACH 4A I/O cell is independent of the flip-flops in the macrocells. It powers up to a logic low.

Zero-Hold-Time Input Register

The ispMACH 4A devices have a zero-hold-time (ZHT) fuse which controls the time delay associated with loading data into all I/O cell registers and latches. When programmed, the ZHT fuse increases the data path setup delays to input storage elements, matching equivalent delays in the clock path. When the fuse is erased, the setup time to the input storage element is minimized. This feature facilitates doing worst-case designs for which data is loaded from sources which have low (or zero) minimum output propagation delays from clock edges.

Input Switch Matrix

The input switch matrix (Figures 12 and 13) optimizes routing of inputs to the central switch matrix. Without the input switch matrix, each input and feedback signal has only one way to enter the central switch matrix. The input switch matrix provides additional ways for these signals to enter the central switch matrix.

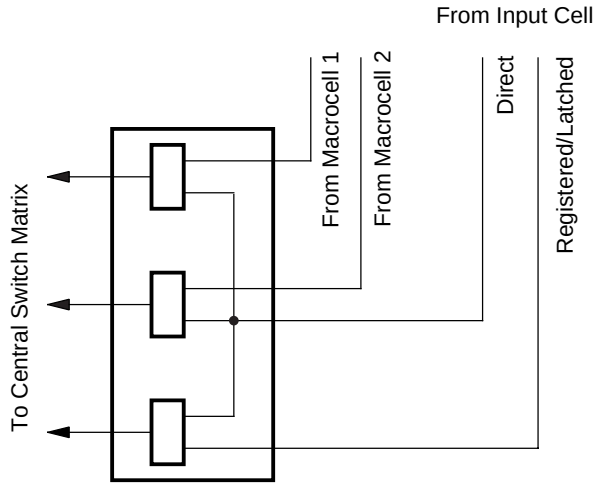

Figure 12. ispMACH 4A with 2:1 Macrocell-I/O Cell Ratio - Input Switch Matrix

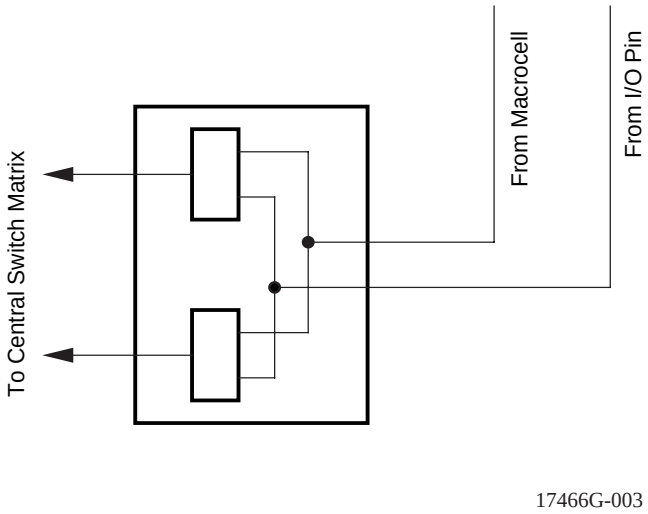

Figure 13. ispMACH 4A with 1:1 Macrocell-I/O Cell Ratio - Input Switch Matrix

PAL Block Clock Generation

Each ispMACH 4A device has four clock pins that can also be used as inputs. These pins drive a clock generator in each PAL block (Figure 14). The clock generator provides four clock signals that can be used anywhere in the PAL block. These four PAL block clock signals can consist of a large number of combinations of the true and complement edges of the global clock signals. Table 14 lists the possible combinations.

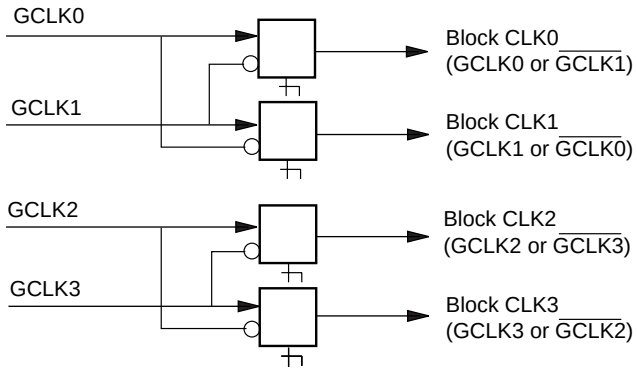

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Figure 14. PAL Block Clock Generator [1]

1. M4A(3,5)-32/32 and M4A(3,5)-64/32 have only two clock pins, GCLK0 and GCLK1. GCLK2 is tied to GCLK0, and GCLK3 is tied to GCLK1.

Table 14. PAL Block Clock Combinations[1]

Block CLK0	Block CLK1	Block CLK2	Block CLK3
GCLK0	GCLK1	X	X
$\overline{\text{GCLK1}}$	GCLK1	X	X
GCLK0	$\overline{\text{GCLK0}}$	X	X
$\overline{\text{GCLK1}}$	$\overline{\text{GCLK0}}$	X	X
X	X	GCLK2 (GCLK0)	GCLK3 (GCLK1)
X	X	$\overline{\text{GCLK3}}$ ($\overline{\text{GCLK1}}$)	GCLK3 (GCLK1)
X	X	GCLK2 (GCLK0)	$\overline{\text{GCLK2}}$ ($\overline{\text{GCLK0}}$)
X	X	$\overline{\text{GCLK3}}$ ($\overline{\text{GCLK1}}$)	$\overline{\text{GCLK2}}$ ($\overline{\text{GCLK0}}$)

Note:

1. Values in parentheses are for the M4A(3,5)-32/32 and M4A(3,5)-64/32.

This feature provides high flexibility for partitioning state machines and dual-phase clocks. It also allows latches to be driven with either polarity of latch enable, and in a master-slave configuration.

IEEE 1149.1-COMPLIANT BOUNDARY SCAN TESTABILITY

All ispMACH 4A devices have boundary scan cells and are compliant to the IEEE 1149.1 standard. This allows functional testing of the circuit board on which the device is mounted through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test node data to be captured and shifted out for verification. In addition, these devices can be linked into a board-level serial scan path for more complete board-level testing.

IEEE 1149.1-COMPLIANT IN-SYSTEM PROGRAMMING

Programming devices in-system provides a number of significant benefits including: rapid prototyping, lower inventory levels, higher quality, and the ability to make in-field modifications. All ispMACH 4A devices provide In-System Programming (ISP) capability through their Boundary ScanTest Access Ports. This capability has been implemented in a manner that ensures that the port remains compliant to the IEEE 1149.1 standard. By using IEEE 1149.1 as the communication interface through which ISP is achieved, customers get the benefit of a standard, well-defined interface.

ispMACH 4A devices can be programmed across the commercial temperature and voltage range. The PC-based ispVM™ software facilitates in-system programming of ispMACH 4A devices. ispVM takes the JEDEC file output produced by the design implementation software, along with information about the JTAG chain, and creates a set of vectors that are used to drive the JTAG chain. ispVM software can use these vectors to drive a JTAG chain via the parallel port of a PC. Alternatively, ispVM software can output files in formats understood by common automated test equipment. This equpment can then be used to program ispMACH 4A devices during the testing of a circuit board.

PCI COMPLIANT

ispMACH 4A devices in the -5/-55/-6/-65/-7/-10/-12 speed grades are compliant with the *PCI Local Bus Specification* version 2.1, published by the PCI Special Interest Group (SIG). The 5-V devices are fully PCI-compliant. The 3.3-V devices are mostly compliant but do not meet the PCI condition to clamp the inputs as they rise above V_{CC} because of their 5-V input tolerant feature.

SAFE FOR MIXED SUPPLY VOLTAGE SYSTEM DESIGNS

Both the 3.3-V and 5-V V_{CC} ispMACH 4A devices are safe for mixed supply voltage system designs. The 5-V devices will not overdrive 3.3-V devices above the output voltage of 3.3 V, while they accept inputs from other 3.3-V devices. The 3.3-V device will accept inputs up to 5.5 V. Both the 5-V and 3.3-V versions have the same high-speed performance and provide easy-to-use mixed-voltage design capability.

PULL UP OR BUS-FRIENDLY INPUTS AND I/Os

All ispMACH 4A devices have inputs and I/Os which feature the Bus-Friendly circuitry incorporating two inverters in series which loop back to the input. This double inversion weakly holds the input at its last driven logic state. While it is good design practice to tie unused pins to a known state, the Bus-Friendly input structure pulls pins away from the input threshold voltage where noise can cause high-frequency switching. At power-up, the Bus-Friendly latches are reset to a logic level “1.” For the circuit diagram, please refer to the document entitled *MACH Endurance Characteristics* on the Lattice Data Book CD-ROM or Lattice web site.

All ispMACH 4A devices have a programmable bit that configures all inputs and I/Os with either pull-up or Bus-Friendly characteristics. If the device is configured in pull-up mode, all inputs and I/O pins are

weakly pulled up. For the circuit diagram, please refer to the document entitled *MACH Endurance Characteristics* on the Lattice Data Book CD-ROM or Lattice web site.

POWER MANAGEMENT

Each individual PAL block in ispMACH 4A devices features a programmable low-power mode, which results in power savings of up to 50%. The signal speed paths in the low-power PAL block will be slower than those in the non-low-power PAL block. This feature allows speed critical paths to run at maximum frequency while the rest of the signal paths operate in the low-power mode.

PROGRAMMABLE SLEW RATE

Each ispMACH 4A device I/O has an individually programmable output slew rate control bit. Each output can be individually configured for the higher speed transition (3 V/ns) or for the lower noise transition (1 V/ns). For high-speed designs with long, unterminated traces, the slow-slew rate will introduce fewer reflections, less noise, and keep ground bounce to a minimum. For designs with short traces or well terminated lines, the fast slew rate can be used to achieve the highest speed. The slew rate is adjusted independent of power.

POWER-UP RESET/SET

All flip-flops power up to a known state for predictable system initialization. If a macrocell is configured to SET on a signal from the control generator, then that macrocell will be SET during device power-up. If a macrocell is configured to RESET on a signal from the control generator or is not configured for set/reset, then that macrocell will RESET on power-up. To guarantee initialization values, the V_{CC} rise must be monotonic, and the clock must be inactive until the reset delay time has elapsed.

SECURITY BIT

A programmable security bit is provided on the ispMACH 4A devices as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, this bit defeats readback of the programmed pattern by a device programmer, securing proprietary designs from competitors. Programming and verification are also defeated by the security bit. The bit can only be reset by erasing the entire device.

HOT SOCKETING

ispMACH 4A devices are well-suited for those applications that require hot socketing capability. Hot socketing a device requires that the device, when powered down, can tolerate active signals on the I/Os and inputs without being damaged. Additionally, it requires that the effects of the powered-down MACH devices be minimal on active signals.

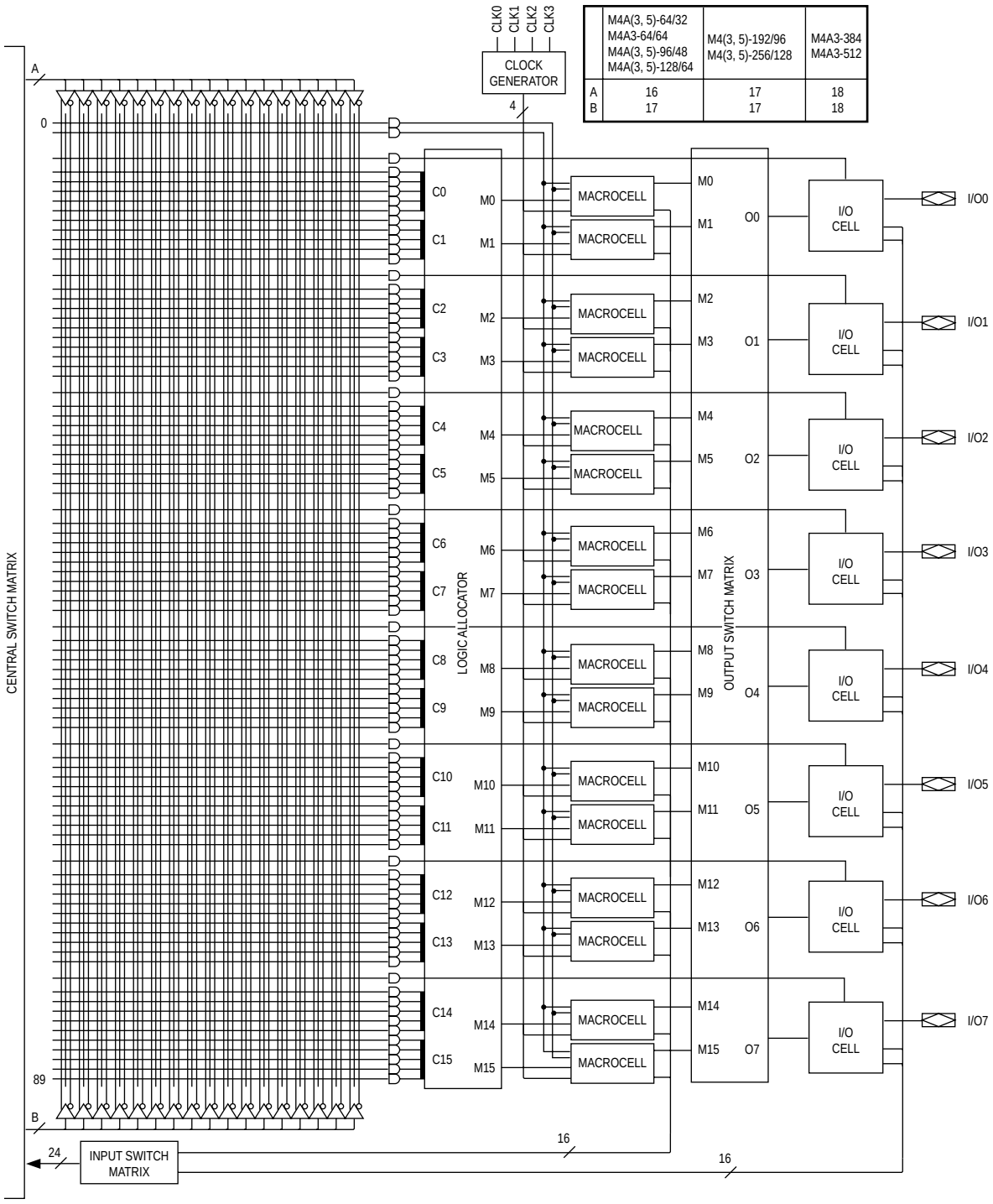
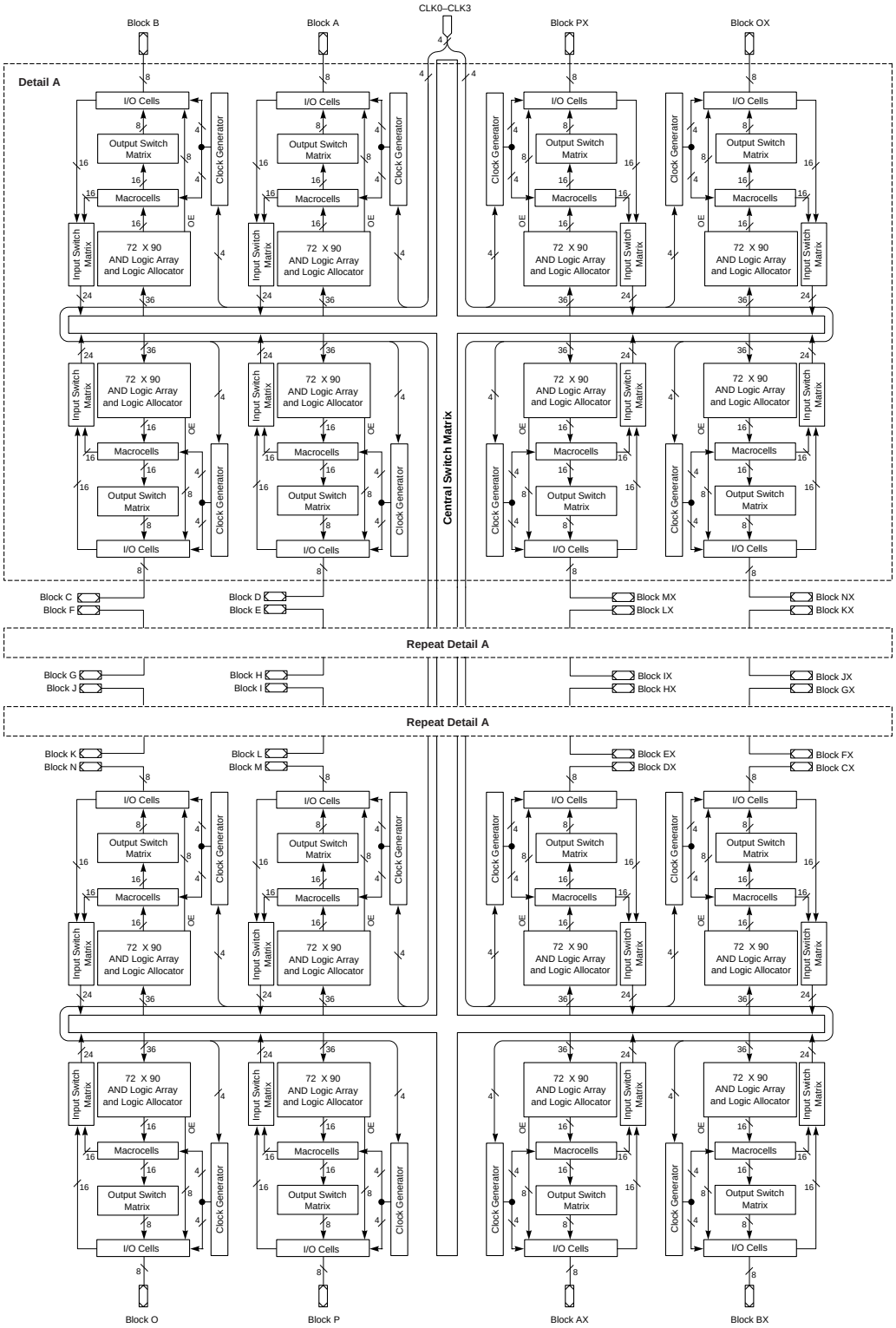


Figure 16. PAL Block for ispMACH 4A with 2:1 Macrocell - I/O Cell Ratio

BLOCK DIAGRAM - M4A3-512/160, M4A3-512/192, M4A3-512/256



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ispMACH 4A TIMING PARAMETERS OVER OPERATING RANGES[1]

		-5		-55		-6		-65		-7		-10		-12		-14		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit
Combinatorial Delay:																		
t_{PDi}	Internal combinatorial propagation delay		3.5		4.0		4.3		4.5		5.0		7.0		9.0		11.0	ns
t_{PD}	Combinatorial propagation delay		5.0		5.5		6.0		6.5		7.5		10.0		12.0		14.0	ns
Registered Delays:																		
t_{SS}	Synchronous clock setup time, D-type register	3.0		3.5		3.5		3.5		5.0		5.5		7.0		10.0		ns
t_{SST}	Synchronous clock setup time, T-type register	4.0		4.0		4.0		4.0		6.0		6.5		8.0		11.0		ns
t_{SA}	Asynchronous clock setup time, D-type register	2.5		2.5		2.5		3.0		3.5		4.0		5.0		8.0		ns
t_{SAT}	Asynchronous clock setup time, T-type register	3.0		3.0		3.0		3.5		4.5		5.0		6.0		9.0		ns
t_{HS}	Synchronous clock hold time	0.0		0.0		0.0		0.0		0.0		0.0		0.0		0.0		ns
t_{HA}	Asynchronous clock hold time	2.5		2.5		2.5		3.0		3.5		4.0		5.0		8.0		ns
t_{COSi}	Synchronous clock to internal output		2.5		2.5		2.8		3.0		3.0		3.0		3.5		3.5	ns
t_{COS}	Synchronous clock to output		4.0		4.0		4.5		5.0		5.5		6.0		6.5		6.5	ns
t_{COAi}	Asynchronous clock to internal output		5.0		5.0		5.0		5.0		6.0		8.0		10.0		12.0	ns
t_{COA}	Asynchronous clock to output		6.5		6.5		6.8		7.0		8.5		11.0		13.0		15.0	ns
Latched Delays:																		
t_{SSL}	Synchronous latch setup time	4.0		4.0		4.0		4.5		6.0		7.0		8.0		10.0		ns
t_{SAL}	Asynchronous latch setup time	3.0		3.0		3.5		3.5		4.0		4.0		5.0		8.0		ns
t_{HSL}	Synchronous latch hold time	0.0		0.0		0.0		0.0		0.0		0.0		0.0		0.0		ns
t_{HAL}	Asynchronous latch hold time	3.0		3.0		3.5		3.5		4.0		4.0		5.0		8.0		ns
t_{PDLi}	Transparent latch to internal output		5.5		5.5		5.8		6.0		7.5		9.0		11.0		12.0	ns
t_{PDL}	Propagation delay through transparent latch to output		7.0		7.0		7.5		8.0		10.0		12.0		14.0		15.0	ns
t_{GOSi}	Synchronous gate to internal output		3.0		3.0		3.0		3.0		3.5		4.5		7.0		8.0	ns
t_{GOS}	Synchronous gate to output		4.5		4.5		4.8		5.0		6.0		7.5		10.0		11.0	ns
t_{GOAi}	Asynchronous gate to internal output		6.0		6.0		6.0		6.0		8.5		10.0		13.0		15.0	ns
t_{GOA}	Asynchronous gate to output		7.5		7.5		7.8		8.0		11.0		13.0		16.0		18.0	ns
Input Register Delays:																		
t_{SIRS}	Input register setup time	1.5		1.5		2.0		2.0		2.0		2.0		2.0		2.0		ns
t_{HIRS}	Input register hold time	2.5		2.5		3.0		3.0		3.0		3.0		3.0		4.0		ns
t_{ICOSi}	Input register clock to internal feedback		3.0		3.0		3.0		3.0		3.5		4.5		6.0		6.0	ns
Input Latch Delays:																		
t_{SIL}	Input latch setup time	1.5		1.5		1.5		2.0		2.0		2.0		2.0		2.0		ns
t_{HIL}	Input latch hold time	2.5		2.5		2.5		3.0		3.0		3.0		3.0		4.0		ns
t_{IGOSi}	Input latch gate to internal feedback		3.5		3.5		3.8		4.0		4.0		4.0		4.0		5.0	ns
t_{PDILi}	Transparent input latch to internal feedback		1.5		1.5		1.5		1.5		2.0		2.0		2.0		2.0	ns

ispMACH 4A TIMING PARAMETERS OVER OPERATING RANGES[1]

		-5		-55		-6		-65		-7		-10		-12		-14		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit
Input Register Delays with ZHT Option:																		
t_{SIRZ}	Input register setup time - ZHT	6.0		6.0		6.0		6.0		6.0		6.0		6.0		6.0		ns
t_{HIRZ}	Input register hold time - ZHT	0.0		0.0		0.0		0.0		0.0		0.0		0.0		0.0		ns
Input Latch Delays with ZHT Option:																		
t_{SILZ}	Input latch setup time - ZHT	6.0		6.0		6.0		6.0		6.0		6.0		6.0		6.0		ns
t_{HILZ}	Input latch hold time - ZHT	0.0		0.0		0.0		0.0		0.0		0.0		0.0		0.0		ns
t_{PDILZi}	Transparent input latch to internal feedback - ZHT		6.0		6.0		6.0		6.0		6.0		6.0		6.0		6.0	ns
Output Delays:																		
t_{BUF}	Output buffer delay		1.5		1.5		1.8		2.0		2.5		3.0		3.0		3.0	ns
t_{SLW}	Slow slew rate delay adder		2.5		2.5		2.5		2.5		2.5		2.5		2.5		2.5	ns
t_{EA}	Output enable time		7.5		7.5		8.5		8.5		9.5		10.0		12.0		15.0	ns
t_{ER}	Output disable time		7.5		7.5		8.5		8.5		9.5		10.0		12.0		15.0	ns
Power Delay:																		
t_{PL}	Power-down mode delay adder		2.5		2.5		2.5		2.5		2.5		2.5		2.5		2.5	ns
Reset and Preset Delays:																		
t_{SRi}	Asynchronous reset or preset to internal register output		7.5		7.7		8.0		8.0		9.5		11.0		13.0		16.0	ns
t_{SR}	Asynchronous reset or preset to register output		9.0		9.2		10.0		10.0		12.0		14.0		16.0		19.0	ns
t_{SRR}	Asynchronous reset and preset register recovery time	7.0		7.0		7.5		7.5		8.0		8.0		10.0		15.0		ns
t_{SRW}	Asynchronous reset or preset width	7.0		7.0		8.0		8.0		10.0		10.0		12.0		15.0		ns
Clock/LE Width:																		
t_{WLS}	Global clock width low	2.0		2.0		2.5		2.5		3.0		4.0		5.0		6.0		ns
t_{WHS}	Global clock width high	2.0		2.0		2.5		2.5		3.0		4.0		5.0		6.0		ns
t_{WLA}	Product term clock width low	3.0		3.0		3.5		3.5		4.0		5.0		8.0		9.0		ns
t_{WHA}	Product term clock width high	3.0		3.0		3.5		3.5		4.0		5.0		8.0		9.0		ns
t_{GWS}	Global gate width low (for low transparent) or high (for high transparent)	4.0		4.0		4.5		4.5		5.0		5.0		6.0		6.0		ns
t_{GWA}	Product term gate width low (for low transparent) or high (for high transparent)	4.0		4.0		4.5		4.5		5.0		5.0		6.0		9.0		ns
t_{WIRL}	Input register clock width low	3.0		3.0		3.5		3.5		4.0		5.0		6.0		6.0		ns
t_{WIRH}	Input register clock width high	3.0		3.0		3.5		3.5		4.0		5.0		6.0		6.0		ns
t_{WIL}	Input latch gate width	4.0		4.0		4.5		4.5		5.0		5.0		6.0		6.0		ns

ispMACH 4A TIMING PARAMETERS OVER OPERATING RANGES[1]

		-5		-55		-6		-65		-7		-10		-12		-14		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Frequency:																		
f_{MAXS}	External feedback, D-type, Min of $1/(t_{WLS} + t_{WHS})$ or $1/(t_{SS} + t_{COS})$	143		133		125		118		95.2		87.0		74.1		60.6		MHz
	External feedback, T-type, Min of $1/(t_{WLS} + t_{WHS})$ or $1/(t_{SST} + t_{COS})$	125		125		118		111		87.0		80.0		69.0		57.1		MHz
	Internal feedback (f_{CNT}), D-type, Min of $1/(t_{WLS} + t_{WHS})$ or $1/(t_{SS} + t_{COSi})$	182		167		160		154		125		118		95.0		74.1		MHz
	Internal feedback (f_{CNT}), T-type, Min of $1/(t_{WLS} + t_{WHS})$ or $1/(t_{SST} + t_{COSi})$	154		154		148		143		111		105		87.0		69.0		MHz
	No feedback[2], Min of $1/(t_{WLS} + t_{WHS})$, $1/(t_{SS} + t_{HS})$ or $1/(t_{SST} + t_{HS})$	250		250		200		200		154		125		100		83.3		MHz
f_{MAXA}	External feedback, D-type, Min of $1/(t_{WLA} + t_{WHA})$ or $1/(t_{SA} + t_{COA})$	111		111		108		100		83.3		66.7		55.6		43.5		MHz
	External feedback, T-type, Min of $1/(t_{WLA} + t_{WHA})$ or $1/(t_{SAT} + t_{COA})$	105		105		102		95.2		76.9		62.5		52.6		41.7		MHz
	Internal feedback (f_{CNTA}), D-type, Min of $1/(t_{WLA} + t_{WHA})$ or $1/(t_{SA} + t_{COAi})$	133		133		125		125		105		83.3		66.7		50.0		MHz
	Internal feedback (f_{CNTA}), T-type, Min of $1/(t_{WLA} + t_{WHA})$ or $1/(t_{SAT} + t_{COAi})$	125		125		125		118		95.2		76.9		62.5		47.6		MHz
	No feedback[2], Min of $1/(t_{WLA} + t_{WHA})$, $1/(t_{SA} + t_{HA})$ or $1/(t_{SAT} + t_{HA})$	167		167		143		143		125		100		62.5		55.6		MHz
f_{MAXI}	Maximum input register frequency, Min of $1/(t_{WIRH} + t_{WIRL})$ or $1/(t_{SIRS} + t_{HIRS})$	167		167		143		143		125		100		83.3		83.3		MHz

Notes:

1. *See "Switching Test Circuit" document on the Literature Download page of the Lattice web site.*
2. *This parameter does not apply to flip-flops in the emulated mode since the feedback path is required for emulation.*

CAPACITANCE [1]

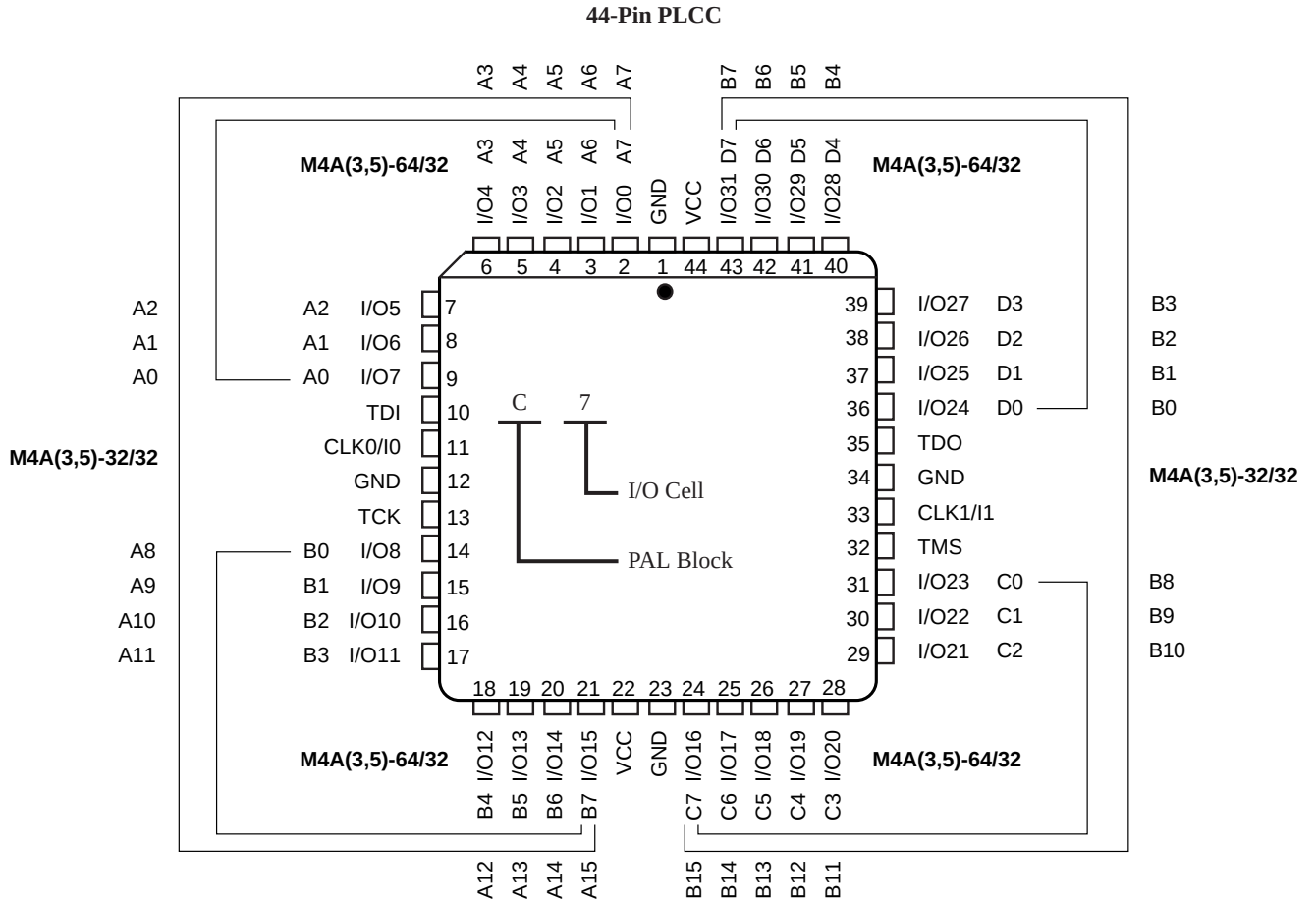
Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input capacitance	V_{IN}=2.0 V	3.3 V or 5 V, 25°C, 1 MHz	6	pF
$C_{I/O}$	Output capacitance	V_{OUT}=2.0V	3.3 V or 5 V, 25°C, 1 MHz	8	pF

Note:

1. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where this parameter may be affected.*

44-PIN PLCC CONNECTION DIAGRAM (M4A(3,5)-32/32 AND M4A(3,5)-64/32)

Top View



17466G-026

PIN DESIGNATIONS

CLK/I = Clock or Input

GND = Ground

I/O = Input/Output

V_{CC} = Supply Voltage

TDI = Test Data In

TCK = Test Clock

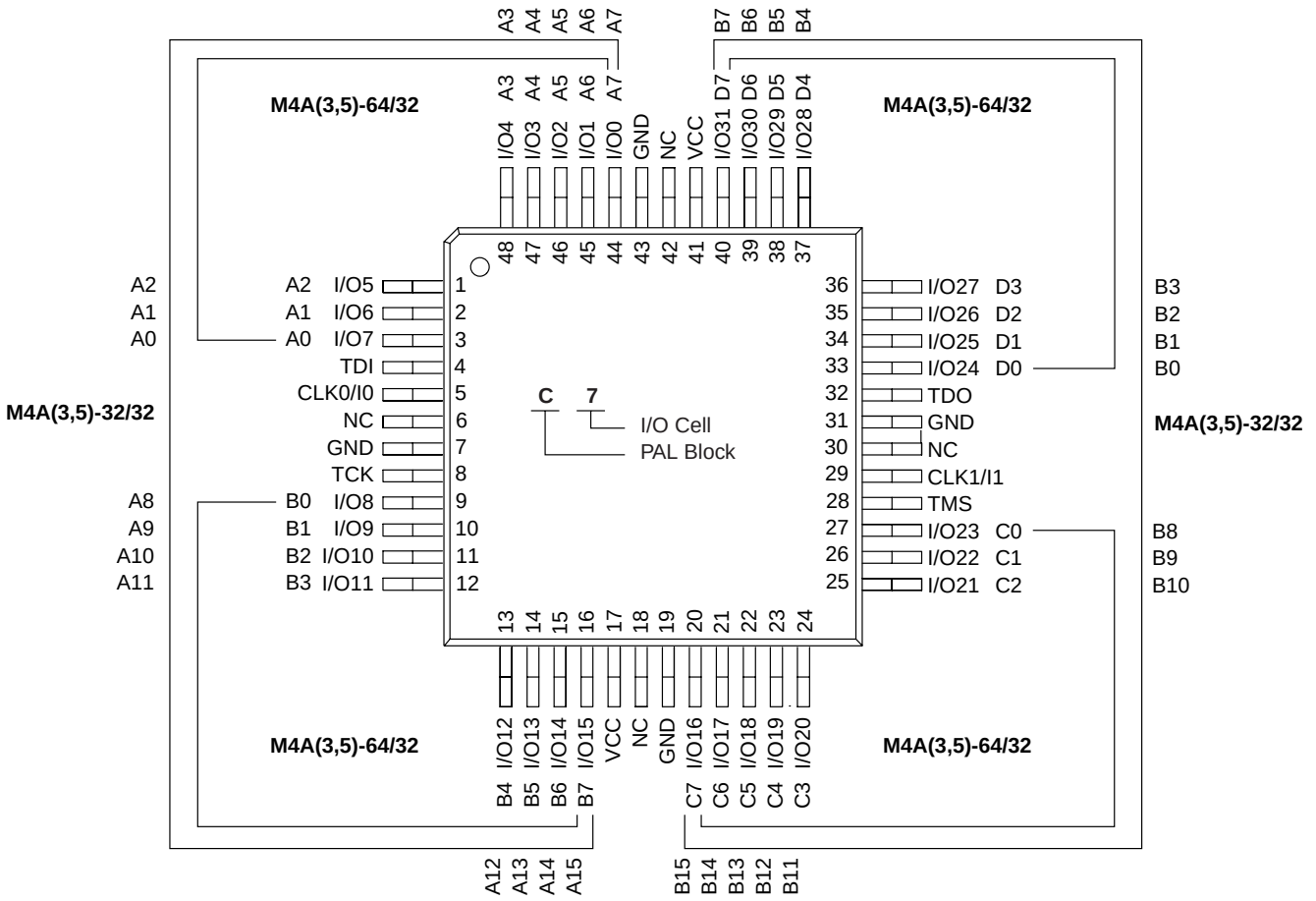
TMS = Test Mode Select

TDO = Test Data Out

48-PIN TQFP CONNECTION DIAGRAM (M4A(3,5)-32/32 AND M4A(3,5)-64/32)

Top View

48-Pin TQFP (1.4mm Thickness)



17466G-028

PIN DESIGNATIONS

CLK/I = Clock or Input

GND = Ground

I/O = Input/Output

V_{CC} = Supply Voltage

NC = No Connect

TDI = Test Data In

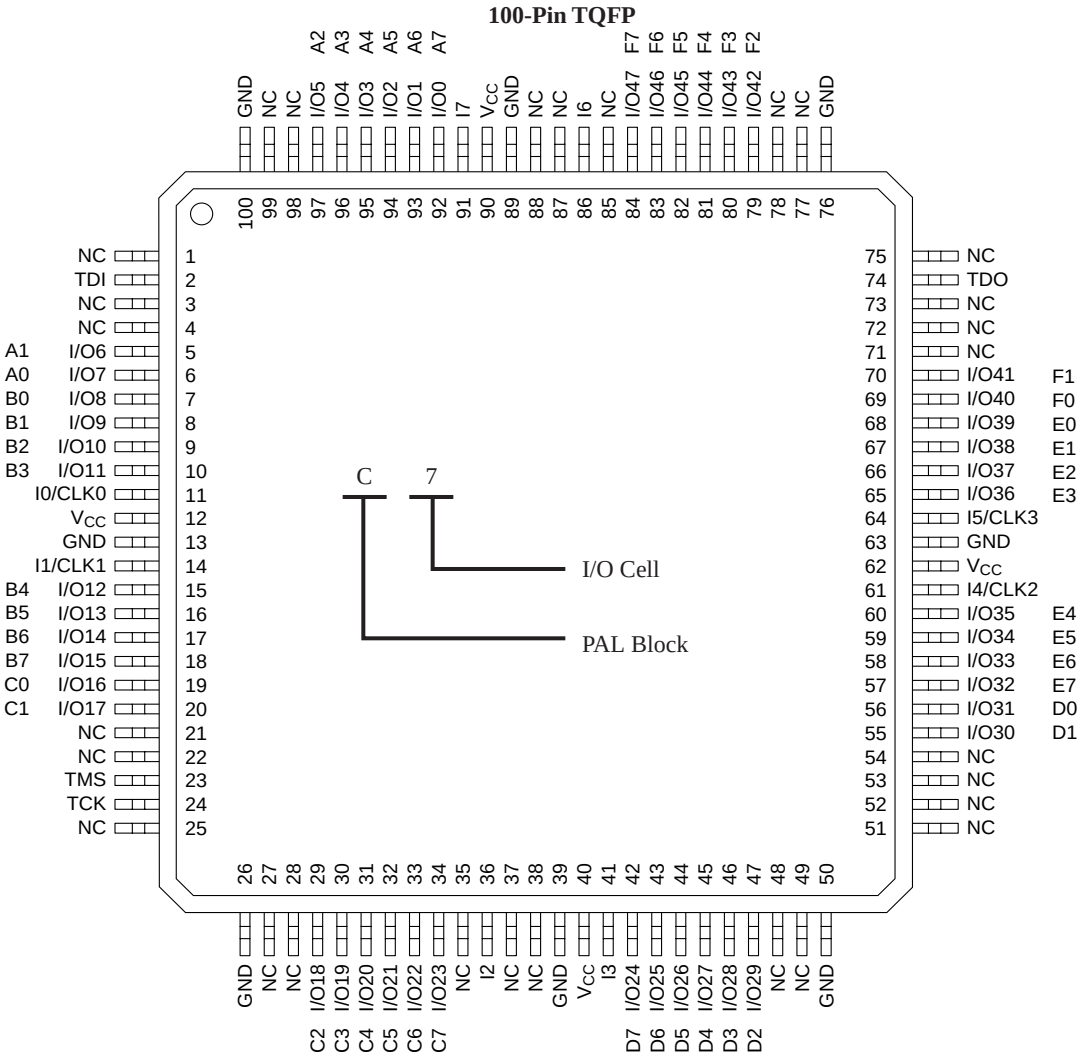
TCK = Test Clock

TMS = Test Mode Select

TDO = Test Data Out

100-PIN TQFP CONNECTION DIAGRAM (M4A(3,5)-96/48)

Top View



17466G-029

PIN DESIGNATIONS

CLK/I = Clock or Input

GND = Ground

I = Input

I/O = Input/Output

V_{CC} = Supply Voltage

NC = No Connect

TDI = Test Data In

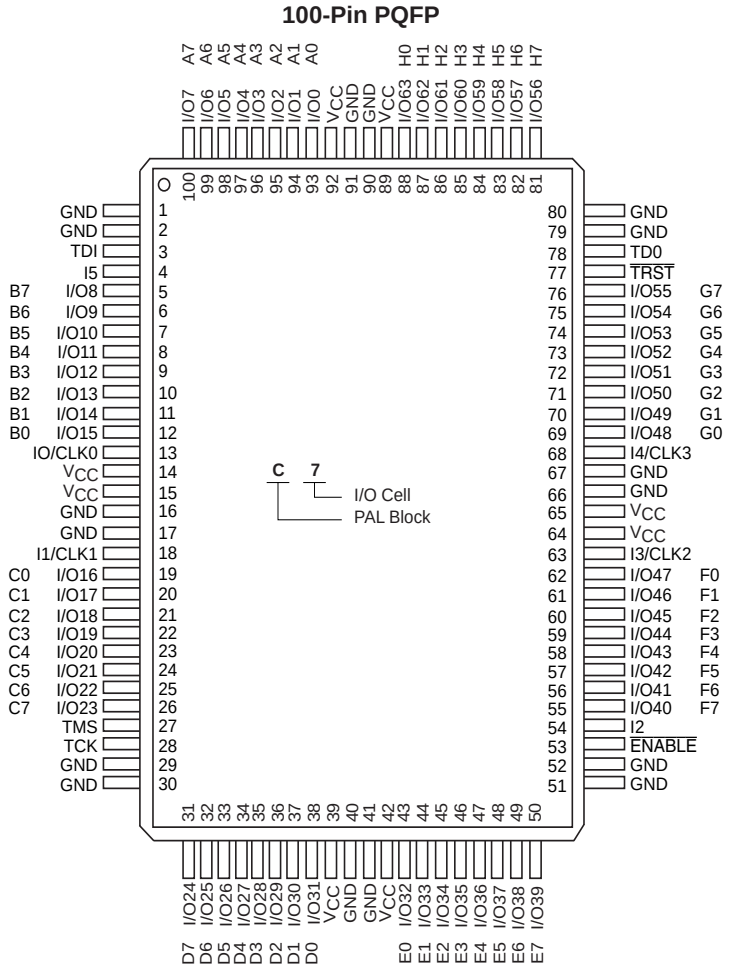
TCK = Test Clock

TMS = Test Mode Select

TDO = Test Data Out

100-PIN PQFP CONNECTION DIAGRAM (M4A(3,5)-128/64)

Top View



PIN DESIGNATIONS

I/CLK = Input or Clock

GND = Ground

I = Input

I/O = Input/Output

V_{CC} = Supply Voltage

TDI = Test Data In

TCK = Test Clock

TMS = Test Mode Select

TDO = Test Data Out

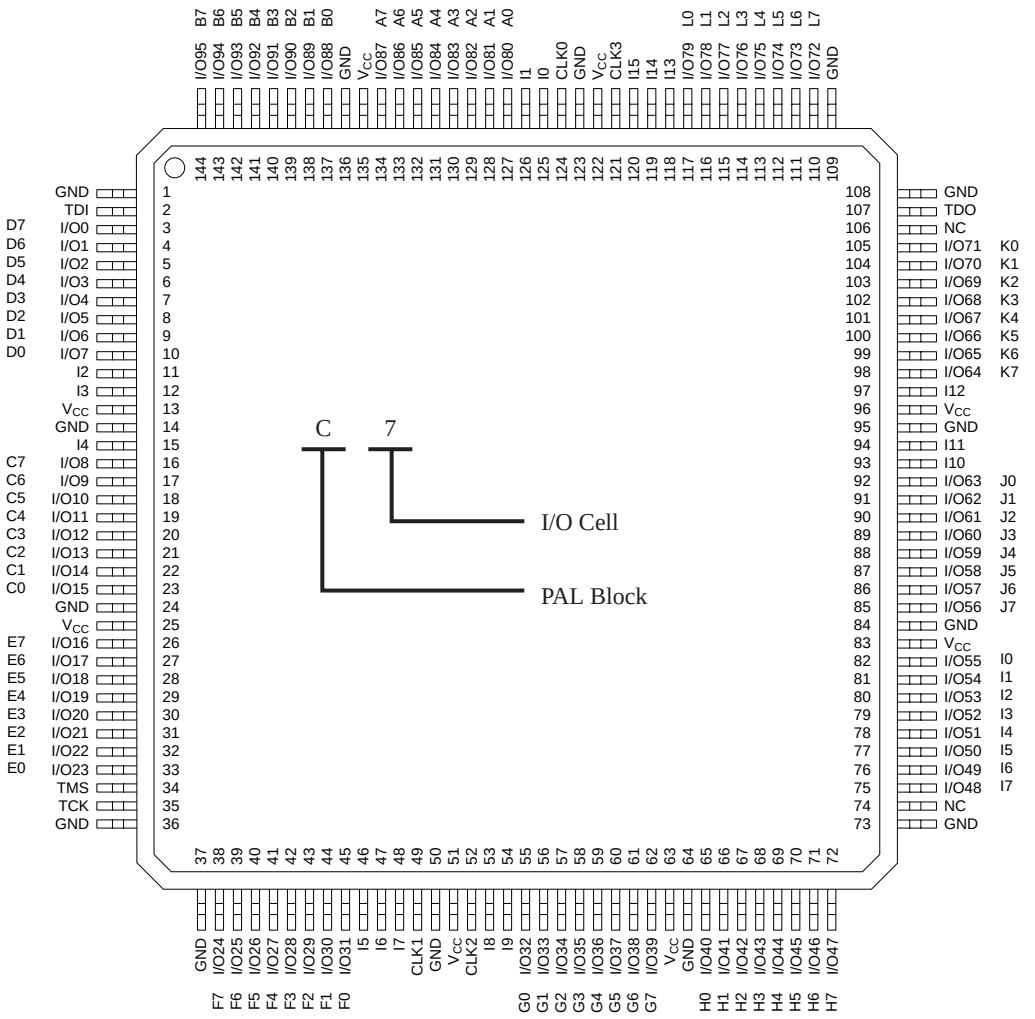
$\overline{TRST}$ = Test Reset

$\overline{ENABLE}$ = Program

144-PIN TQFP CONNECTION DIAGRAM (M4A(3,5)-192/96)

Top View

144-Pin TQFP



17466G-033

PIN DESIGNATIONS

CLK = Clock

GND = Ground

I = Input

I/O = Input/Output

V_{CC} = Supply Voltage

TDI = Test Data In

TCK = Test Clock

TMS = Test Mode Select

TDO = Test Data Out

144-BALL FPBGA CONNECTION DIAGRAM (M4A3-192/96)

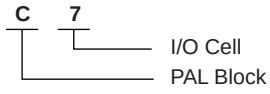
Bottom View

144-Ball fpBGA

	12	11	10	9	8	7	6	5	4	3	2	1	
A	GND	I/O72 L7	I/O76 L3	I13	GBCLK3	I0	I/O82 A2	I/O86 A6	I/O88 B0	I/O93 B5	I/O95 B7	GND	**A**
B	GND	I/O73 L6	I/O77 L2	I/O79 L0	VCC	I1	I/O83 A3	I/O87 A7	I/O90 B2	I/O94 B6	I/O0 D7	TDI	**B**
C	GND	TDO	I/O74 L5	I14	GND	I/O80 A0	I/O84 A4	GND	I/O92 B4	I/O1 D6	I/O4 D3	I/O3 D4	**C**
D	I/O67 K4	I/O69 K2	I/O71 K0	I/O75 L4	GBCLK0	I/O81 A1	VCC	I/O91 B3	I/O2 D5	I2	I/O6 D1	I/O7 D0	**D**
E	I12	I/O64 K7	I/O66 K5	I/O70 K1	I/O78 L1	I/O85 A5	I/O89 B1	I/O5 D2	I/O8 C7	I4	GND	VCC	**E**
F	I10	I11	GND	I/065 K6	I/O68 K3	I15	I3	GND	I/O12 C3	I/O11 C4	I/O10 C5	I/O9 C6	**F**
G	I/O60 J3	I/O61 J2	I/O62 J1	I/O63 J0	VCC	GND	I7	I/O20 E3	I/O17 E6	I/O15 C0	I/O14 C1	I/O13 C2	**G**
H	I/O56 J7	I/O57 J6	I/O58 J5	I/O59 J4	I/O53 I2	I/O41 H1	I/O37 G5	I/O30 F1	I/O22 E1	I/O18 E5	I/O16 E7	VCC	**H**
J	I/O55 I0	I/O54 I1	VCC	I/O50 I5	I/O43 H3	VCC	I/O33 G1	GBCLK2	I/O27 F4	I/O23 E0	I/O21 E2	I/O19 E4	**J**
K	I/O51 I4	I/O52 I3	I/O49 I6	I/O44 H4	GND	I/O36 G4	I/O32 G0	VCC	I6	I/O26 F5	TCK	TMS	**K**
L	GND	I/O48 I7	I/O46 H6	I/O42 H2	I/O39 G7	I/O35 G3	I9	GND	I/O31 F0	I/O29 F2	I/O25 F6	GND	**L**
M	GND	I/O47 H7	I/O45 H5	I/O40 H0	I/O38 G6	I/O34 G2	I8	GBCLK1	I5	I/O28 F3	I/O24 F7	GND	**M**
	12	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	

PIN DESIGNATIONS

CLK = Clock
GND = Ground
I = Input
I/O = Input/Output
N/C = No Connect
VCC = Supply Voltage
TDI = Test Data In
TCK = Test Clock
TMS = Test Mode Select
TDO = Test Data Out

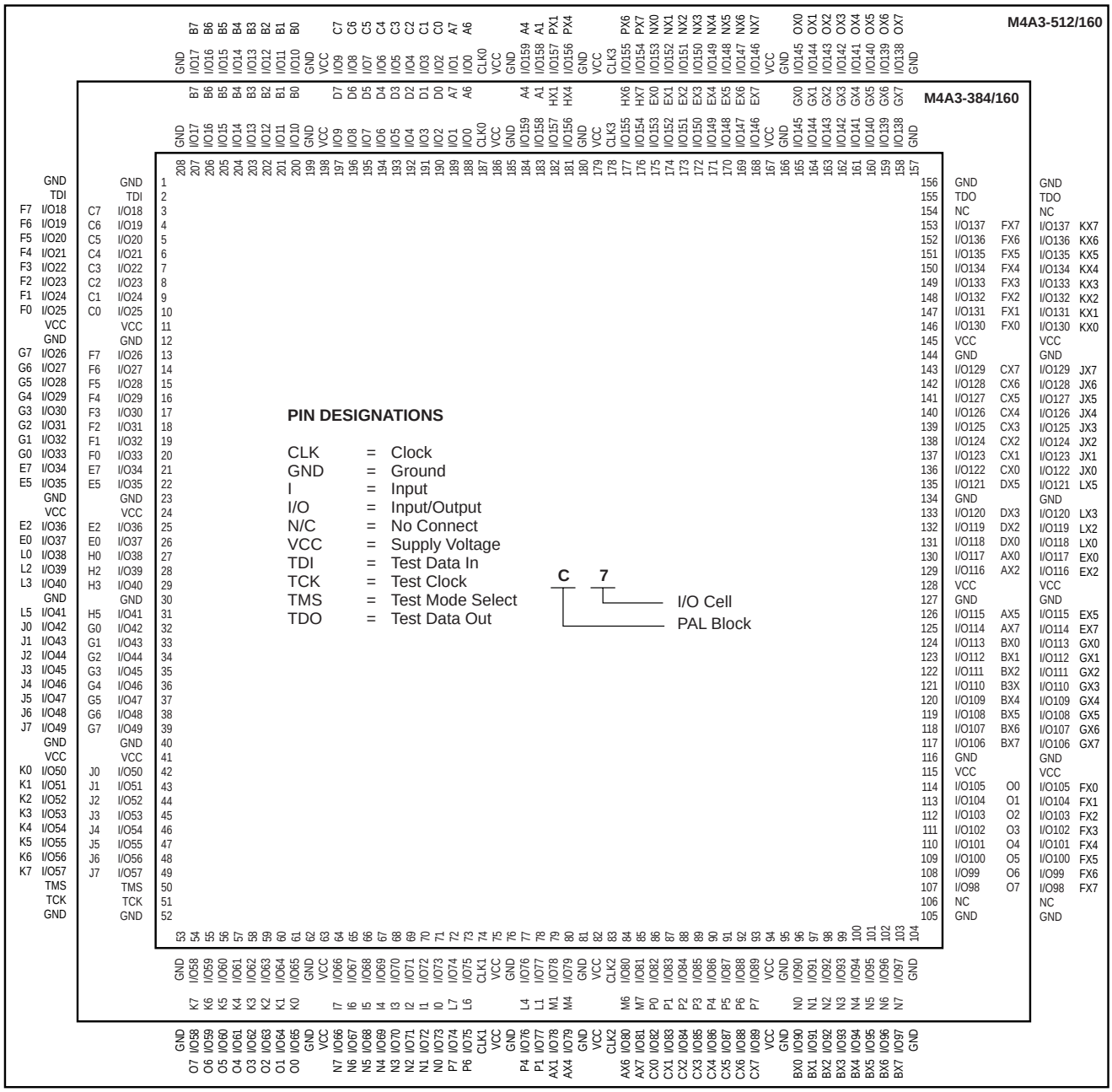


m4a3.192.96_144bga

208-PIN PQFP CONNECTION DIAGRAM (M4A3-384/160 AND M4A3-512/160)

Top View

208-Pin PQFP



17466Ga-044

256-BALL BGA CONNECTION DIAGRAM - (M4A3-384/192)

Bottom View

256-Ball BGA

	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	GND	I/O11 FX7	GND	I/O44 FX6	I/O58 CX6	GND	I/O70 CX2	I/O76 DX6	GND	GND	GND	GND	I/O108 AX5	I/O116 BX0	GND	I/O128 BX7	I/O134 O3	GND	GND	GND	A
B	GND	I/O12 GX7	I/O28 FX5	I/O45 FX3	I/O59 CX7	I/O64 CX5	I/O71 CX3	I/O77 DX7	I/O84 DX5	I/O90 DX2	I/O96 AX0	I/O102 AX3	I/O109 AX6	I/O117 BX1	I/O122 BX4	I/O129 BX6	I/O135 O4	I/O148 O6	I/O164 O7	GND	B
C	I/O0 GX6	I/O13 GX5	VCC	I/O46 FX4	I/O60 FX2	I/O65 FX1	I/O72 CX4	I/O78 CX0	I/O85 DX4	I/O91 DX1	I/O97 AX1	I/O103 AX4	I/O110 BX2	I/O118 BX5	I/O123 O0	I/O130 O1	I/O136 O5	VCC	I/O165 N7	I/O181 N6	C
D	I/O1 EX7	I/O14 GX3	I/O29 GX4	VCC	VCC	I/O66 FX0	VCC	I/O79 CX1	I/O86 DX3	I/O92 DX0	I/O98 AX2	I/O104 AX7	I/O111 B3X	VCC	I/O124 O2	VCC	VCC	I/O149 N4	I/O166 N5	I/O182 P7	D
E	I/O2 EX0	I/O15 GX0	I/O30 GX1	TDI													TDO	I/O150 N2	I/O167 N3	I/O183 P6	E
F	GND	I/O16 EX1	I/O31 EX6	I/O47 GX2													I/O137 N1	I/O151 N0	I/O168 P5	GND	F
G	I/O3 HX6	I/O17 EX4	I/O32 EX5	VCC													VCC	I/O152 P4	I/O169 P3	I/O184 M7	G
H	GND	I/O18 HX5	I/O33 EX2	I/O48 EX3													I/O138 P2	I/O153 P1	I/O170 P0	GND	H
J	I/O4 HX0	I/O19 HX1	I/O34 HX4	I/O49 HX7													I/O139 M6	I/O154 M5	I/O171 M4	I/O185 M3	J
K	GND	CLK3	I/O35 HX2	I/O50 HX3													I/O140 M0	I/O155 M1	CLK2	I/O186 M2	K
L	I/O5 A2	CLK0	I/O36 A0	I/O51 A1													I/O141 L3	I/O156 L4	CLK1	GND	L
M	I/O6 A4	I/O20 A3	I/O37 A5	I/O52 A6													I/O142 L6	I/O157 L5	I/O172 L0	I/O187 L1	M
N	GND	I/O21 A7	I/O38 D0	I/O53 D1													I/O143 I5	I/O158 I0	I/O173 L7	GND	N
P	I/O7 D2	I/O22 D3	I/O39 D4	VCC													VCC	I/O159 I4	I/O174 I1	I/O188 L2	P
R	GND	I/O23 D5	I/O40 D6	I/O54 D7													I/O144 K5	I/O160 K0	I/O175 I3	GND	R
T	I/O8 B3	I/O24 B0	I/O41 B7	TCK													TMS	I/O161 K4	I/O176 K1	I/O189 I2	T
U	I/O9 B4	I/O25 B1	I/O42 B6	VCC	VCC	I/O67 C0	VCC	I/O80 F0	I/O87 E5	I/O93 E2	I/O99 H2	I/O105 H5	I/O112 G0	VCC	I/O125 J1	VCC	VCC	I/O162 K7	I/O177 K2	I/O190 I6	U
V	I/O10 B5	I/O26 B2	VCC	I/O55 C5	I/O61 C2	I/O68 C1	I/O73 F4	I/O81 F1	I/O88 E4	I/O94 E1	I/O100 H1	I/O106 H4	I/O113 G1	I/O119 G4	I/O126 J0	I/O131 J2	I/O145 J5	VCC	I/O178 K3	I/O191 I7	V
W	GND	I/O27 C7	I/O43 C6	I/O56 C3	I/O62 F7	I/O69 F5	I/O74 F3	I/O82 E7	I/O89 E3	I/O95 E0	I/O101 H0	I/O107 H3	I/O114 H7	I/O120 G3	I/O127 G5	I/O132 G7	I/O146 J4	I/O163 J6	I/O179 J7	GND	W
Y	GND	GND	GND	I/O57 C4	I/O63 F6	GND	I/O75 F2	I/O83 E6	GND	GND	GND	GND	I/O115 H6	I/O121 G2	GND	I/O133 G6	I/O147 J3	GND	I/O180 K6	GND	Y
	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

PIN DESIGNATIONS

CLK	=	Clock
GND	=	Ground
I	=	Input
I/O	=	Input/Output
N/C	=	No Connect
VCC	=	Supply Voltage
TDI	=	Test Data In
TCK	=	Test Clock
TMS	=	Test Mode Select
TDO	=	Test Data Out

C 7
I/O Cell
PAL Block

17466G-046

256-BALL fpBGA CONNECTION DIAGRAM (M4A3-512/192)

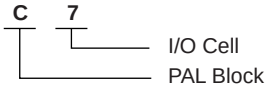
Bottom View

256-Ball fpBGA

	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	I/O159 KX7	I/O181 OX5	I/O180 OX4	I/O177 OX1	I/O174 NX6	I/O172 NX4	I/O191 PX7	I/O186 PX2	I/O1 A1	I/O3 A3	CLK0	I/O17 C1	I/O21 C5	I/O23 C7	I/O10 B2	I/O12 B4	**A**
B	I/O157 KX5	I/O158 KX6	I/O182 OX6	I/O179 OX3	I/O175 NX7	I/O173 NX5	I/O168 NX0	I/O187 PX3	I/O0 A0	I/O5 A5	I/O7 A7	I/O18 C2	I/O8 B0	I/O11 B3	I/O13 B5	N/C	**B**
C	I/O155 KX3	I/O156 KX4	N/C	I/O183 OX7	I/O178 OX2	I/O170 NX2	I/O171 NX3	I/O189 PX5	I/O184 PX0	I/O6 A6	I/O20 C4	I/O22 C6	I/O15 B7	I/O14 B6	TDI	I/O39 F7	**C**
D	I/O150 JX6	I/O151 JX7	TDO	GND	GND	VCC	GND	VCC	GND	GND	VCC	GND	VCC	I/O9 B1	I/O38 F6	I/O37 F5	**D**
E	I/O148 JX4	N/C	I/O154 KX2	VCC	I/O152 KX0	I/O153 KX1	I/O190 PX6	CLK3	I/O188 PX4	I/O2 A2	I/O16 C0	N/C	GND	I/O36 F4	I/O35 F3	I/O47 G7	**E**
F	I/O144 JX0	I/O149 JX5	I/O147 JX3	GND	I/O146 JX2	I/O145 JX1	I/O176 OX0	I/O169 NX1	I/O185 PX1	I/O4 A4	I/O19 C3	I/O34 F2	VCC	I/O32 F0	I/O46 G6	I/O45 G5	**F**
G	I/O163 LX3	I/O166 LX6	I/O165 LX5	VCC	I/O164 LX4	I/O167 LX7	VCC	GND	GND	VCC	I/O33 F1	I/O44 G4	GND	I/O42 G2	I/O41 G1	I/O31 E7	**G**
H	I/O160 LX0	I/O162 LX2	I/O161 LX1	GND	I/O120 EX0	I/O121 EX1	GND	VCC	VCC	GND	I/O43 G3	I/O40 G0	VCC	I/O28 E4	I/O27 E3	I/O26 E2	**H**
J	I/O122 EX2	I/O123 EX3	I/O124 EX4	GND	I/O126 EX6	I/O125 EX5	GND	VCC	VCC	GND	I/O30 E6	I/O29 E5	GND	I/O65 L1	I/O64 L0	I/O66 L2	**J**
K	I/O127 EX7	I/O136 GX0	I/O137 GX1	VCC	I/O139 GX3	I/O138 GX2	VCC	GND	GND	VCC	I/O25 E1	I/O24 E0	VCC	I/O71 L7	I/O70 L6	I/O48 J0	**K**
L	I/O140 GX4	I/O141 GX5	I/O143 GX7	GND	I/O130 FX2	I/O142 GX6	I/O98 AX2	I/O91 P3	I/O75 N3	I/O77 N5	I/O68 L4	I/O67 L3	GND	I/O51 J3	I/O52 J4	I/O49 J1	**L**
M	I/O128 FX0	I/O129 FX1	I/O131 FX3	GND	I/O115 CX3	I/O113 CX1	I/O100 AX4	I/O90 P2	I/O74 N2	I/O80 O0	I/O83 O3	I/O69 L5	VCC	I/O60 K4	I/O55 J7	I/O50 J2	**M**
N	I/O132 FX4	I/O133 FX5	I/O135 FX7	VCC	GND	VCC	GND	VCC	GND	GND	VCC	GND	GND	TCK	I/O56 K0	I/O53 J5	**N**
P	I/O134 FX6	I/O109 BX5	I/O110 BX6	I/O111 BX7	I/O116 CX4	I/O114 CX2	I/O101 AX5	I/O89 P1	I/O93 P5	I/O94 P6	I/O79 N7	I/O84 O4	I/O87 O7	TMS	I/O57 K1	I/O54 J6	**P**
R	I/O108 BX4	I/O107 BX3	I/O104 BX0	I/O119 CX7	I/O112 CX0	I/O102 AX6	I/O99 AX3	I/O96 AX0	I/O92 P4	I/O72 N0	I/O76 N4	I/O81 O1	I/O85 O5	I/O63 K7	I/O59 K3	I/O58 K2	**R**
T	I/O106 BX2	I/O105 BX1	I/O118 CX6	I/O117 CX5	I/O103 AX7	CLK2	I/O97 AX1	I/O88 P0	CLK1	I/O95 P7	I/O73 N1	I/O78 N6	I/O82 O2	I/O86 O6	I/O62 K6	I/O61 K5	**T**
	16	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	

PIN DESIGNATIONS

CLK = Clock
GND = Ground
I = Input
I/O = Input/Output
N/C = No Connect
VCC = Supply Voltage
TDI = Test Data In
TCK = Test Clock
TMS = Test Mode Select
TDO = Test Data Out



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