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## Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

## Applications of Embedded - CPLDs

### Details

Product Status	Not For New Designs
Programmable Type	In System Programmable
Delay Time tpd(1) Max	5.5 ns
Voltage Supply - Internal	3V ~ 3.6V
Number of Logic Elements/Blocks	-
Number of Macrocells	64
Number of Gates	-
Number of I/O	32
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/lattice-semiconductor/m4a3-64-32-55vnc">https://www.e-xfl.com/product-detail/lattice-semiconductor/m4a3-64-32-55vnc</a>

## GENERAL DESCRIPTION

The ispMACH™ 4A family from Lattice offers an exceptionally flexible architecture and delivers a superior Complex Programmable Logic Device (CPLD) solution of easy-to-use silicon products and software tools. The overall benefits for users are a guaranteed and predictable CPLD solution, faster time-to-market, greater flexibility and lower cost. The ispMACH 4A devices offer densities ranging from 32 to 512 macrocells with 100% utilization and 100% pin-out retention. The ispMACH 4A families offer 5-V (M4A5-xxx) and 3.3-V (M4A3-xxx) operation.

ispMACH 4A products are 5-V or 3.3-V in-system programmable through the JTAG (IEEE Std. 1149.1) interface. JTAG boundary scan testing also allows product testability on automated test equipment for device connectivity.

All ispMACH 4A family members deliver First-Time-Fit and easy system integration with pin-out retention after any design change and refit. For both 3.3-V and 5-V operation, ispMACH 4A products can deliver guaranteed fixed timing as fast as 5.0 ns  $t_{PD}$  and 182 MHz  $f_{CNT}$  through the SpeedLocking feature when using up to 20 product terms per output (Table 2).

**Table 2. ispMACH 4A Speed Grades**

Device	Speed Grade							
	-5	-55	-6	-65	-7	-10	-12	-14
M4A3-32 M4A5-32	C				C, I	C, I	I	
M4A3-64/32 M4A5-64/32		C			C, I	C, I	I	
M4A3-64/64		C			C, I	C, I	I	
M4A3-96 M4A5-96		C			C, I	C, I	I	
M4A3-128 M4A5-128		C			C, I	C, I	I	
M4A3-192 M4A5-192			C		C, I	C, I	I	
M4A3-256/128 M4A5-256/128		C		C	C, I	C, I	I	
M4A3-256/192 M4A3-256/160					C	C, I	I	
M4A3-384				C		C, I	C, I	I
M4A3-512					C	C, I	C, I	I

**Note:**

1. C = Commercial, I = Industrial

**Table 8. Register/Latch Operation**

Configuration	Input(s)	CLK/LE <sup>1</sup>	Q+
D-type Register	D=X	0, 1, ↓ (↑)	Q
	D=0	↑ (↓)	0
	D=1	↑ (↓)	1
T-type Register	T=X	0, 1, ↓ (↑)	Q
	T=0	↑ (↓)	Q
	T=1	↑ (↓)	$\bar{Q}$
D-type Latch	D=X	1 (0)	Q
	D=0	0 (1)	0
	D=1	0 (1)	1

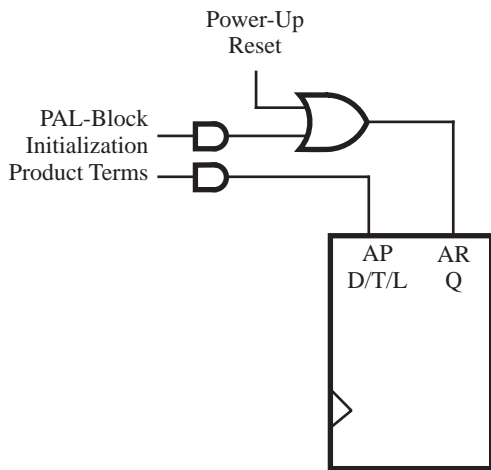
**Note:**

1. Polarity of CLK/LE can be programmed

Although the macrocell shows only one input to the register, the XOR gate in the logic allocator allows the D-, T-type register to emulate J-K, and S-R behavior. In this case, the available product terms are divided between J and K (or S and R). When configured as J-K, S-R, or T-type, the extra product term must be used on the XOR gate input for flip-flop emulation. In any register type, the polarity of the inputs can be programmed.

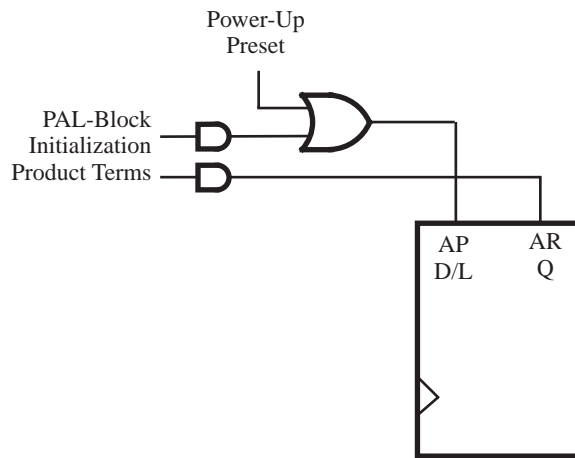
The clock input to the flip-flop can select any of the four PAL block clocks in synchronous mode, with the additional choice of either polarity of an individual product term clock in the asynchronous mode.

The initialization circuit depends on the mode. In synchronous mode (Figure 7), asynchronous reset and preset are provided, each driven by a product term common to the entire PAL block.



a. Power-up reset

17466G-012



b. Power-up preset

17466G-013

**Figure 7. Synchronous Mode Initialization Configurations**

**Table 10. Output Switch Matrix Combinations for ispMACH 4A Devices with 2:1 Macrocell-I/O Cell Ratio**

Macrocell	Routable to I/O Cells
M12, M13	I/03, I/04, I/05, I/06
M14, M15	I/04, I/05, I/06, I/07

I/O Cell	Available Macrocells
I/00	M0, M1, M2, M3, M4, M5, M6, M7
I/01	M2, M3, M4, M5, M6, M7, M8, M9
I/02	M4, M5, M6, M7, M8, M9, M10, M11
I/03	M6, M7, M8, M9, M10, M11, M12, M13
I/04	M8, M9, M10, M11, M12, M13, M14, M15
I/05	M0, M1, M10, M11, M12, M13, M14, M15
I/06	M0, M1, M2, M3, M12, M13, M14, M15
I/07	M0, M1, M2, M3, M4, M5, M14, M15

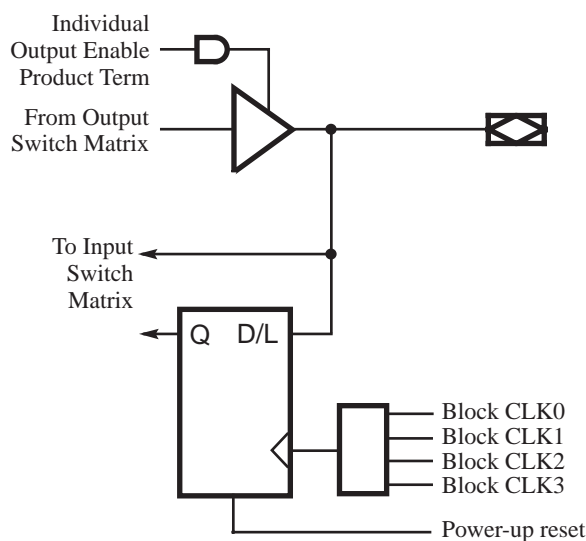
**Table 11. Output Switch Matrix Combinations for M4A3-256/160 and M4A3-256/192**

Macrocell	Routable to I/O Cells							
M0	I/00	I/01	I/02	I/03	I/04	I/05	I/06	I/07
M1	I/00	I/01	I/02	I/03	I/04	I/05	I/06	I/07
M2	I/00	I/01	I/02	I/03	I/04	I/05	I/06	I/07
M3	I/00	I/01	I/02	I/03	I/04	I/05	I/06	I/07
M4	I/00	I/01	I/02	I/03	I/04	I/05	I/06	I/07
M5	I/00	I/01	I/02	I/03	I/04	I/05	I/06	I/07
M6	I/00	I/01	I/02	I/03	I/04	I/05	I/06	I/07
M7	I/00	I/01	I/02	I/03	I/04	I/05	I/06	I/07
M8	I/08	I/09	I/010	I/011	I/012	I/013	I/014	I/015
M9	I/08	I/09	I/010	I/011	I/012	I/013	I/014	I/015
M10	I/08	I/09	I/010	I/011	I/012	I/013	I/014	I/015
M11	I/08	I/09	I/010	I/011	I/012	I/013	I/014	I/015
M12	I/08	I/09	I/010	I/011	I/012	I/013	I/014	I/015
M13	I/08	I/09	I/010	I/011	I/012	I/013	I/014	I/015
M14	I/08	I/09	I/010	I/011	I/012	I/013	I/014	I/015
M15	I/08	I/09	I/010	I/011	I/012	I/013	I/014	I/015

I/O Cell	Available Macrocells							
I/00	M0	M1	M2	M3	M4	M5	M6	M7
I/01	M0	M1	M2	M3	M4	M5	M6	M7
I/02	M0	M1	M2	M3	M4	M5	M6	M7
I/03	M0	M1	M2	M3	M4	M5	M6	M7
I/04	M0	M1	M2	M3	M4	M5	M6	M7
I/05	M0	M1	M2	M3	M4	M5	M6	M7
I/06	M0	M1	M2	M3	M4	M5	M6	M7
I/07	M0	M1	M2	M3	M4	M5	M6	M7

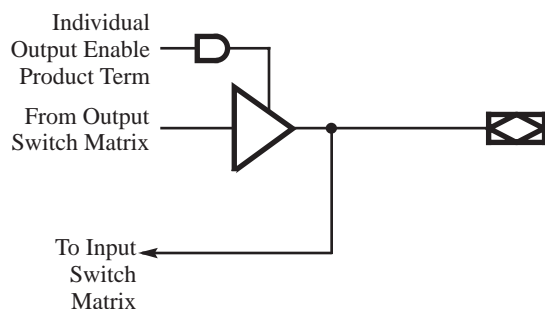
## I/O Cell

The I/O cell (Figures 10 and 11) simply consists of a programmable output enable, a feedback path, and flip-flop (except ispMACH 4A devices with 1:1 macrocell-I/O cell ratio). An individual output enable product term is provided for each I/O cell. The feedback signal drives the input switch matrix.



17466G-017

**Figure 10. I/O Cell for ispMACH 4A Devices with 2:1 Macrocell-I/O Cell Ratio**



17466G-018

**Figure 11. I/O Cell for ispMACH 4A Devices with 1:1 Macrocell-I/O Cell Ratio**

The I/O cell (Figure 10) contains a flip-flop, which provides the capability for storing the input in a D-type register or latch. The clock can be any of the PAL block clocks. Both the direct and registered versions of the input are sent to the input switch matrix. This allows for such functions as “time-domain-multiplexed” data comparison, where the first data value is stored, and then the second data value is put on the I/O pin and compared with the previous stored value.

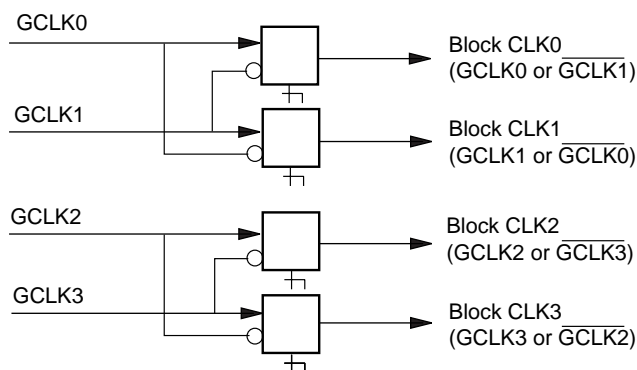
Note that the flip-flop used in the ispMACH 4A I/O cell is independent of the flip-flops in the macrocells. It powers up to a logic low.

### **Zero-Hold-Time Input Register**

The ispMACH 4A devices have a zero-hold-time (ZHT) fuse which controls the time delay associated with loading data into all I/O cell registers and latches. When programmed, the ZHT fuse increases the data path setup delays to input storage elements, matching equivalent delays in the clock path. When the fuse is erased, the setup time to the input storage element is minimized. This feature facilitates doing worst-case designs for which data is loaded from sources which have low (or zero) minimum output propagation delays from clock edges.

## PAL Block Clock Generation

Each ispMACH 4A device has four clock pins that can also be used as inputs. These pins drive a clock generator in each PAL block (Figure 14). The clock generator provides four clock signals that can be used anywhere in the PAL block. These four PAL block clock signals can consist of a large number of combinations of the true and complement edges of the global clock signals. Table 14 lists the possible combinations.



17466G-004

**Figure 14. PAL Block Clock Generator**<sup>1</sup>

1. *M4A(3,5)-32/32 and M4A(3,5)-64/32 have only two clock pins, GCLK0 and GCLK1. GCLK2 is tied to GCLK0, and GCLK3 is tied to GCLK1.*

**Table 14. PAL Block Clock Combinations**<sup>1</sup>

Block CLK0	Block CLK1	Block CLK2	Block CLK3
GCLK0	GCLK1	X	X
$\overline{GCLK1}$	GCLK1	X	X
GCLK0	$\overline{GCLK0}$	X	X
$\overline{GCLK1}$	$\overline{GCLK0}$	X	X
X	X	GCLK2 (GCLK0)	GCLK3 (GCLK1)
X	X	$\overline{GCLK3}$ ( $\overline{GCLK1}$ )	GCLK3 (GCLK1)
X	X	GCLK2 (GCLK0)	$\overline{GCLK2}$ ( $\overline{GCLK0}$ )
X	X	$\overline{GCLK3}$ ( $\overline{GCLK1}$ )	$\overline{GCLK2}$ ( $\overline{GCLK0}$ )

**Note:**

1. *Values in parentheses are for the M4A(3,5)-32/32 and M4A(3,5)-64/32.*

This feature provides high flexibility for partitioning state machines and dual-phase clocks. It also allows latches to be driven with either polarity of latch enable, and in a master-slave configuration.

## IEEE 1149.1-COMPLIANT BOUNDARY SCAN TESTABILITY

All ispMACH 4A devices have boundary scan cells and are compliant to the IEEE 1149.1 standard. This allows functional testing of the circuit board on which the device is mounted through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test node data to be captured and shifted out for verification. In addition, these devices can be linked into a board-level serial scan path for more complete board-level testing.

## IEEE 1149.1-COMPLIANT IN-SYSTEM PROGRAMMING

Programming devices in-system provides a number of significant benefits including: rapid prototyping, lower inventory levels, higher quality, and the ability to make in-field modifications. All ispMACH 4A devices provide In-System Programming (ISP) capability through their Boundary ScanTest Access Ports. This capability has been implemented in a manner that ensures that the port remains compliant to the IEEE 1149.1 standard. By using IEEE 1149.1 as the communication interface through which ISP is achieved, customers get the benefit of a standard, well-defined interface.

ispMACH 4A devices can be programmed across the commercial temperature and voltage range. The PC-based ispVM™ software facilitates in-system programming of ispMACH 4A devices. ispVM takes the JEDEC file output produced by the design implementation software, along with information about the JTAG chain, and creates a set of vectors that are used to drive the JTAG chain. ispVM software can use these vectors to drive a JTAG chain via the parallel port of a PC. Alternatively, ispVM software can output files in formats understood by common automated test equipment. This equipment can then be used to program ispMACH 4A devices during the testing of a circuit board.

## PCI COMPLIANT

ispMACH 4A devices in the -5/-55/-6/-65/-7/-10/-12 speed grades are compliant with the *PCI Local Bus Specification* version 2.1, published by the PCI Special Interest Group (SIG). The 5-V devices are fully PCI-compliant. The 3.3-V devices are mostly compliant but do not meet the PCI condition to clamp the inputs as they rise above  $V_{CC}$  because of their 5-V input tolerant feature.

## SAFE FOR MIXED SUPPLY VOLTAGE SYSTEM DESIGNS

Both the 3.3-V and 5-V  $V_{CC}$  ispMACH 4A devices are safe for mixed supply voltage system designs. The 5-V devices will not overdrive 3.3-V devices above the output voltage of 3.3 V, while they accept inputs from other 3.3-V devices. The 3.3-V device will accept inputs up to 5.5 V. Both the 5-V and 3.3-V versions have the same high-speed performance and provide easy-to-use mixed-voltage design capability.

## PULL UP OR BUS-FRIENDLY INPUTS AND I/Os

All ispMACH 4A devices have inputs and I/Os which feature the Bus-Friendly circuitry incorporating two inverters in series which loop back to the input. This double inversion weakly holds the input at its last driven logic state. While it is good design practice to tie unused pins to a known state, the Bus-Friendly input structure pulls pins away from the input threshold voltage where noise can cause high-frequency switching. At power-up, the Bus-Friendly latches are reset to a logic level "1." For the circuit diagram, please refer to the document entitled *MACH Endurance Characteristics* on the Lattice Data Book CD-ROM or Lattice web site.

All ispMACH 4A devices have a programmable bit that configures all inputs and I/Os with either pull-up or Bus-Friendly characteristics. If the device is configured in pull-up mode, all inputs and I/O pins are

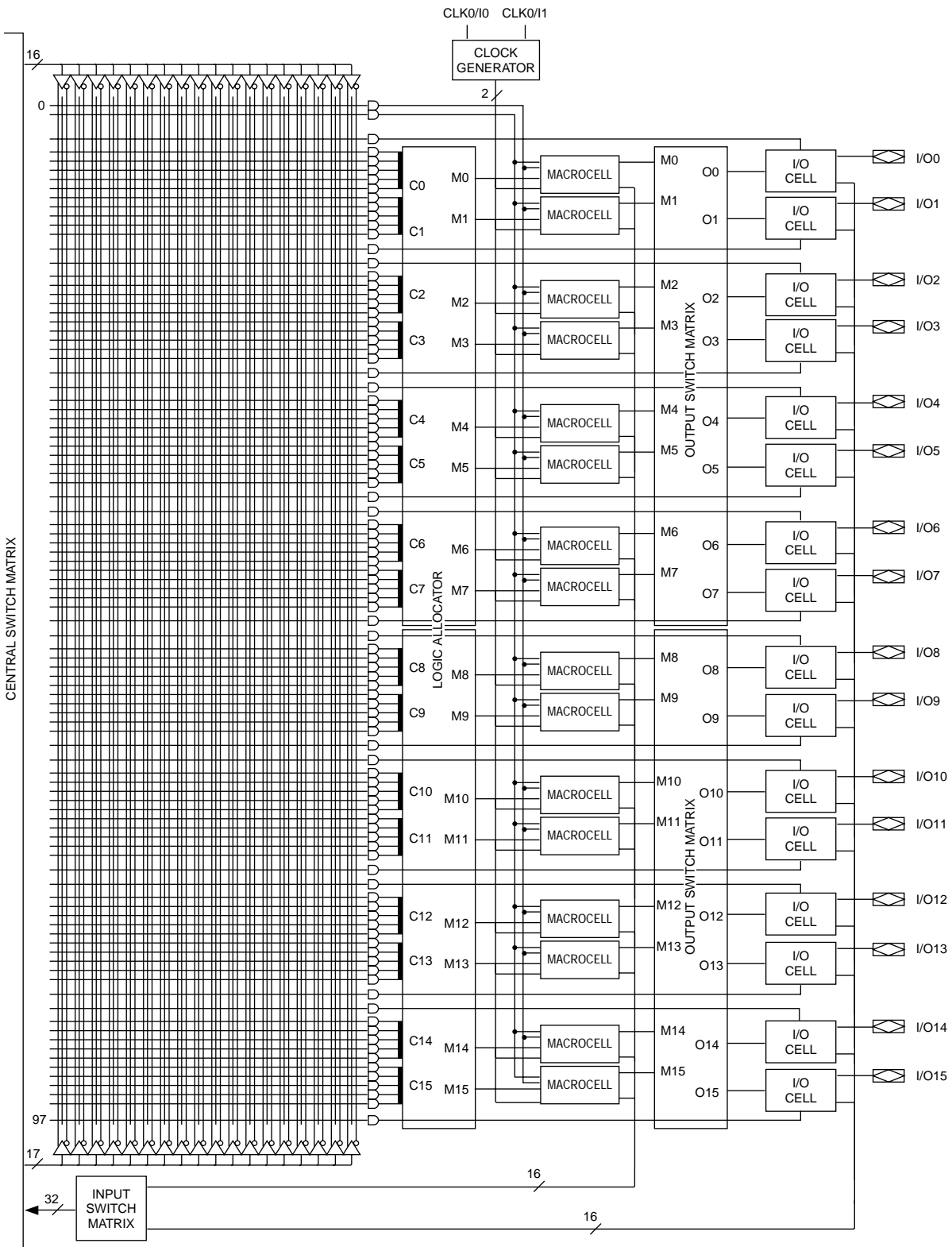
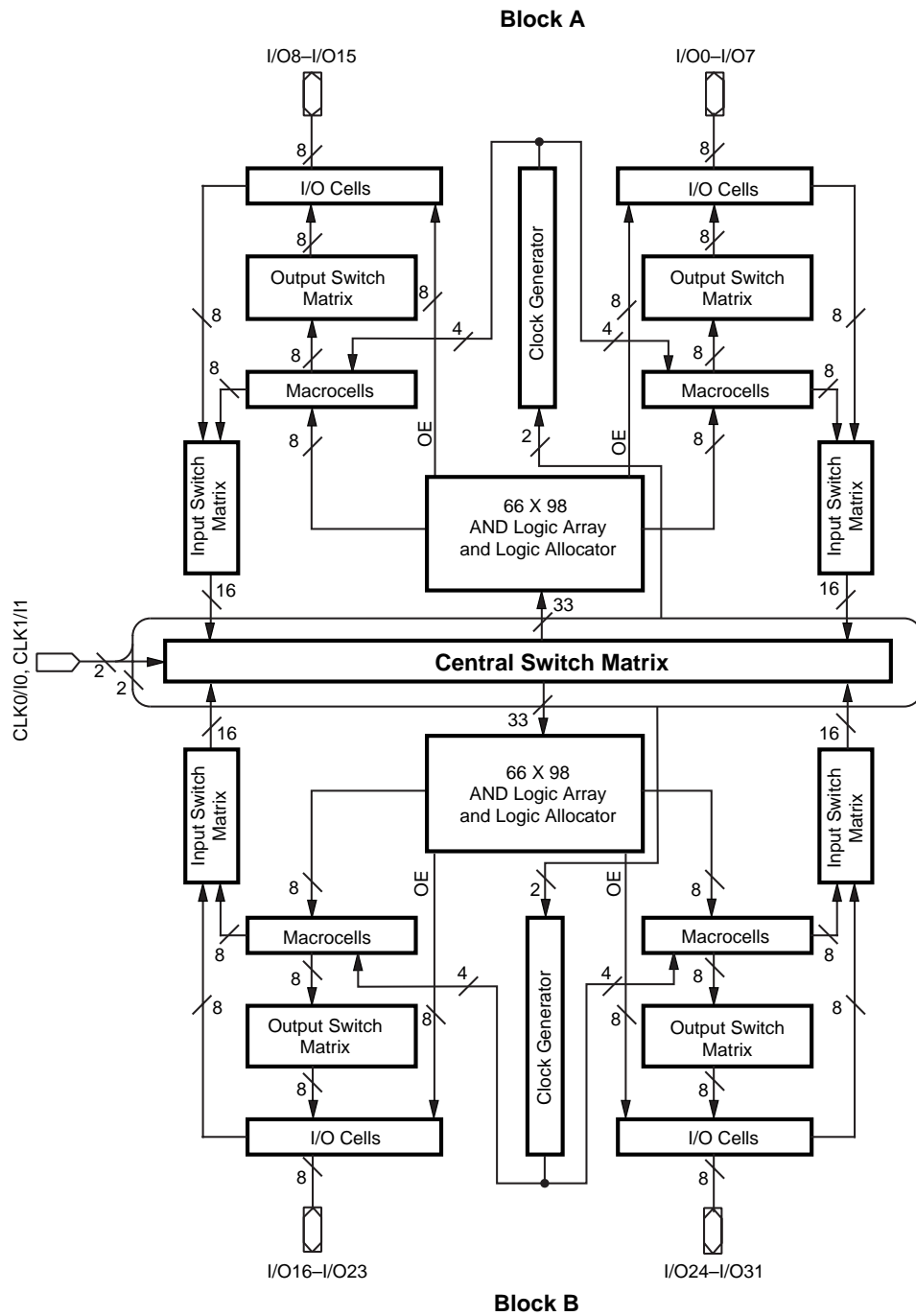


Figure 18. PAL Block for M4A (3,5)-32/32

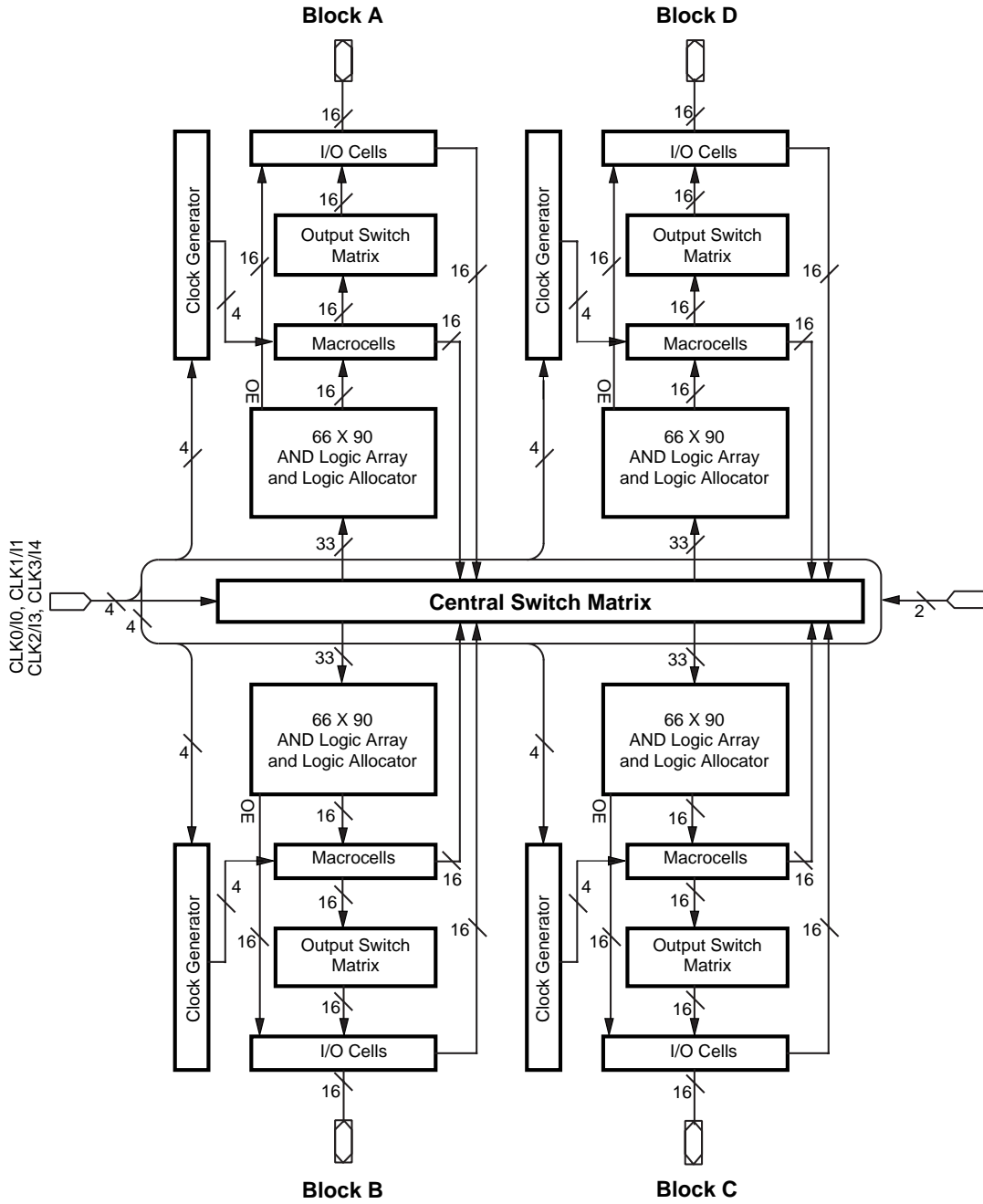
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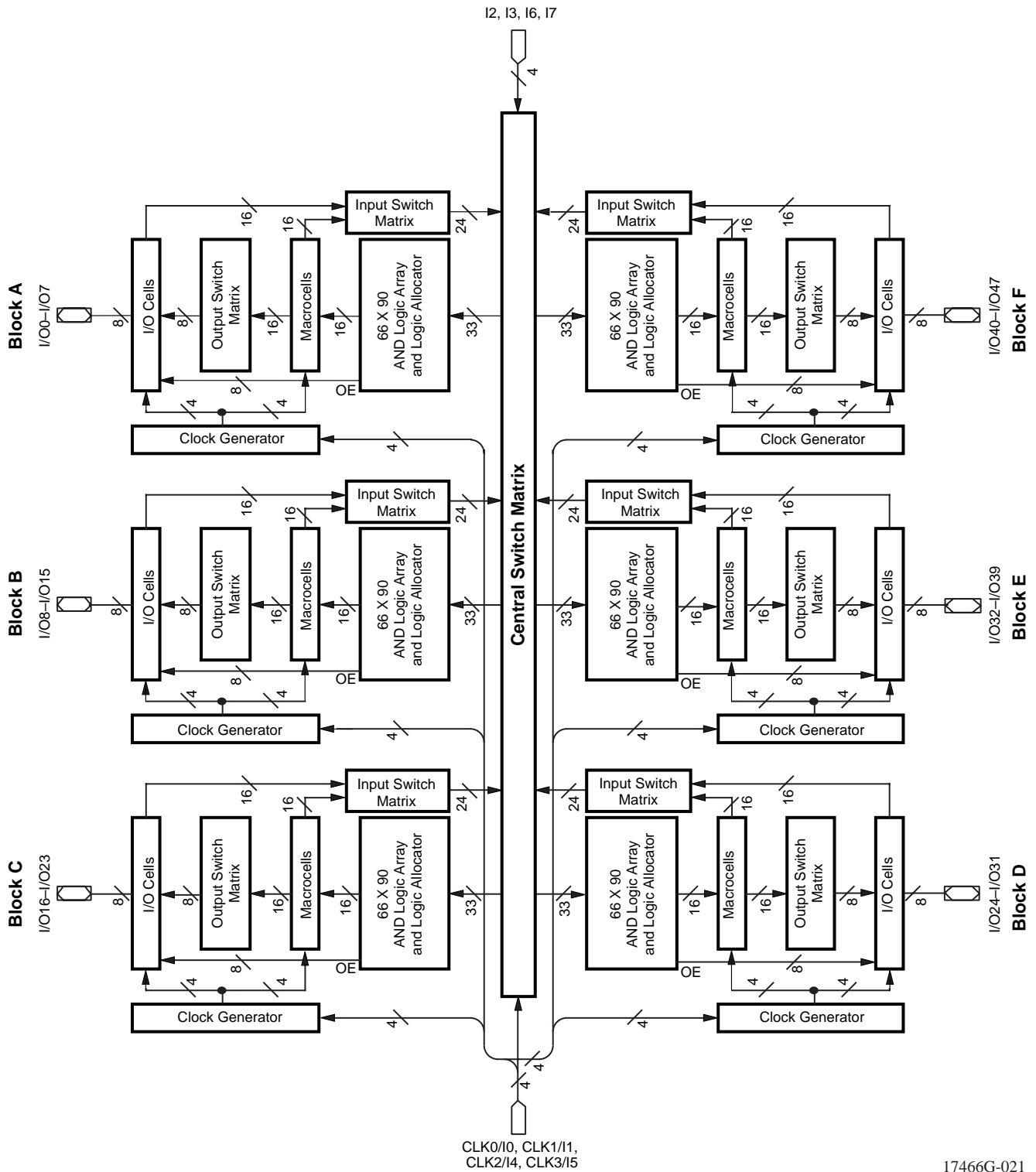
## BLOCK DIAGRAM – M4A(3,5)-32/32



## BLOCK DIAGRAM – M4A3-64/64

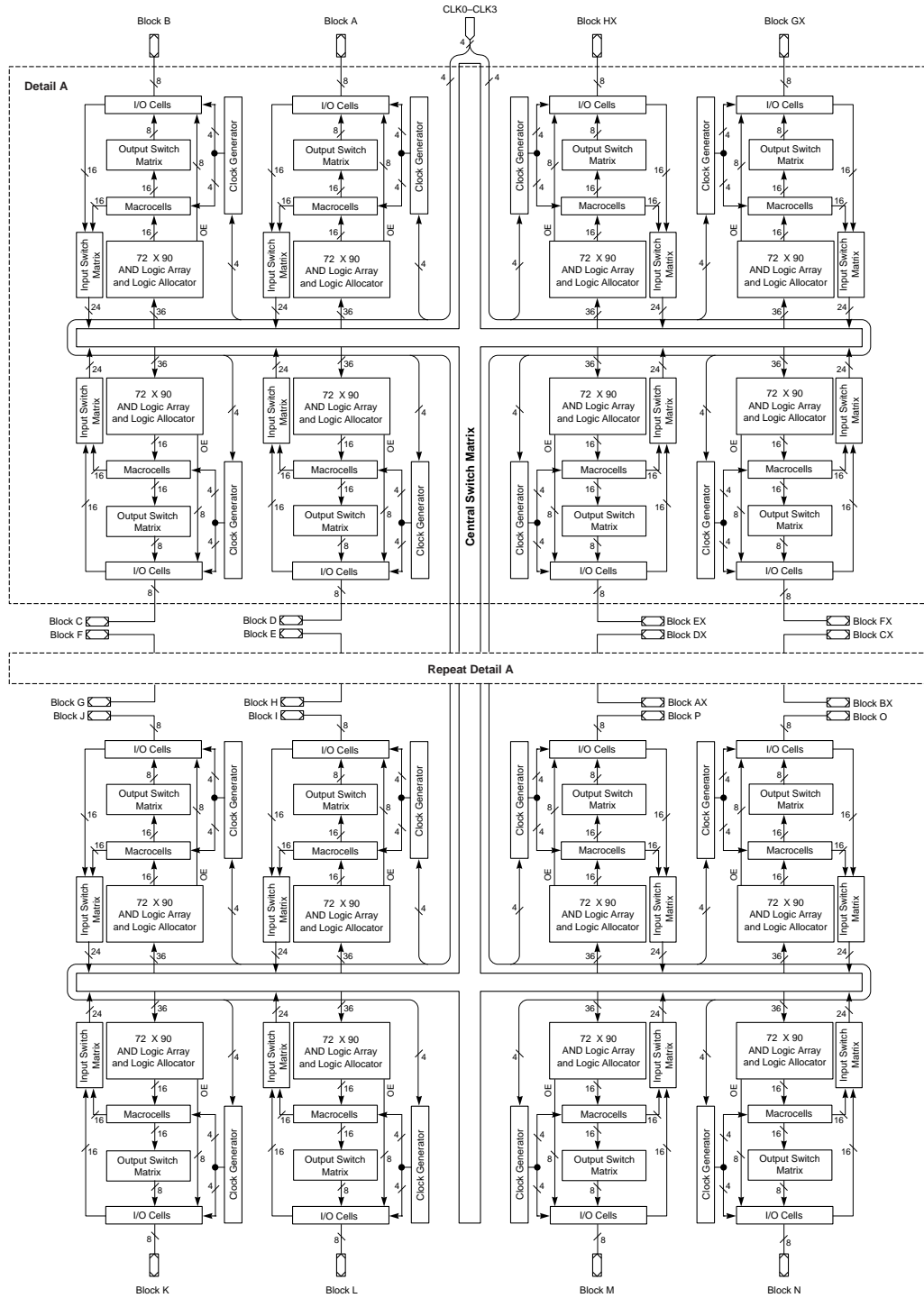


# BLOCK DIAGRAM – M4A(3,5)-96/48



17466G-021

# BLOCK DIAGRAM – M4A3-384/160, M4A3-384/192



## ABSOLUTE MAXIMUM RATINGS

### M4A3

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-55°C to +100°C
Device Junction Temperature	+130°C
Supply Voltage with Respect to Ground	-0.5 V to +4.5 V
DC Input Voltage	-0.5 V to 6.0 V
Static Discharge Voltage	2000 V
Latchup Current ( $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ )	200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

## OPERATING RANGES

### Commercial (C) Devices

Ambient Temperature ( $T_A$ )	
Operating in Free Air	0°C to +70°C
Supply Voltage ( $V_{CC}$ ) with Respect to Ground	+3.0 V to +3.6 V

### Industrial (I) Devices

Ambient Temperature ( $T_A$ )	
Operating in Free Air	-40°C to +85°C
Supply Voltage ( $V_{CC}$ ) with Respect to Ground	+3.0 V to +3.6 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

## 3.3-V DC CHARACTERISTICS OVER OPERATING RANGES

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
$V_{OH}$	Output HIGH Voltage	$V_{CC} = \text{Min}$ $V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -100 \mu\text{A}$	$V_{CC} - 0.2$		V
			$I_{OH} = -3.2 \text{ mA}$	2.4		V
$V_{OL}$	Output LOW Voltage	$V_{CC} = \text{Min}$ $V_{IN} = V_{IH}$ or $V_{IL}$ (Note 1)	$I_{OL} = 100 \mu\text{A}$		0.2	V
			$I_{OL} = 24 \text{ mA}$		0.5	V
$V_{IH}$	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs	2.0		5.5	V
$V_{IL}$	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs	-0.3		0.8	V
$I_{IH}$	Input HIGH Leakage Current	$V_{IN} = 3.6 \text{ V}$ , $V_{CC} = \text{Max}$ (Note 2)			5	$\mu\text{A}$
$I_{IL}$	Input LOW Leakage Current	$V_{IN} = 0 \text{ V}$ , $V_{CC} = \text{Max}$ (Note 2)			-5	$\mu\text{A}$
$I_{OZH}$	Off-State Output Leakage Current HIGH	$V_{OUT} = 3.6 \text{ V}$ , $V_{CC} = \text{Max}$ $V_{IN} = V_{IH}$ or $V_{IL}$ (Note 2)			5	$\mu\text{A}$
$I_{OZL}$	Off-State Output Leakage Current LOW	$V_{OUT} = 0 \text{ V}$ , $V_{CC} = \text{Max}$ $V_{IN} = V_{IH}$ or $V_{IL}$ (Note 2)			-5	$\mu\text{A}$
$I_{SC}$	Output Short-Circuit Current	$V_{OUT} = 0.5 \text{ V}$ , $V_{CC} = \text{Max}$ (Note 3)	-15		-160	mA

#### Notes:

- Total  $I_{OL}$  for one PAL block should not exceed 64 mA.
- I/O pin leakage is the worst case of  $I_{IL}$  and  $I_{OZL}$  (or  $I_{IH}$  and  $I_{OZH}$ ).
- Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

#### Notes:

- See "MACH Switching Test Circuit" document on the Literature Download page of the Lattice web site.
- This parameter does not apply to flip-flops in the emulated mode since the feedback path is required for emulation.

## ispMACH 4A TIMING PARAMETERS OVER OPERATING RANGES<sup>1</sup>

		-5		-55		-6		-65		-7		-10		-12		-14		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
<b>Combinatorial Delay:</b>																		
$t_{PDi}$	Internal combinatorial propagation delay		3.5		4.0		4.3		4.5		5.0		7.0		9.0		11.0	ns
$t_{PD}$	Combinatorial propagation delay		5.0		5.5		6.0		6.5		7.5		10.0		12.0		14.0	ns
<b>Registered Delays:</b>																		
$t_{SS}$	Synchronous clock setup time, D-type register	3.0		3.5		3.5		3.5		5.0		5.5		7.0		10.0		ns
$t_{SST}$	Synchronous clock setup time, T-type register	4.0		4.0		4.0		4.0		6.0		6.5		8.0		11.0		ns
$t_{SA}$	Asynchronous clock setup time, D-type register	2.5		2.5		2.5		3.0		3.5		4.0		5.0		8.0		ns
$t_{SAT}$	Asynchronous clock setup time, T-type register	3.0		3.0		3.0		3.5		4.5		5.0		6.0		9.0		ns
$t_{HS}$	Synchronous clock hold time	0.0		0.0		0.0		0.0		0.0		0.0		0.0		0.0		ns
$t_{HA}$	Asynchronous clock hold time	2.5		2.5		2.5		3.0		3.5		4.0		5.0		8.0		ns
$t_{COSi}$	Synchronous clock to internal output		2.5		2.5		2.8		3.0		3.0		3.0		3.5		3.5	ns
$t_{COS}$	Synchronous clock to output		4.0		4.0		4.5		5.0		5.5		6.0		6.5		6.5	ns
$t_{COAi}$	Asynchronous clock to internal output		5.0		5.0		5.0		5.0		6.0		8.0		10.0		12.0	ns
$t_{COA}$	Asynchronous clock to output		6.5		6.5		6.8		7.0		8.5		11.0		13.0		15.0	ns
<b>Latched Delays:</b>																		
$t_{SSL}$	Synchronous latch setup time	4.0		4.0		4.0		4.5		6.0		7.0		8.0		10.0		ns
$t_{SAL}$	Asynchronous latch setup time	3.0		3.0		3.5		3.5		4.0		4.0		5.0		8.0		ns
$t_{HSL}$	Synchronous latch hold time	0.0		0.0		0.0		0.0		0.0		0.0		0.0		0.0		ns
$t_{HAL}$	Asynchronous latch hold time	3.0		3.0		3.5		3.5		4.0		4.0		5.0		8.0		ns
$t_{PDLi}$	Transparent latch to internal output		5.5		5.5		5.8		6.0		7.5		9.0		11.0		12.0	ns
$t_{PDL}$	Propagation delay through transparent latch to output		7.0		7.0		7.5		8.0		10.0		12.0		14.0		15.0	ns
$t_{GOSi}$	Synchronous gate to internal output		3.0		3.0		3.0		3.0		3.5		4.5		7.0		8.0	ns
$t_{GOS}$	Synchronous gate to output		4.5		4.5		4.8		5.0		6.0		7.5		10.0		11.0	ns
$t_{GOAi}$	Asynchronous gate to internal output		6.0		6.0		6.0		6.0		8.5		10.0		13.0		15.0	ns
$t_{GOA}$	Asynchronous gate to output		7.5		7.5		7.8		8.0		11.0		13.0		16.0		18.0	ns
<b>Input Register Delays:</b>																		
$t_{SIRS}$	Input register setup time	1.5		1.5		2.0		2.0		2.0		2.0		2.0		2.0		ns
$t_{HIRS}$	Input register hold time	2.5		2.5		3.0		3.0		3.0		3.0		3.0		4.0		ns
$t_{ICOSi}$	Input register clock to internal feedback		3.0		3.0		3.0		3.0		3.5		4.5		6.0		6.0	ns
<b>Input Latch Delays:</b>																		
$t_{SIL}$	Input latch setup time	1.5		1.5		1.5		2.0		2.0		2.0		2.0		2.0		ns
$t_{HIL}$	Input latch hold time	2.5		2.5		2.5		3.0		3.0		3.0		3.0		4.0		ns
$t_{IGOSi}$	Input latch gate to internal feedback		3.5		3.5		3.8		4.0		4.0		4.0		4.0		5.0	ns
$t_{PDILi}$	Transparent input latch to internal feedback		1.5		1.5		1.5		1.5		2.0		2.0		2.0		2.0	ns

## ispMACH 4A TIMING PARAMETERS OVER OPERATING RANGES<sup>1</sup>

		-5		-55		-6		-65		-7		-10		-12		-14		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
<b>Input Register Delays with ZHT Option:</b>																		
$t_{SIRZ}$	Input register setup time - ZHT	6.0		6.0		6.0		6.0		6.0		6.0		6.0		6.0		ns
$t_{HIRZ}$	Input register hold time - ZHT	0.0		0.0		0.0		0.0		0.0		0.0		0.0		0.0		ns
<b>Input Latch Delays with ZHT Option:</b>																		
$t_{SILZ}$	Input latch setup time - ZHT	6.0		6.0		6.0		6.0		6.0		6.0		6.0		6.0		ns
$t_{HILZ}$	Input latch hold time - ZHT	0.0		0.0		0.0		0.0		0.0		0.0		0.0		0.0		ns
$t_{PDIL}$ $Z_i$	Transparent input latch to internal feedback - ZHT		6.0		6.0		6.0		6.0		6.0		6.0		6.0		6.0	ns
<b>Output Delays:</b>																		
$t_{BUF}$	Output buffer delay		1.5		1.5		1.8		2.0		2.5		3.0		3.0		3.0	ns
$t_{SIW}$	Slow slew rate delay adder		2.5		2.5		2.5		2.5		2.5		2.5		2.5		2.5	ns
$t_{EA}$	Output enable time		7.5		7.5		8.5		8.5		9.5		10.0		12.0		15.0	ns
$t_{ER}$	Output disable time		7.5		7.5		8.5		8.5		9.5		10.0		12.0		15.0	ns
<b>Power Delay:</b>																		
$t_{PL}$	Power-down mode delay adder		2.5		2.5		2.5		2.5		2.5		2.5		2.5		2.5	ns
<b>Reset and Preset Delays:</b>																		
$t_{SRi}$	Asynchronous reset or preset to internal register output		7.5		7.7		8.0		8.0		9.5		11.0		13.0		16.0	ns
$t_{SR}$	Asynchronous reset or preset to register output		9.0		9.2		10.0		10.0		12.0		14.0		16.0		19.0	ns
$t_{SRR}$	Asynchronous reset and preset register recovery time	7.0		7.0		7.5		7.5		8.0		8.0		10.0		15.0		ns
$t_{SRW}$	Asynchronous reset or preset width	7.0		7.0		8.0		8.0		10.0		10.0		12.0		15.0		ns
<b>Clock/LE Width:</b>																		
$t_{WLS}$	Global clock width low	2.0		2.0		2.5		2.5		3.0		4.0		5.0		6.0		ns
$t_{WHS}$	Global clock width high	2.0		2.0		2.5		2.5		3.0		4.0		5.0		6.0		ns
$t_{WLA}$	Product term clock width low	3.0		3.0		3.5		3.5		4.0		5.0		8.0		9.0		ns
$t_{WHA}$	Product term clock width high	3.0		3.0		3.5		3.5		4.0		5.0		8.0		9.0		ns
$t_{CWS}$	Global gate width low (for low transparent) or high (for high transparent)	4.0		4.0		4.5		4.5		5.0		5.0		6.0		6.0		ns
$t_{CWA}$	Product term gate width low (for low transparent) or high (for high transparent)	4.0		4.0		4.5		4.5		5.0		5.0		6.0		9.0		ns
$t_{WIRL}$	Input register clock width low	3.0		3.0		3.5		3.5		4.0		5.0		6.0		6.0		ns
$t_{WIRH}$	Input register clock width high	3.0		3.0		3.5		3.5		4.0		5.0		6.0		6.0		ns
$t_{WIL}$	Input latch gate width	4.0		4.0		4.5		4.5		5.0		5.0		6.0		6.0		ns

## I<sub>CC</sub> vs. FREQUENCY

These curves represent the typical power consumption for a particular device at system frequency. The selected “typical” pattern is a 16-bit up-down counter. This pattern fills the device and exercises every macrocell. Maximum frequency shown uses internal feedback and a D-type register. Power/Speed are optimized to obtain the highest counter frequency and the lowest power. The highest frequency (LSBs) is placed in common PAL blocks, which are set to high power. The lowest frequency signals (MSBs) are placed in a common PAL block and set to lowest power.

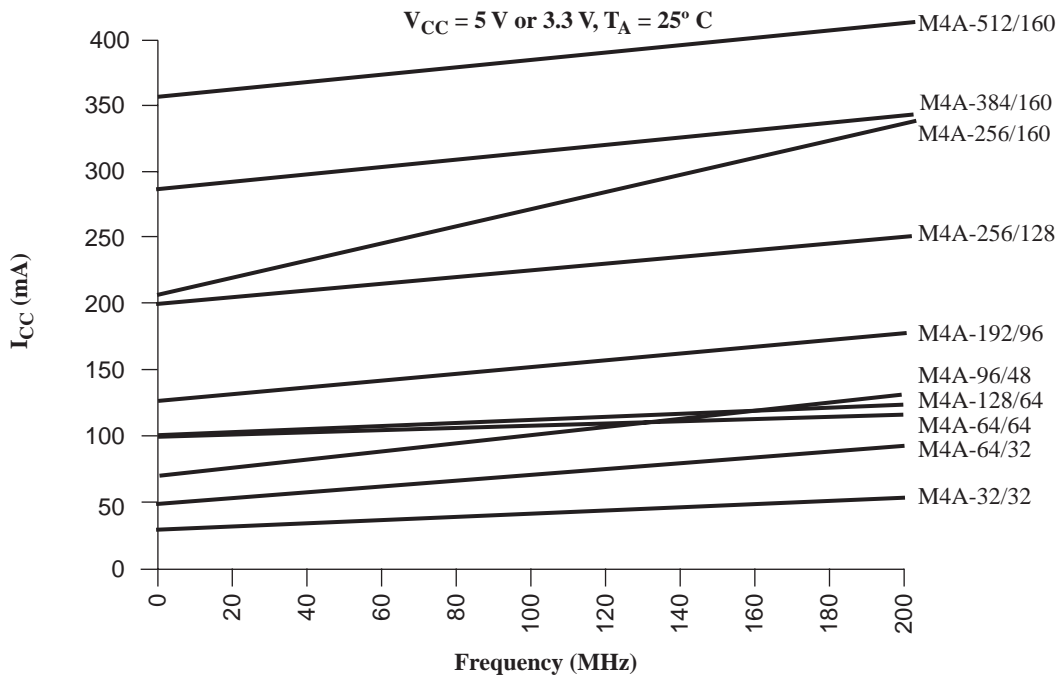


Figure 19. ispMACH 4A I<sub>CC</sub> Curves at High Speed Mode

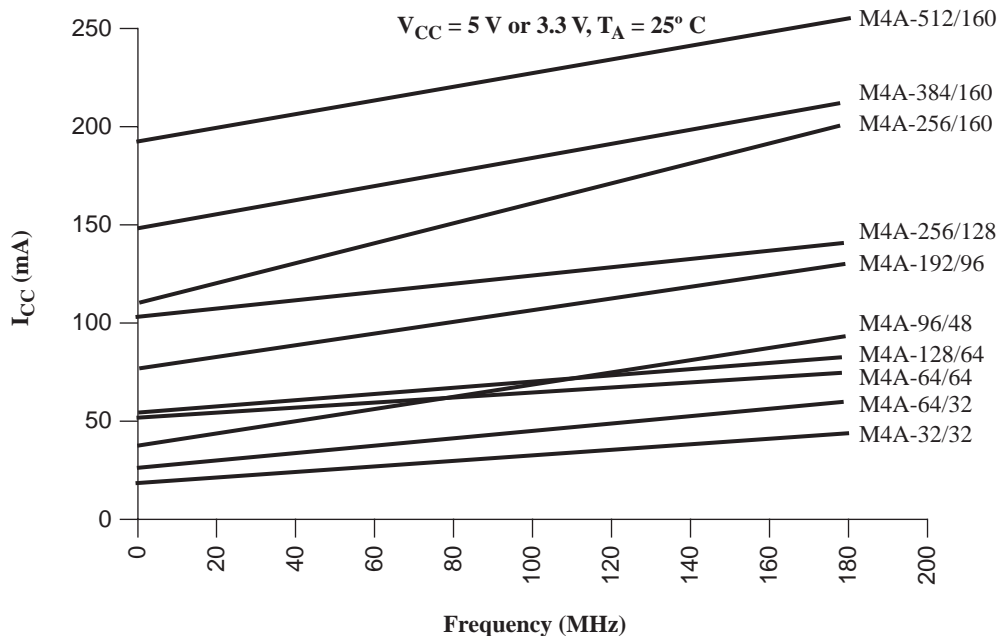
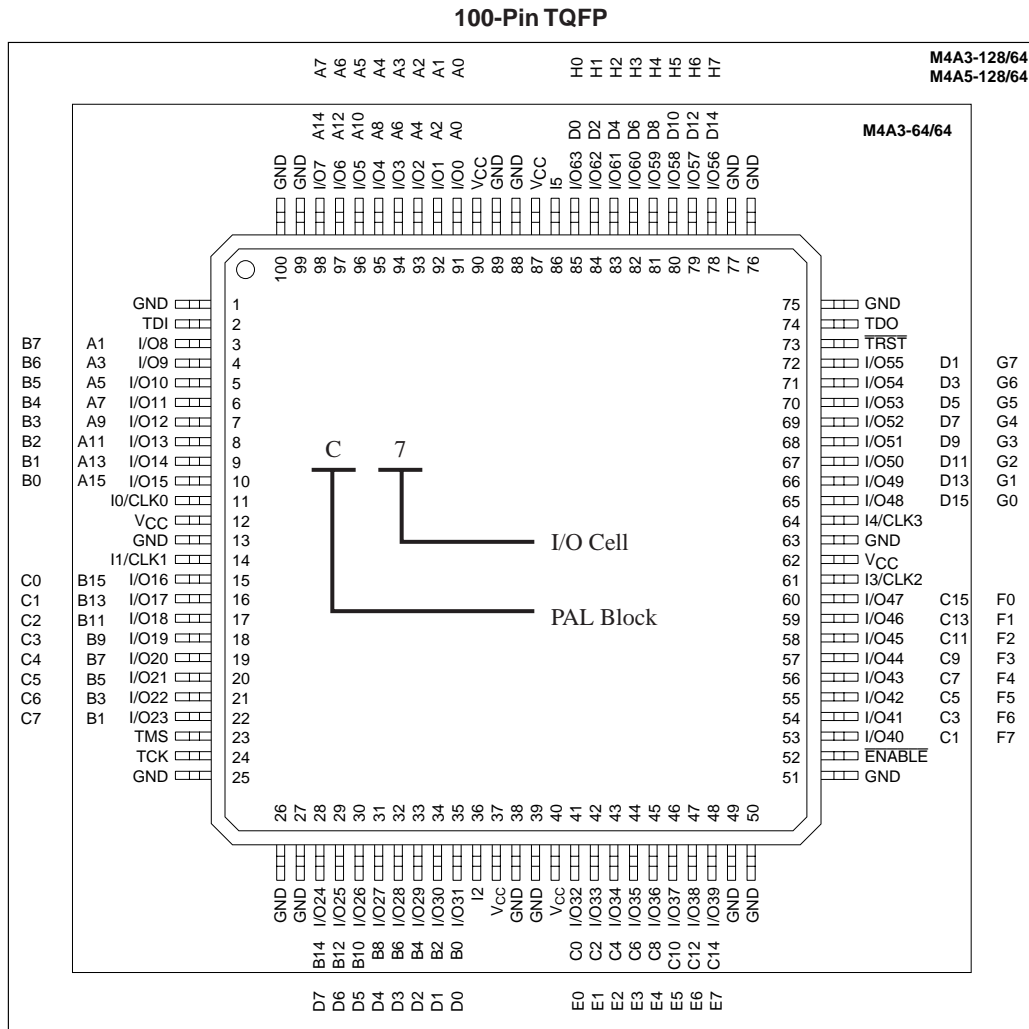


Figure 20. ispMACH 4A I<sub>CC</sub> Curves at Low Power Mode



# 100-PIN TQFP CONNECTION DIAGRAM (M4A3-64/64 AND M4A(3,5)-128/64)

## Top View



## PIN DESIGNATIONS

CLK/I = Clock or Input

GND = Ground

I = Input

I/O = Input/Output

V<sub>CC</sub> = Supply Voltage

TDI = Test Data In

TCK = Test Clock

TMS = Test Mode Select

TDO = Test Data Out

TRST = Test Reset

ENABLE = Program

# 100-BALL caBGA CONNECTION DIAGRAM (M4A3-128/64)

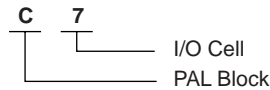
## Bottom View

### 100-Ball caBGA

	10	9	8	7	6	5	4	3	2	1	
A	GND	I/O63 H7	I/O60 H4	I/O57 H1	GND	GND	I/O1 A1	I/O4 A4	I/O7 A7	GND	A
B	$\overline{\text{TRST}}$	GND	I/O61 H5	I5	VCC	I/O0 A0	I/O6 A6	GND	TDI	I/O15 B7	B
C	I/O53 G5	TDO	I/O62 H6	I/O58 H2	I/O56 H0	I/O2 A2	GND	I/O14 B6	I/O13 B5	I/O12 B4	C
D	I/O50 G2	I/O55 G7	GND	I/O59 H3	I/O3 A3	I/O5 A5	I/O11 B3	I/O10 B2	CLK0/I0	I/O9 B1	D
E	CLK3/I4	I/O49 G1	I/O51 G3	I/O54 G6	VCC	I/O16 C0	I/O20 C4	I/O8 B0	VCC	GND	E
F	GND	VCC	I/O40 F0	I/O52 G4	I/O48 G0	VCC	I/O22 C6	I/O19 C3	I/O17 C1	CLK1/I1	F
G	I/O41 F1	CLK2/I3	I/O42 F2	I/O43 F3	I/O37 E5	I/O35 E3	I/O27 D3	GND	I/O23 C7	I/O18 C2	G
H	I/O44 F4	I/O45 F5	I/O46 F6	GND	I/O34 E2	I/O24 D0	I/O26 D2	I/O30 D6	TCK	I/O21 C5	H
J	I/O47 F7	$\overline{\text{ENABLE}}$	GND	I/O38 E6	I/O32 E0	VCC	I2	I/O29 D5	GND	TMS	J
K	GND	I/O39 E7	I/O36 E4	I/O33 E1	GND	GND	I/O25 D1	I/O28 D4	I/O31 D7	GND	K

#### PIN DESIGNATIONS

CLK = Clock  
 GND = Ground  
 I = Input  
 I/O = Input/Output  
 N/C = No Connect  
 VCC = Supply Voltage  
 TDI = Test Data In  
 TCK = Test Clock  
 TMS = Test Mode Select  
 TDO = Test Data Out  
 $\overline{\text{TRST}}$  = Test Reset  
 ENABLE = Program



17466G-100cabga

# 144-BALL FPBGA CONNECTION DIAGRAM (M4A3-192/96)

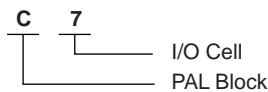
## Bottom View

144-Ball fpBGA

	12	11	10	9	8	7	6	5	4	3	2	1	
A	GND	I/O72 L7	I/O76 L3	I13	GBCLK3	I0	I/O82 A2	I/O86 A6	I/O88 B0	I/O93 B5	I/O95 B7	GND	A
B	GND	I/O73 L6	I/O77 L2	I/O79 L0	VCC	I1	I/O83 A3	I/O87 A7	I/O90 B2	I/O94 B6	I/O0 D7	TDI	B
C	GND	TD0	I/O74 L5	I14	GND	I/O80 A0	I/O84 A4	GND	I/O92 B4	I/O1 D6	I/O4 D3	I/O3 D4	C
D	I/O67 K4	I/O69 K2	I/O71 K0	I/O75 L4	GBCLK0	I/O81 A1	VCC	I/O91 B3	I/O2 D5	I2	I/O6 D1	I/O7 D0	D
E	I12	I/O64 K7	I/O66 K5	I/O70 K1	I/O78 L1	I/O85 A5	I/O89 B1	I/O5 D2	I/O8 C7	I4	GND	VCC	E
F	I10	I11	GND	I/O65 K6	I/O68 K3	I15	I3	GND	I/O12 C3	I/O11 C4	I/O10 C5	I/O9 C6	F
G	I/O60 J3	I/O61 J2	I/O62 J1	I/O63 J0	VCC	GND	I7	I/O20 E3	I/O17 E6	I/O15 C0	I/O14 C1	I/O13 C2	G
H	I/O56 J7	I/O57 J6	I/O58 J5	I/O59 J4	I/O53 I2	I/O41 H1	I/O37 G5	I/O30 F1	I/O22 E1	I/O18 E5	I/O16 E7	VCC	H
J	I/O55 I0	I/O54 I1	VCC	I/O50 I5	I/O43 H3	VCC	I/O33 G1	GBCLK2	I/O27 F4	I/O23 E0	I/O21 E2	I/O19 E4	J
K	I/O51 I4	I/O52 I3	I/O49 I6	I/O44 H4	GND	I/O36 G4	I/O32 G0	VCC	I6	I/O26 F5	TCK	TMS	K
L	GND	I/O48 I7	I/O46 H6	I/O42 H2	I/O39 G7	I/O35 G3	I9	GND	I/O31 F0	I/O29 F2	I/O25 F6	GND	L
M	GND	I/O47 H7	I/O45 H5	I/O40 H0	I/O38 G6	I/O34 G2	I8	GBCLK1	I5	I/O28 F3	I/O24 F7	GND	M
	12	11	10	9	8	7	6	5	4	3	2	1	

### PIN DESIGNATIONS

- CLK = Clock
- GND = Ground
- I = Input
- I/O = Input/Output
- N/C = No Connect
- VCC = Supply Voltage
- TDI = Test Data In
- TCK = Test Clock
- TMS = Test Mode Select
- TD0 = Test Data Out



## 256-BALL fpBGA CONNECTION DIAGRAM (M4A3-256/192)

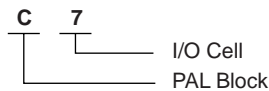
### Bottom View

#### 256-Ball fpBGA

	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	I/O167 N15	I/O181 O13	I/O180 O12	I/O177 O9	I/O174 O6	I/O172 O4	I/O191 P14	I/O186 P4	I/O1 A2	I/O3 A6	GCLK0	I/O9 B1	I/O13 B5	I/O15 B7	I/O18 B10	I/O20 B12	A
B	I/O165 N13	I/O166 N14	I/O182 O14	I/O179 O11	I/O175 O7	I/O173 O5	I/O168 O0	I/O187 P6	I/O0 A0	I/O5 A10	I/O7 A14	I/O10 B2	I/O16 B8	I/O19 B11	I/O21 B13	NC	B
C	I/O163 N11	I/O164 N12	NC	I/O183 O15	I/O178 O10	I/O170 O2	I/O171 O3	I/O189 P10	I/O184 P0	I/O6 A12	I/O12 B4	I/O14 B6	I/O23 B15	I/O22 B14	TDI	I/O39 C15	C
D	I/O158 N6	I/O159 N7	TDO	GND	GND	VCC	GND	VCC	GND	GND	VCC	GND	VCC	I/O17 B9	I/O38 C14	I/O37 C13	D
E	I/O156 N4	NC	I/O162 N10	VCC	I/O160 N8	I/O161 N9	I/O190 P12	GCLK3	I/O188 P8	I/O2 A4	I/O8 B0	NC	GND	I/O36 C12	I/O35 C11	I/O31 C7	E
F	I/O152 N0	I/O157 N5	I/O155 N3	GND	I/O154 N2	I/O153 N1	I/O176 O8	I/O169 O1	I/O185 P2	I/O4 A8	I/O11 B3	I/O34 C10	VCC	I/O32 C8	I/O30 C6	I/O29 C5	F
G	I/O147 M6	I/O150 M12	I/O149 M10	VCC	I/O148 M8	I/O151 M14	VCC	GND	GND	VCC	I/O33 C9	I/O28 C4	GND	I/O26 C2	I/O25 C1	I/O47 D14	G
H	I/O144 M0	I/O146 M4	I/O145 OM2	GND	I/O136 L0	I/O137 L2	GND	VCC	VCC	GND	I/O27 C3	I/O24 C0	VCC	I/O44 D8	I/O43 D6	I/O42 D4	H
J	I/O138 L4	I/O139 L6	I/O140 L8	GND	I/O142 L12	I/O141 L10	GND	VCC	VCC	GND	I/O46 D12	I/O45 D10	GND	I/O49 E2	I/O48 E0	I/O50 E4	J
K	I/O143 L14	I/O120 K0	I/O121 K1	VCC	I/O123 K3	I/O122 K2	VCC	GND	GND	VCC	I/O41 D2	I/O40 D0	VCC	I/O55 E14	I/O54 E12	I/O56 F0	K
L	I/O124 K4	I/O125 K5	I/O127 K7	GND	I/O130 K10	I/O126 K6	I/O98 I4	I/O91 H6	I/O75 G3	I/O77 G5	I/O52 E8	I/O51 E6	GND	I/O59 F3	I/O60 F4	I/O57 F1	L
M	I/O128 K8	I/O129 K9	I/O131 K11	GND	I/O107 J3	I/O105 J1	I/O100 I8	I/O90 H4	I/O74 G2	I/O80 G8	I/O83 G11	I/O53 E10	VCC	I/O68 F12	I/O63 F7	I/O58 F2	M
N	I/O132 K12	I/O133 K13	I/O135 K15	VCC	GND	VCC	GND	VCC	GND	GND	VCC	GND	GND	TCK	I/O64 F8	I/O61 F5	N
P	I/O134 K14	I/O117 J13	I/O118 J14	I/O119 J15	I/O108 J4	I/O106 J2	I/O101 I10	I/O89 H2	I/O93 H10	I/O94 H12	I/O79 G7	I/O84 G12	I/O87 G15	TMS	I/O65 F9	I/O62 F6	P
R	I/O116 J12	I/O115 J11	I/O112 J8	I/O111 J7	I/O104 J0	I/O102 I12	I/O99 I6	I/O96 I0	I/O92 H8	I/O72 G0	I/O76 G4	I/O81 G9	I/O85 G13	I/O71 F15	I/O67 F11	I/O66 F10	R
T	I/O114 J10	I/O113 J9	I/O110 J6	I/O109 J5	I/O103 I14	GCLK2	I/O97 I2	I/O88 H0	GCLK1	I/O95 H14	I/O73 G1	I/O78 G6	I/O82 G10	I/O86 G14	I/O70 F14	I/O69 F13	T

#### PIN DESIGNATIONS

CLK = Clock  
 GND = Ground  
 I = Input  
 I/O = Input/Output  
 N/C = No Connect  
 VCC = Supply Voltage  
 TDI = Test Data In  
 TCK = Test Clock  
 TMS = Test Mode Select  
 TDO = Test Data Out



17466G-047

# 388-BALL fpBGA CONNECTION DIAGRAM (M4A3-512/256)

## Bottom View

### 388-Ball fpBGA

	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	GND	I/O243 OX3	I/O240 OX0	I/O241 OX1	I/O236 NX4	I/O231 MX7	I/O228 MX4	I/O226 MX2	I/O255 PX7	I/O251 PX3	I/O248 PX0	I/O0 A0	I/O5 A5	I/O6 A6	I/O27 D3	I/O30 D6	I/O17 C1	I/O22 C6	I/O8 B0	I/O10 B2	N/C	GND	A
B	N/C	GND	I/O245 OX5	I/O242 OX2	I/O238 NX6	I/O234 NX2	I/O232 NX0	I/O229 MX5	I/O224 MX0	I/O253 PX5	I/O249 PX1	I/O2 A2	CLK0	I/O26 D2	I/O29 D5	I/O31 D7	I/O20 C4	I/O9 B1	I/O12 B4	I/O13 B5	GND	TDI	B
C	I/O213 KX5	TDO	GND	I/O247 OX7	I/O244 OX4	I/O239 NX7	I/O235 NX3	I/O230 MX6	I/O227 MX3	CLK3	I/O250 PX2	I/O1 A1	I/O7 A7	I/O25 D1	I/O16 C0	I/O18 C2	I/O23 C7	I/O11 B3	I/O15 B7	GND	I/O47 F7	I/O44 F4	C
D	I/O210 KX2	I/O212 KX4	I/O215 KX7	GND	I/O246 OX6	VCC	I/O237 NX5	I/O233 NX1	VCC	I/O254 PX6	VCC	I/O3 A3	I/O24 D0	VCC	I/O19 C3	I/O21 C5	VCC	I/O14 B6	GND	I/O46 F6	I/O43 F3	I/O41 F1	D
E	I/O207 JX7	I/O209 KX1	I/O211 KX3	I/O214 KX6															I/O45 F5	I/O42 F2	I/O40 F0	I/O54 G6	E
F	I/O203 JX3	I/O205 JX5	I/O208 KX0	VCC															VCC	I/O55 G7	I/O52 G4	I/O50 G2	F
G	I/O200 JX0	I/O202 JX2	I/O204 JX4	I/O206 JX6			VCC	VCC	N/C	I/O225 MX1	I/O252 PX4	I/O4 A4	I/O28 D4	N/C	VCC	VCC			I/O53 G5	I/O51 G3	I/O49 G1	I/O39 E7	G
H	I/O221 LX5	I/O222 LX6	I/O223 LX7	I/O201 JX1			VCC	N/C	GND	GND	GND	GND	GND	GND	N/C	VCC			I/O48 G0	I/O38 E6	I/O37 E5	I/O36 E4	H
J	I/O218 LX2	I/O219 LX3	I/O220 LX4	VCC			N/C	GND	GND	GND	GND	GND	GND	GND	GND	N/C			VCC	I/O35 E3	I/O34 E2	I/O32 E0	J
K	I/O197 IX5	I/O198 IX6	I/O199 IX7	I/O216 LX0			I/O217 LX1	GND	GND	GND	GND	GND	GND	GND	GND	I/O33 E1			I/O63 H7	I/O62 H6	I/O61 H5	I/O60 H4	K
L	I/O192 IX0	I/O194 IX2	I/O195 IX3	I/O196 IX4			I/O193 IX1	GND	GND	GND	GND	GND	GND	GND	GND	I/O58 H2			VCC	I/O59 H3	I/O57 H1	I/O56 H0	L
M	I/O184 HX0	I/O185 HX1	I/O187 HX3	VCC			I/O186 HX2	GND	GND	GND	GND	GND	GND	GND	GND	I/O69 I5			I/O67 I3	I/O65 I1	I/O66 I2	I/O64 I0	M
N	I/O188 HX4	I/O189 HX5	I/O191 HX7	I/O190 HX6			I/O182 EX2	GND	GND	GND	GND	GND	GND	GND	GND	I/O89 L1			I/O88 L0	I/O71 I7	I/O70 I6	I/O68 I4	N
P	I/O160 EX0	I/O161 EX1	I/O163 EX3	VCC			N/C	GND	GND	GND	GND	GND	GND	GND	GND	N/C			VCC	I/O92 L4	I/O91 L3	I/O90 L2	P
R	I/O164 EX4	I/O165 EX5	I/O166 EX6	I/O177 GX1			VCC	N/C	GND	GND	GND	GND	GND	GND	N/C	VCC			I/O74 J2	I/O95 L7	I/O94 L6	I/O93 L5	R
T	I/O167 EX7	I/O176 GX0	I/O179 GX3	I/O181 GX5			VCC	VCC	N/C	I/O152 DX0	I/O131 AX3	I/O122 P2	I/O98 M2	N/C	VCC	VCC			I/O78 J6	I/O76 J4	I/O73 J1	I/O72 J0	T
U	I/O178 GX2	I/O180 GX4	I/O183 GX7	VCC															VCC	I/O80 K0	I/O77 J5	I/O75 J3	U
V	I/O182 GX6	N/C	I/O169 FX1	I/O172 FX4															I/O86 K6	I/O83 K3	I/O81 K1	I/O79 J7	V
W	I/O168 FX0	I/O170 FX2	I/O173 FX5	GND	I/O143 BX7	VCC	I/O150 CX6	I/O145 CX1	VCC	I/O153 DX1	I/O123 P3	VCC	I/O96 M0	VCC	I/O104 N0	I/O111 N7	VCC	I/O119 O7	GND	I/O87 K7	I/O84 K4	I/O82 K2	W
Y	I/O171 FX3	I/O174 FX6	GND	I/O141 BX5	I/O138 BX2	I/O136 BX0	I/O147 CX3	I/O158 DX6	I/O156 DX4	CLK2	I/O132 AX4	I/O121 P1	I/O125 P5	I/O99 M3	I/O101 M5	I/O106 N2	I/O110 N6	I/O115 O3	I/O118 O6	GND	TMS	I/O85 K5	Y
AA	I/O175 FX7	GND	I/O142 BX6	I/O140 BX4	I/O151 CX7	I/O149 CX5	I/O144 CX0	I/O157 DX5	I/O154 DX2	I/O134 AX6	I/O130 AX2	I/O128 AX0	CLK1	I/O127 P7	I/O100 M4	I/O103 M7	I/O108 N4	I/O109 N5	I/O113 O1	I/O116 O4	GND	TCK	AA
AB	GND	N/C	I/O139 BX3	I/O137 BX1	I/O148 CX4	I/O146 CX2	I/O159 DX7	I/O155 DX3	I/O135 AX7	I/O133 AX5	I/O129 AX1	I/O120 P0	I/O124 P4	I/O126 P6	I/O97 M1	I/O102 M6	I/O105 N1	I/O107 N3	I/O112 O0	I/O114 O2	I/O117 O5	GND	AB

#### PIN DESIGNATIONS

- CLK = Clock
- GND = Ground
- I = Input
- I/O = Input/Output
- N/C = No Connect
- VCC = Supply Voltage
- TDI = Test Data In
- TCK = Test Clock
- TMS = Test Mode Select
- TDO = Test Data Out



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