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Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details

Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	7.5 ns
Voltage Supply - Internal	3V ~ 3.6V
Number of Logic Elements/Blocks	-
Number of Macrocells	64
Number of Gates	-
Number of I/O	32
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.59x16.59)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/m4a3-64-32-7jni

Table 1. ispMACH 4A Device Features

3.3 V Devices								
Feature	M4A3-32	M4A3-64	M4A3-96	M4A3-128	M4A3-192	M4A3-256	M4A3-384	M4A3-512
Macrocells	32	64	96	128	192	256	384	512
User I/O options	32	32/64	48	64	96	128/160/192	160/192	160/192/256
t_{PD} (ns)	5.0	5.5	5.5	5.5	6.0	5.5	6.5	7.5
f_{CNT} (MHz)	182	167	167	167	160	167	154	125
t_{COS} (ns)	4.0	4.0	4.0	4.0	4.5	4.0	4.5	5.5
t_{SS} (ns)	3.0	3.5	3.5	3.5	3.5	3.5	3.5	5.0
Static Power (mA)	20	25/52	40	55	85	110/150	149/155	179
JTAG Compliant	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
PCI Compliant	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes

5 V Devices						
Feature	M4A5-32	M4A5-64	M4A5-96	M4A5-128	M4A5-192	M4A5-256
Macrocells	32	64	96	128	192	256
User I/O options	32	32	48	64	96	128
t_{PD} (ns)	5.0	5.5	5.5	5.5	6.0	6.5
f_{CNT} (MHz)	182	167	167	167	160	154
t_{COS} (ns)	4.0	4.0	4.0	4.0	4.5	5.0
t_{SS} (ns)	3.0	3.5	3.5	3.5	3.5	3.5
Static Power (mA)	20	25	40	55	74	110
JTAG Compliant	Yes	Yes	Yes	Yes	Yes	Yes
PCI Compliant	Yes	Yes	Yes	Yes	Yes	Yes

GENERAL DESCRIPTION

The ispMACH™ 4A family from Lattice offers an exceptionally flexible architecture and delivers a superior Complex Programmable Logic Device (CPLD) solution of easy-to-use silicon products and software tools. The overall benefits for users are a guaranteed and predictable CPLD solution, faster time-to-market, greater flexibility and lower cost. The ispMACH 4A devices offer densities ranging from 32 to 512 macrocells with 100% utilization and 100% pin-out retention. The ispMACH 4A families offer 5-V (M4A5-xxx) and 3.3-V (M4A3-xxx) operation.

ispMACH 4A products are 5-V or 3.3-V in-system programmable through the JTAG (IEEE Std. 1149.1) interface. JTAG boundary scan testing also allows product testability on automated test equipment for device connectivity.

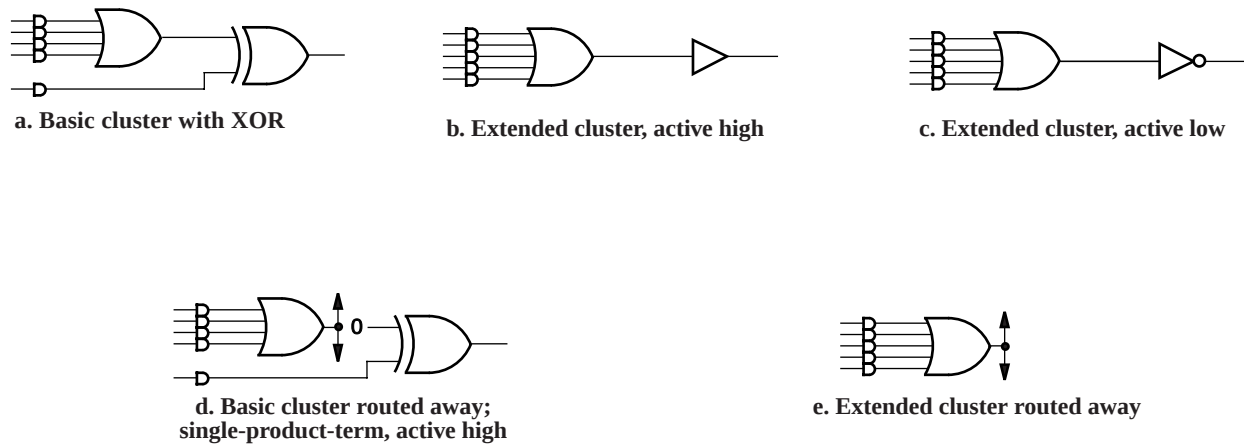
All ispMACH 4A family members deliver First-Time-Fit and easy system integration with pin-out retention after any design change and refit. For both 3.3-V and 5-V operation, ispMACH 4A products can deliver guaranteed fixed timing as fast as 5.0 ns t_{PD} and 182 MHz f_{CNT} through the SpeedLocking feature when using up to 20 product terms per output (Table 2).

Table 2. ispMACH 4A Speed Grades

Device	Speed Grade							
	-5	-55	-6	-65	-7	-10	-12	-14
M4A3-32 M4A5-32	C				C, I	C, I	I	
M4A3-64/32 M4A5-64/32		C			C, I	C, I	I	
M4A3-64/64		C			C, I	C, I	I	
M4A3-96 M4A5-96		C			C, I	C, I	I	
M4A3-128 M4A5-128		C			C, I	C, I	I	
M4A3-192 M4A5-192			C		C, I	C, I	I	
M4A3-256/128		C		C	C, I	C, I	I	
M4A5-256/128				C	C	C, I	I	
M4A3-256/192 M4A3-256/160					C	C, I	I	
M4A3-384				C		C, I	C, I	I
M4A3-512					C	C, I	C, I	I

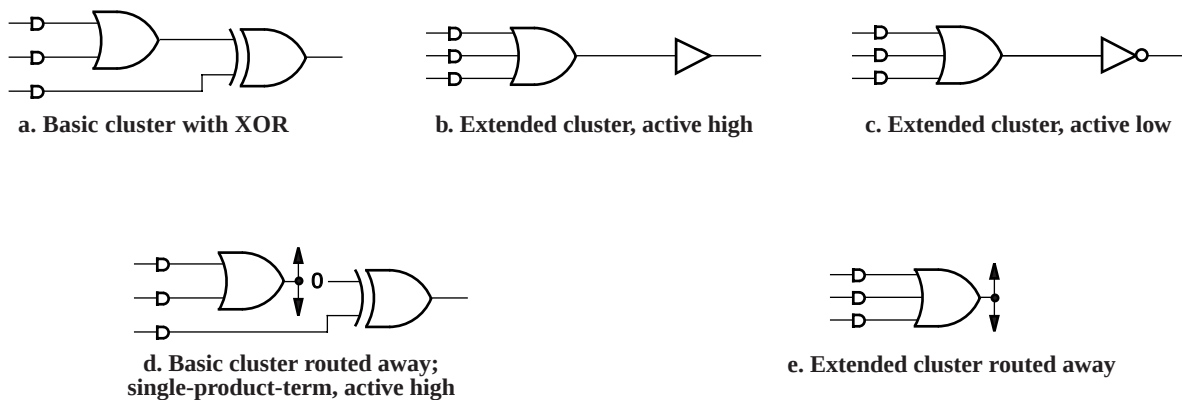
Note:

1. C = Commercial, I = Industrial



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Figure 3. Logic Allocator Configurations: Synchronous Mode



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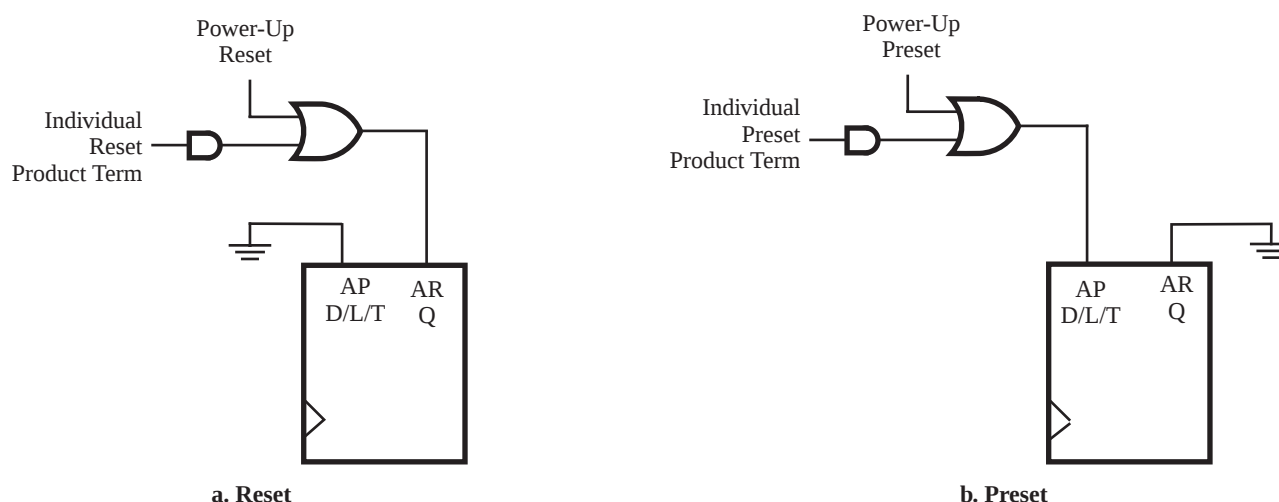
Figure 4. Logic Allocator Configurations: Asynchronous Mode

Note that the configuration of the logic allocator has absolutely no impact on the speed of the signal. All configurations have the same delay. This means that designers do not have to decide between optimizing resources or speed; both can be optimized.

If not used in the cluster, the extra product term can act in conjunction with the basic cluster to provide XOR logic for such functions as data comparison, or it can work with the D-,T-type flip-flop to provide for J-K, and S-R register operation. In addition, if the basic cluster is routed to another macrocell, the extra product term is still available for logic. In this case, the first XOR input will be a logic 0. This circuit has the flexibility to route product terms elsewhere without giving up the use of the macrocell.

Product term clusters do not “wrap” around a PAL block. This means that the macrocells at the ends of the block have fewer product terms available.

A reset/preset swapping feature in each macrocell allows for reset and preset to be exchanged, providing flexibility. In asynchronous mode (Figure 8), a single individual product term is provided for initialization. It can be selected to control reset or preset.



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Figure 8. Asynchronous Mode Initialization Configurations

Note that the reset/preset swapping selection feature effects power-up reset as well. The initialization functionality of the flip-flops is illustrated in Table 9. The macrocell sends its data to the output switch matrix and the input switch matrix. The output switch matrix can route this data to an output if so desired. The input switch matrix can send the signal back to the central switch matrix as feedback.

Table 9. Asynchronous Reset/Preset Operation

AR	AP	CLK/LE ¹	Q+
0	0	X	See Table 8
0	1	X	1
1	0	X	0
1	1	X	0

Note:

- Transparent latch is unaffected by AR, AP

Table 10. Output Switch Matrix Combinations for ispMACH 4A Devices with 2:1 Macrocell-I/O Cell Ratio

Macrocell	Routable to I/O Cells
M12, M13	I/O3, I/O4, I/O5, I/O6
M14, M15	I/O4, I/O5, I/O6, I/O7

I/O Cell	Available Macrocells
I/O0	M0, M1, M2, M3, M4, M5, M6, M7
I/O1	M2, M3, M4, M5, M6, M7, M8, M9
I/O2	M4, M5, M6, M7, M8, M9, M10, M11
I/O3	M6, M7, M8, M9, M10, M11, M12, M13
I/O4	M8, M9, M10, M11, M12, M13, M14, M15
I/O5	M0, M1, M10, M11, M12, M13, M14, M15
I/O6	M0, M1, M2, M3, M12, M13, M14, M15
I/O7	M0, M1, M2, M3, M4, M5, M14, M15

Table 11. Output Switch Matrix Combinations for M4A3-256/160 and M4A3-256/192

Macrocell	Routable to I/O Cells							
M0	I/O0	I/O1	I/O2	I/O3	I/O4	I/O5	I/O6	I/O7
M1	I/O0	I/O1	I/O2	I/O3	I/O4	I/O5	I/O6	I/O7
M2	I/O0	I/O1	I/O2	I/O3	I/O4	I/O5	I/O6	I/O7
M3	I/O0	I/O1	I/O2	I/O3	I/O4	I/O5	I/O6	I/O7
M4	I/O0	I/O1	I/O2	I/O3	I/O4	I/O5	I/O6	I/O7
M5	I/O0	I/O1	I/O2	I/O3	I/O4	I/O5	I/O6	I/O7
M6	I/O0	I/O1	I/O2	I/O3	I/O4	I/O5	I/O6	I/O7
M7	I/O0	I/O1	I/O2	I/O3	I/O4	I/O5	I/O6	I/O7
M8	I/O8	I/O9	I/O10	I/O11	I/O12	I/O13	I/O14	I/O15
M9	I/O8	I/O9	I/O10	I/O11	I/O12	I/O13	I/O14	I/O15
M10	I/O8	I/O9	I/O10	I/O11	I/O12	I/O13	I/O14	I/O15
M11	I/O8	I/O9	I/O10	I/O11	I/O12	I/O13	I/O14	I/O15
M12	I/O8	I/O9	I/O10	I/O11	I/O12	I/O13	I/O14	I/O15
M13	I/O8	I/O9	I/O10	I/O11	I/O12	I/O13	I/O14	I/O15
M14	I/O8	I/O9	I/O10	I/O11	I/O12	I/O13	I/O14	I/O15
M15	I/O8	I/O9	I/O10	I/O11	I/O12	I/O13	I/O14	I/O15

I/O Cell	Available Macrocells							
I/O0	M0	M1	M2	M3	M4	M5	M6	M7
I/O1	M0	M1	M2	M3	M4	M5	M6	M7
I/O2	M0	M1	M2	M3	M4	M5	M6	M7
I/O3	M0	M1	M2	M3	M4	M5	M6	M7
I/O4	M0	M1	M2	M3	M4	M5	M6	M7
I/O5	M0	M1	M2	M3	M4	M5	M6	M7
I/O6	M0	M1	M2	M3	M4	M5	M6	M7
I/O7	M0	M1	M2	M3	M4	M5	M6	M7

Table 11. Output Switch Matrix Combinations for M4A3-256/160 and M4A3-256/192

Macrocell	Routable to I/O Cells							
I/O8	M8	M9	M10	M11	M12	M13	M14	M15
I/O9	M8	M9	M10	M11	M12	M13	M14	M15
I/O10	M8	M9	M10	M11	M12	M13	M14	M15
I/O11	M8	M9	M10	M11	M12	M13	M14	M15
I/O12	M8	M9	M10	M11	M12	M13	M14	M15
I/O13	M8	M9	M10	M11	M12	M13	M14	M15
I/O14	M8	M9	M10	M11	M12	M13	M14	M15
I/O15	M8	M9	M10	M11	M12	M13	M14	M15

Table 12. Output Switch Matrix Combinations for M4A(3,5)-32/32

Macrocell	Routable to I/O Cells
M0, M1, M2, M3, M4, M5, M6, M7	I/O0, I/O1, I/O2, I/O3, I/O4, I/O5, I/O6, I/O7
M8, M9, M10, M11, M12, M13, M14, M15	I/O8, I/O9, I/O10, I/O11, I/O12, I/O13, I/O14, I/O15

I/O Cell	Available Macrocells
I/O0, I/O1, I/O2, I/O3, I/O4, I/O5, I/O6, I/O7	M0, M1, M2, M3, M4, M5, M6, M7
I/O8, I/O9, I/O10, I/O11, I/O12, I/O13, I/O14, I/O15	M8, M9, M10, M11, M12, M13, M14, M15

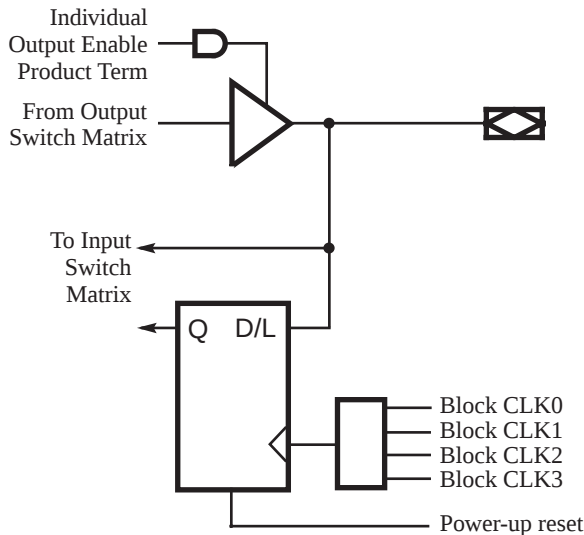
Table 13. Output Switch Matrix Combinations for M4A3-64/64

Macrocell	Routable to I/O Cells
M0, M1	I/O0, I/O1, I/O10, I/O11, I/O12, I/O13, I/O14, I/O15
M2, M3	I/O0, I/O1, I/O2, I/O3, I/O12, I/O13, I/O14, I/O15
M4, M5	I/O0, I/O1, I/O2, I/O3, I/O4, I/O5, I/O14, I/O15
M6, M7	I/O0, I/O1, I/O2, I/O3, I/O4, I/O5, I/O6, I/O7
M8, M9	I/O2, I/O3, I/O4, I/O5, I/O6, I/O7, I/O8, I/O9
M10, M11	I/O4, I/O5, I/O6, I/O7, I/O8, I/O9, I/O10, I/O11
M12, M13	I/O6, I/O7, I/O8, I/O9, I/O10, I/O11, I/O12, I/O13
M14, M15	I/O8, I/O9, I/O10, I/O11, I/O12, I/O13, I/O14, I/O15

I/O Cell	Available Macrocells
I/O0, I/O1	M0, M1, M2, M3, M4, M5, M6, M7
I/O2, I/O3	M2, M3, M4, M5, M6, M7, M8, M9
I/O4, I/O5	M4, M5, M6, M7, M8, M9, M10, M11
I/O6, I/O7	M6, M7, M8, M9, M10, M11, M12, M13
I/O8, I/O9	M8, M9, M10, M11, M12, M13, M14, M15
I/O10, I/O11	M0, M1, M10, M11, M12, M13, M14, M15
I/O12, I/O13	M0, M1, M2, M3, M12, M13, M14, M15
I/O14, I/O15	M0, M1, M2, M3, M4, M5, M14, M15

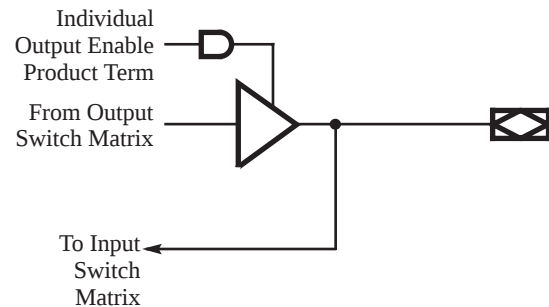
I/O Cell

The I/O cell (Figures 10 and 11) simply consists of a programmable output enable, a feedback path, and flip-flop (except ispMACH 4A devices with 1:1 macrocell-I/O cell ratio). An individual output enable product term is provided for each I/O cell. The feedback signal drives the input switch matrix.



17466G-017

Figure 10. I/O Cell for ispMACH 4A Devices with 2:1 Macrocell-I/O Cell Ratio



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Figure 11. I/O Cell for ispMACH 4A Devices with 1:1 Macrocell-I/O Cell Ratio

The I/O cell (Figure 10) contains a flip-flop, which provides the capability for storing the input in a D-type register or latch. The clock can be any of the PAL block clocks. Both the direct and registered versions of the input are sent to the input switch matrix. This allows for such functions as “time-domain-multiplexed” data comparison, where the first data value is stored, and then the second data value is put on the I/O pin and compared with the previous stored value.

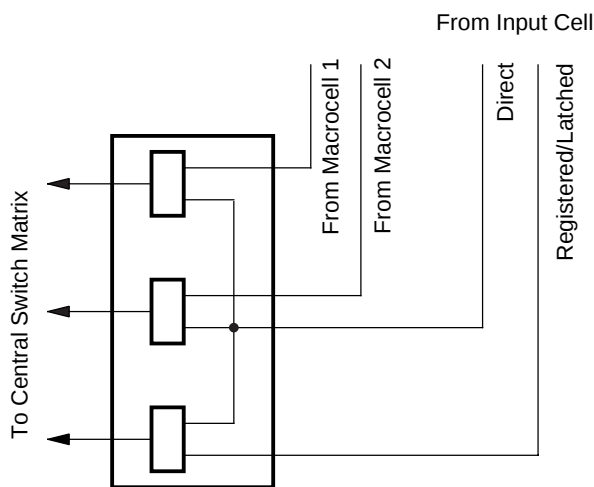
Note that the flip-flop used in the ispMACH 4A I/O cell is independent of the flip-flops in the macrocells. It powers up to a logic low.

Zero-Hold-Time Input Register

The ispMACH 4A devices have a zero-hold-time (ZHT) fuse which controls the time delay associated with loading data into all I/O cell registers and latches. When programmed, the ZHT fuse increases the data path setup delays to input storage elements, matching equivalent delays in the clock path. When the fuse is erased, the setup time to the input storage element is minimized. This feature facilitates doing worst-case designs for which data is loaded from sources which have low (or zero) minimum output propagation delays from clock edges.

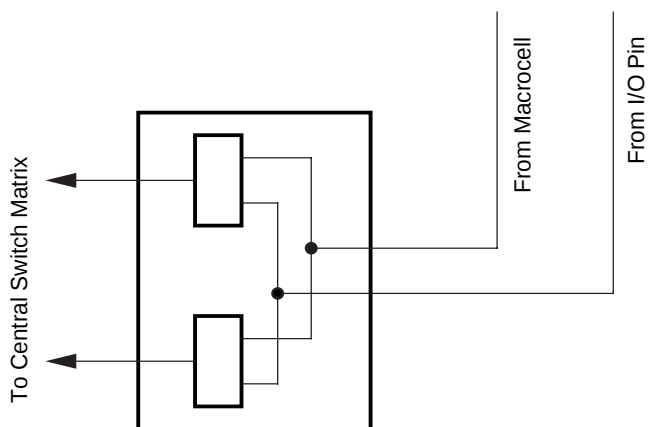
Input Switch Matrix

The input switch matrix (Figures 12 and 13) optimizes routing of inputs to the central switch matrix. Without the input switch matrix, each input and feedback signal has only one way to enter the central switch matrix. The input switch matrix provides additional ways for these signals to enter the central switch matrix.



17466G-002

Figure 12. ispMACH 4A with 2:1 Macrocell-I/O Cell Ratio - Input Switch Matrix



17466G-003

Figure 13. ispMACH 4A with 1:1 Macrocell-I/O Cell Ratio - Input Switch Matrix

IEEE 1149.1-COMPLIANT BOUNDARY SCAN TESTABILITY

All ispMACH 4A devices have boundary scan cells and are compliant to the IEEE 1149.1 standard. This allows functional testing of the circuit board on which the device is mounted through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test node data to be captured and shifted out for verification. In addition, these devices can be linked into a board-level serial scan path for more complete board-level testing.

IEEE 1149.1-COMPLIANT IN-SYSTEM PROGRAMMING

Programming devices in-system provides a number of significant benefits including: rapid prototyping, lower inventory levels, higher quality, and the ability to make in-field modifications. All ispMACH 4A devices provide In-System Programming (ISP) capability through their Boundary ScanTest Access Ports. This capability has been implemented in a manner that ensures that the port remains compliant to the IEEE 1149.1 standard. By using IEEE 1149.1 as the communication interface through which ISP is achieved, customers get the benefit of a standard, well-defined interface.

ispMACH 4A devices can be programmed across the commercial temperature and voltage range. The PC-based ispVM™ software facilitates in-system programming of ispMACH 4A devices. ispVM takes the JEDEC file output produced by the design implementation software, along with information about the JTAG chain, and creates a set of vectors that are used to drive the JTAG chain. ispVM software can use these vectors to drive a JTAG chain via the parallel port of a PC. Alternatively, ispVM software can output files in formats understood by common automated test equipment. This equipment can then be used to program ispMACH 4A devices during the testing of a circuit board.

PCI COMPLIANT

ispMACH 4A devices in the -5/-55/-6/-65/-7/-10/-12 speed grades are compliant with the *PCI Local Bus Specification* version 2.1, published by the PCI Special Interest Group (SIG). The 5-V devices are fully PCI-compliant. The 3.3-V devices are mostly compliant but do not meet the PCI condition to clamp the inputs as they rise above V_{CC} because of their 5-V input tolerant feature.

SAFE FOR MIXED SUPPLY VOLTAGE SYSTEM DESIGNS

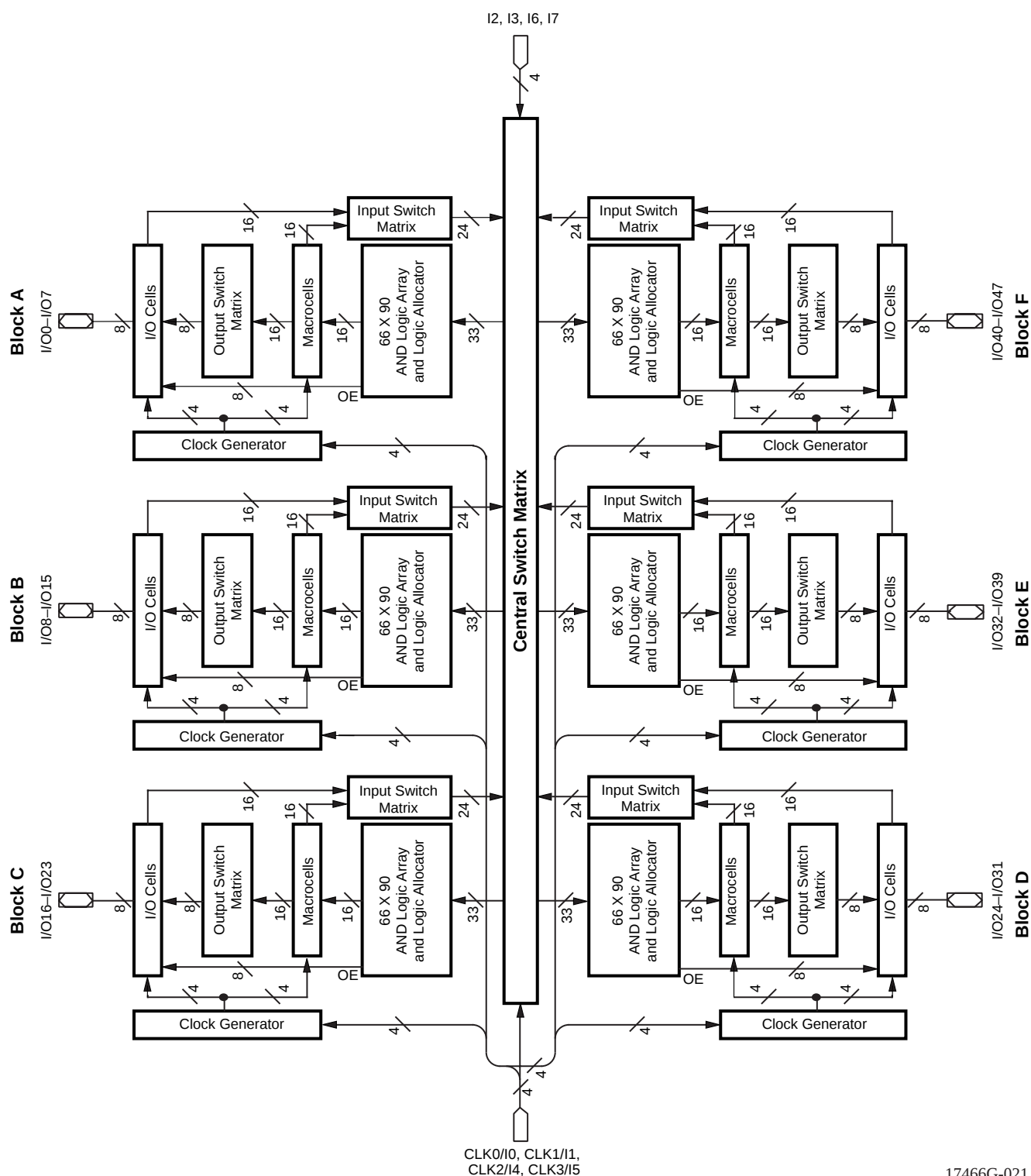
Both the 3.3-V and 5-V V_{CC} ispMACH 4A devices are safe for mixed supply voltage system designs. The 5-V devices will not overdrive 3.3-V devices above the output voltage of 3.3 V, while they accept inputs from other 3.3-V devices. The 3.3-V device will accept inputs up to 5.5 V. Both the 5-V and 3.3-V versions have the same high-speed performance and provide easy-to-use mixed-voltage design capability.

PULL UP OR BUS-FRIENDLY INPUTS AND I/Os

All ispMACH 4A devices have inputs and I/Os which feature the Bus-Friendly circuitry incorporating two inverters in series which loop back to the input. This double inversion weakly holds the input at its last driven logic state. While it is good design practice to tie unused pins to a known state, the Bus-Friendly input structure pulls pins away from the input threshold voltage where noise can cause high-frequency switching. At power-up, the Bus-Friendly latches are reset to a logic level “1.” For the circuit diagram, please refer to the document entitled *MACH Endurance Characteristics* on the Lattice Data Book CD-ROM or Lattice web site.

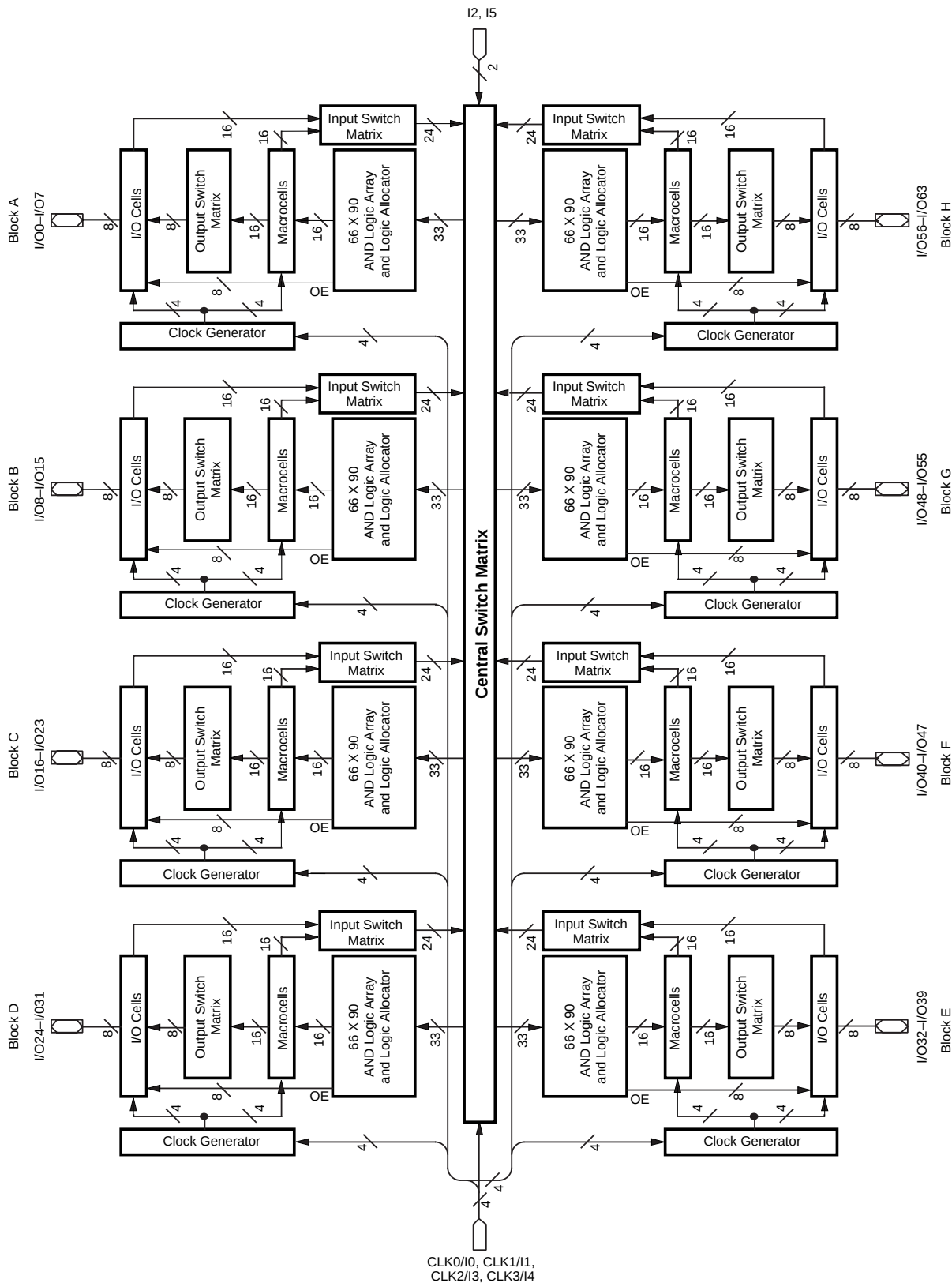
All ispMACH 4A devices have a programmable bit that configures all inputs and I/Os with either pull-up or Bus-Friendly characteristics. If the device is configured in pull-up mode, all inputs and I/O pins are

BLOCK DIAGRAM – M4A(3,5)-96/48



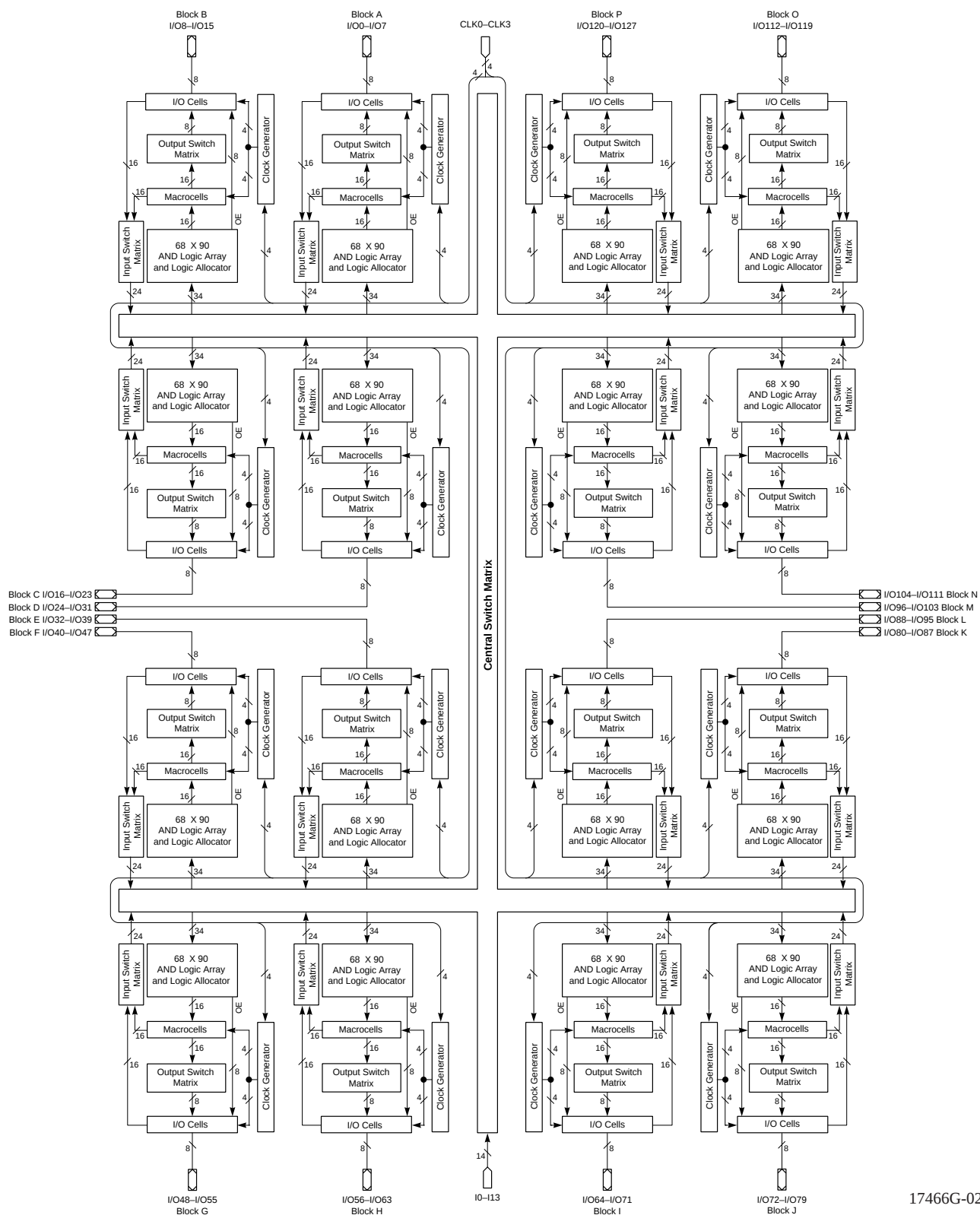
17466G-021

BLOCK DIAGRAM – M4A(3,5)-128/64



17466H-022

BLOCK DIAGRAM – M4A(3,5)-256/128



17466G-024

ABSOLUTE MAXIMUM RATINGS

M4A5

Storage Temperature. -65°C to +150°C
 Ambient Temperature
 with Power Applied. -55°C to +100°C
 Device Junction Temperature. +130°C
 Supply Voltage
 with Respect to Ground -0.5 V to +7.0 V
 DC Input Voltage -0.5 V to $V_{CC} + 0.5$ V
 Static Discharge Voltage 2000 V
 Latchup Current ($T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$) 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)
 Operating in Free Air. 0°C to $+70^\circ\text{C}$
 Supply Voltage (V_{CC})
 with Respect to Ground. +4.75 V to +5.25 V

Industrial (I) Devices

Ambient Temperature (T_A)
 Operating in Free Air. -40°C to $+85^\circ\text{C}$
 Supply Voltage (V_{CC})
 with Respect to Ground. +4.50 V to +5.5 V
Operating ranges define those limits between which the functionality of the device is guaranteed.

5-V DC CHARACTERISTICS OVER OPERATING RANGES

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	$I_{OH} = -3.2$ mA, $V_{CC} = \text{Min}$, $V_{IN} = V_{IH}$ or V_{IL}	2.4			V
		$I_{OH} = -100$ μA , $V_{CC} = \text{Max}$, $V_{IN} = V_{IH}$ or V_{IL}		3.3	3.6	V
V_{OL}	Output LOW Voltage	$I_{OL} = 24$ mA, $V_{CC} = \text{Min}$, $V_{IN} = V_{IH}$ or V_{IL} (Note 1)			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 2)	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 2)			0.8	V
I_{IH}	Input HIGH Leakage Current	$V_{IN} = 5.25$ V, $V_{CC} = \text{Max}$ (Note 3)			10	μA
I_{IL}	Input LOW Leakage Current	$V_{IN} = 0$ V, $V_{CC} = \text{Max}$ (Note 3)			-10	μA
I_{OZH}	Off-State Output Leakage Current HIGH	$V_{OUT} = 5.25$ V, $V_{CC} = \text{Max}$, $V_{IN} = V_{IH}$ or V_{IL} (Note 3)			10	μA
I_{OZL}	Off-State Output Leakage Current LOW	$V_{OUT} = 0$ V, $V_{CC} = \text{Max}$, $V_{IN} = V_{IH}$ or V_{IL} (Note 3)			-10	μA
I_{SC}	Output Short-Circuit Current	$V_{OUT} = 0.5$ V, $V_{CC} = \text{Max}$ (Note 4)	-30		-160	mA

Notes:

1. Total I_{OL} for one PAL block should not exceed 64 mA.
2. These are absolute values with respect to device ground, and all overshoots due to system or tester noise are included.
3. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
4. Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
 $V_{OUT} = 0.5$ V has been chosen to avoid test problems caused by tester ground degradation.

ispMACH 4A TIMING PARAMETERS OVER OPERATING RANGES¹

		-5		-55		-6		-65		-7		-10		-12		-14		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Frequency:																		
f _{MAXS}	External feedback, D-type, Min of 1/(t _{WLS} + t _{WHS}) or 1/(t _{SS} + t _{COS})	143		133		125		118		95.2		87.0		74.1		60.6		MHz
	External feedback, T-type, Min of 1/(t _{WLS} + t _{WHS}) or 1/(t _{SST} + t _{COS})	125		125		118		111		87.0		80.0		69.0		57.1		MHz
	Internal feedback (f _{CNT}), D-type, Min of 1/(t _{WLS} + t _{WHS}) or 1/(t _{SS} + t _{COSi})	182		167		160		154		125		118		95.0		74.1		MHz
	Internal feedback (f _{CNT}), T-type, Min of 1/(t _{WLS} + t _{WHS}) or 1/(t _{SST} + t _{COSi})	154		154		148		143		111		105		87.0		69.0		MHz
	No feedback ² , Min of 1/(t _{WLS} + t _{WHS}), 1/(t _{SS} + t _{HS}) or 1/(t _{SST} + t _{HS})	250		250		200		200		154		125		100		83.3		MHz
f _{MAXA}	External feedback, D-type, Min of 1/(t _{WLA} + t _{WHA}) or 1/(t _{SA} + t _{COA})	111		111		108		100		83.3		66.7		55.6		43.5		MHz
	External feedback, T-type, Min of 1/(t _{WLA} + t _{WHA}) or 1/(t _{SAT} + t _{COA})	105		105		102		95.2		76.9		62.5		52.6		41.7		MHz
	Internal feedback (f _{CNTA}), D-type, Min of 1/(t _{WLA} + t _{WHA}) or 1/(t _{SA} + t _{COAi})	133		133		125		125		105		83.3		66.7		50.0		MHz
	Internal feedback (f _{CNTA}), T-type, Min of 1/(t _{WLA} + t _{WHA}) or 1/(t _{SAT} + t _{COAi})	125		125		125		118		95.2		76.9		62.5		47.6		MHz
	No feedback ² , Min of 1/(t _{WLA} + t _{WHA}), 1/(t _{SA} + t _{HA}) or 1/(t _{SAT} + t _{HA})	167		167		143		143		125		100		62.5		55.6		MHz
f _{MAXI}	Maximum input register frequency, Min of 1/(t _{WIRH} + t _{WIRL}) or 1/(t _{SIRS} + t _{HIRS})	167		167		143		143		125		100		83.3		83.3		MHz

Notes:

- See "Switching Test Circuit" document on the Literature Download page of the Lattice web site.
- This parameter does not apply to flip-flops in the emulated mode since the feedback path is required for emulation.

CAPACITANCE¹

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input capacitance	$V_{IN}=2.0\text{ V}$	3.3 V or 5 V, 25°C, 1 MHz	6	pF
$C_{I/O}$	Output capacitance	$V_{OUT}=2.0\text{ V}$	3.3 V or 5 V, 25°C, 1 MHz	8	pF

Note:

- These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where this parameter may be affected.

I_{CC} vs. FREQUENCY

These curves represent the typical power consumption for a particular device at system frequency. The selected “typical” pattern is a 16-bit up-down counter. This pattern fills the device and exercises every macrocell. Maximum frequency shown uses internal feedback and a D-type register. Power/Speed are optimized to obtain the highest counter frequency and the lowest power. The highest frequency (LSBs) is placed in common PAL blocks, which are set to high power. The lowest frequency signals (MSBs) are placed in a common PAL block and set to lowest power.

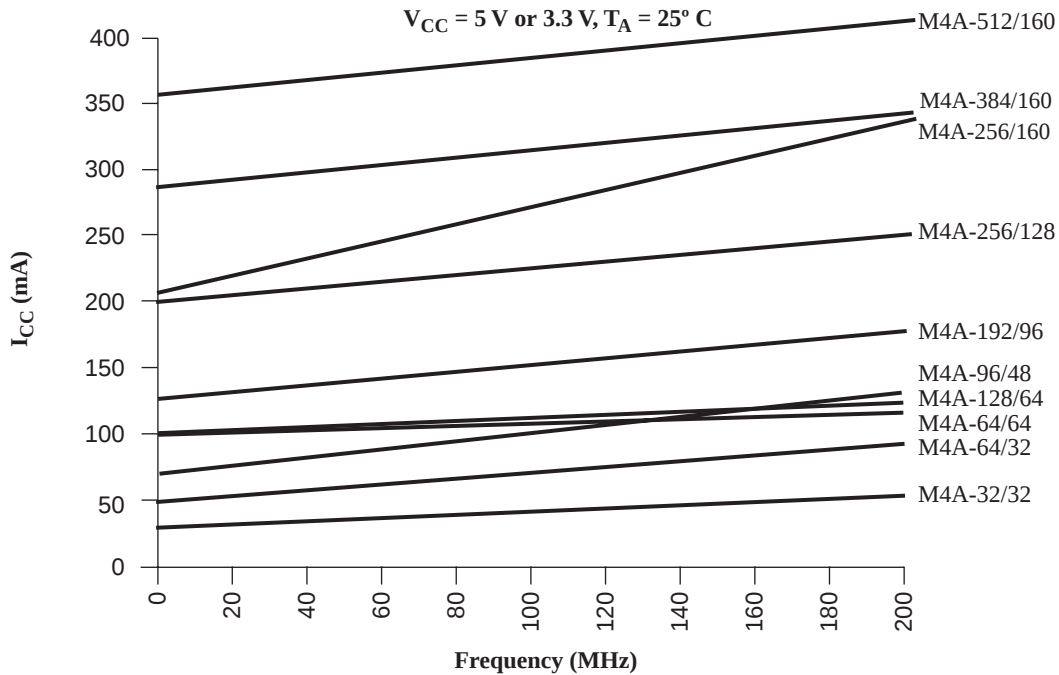


Figure 19. ispMACH 4A I_{CC} Curves at High Speed Mode

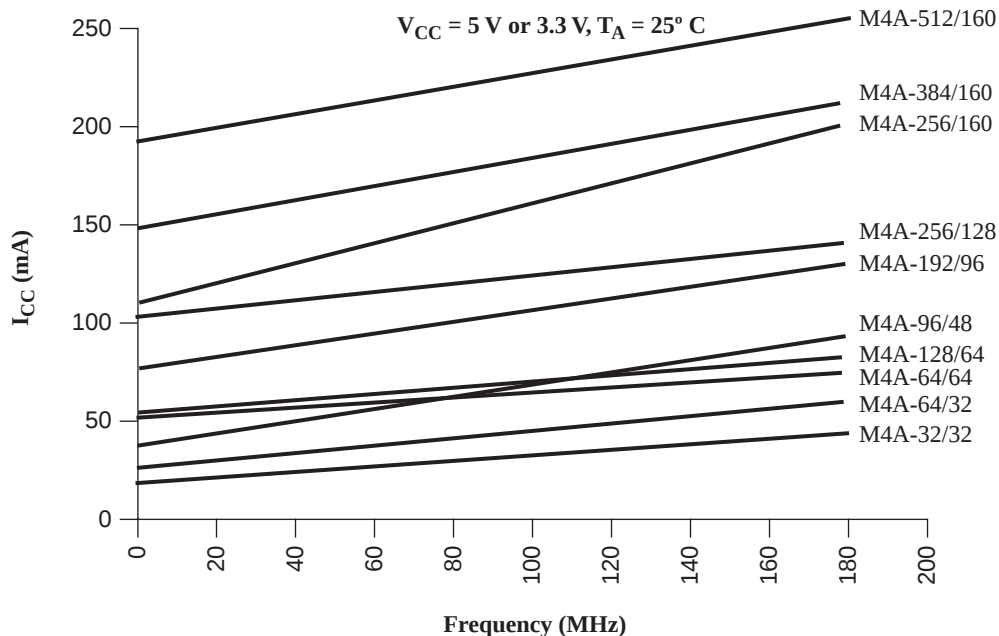
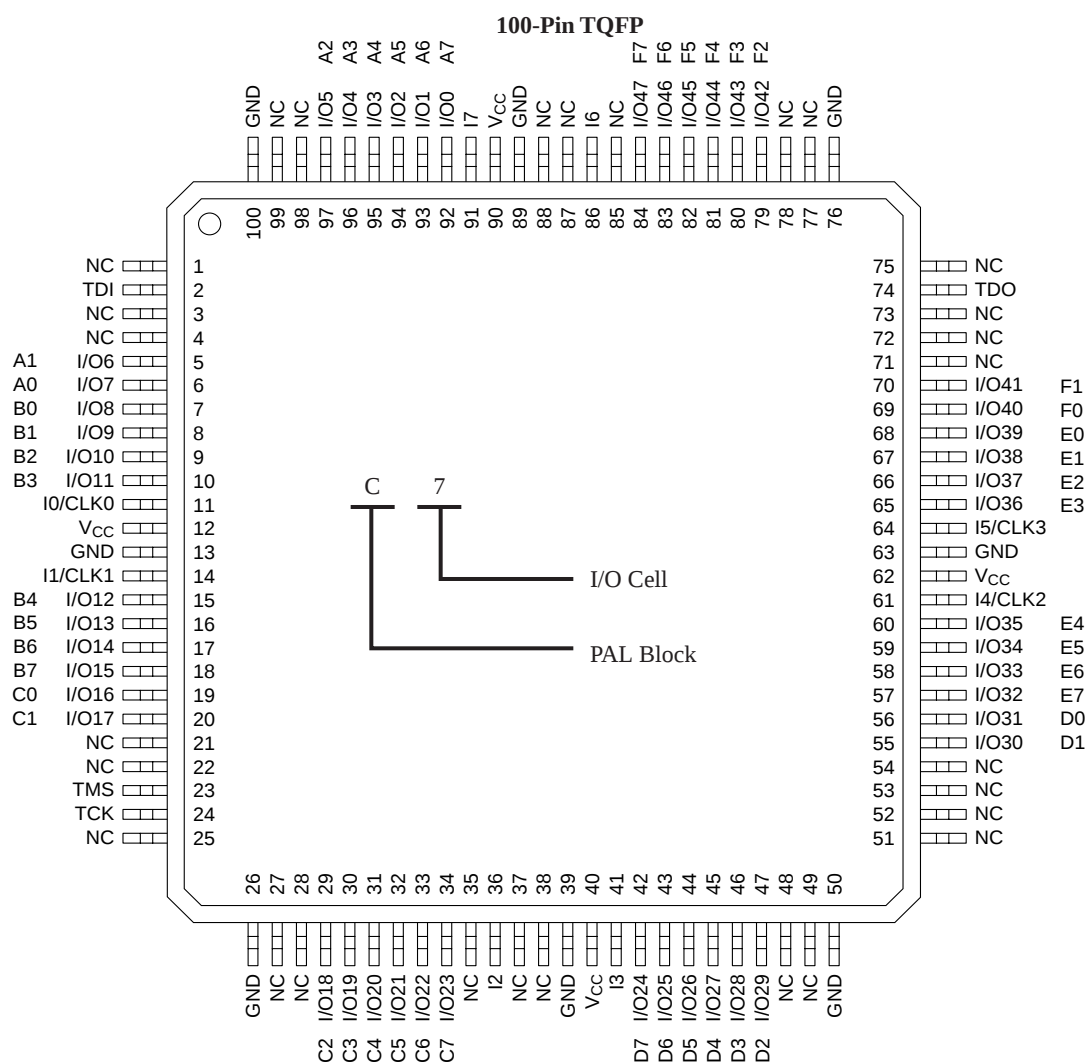


Figure 20. ispMACH 4A I_{CC} Curves at Low Power Mode

100-PIN TQFP CONNECTION DIAGRAM (M4A(3,5)-96/48)

Top View



PIN DESIGNATIONS

CLK/I = Clock or Input

GND = Ground

I = Input

I/O = Input/Output

V_{CC} = Supply Voltage

NC = No Connect

TDI = Test Data In

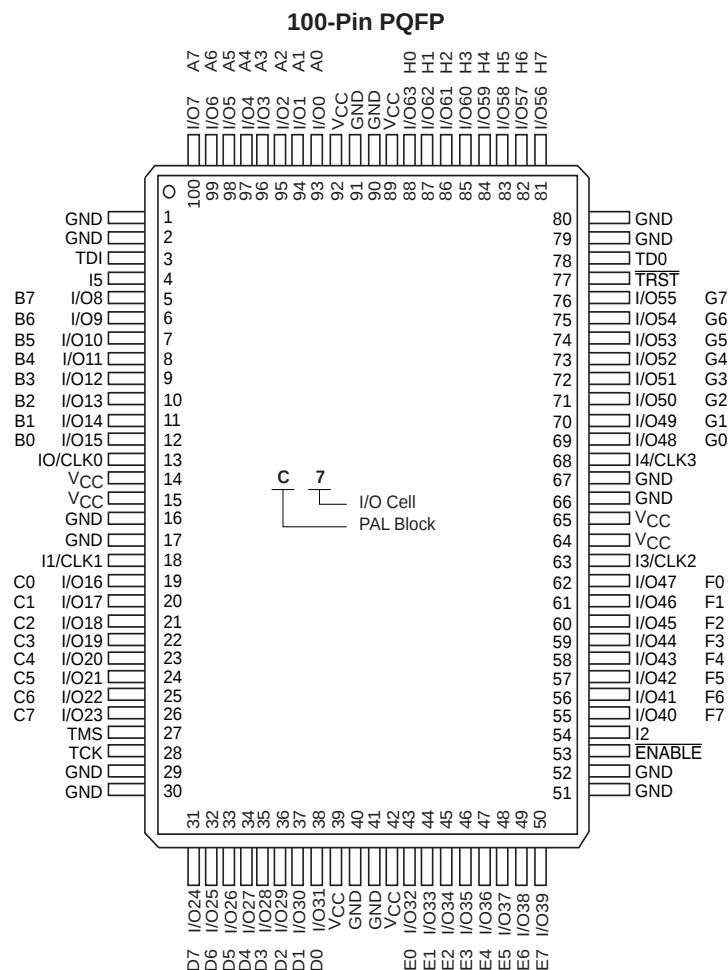
TCK = Test Clock

TMS = Test Mode Select

TDO = Test Data Out

100-PIN PQFP CONNECTION DIAGRAM (M4A(3,5)-128/64)

Top View



17466G-031

PIN DESIGNATIONS

I/CLK = Input or Clock

GND = Ground

I = Input

I/O = Input/Output

V_{CC} = Supply Voltage

TDI = Test Data In

TCK = Test Clock

TMS = Test Mode Select

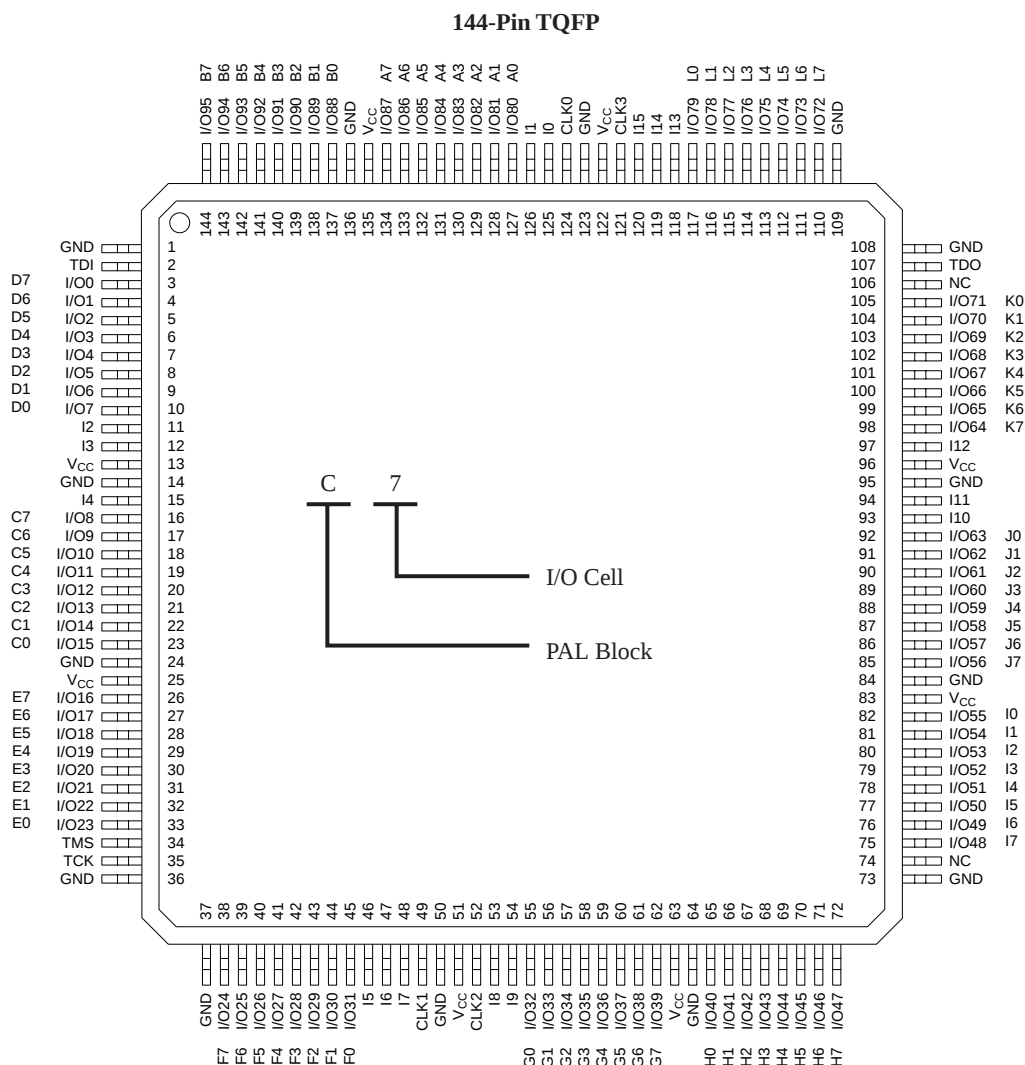
TDO = Test Data Out

TRST = Test Reset

ENABLE = Program

144-PIN TQFP CONNECTION DIAGRAM (M4A(3,5)-192/96)

Top View



256-BALL BGA CONNECTION DIAGRAM - (M4A3-384/192)

Bottom View

256-Ball BGA

	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	GND	I/O11 FX7	GND	I/O44 FX6	I/O58 CX6	GND	I/O70 CX2	I/O76 DX6	GND	GND	GND	GND	I/O108 AX5	I/O116 BX0	GND	I/O128 BX7	I/O134 O3	GND	GND	GND	A
B	GND	I/O12 GX7	I/O28 FX5	I/O45 FX3	I/O59 CX7	I/O64 CX5	I/O71 CX3	I/O77 DX7	I/O84 DX5	I/O90 DX2	I/O96 AX0	I/O102 AX3	I/O109 AX6	I/O117 BX1	I/O122 BX4	I/O129 BX6	I/O135 O4	I/O148 O6	I/O164 O7	GND	B
C	I/O0 GX6	I/O13 GX5	VCC	I/O46 FX4	I/O60 FX2	I/O65 FX1	I/O72 CX4	I/O78 CX0	I/O85 DX4	I/O91 DX1	I/O97 AX1	I/O103 AX4	I/O110 BX2	I/O118 BX5	I/O123 O0	I/O130 O1	I/O136 O5	VCC	I/O165 N7	I/O181 N6	C
D	I/O1 EX7	I/O14 GX3	I/O29 GX4	VCC	VCC	I/O66 FX0	VCC	I/O79 CX1	I/O86 DX3	I/O92 DX0	I/O98 AX2	I/O104 AX7	I/O111 BX3	VCC	I/O124 O2	VCC	VCC	I/O149 N4	I/O166 N5	I/O182 P7	D
E	I/O2 EX0	I/O15 GX0	I/O30 GX1	TDI	PIN DESIGNATIONS CLK = Clock GND = Ground I = Input I/O = Input/Output N/C = No Connect VCC = Supply Voltage TDI = Test Data In TCK = Test Clock TMS = Test Mode Select TDO = Test Data Out												TDO	I/O150 N2	I/O167 N3	I/O183 P6	E
F	GND	I/O16 EX1	I/O31 EX6	I/O47 GX2													I/O137 N1	I/O151 N0	I/O168 P5	GND	F
G	I/O3 HX6	I/O17 EX4	I/O32 EX5	VCC													VCC	I/O152 P4	I/O169 P3	I/O184 M7	G
H	GND	I/O18 HX5	I/O33 EX2	I/O48 EX3													I/O138 P2	I/O153 P1	I/O170 P0	GND	H
J	I/O4 HX0	I/O19 HX1	I/O34 HX4	I/O49 HX7													I/O139 M6	I/O154 M5	I/O171 M4	I/O185 M3	J
K	GND	CLK3	I/O35 HX2	I/O50 HX3													I/O140 M0	I/O155 M1	CLK2	I/O186 M2	K
L	I/O5 A2	CLK0	I/O36 A0	I/O51 A1													I/O141 L3	I/O156 L4	CLK1	GND	L
M	I/O6 A4	I/O20 A3	I/O37 A5	I/O52 A6													I/O142 L6	I/O157 L5	I/O172 L0	I/O187 L1	M
N	GND	I/O21 A7	I/O38 D0	I/O53 D1													I/O143 I5	I/O158 I0	I/O173 L7	GND	N
P	I/O7 D2	I/O22 D3	I/O39 D4	VCC													VCC	I/O159 I4	I/O174 I1	I/O188 L2	P
R	GND	I/O23 D5	I/O40 D6	I/O54 D7													I/O144 K5	I/O160 K0	I/O175 I3	GND	R
T	I/O8 B3	I/O24 B0	I/O41 B7	TCK													TMS	I/O161 K4	I/O176 K1	I/O189 I2	T
U	I/O9 B4	I/O25 B1	I/O42 B6	VCC	VCC	I/O67 C0	VCC	I/O80 F0	I/O87 E5	I/O93 E2	I/O99 H2	I/O105 H5	I/O112 G0	VCC	I/O125 J1	VCC	VCC	I/O162 K7	I/O177 K2	I/O190 I6	U
V	I/O10 B5	I/O26 B2	VCC	I/O55 C5	I/O61 C2	I/O68 C1	I/O73 F4	I/O81 F1	I/O88 E4	I/O94 E1	I/O100 H1	I/O106 H4	I/O113 G1	I/O119 G4	I/O126 J0	I/O131 J2	I/O145 J5	VCC	I/O178 K3	I/O191 I7	V
W	GND	I/O27 C7	I/O43 C6	I/O56 C3	I/O62 F7	I/O69 F5	I/O74 F3	I/O82 E7	I/O89 E3	I/O95 E0	I/O101 H0	I/O107 H3	I/O114 H7	I/O120 G3	I/O127 G5	I/O132 G7	I/O146 J4	I/O163 J6	I/O179 J7	GND	W
Y	GND	GND	GND	I/O57 C4	I/O63 F6	GND	I/O75 F2	I/O83 E6	GND	GND	GND	GND	I/O115 H6	I/O121 G2	GND	I/O133 G6	I/O147 J3	GND	I/O180 K6	GND	Y
	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

17466G-046

388-BALL fpBGA CONNECTION DIAGRAM (M4A3-512/256)

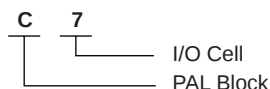
Bottom View

388-Ball fpBGA

	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	GND	I/O243 OX3	I/O240 OX0	I/O241 OX1	I/O236 NX4	I/O231 MX7	I/O228 MX4	I/O226 MX2	I/O255 PX7	I/O251 PX3	I/O248 PX0	I/O0 A0	I/O5 A5	I/O6 A6	I/O27 D3	I/O30 D6	I/O17 C1	I/O22 C6	I/O8 B0	I/O10 B2	N/C	GND	A
B	N/C	GND	I/O245 OX5	I/O242 OX2	I/O238 NX6	I/O234 NX2	I/O232 NX0	I/O229 MX5	I/O224 MX0	I/O253 PX5	I/O249 PX1	I/O2 A2	CLK0	I/O26 D2	I/O29 D5	I/O31 D7	I/O20 C4	I/O9 B1	I/O12 B4	I/O13 B5	GND	TDI	B
C	I/O213 KX5	TDO	GND	I/O247 OX7	I/O244 OX4	I/O239 NX7	I/O235 NX3	I/O230 MX6	I/O227 MX3	CLK3	I/O250 PX2	I/O1 A1	I/O7 A7	I/O25 D1	I/O16 C0	I/O18 C2	I/O23 C7	I/O11 B3	I/O15 B7	GND	I/O47 F7	I/O44 F4	C
D	I/O210 KX2	I/O212 KX4	I/O215 KX7	GND	I/O246 OX6	VCC	I/O237 NX5	I/O233 NX1	VCC	I/O254 PX6	VCC	I/O3 A3	I/O24 D0	VCC	I/O19 C3	I/O21 C5	VCC	I/O14 B6	GND	I/O46 F6	I/O43 F3	I/O41 F1	D
E	I/O207 JX7	I/O209 KX1	I/O211 KX3	I/O214 KX6															I/O45 F5	I/O42 F2	I/O40 F0	I/O54 G6	E
F	I/O203 JX3	I/O205 JX5	I/O208 KX0	VCC															VCC	I/O55 G7	I/O52 G4	I/O50 G2	F
G	I/O200 JX0	I/O202 JX2	I/O204 JX4	I/O206 JX6			VCC	VCC	N/C	I/O225 MX1	I/O252 PX4	I/O4 A4	I/O28 D4	N/C	VCC	VCC			I/O53 G5	I/O51 G3	I/O49 G1	I/O39 E7	G
H	I/O221 LX5	I/O222 LX6	I/O223 LX7	I/O201 JX1			VCC	N/C	GND	GND	GND	GND	GND	GND	N/C	VCC			I/O48 G0	I/O38 E6	I/O37 E5	I/O36 E4	H
J	I/O218 LX2	I/O219 LX3	I/O220 LX4	VCC			N/C	GND	GND	GND	GND	GND	GND	GND	GND	N/C			VCC	I/O35 E3	I/O34 E2	I/O32 E0	J
K	I/O197 IX5	I/O198 IX6	I/O199 IX7	I/O216 LX0			I/O217 LX1	GND	GND	GND	GND	GND	GND	GND	GND	I/O33 E1			I/O63 H7	I/O62 H6	I/O61 H5	I/O60 H4	K
L	I/O192 IX0	I/O194 IX2	I/O195 IX3	I/O196 IX4			I/O193 IX1	GND	GND	GND	GND	GND	GND	GND	GND	I/O58 H2			VCC	I/O59 H3	I/O57 H1	I/O56 H0	L
M	I/O184 HX0	I/O185 HX1	I/O187 HX3	VCC			I/O186 HX2	GND	GND	GND	GND	GND	GND	GND	GND	I/O69 I5			I/O67 I3	I/O65 I1	I/O66 I2	I/O64 I0	M
N	I/O188 HX4	I/O189 HX5	I/O191 HX7	I/O190 HX6			I/O162 EX2	GND	GND	GND	GND	GND	GND	GND	GND	I/O89 L1			I/O88 L0	I/O71 I7	I/O70 I6	I/O68 I4	N
P	I/O160 EX0	I/O161 EX1	I/O163 EX3	VCC			N/C	GND	GND	GND	GND	GND	GND	GND	GND	N/C			VCC	I/O92 L4	I/O91 L3	I/O90 L2	P
R	I/O164 EX4	I/O165 EX5	I/O166 EX6	I/O177 GX1			VCC	N/C	GND	GND	GND	GND	GND	GND	N/C	VCC			I/O74 J2	I/O95 L7	I/O94 L6	I/O93 L5	R
T	I/O167 EX7	I/O176 GX0	I/O179 GX3	I/O181 GX5			VCC	VCC	N/C	I/O152 DX0	I/O131 AX3	I/O122 P2	I/O98 M2	N/C	VCC	VCC			I/O78 J6	I/O76 J4	I/O73 J1	I/O72 J0	T
U	I/O178 GX2	I/O180 GX4	I/O183 GX7	VCC															VCC	I/O80 K0	I/O77 J5	I/O75 J3	U
V	I/O182 GX6	N/C	I/O169 FX1	I/O172 FX4															I/O86 K6	I/O83 K3	I/O81 K1	I/O79 J7	V
W	I/O168 FX0	I/O170 FX2	I/O173 FX5	GND	I/O143 BX7	VCC	I/O150 CX6	I/O145 CX1	VCC	I/O153 DX1	I/O123 P3	VCC	I/O96 M0	VCC	I/O104 N0	I/O111 N7	VCC	I/O119 O7	GND	I/O87 K7	I/O84 K4	I/O82 K2	W
Y	I/O171 FX3	I/O174 FX6	GND	I/O141 BX5	I/O138 BX2	I/O136 BX0	I/O147 CX3	I/O158 DX6	I/O156 DX4	CLK2	I/O132 AX4	I/O121 P1	I/O125 P5	I/O99 M3	I/O101 M5	I/O106 N2	I/O110 N6	I/O115 O3	I/O118 O6	GND	TMS	I/O85 K5	Y
AA	I/O175 FX7	GND	I/O142 BX6	I/O140 BX4	I/O151 CX7	I/O149 CX5	I/O144 CX0	I/O157 DX5	I/O154 DX2	I/O134 AX6	I/O130 AX2	I/O128 AX0	CLK1	I/O127 P7	I/O100 M4	I/O103 M7	I/O108 N4	I/O109 N5	I/O113 O1	I/O116 O4	GND	TCK	AA
AB	GND	N/C	I/O139 BX3	I/O137 BX1	I/O148 CX4	I/O146 CX2	I/O159 DX7	I/O155 DX3	I/O135 AX7	I/O133 AX5	I/O129 AX1	I/O120 P0	I/O124 P4	I/O126 P6	I/O97 M1	I/O102 M6	I/O105 N1	I/O107 N3	I/O112 O0	I/O114 O2	I/O117 O5	GND	AB

PIN DESIGNATIONS

CLK = Clock
 GND = Ground
 I = Input
 I/O = Input/Output
 N/C = No Connect
 VCC = Supply Voltage
 TDI = Test Data In
 TCK = Test Clock
 TMS = Test Mode Select
 TDO = Test Data Out



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