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Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details

Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	7.5 ns
Voltage Supply - Internal	3V ~ 3.6V
Number of Logic Elements/Blocks	-
Number of Macrocells	64
Number of Gates	-
Number of I/O	32
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/m4a3-64-32-7vc

GENERAL DESCRIPTION

The ispMACH™ 4A family from Lattice offers an exceptionally flexible architecture and delivers a superior Complex Programmable Logic Device (CPLD) solution of easy-to-use silicon products and software tools. The overall benefits for users are a guaranteed and predictable CPLD solution, faster time-to-market, greater flexibility and lower cost. The ispMACH 4A devices offer densities ranging from 32 to 512 macrocells with 100% utilization and 100% pin-out retention. The ispMACH 4A families offer 5-V (M4A5-xxx) and 3.3-V (M4A3-xxx) operation.

ispMACH 4A products are 5-V or 3.3-V in-system programmable through the JTAG (IEEE Std. 1149.1) interface. JTAG boundary scan testing also allows product testability on automated test equipment for device connectivity.

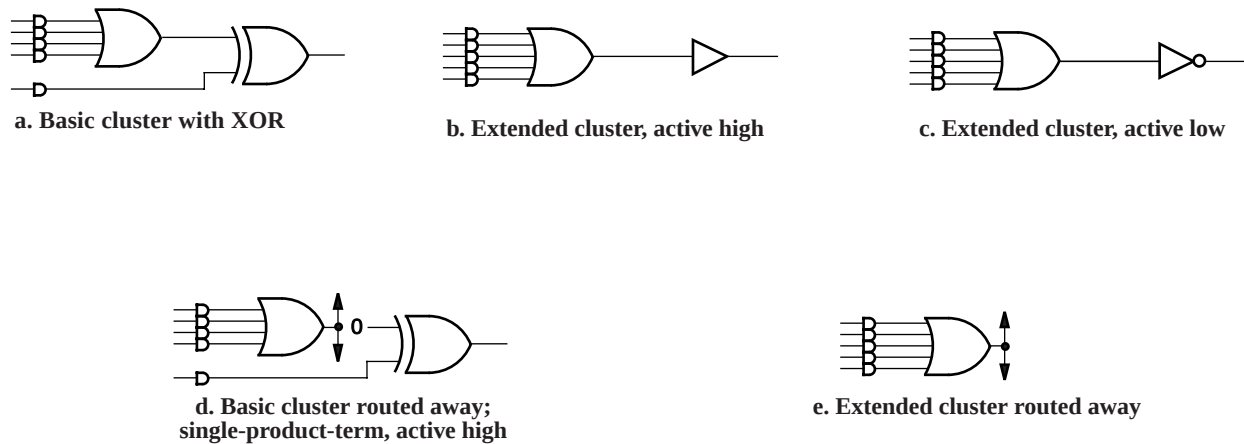
All ispMACH 4A family members deliver First-Time-Fit and easy system integration with pin-out retention after any design change and refit. For both 3.3-V and 5-V operation, ispMACH 4A products can deliver guaranteed fixed timing as fast as 5.0 ns t_{PD} and 182 MHz f_{CNT} through the SpeedLocking feature when using up to 20 product terms per output (Table 2).

Table 2. ispMACH 4A Speed Grades

Device	Speed Grade							
	-5	-55	-6	-65	-7	-10	-12	-14
M4A3-32 M4A5-32	C				C, I	C, I	I	
M4A3-64/32 M4A5-64/32		C			C, I	C, I	I	
M4A3-64/64		C			C, I	C, I	I	
M4A3-96 M4A5-96		C			C, I	C, I	I	
M4A3-128 M4A5-128		C			C, I	C, I	I	
M4A3-192 M4A5-192			C		C, I	C, I	I	
M4A3-256/128		C		C	C, I	C, I	I	
M4A5-256/128				C	C	C, I	I	
M4A3-256/192 M4A3-256/160					C	C, I	I	
M4A3-384				C		C, I	C, I	I
M4A3-512					C	C, I	C, I	I

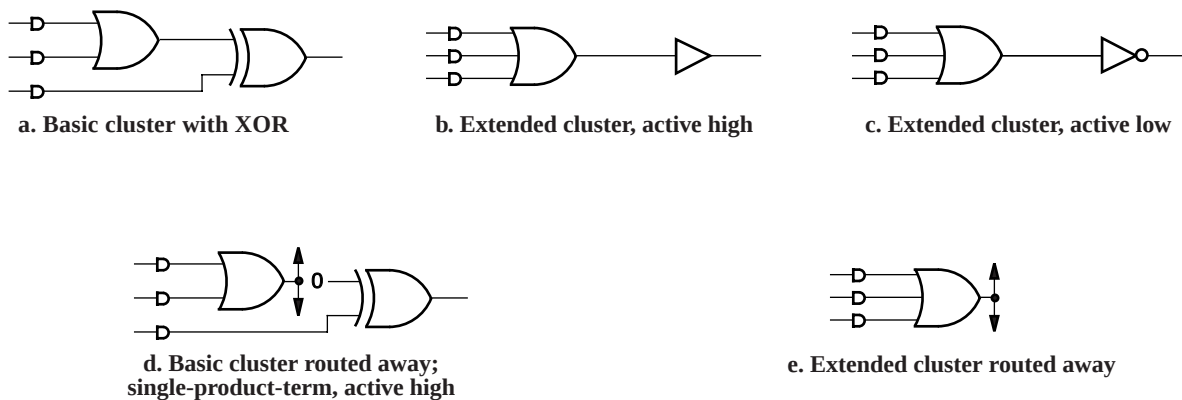
Note:

1. C = Commercial, I = Industrial



17466G-007

Figure 3. Logic Allocator Configurations: Synchronous Mode



17466G-008

Figure 4. Logic Allocator Configurations: Asynchronous Mode

Note that the configuration of the logic allocator has absolutely no impact on the speed of the signal. All configurations have the same delay. This means that designers do not have to decide between optimizing resources or speed; both can be optimized.

If not used in the cluster, the extra product term can act in conjunction with the basic cluster to provide XOR logic for such functions as data comparison, or it can work with the D-,T-type flip-flop to provide for J-K, and S-R register operation. In addition, if the basic cluster is routed to another macrocell, the extra product term is still available for logic. In this case, the first XOR input will be a logic 0. This circuit has the flexibility to route product terms elsewhere without giving up the use of the macrocell.

Product term clusters do not “wrap” around a PAL block. This means that the macrocells at the ends of the block have fewer product terms available.

Table 11. Output Switch Matrix Combinations for M4A3-256/160 and M4A3-256/192

Macrocell	Routable to I/O Cells							
I/O8	M8	M9	M10	M11	M12	M13	M14	M15
I/O9	M8	M9	M10	M11	M12	M13	M14	M15
I/O10	M8	M9	M10	M11	M12	M13	M14	M15
I/O11	M8	M9	M10	M11	M12	M13	M14	M15
I/O12	M8	M9	M10	M11	M12	M13	M14	M15
I/O13	M8	M9	M10	M11	M12	M13	M14	M15
I/O14	M8	M9	M10	M11	M12	M13	M14	M15
I/O15	M8	M9	M10	M11	M12	M13	M14	M15

Table 12. Output Switch Matrix Combinations for M4A(3,5)-32/32

Macrocell	Routable to I/O Cells
M0, M1, M2, M3, M4, M5, M6, M7	I/O0, I/O1, I/O2, I/O3, I/O4, I/O5, I/O6, I/O7
M8, M9, M10, M11, M12, M13, M14, M15	I/O8, I/O9, I/O10, I/O11, I/O12, I/O13, I/O14, I/O15

I/O Cell	Available Macrocells
I/O0, I/O1, I/O2, I/O3, I/O4, I/O5, I/O6, I/O7	M0, M1, M2, M3, M4, M5, M6, M7
I/O8, I/O9, I/O10, I/O11, I/O12, I/O13, I/O14, I/O15	M8, M9, M10, M11, M12, M13, M14, M15

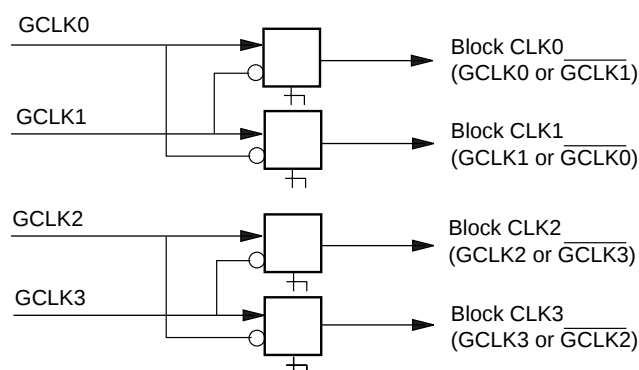
Table 13. Output Switch Matrix Combinations for M4A3-64/64

Macrocell	Routable to I/O Cells
M0, M1	I/O0, I/O1, I/O10, I/O11, I/O12, I/O13, I/O14, I/O15
M2, M3	I/O0, I/O1, I/O2, I/O3, I/O12, I/O13, I/O14, I/O15
M4, M5	I/O0, I/O1, I/O2, I/O3, I/O4, I/O5, I/O14, I/O15
M6, M7	I/O0, I/O1, I/O2, I/O3, I/O4, I/O5, I/O6, I/O7
M8, M9	I/O2, I/O3, I/O4, I/O5, I/O6, I/O7, I/O8, I/O9
M10, M11	I/O4, I/O5, I/O6, I/O7, I/O8, I/O9, I/O10, I/O11
M12, M13	I/O6, I/O7, I/O8, I/O9, I/O10, I/O11, I/O12, I/O13
M14, M15	I/O8, I/O9, I/O10, I/O11, I/O12, I/O13, I/O14, I/O15

I/O Cell	Available Macrocells
I/O0, I/O1	M0, M1, M2, M3, M4, M5, M6, M7
I/O2, I/O3	M2, M3, M4, M5, M6, M7, M8, M9
I/O4, I/O5	M4, M5, M6, M7, M8, M9, M10, M11
I/O6, I/O7	M6, M7, M8, M9, M10, M11, M12, M13
I/O8, I/O9	M8, M9, M10, M11, M12, M13, M14, M15
I/O10, I/O11	M0, M1, M10, M11, M12, M13, M14, M15
I/O12, I/O13	M0, M1, M2, M3, M12, M13, M14, M15
I/O14, I/O15	M0, M1, M2, M3, M4, M5, M14, M15

PAL Block Clock Generation

Each ispMACH 4A device has four clock pins that can also be used as inputs. These pins drive a clock generator in each PAL block (Figure 14). The clock generator provides four clock signals that can be used anywhere in the PAL block. These four PAL block clock signals can consist of a large number of combinations of the true and complement edges of the global clock signals. Table 14 lists the possible combinations.



17466G-004

Figure 14. PAL Block Clock Generator¹

1. M4A(3,5)-32/32 and M4A(3,5)-64/32 have only two clock pins, GCLK0 and GCLK1. GCLK2 is tied to GCLK0, and GCLK3 is tied to GCLK1.

Table 14. PAL Block Clock Combinations¹

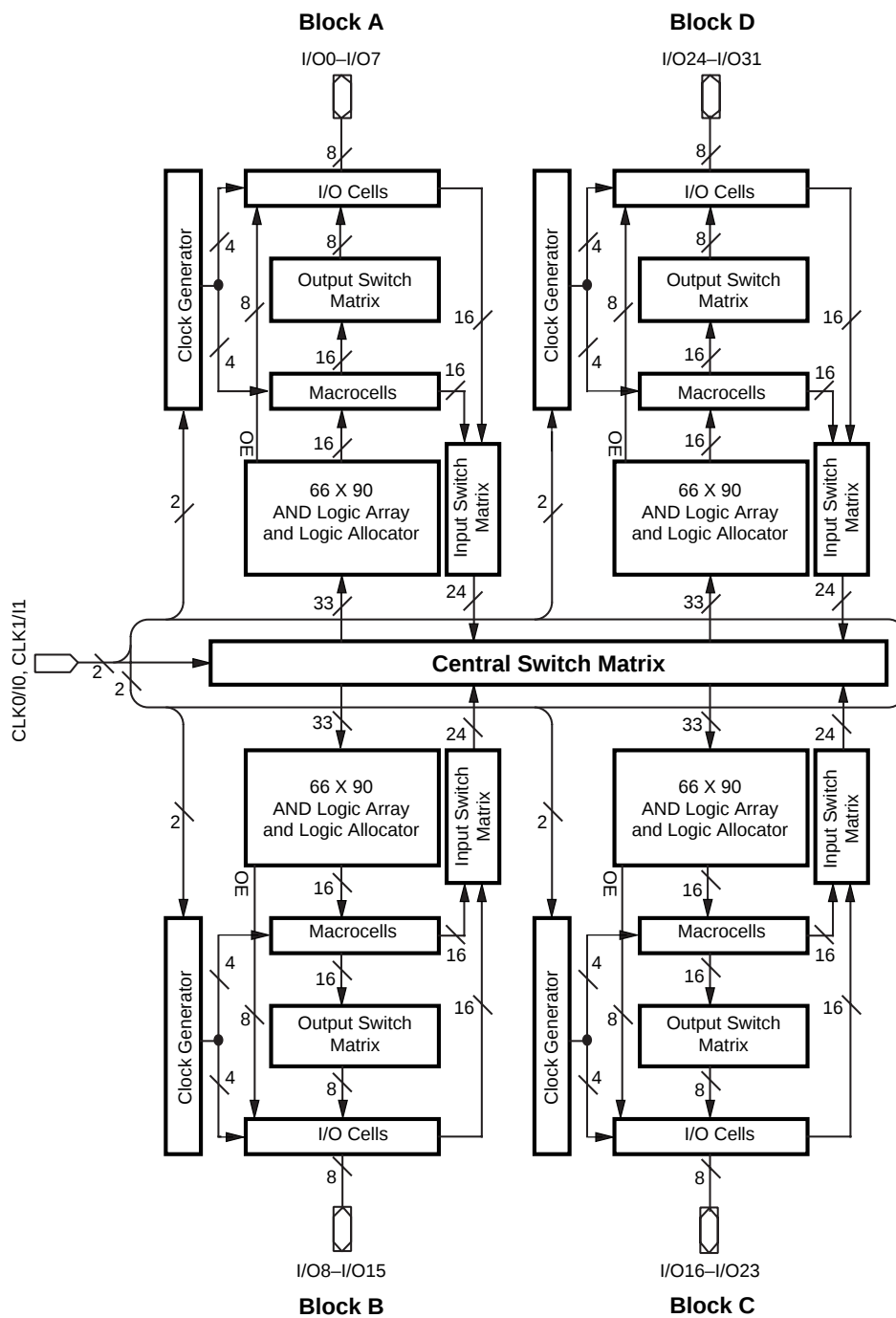
Block CLK0	Block CLK1	Block CLK2	Block CLK3
GCLK0	GCLK1	X	X
$\overline{\text{GCLK1}}$	GCLK1	X	X
GCLK0	$\overline{\text{GCLK0}}$	X	X
$\overline{\text{GCLK1}}$	$\overline{\text{GCLK0}}$	X	X
X	X	GCLK2 (GCLK0)	GCLK3 (GCLK1)
X	X	$\overline{\text{GCLK3}}$ ($\overline{\text{GCLK1}}$)	GCLK3 (GCLK1)
X	X	GCLK2 (GCLK0)	$\overline{\text{GCLK2}}$ ($\overline{\text{GCLK0}}$)
X	X	$\overline{\text{GCLK3}}$ (GCLK1)	$\overline{\text{GCLK2}}$ ($\overline{\text{GCLK0}}$)

Note:

1. Values in parentheses are for the M4A(3,5)-32/32 and M4A(3,5)-64/32.

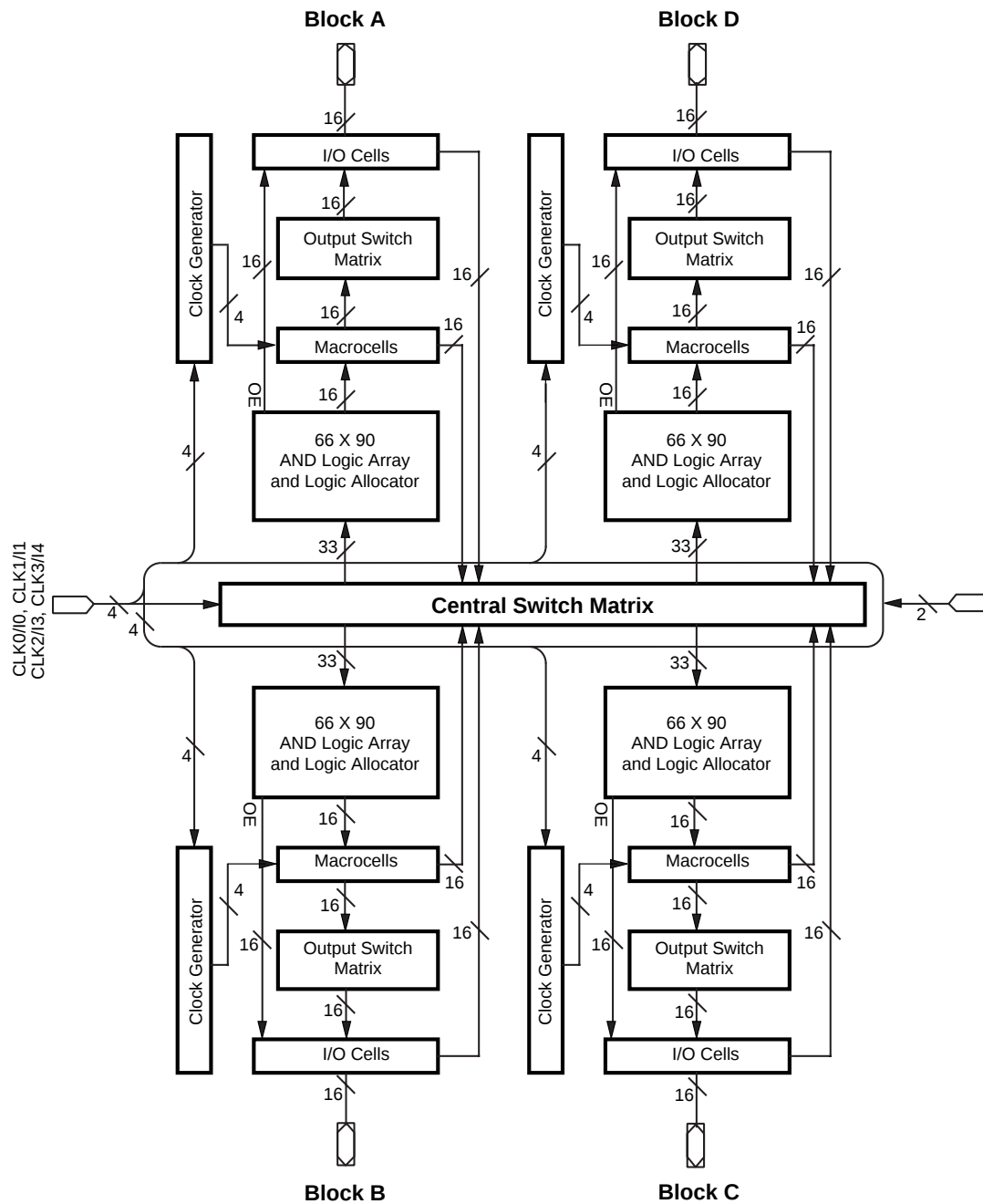
This feature provides high flexibility for partitioning state machines and dual-phase clocks. It also allows latches to be driven with either polarity of latch enable, and in a master-slave configuration.

BLOCK DIAGRAM – M4A(3,5)-64/32



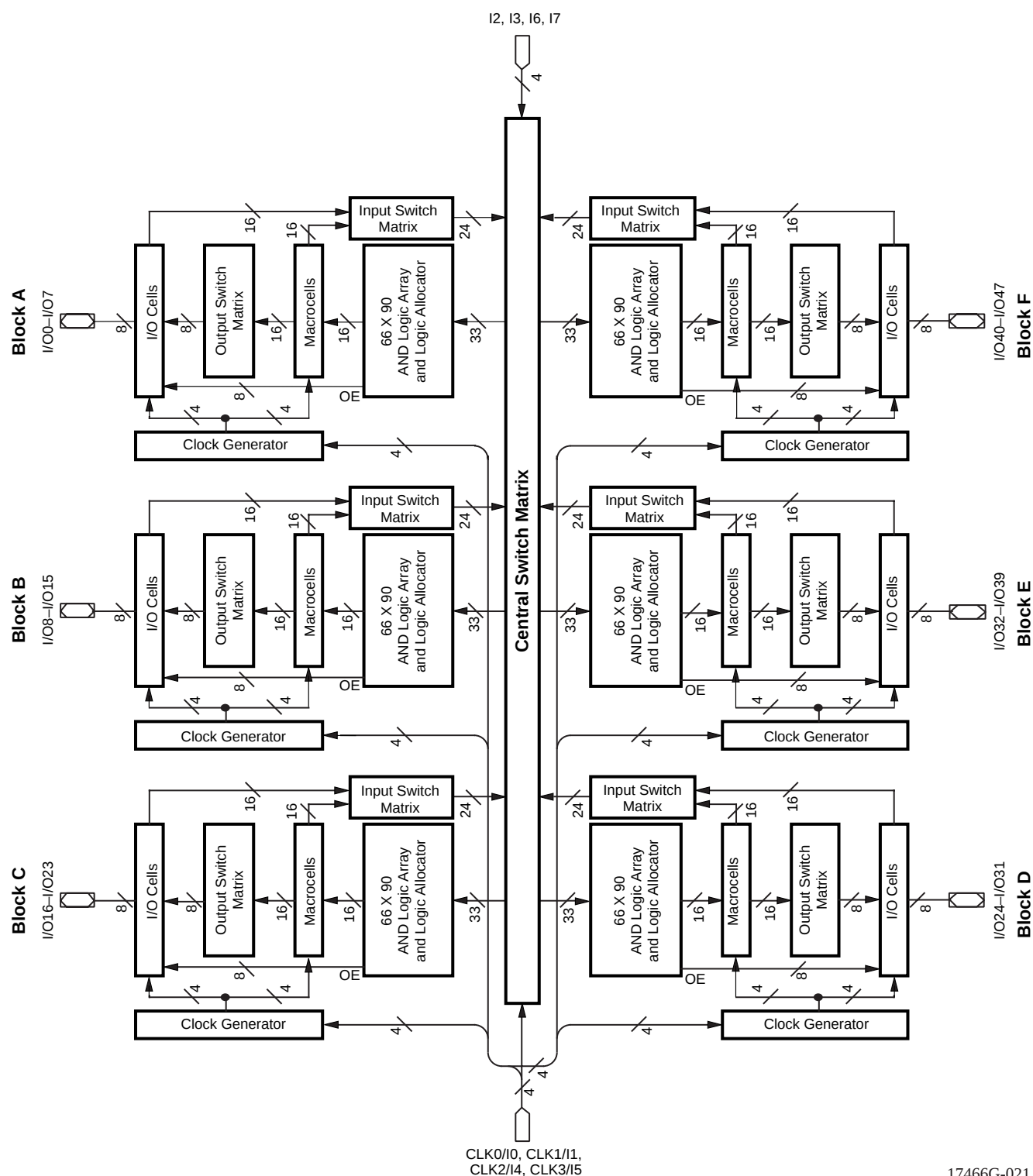
17466H-020

BLOCK DIAGRAM – M4A3-64/64



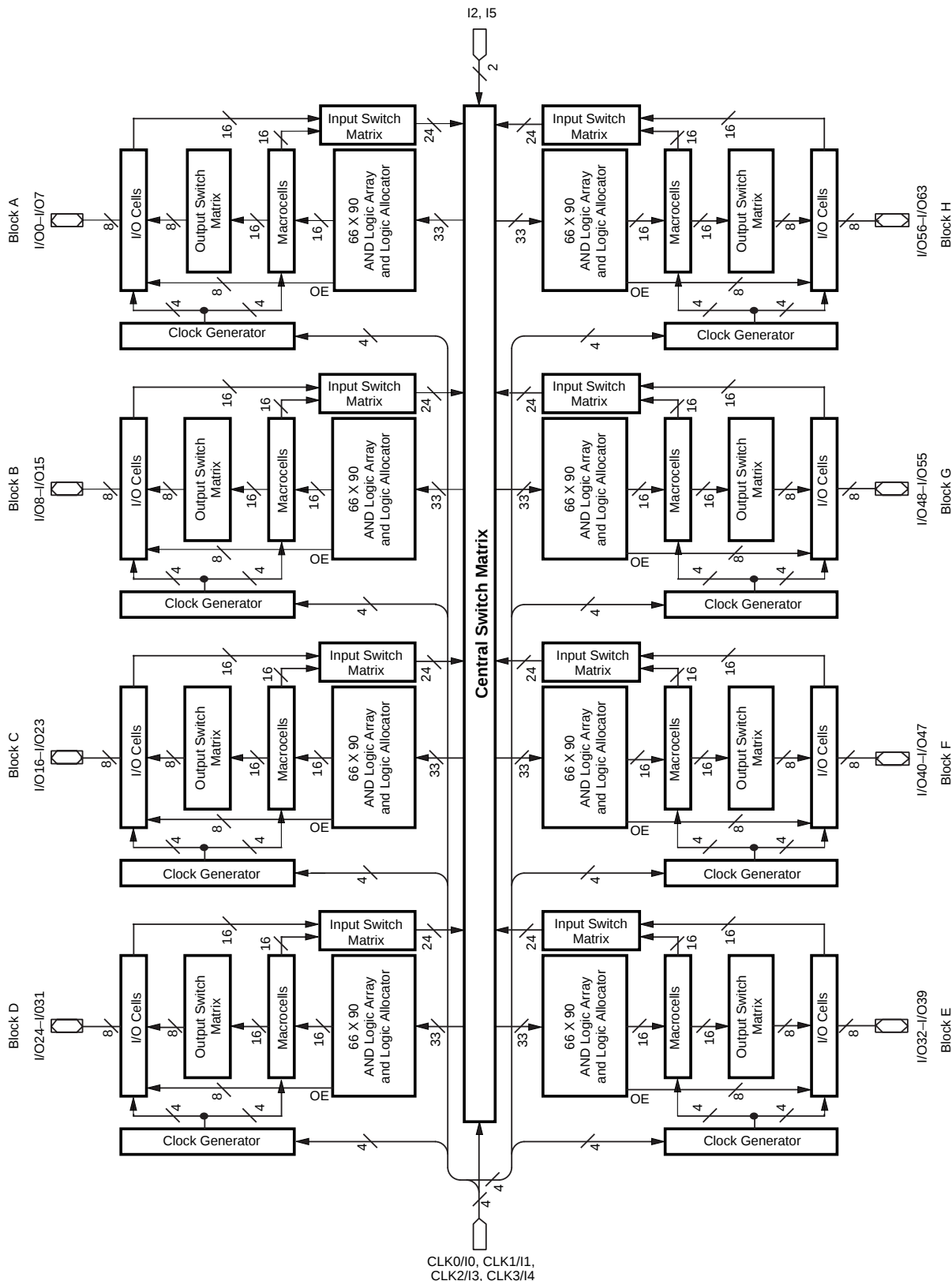
17466H-020A

BLOCK DIAGRAM – M4A(3,5)-96/48



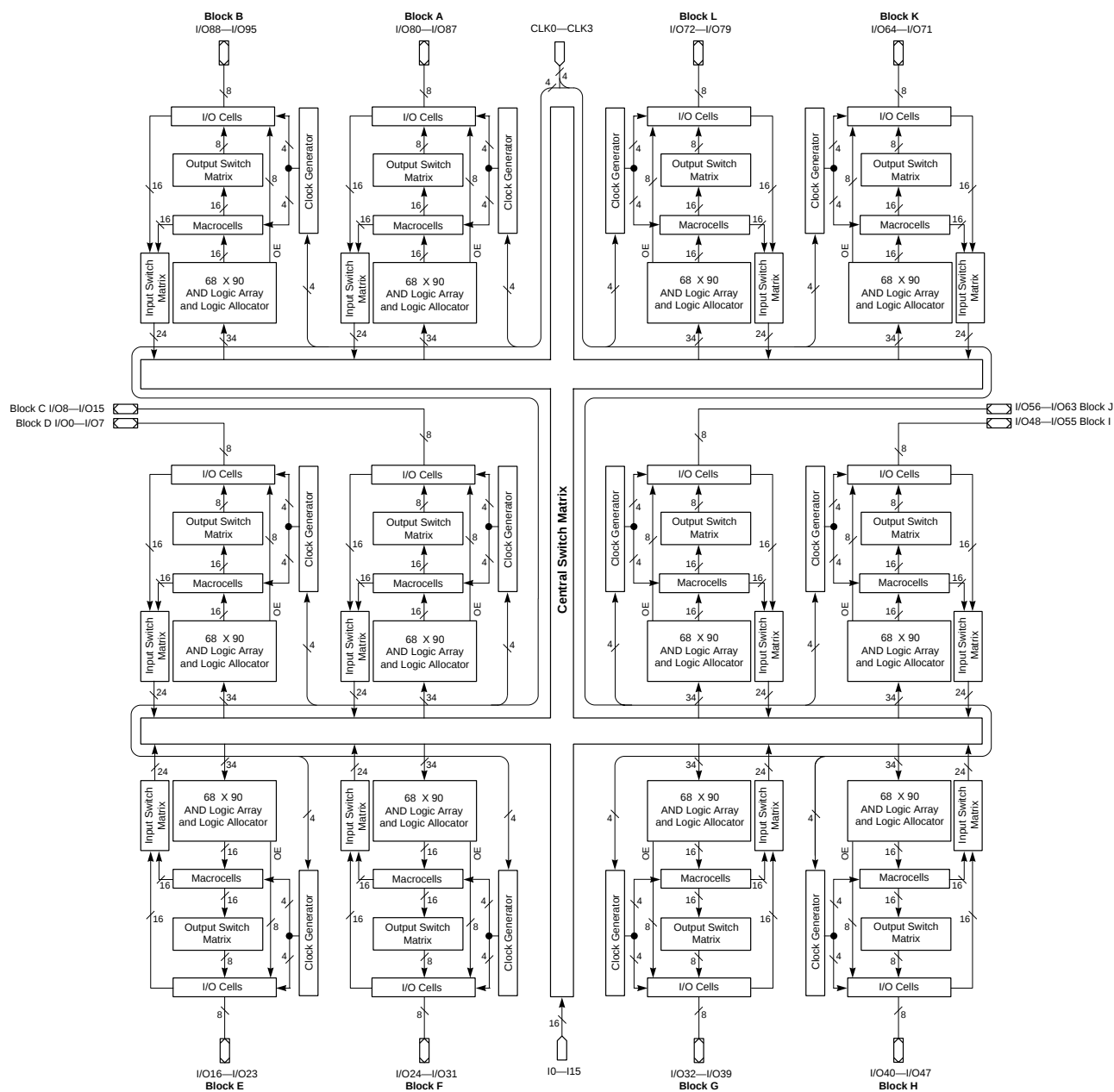
17466G-021

BLOCK DIAGRAM – M4A(3,5)-128/64



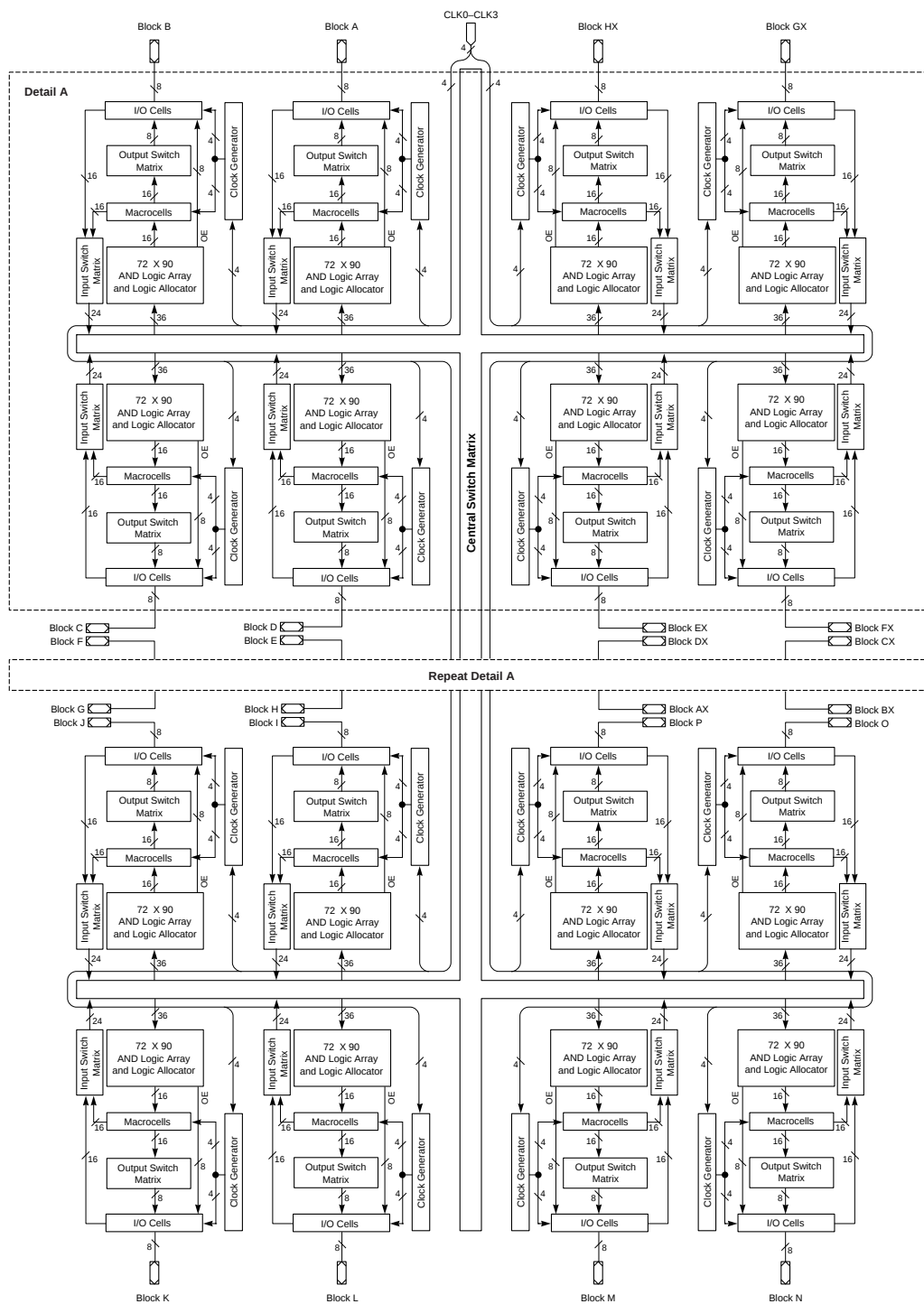
17466H-022

BLOCK DIAGRAM – M4A(3,5)-192/96



17466G-067

BLOCK DIAGRAM – M4A3-384/160, M4A3-384/192



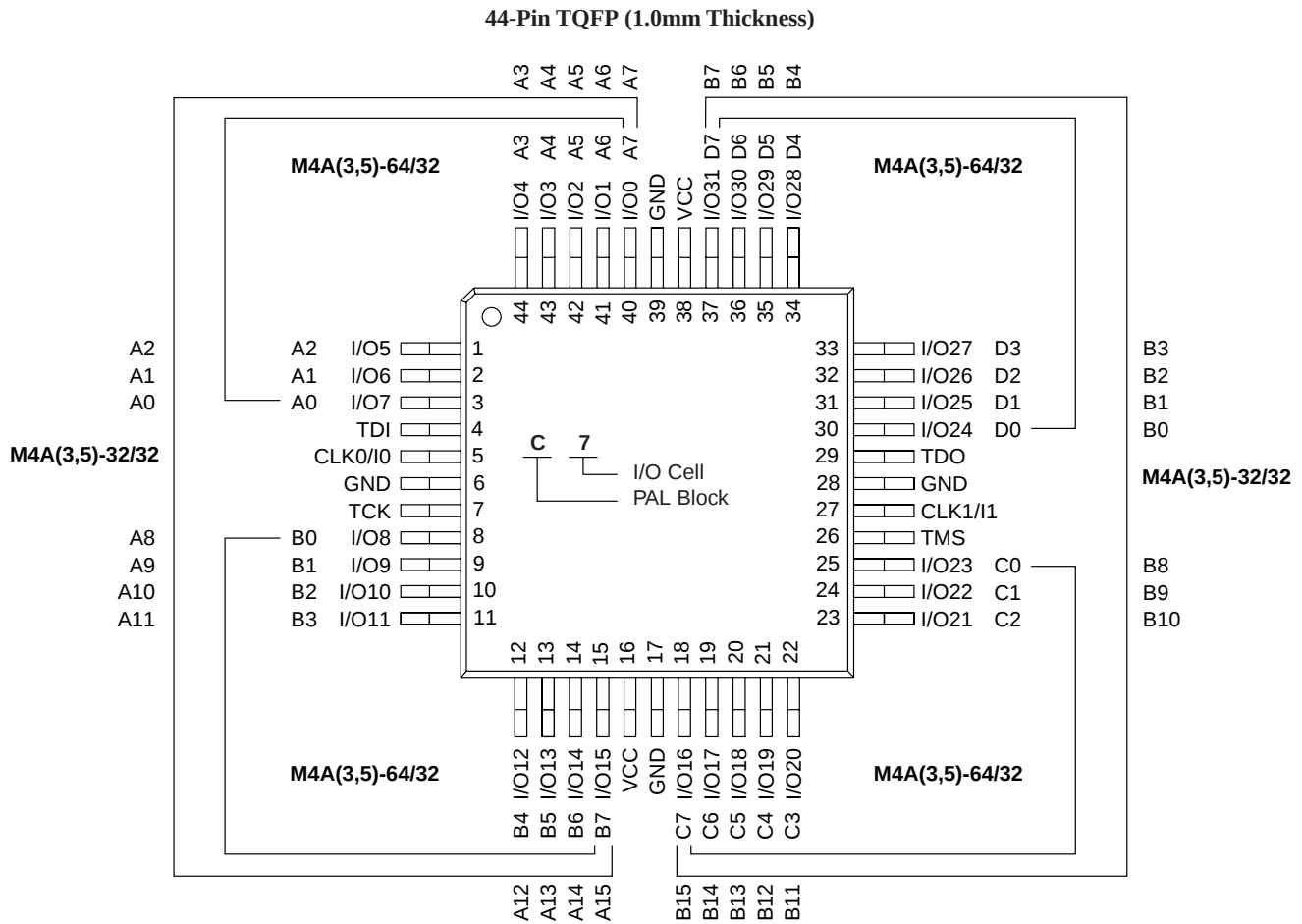
17466G-067

ispMACH 4A TIMING PARAMETERS OVER OPERATING RANGES¹

		-5		-55		-6		-65		-7		-10		-12		-14		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Input Register Delays with ZHT Option:																		
t _{SIRZ}	Input register setup time - ZHT	6.0		6.0		6.0		6.0		6.0		6.0		6.0		6.0		ns
t _{HIRZ}	Input register hold time - ZHT	0.0		0.0		0.0		0.0		0.0		0.0		0.0		0.0		ns
Input Latch Delays with ZHT Option:																		
t _{SILZ}	Input latch setup time - ZHT	6.0		6.0		6.0		6.0		6.0		6.0		6.0		6.0		ns
t _{HILZ}	Input latch hold time - ZHT	0.0		0.0		0.0		0.0		0.0		0.0		0.0		0.0		ns
t _{PDIL} Z _i	Transparent input latch to internal feedback - ZHT		6.0		6.0		6.0		6.0		6.0		6.0		6.0		6.0	ns
Output Delays:																		
t _{BUF}	Output buffer delay		1.5		1.5		1.8		2.0		2.5		3.0		3.0		3.0	ns
t _{SLW}	Slow slew rate delay adder		2.5		2.5		2.5		2.5		2.5		2.5		2.5		2.5	ns
t _{EA}	Output enable time		7.5		7.5		8.5		8.5		9.5		10.0		12.0		15.0	ns
t _{ER}	Output disable time		7.5		7.5		8.5		8.5		9.5		10.0		12.0		15.0	ns
Power Delay:																		
t _{PL}	Power-down mode delay adder		2.5		2.5		2.5		2.5		2.5		2.5		2.5		2.5	ns
Reset and Preset Delays:																		
t _{SRI}	Asynchronous reset or preset to internal register output		7.5		7.7		8.0		8.0		9.5		11.0		13.0		16.0	ns
t _{SR}	Asynchronous reset or preset to register output		9.0		9.2		10.0		10.0		12.0		14.0		16.0		19.0	ns
t _{SRR}	Asynchronous reset and preset register recovery time	7.0		7.0		7.5		7.5		8.0		8.0		10.0		15.0		ns
t _{SRW}	Asynchronous reset or preset width	7.0		7.0		8.0		8.0		10.0		10.0		12.0		15.0		ns
Clock/LE Width:																		
t _{WLS}	Global clock width low	2.0		2.0		2.5		2.5		3.0		4.0		5.0		6.0		ns
t _{WHS}	Global clock width high	2.0		2.0		2.5		2.5		3.0		4.0		5.0		6.0		ns
t _{WLA}	Product term clock width low	3.0		3.0		3.5		3.5		4.0		5.0		8.0		9.0		ns
t _{WHA}	Product term clock width high	3.0		3.0		3.5		3.5		4.0		5.0		8.0		9.0		ns
t _{GWS}	Global gate width low (for low transparent) or high (for high transparent)	4.0		4.0		4.5		4.5		5.0		5.0		6.0		6.0		ns
t _{GWA}	Product term gate width low (for low transparent) or high (for high transparent)	4.0		4.0		4.5		4.5		5.0		5.0		6.0		9.0		ns
t _{WIRL}	Input register clock width low	3.0		3.0		3.5		3.5		4.0		5.0		6.0		6.0		ns
t _{WIRH}	Input register clock width high	3.0		3.0		3.5		3.5		4.0		5.0		6.0		6.0		ns
t _{WIL}	Input latch gate width	4.0		4.0		4.5		4.5		5.0		5.0		6.0		6.0		ns

44-PIN TQFP CONNECTION DIAGRAM (M4A(3,5)-32/32 AND M4A(3,5)-64/32)

Top View



PIN DESIGNATIONS

CLK/I = Clock or Input

GND = Ground

I/O = Input/Output

V_{CC} = Supply Voltage

TDI = Test Data In

TCK = Test Clock

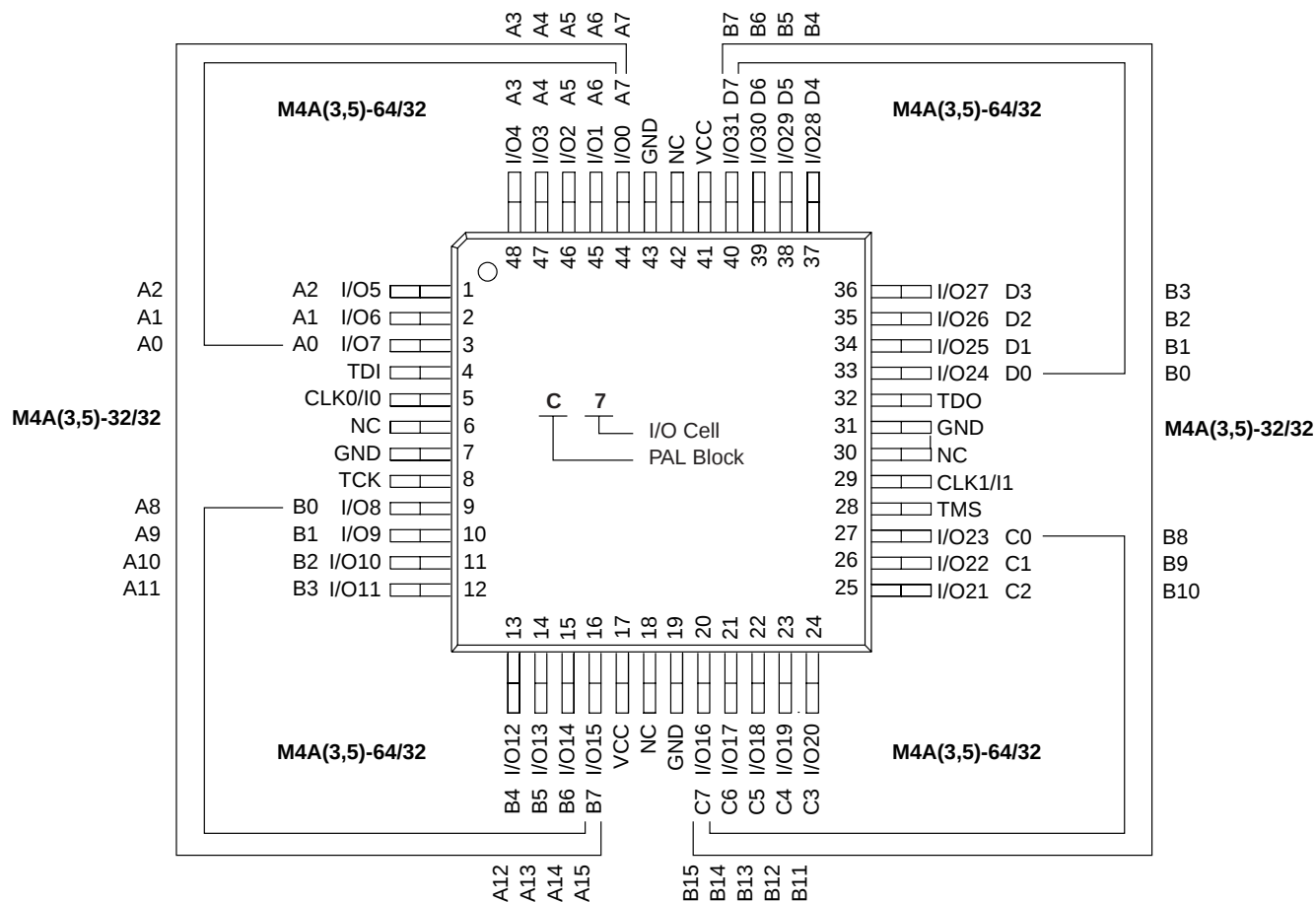
TMS = Test Mode Select

TDO = Test Data Out

48-PIN TQFP CONNECTION DIAGRAM (M4A(3,5)-32/32 AND M4A(3,5)-64/32)

Top View

48-Pin TQFP (1.4mm Thickness)



17466G-028

PIN DESIGNATIONS

CLK/I = Clock or Input

GND = Ground

I/O = Input/Output

V_{CC} = Supply Voltage

NC = No Connect

TDI = Test Data In

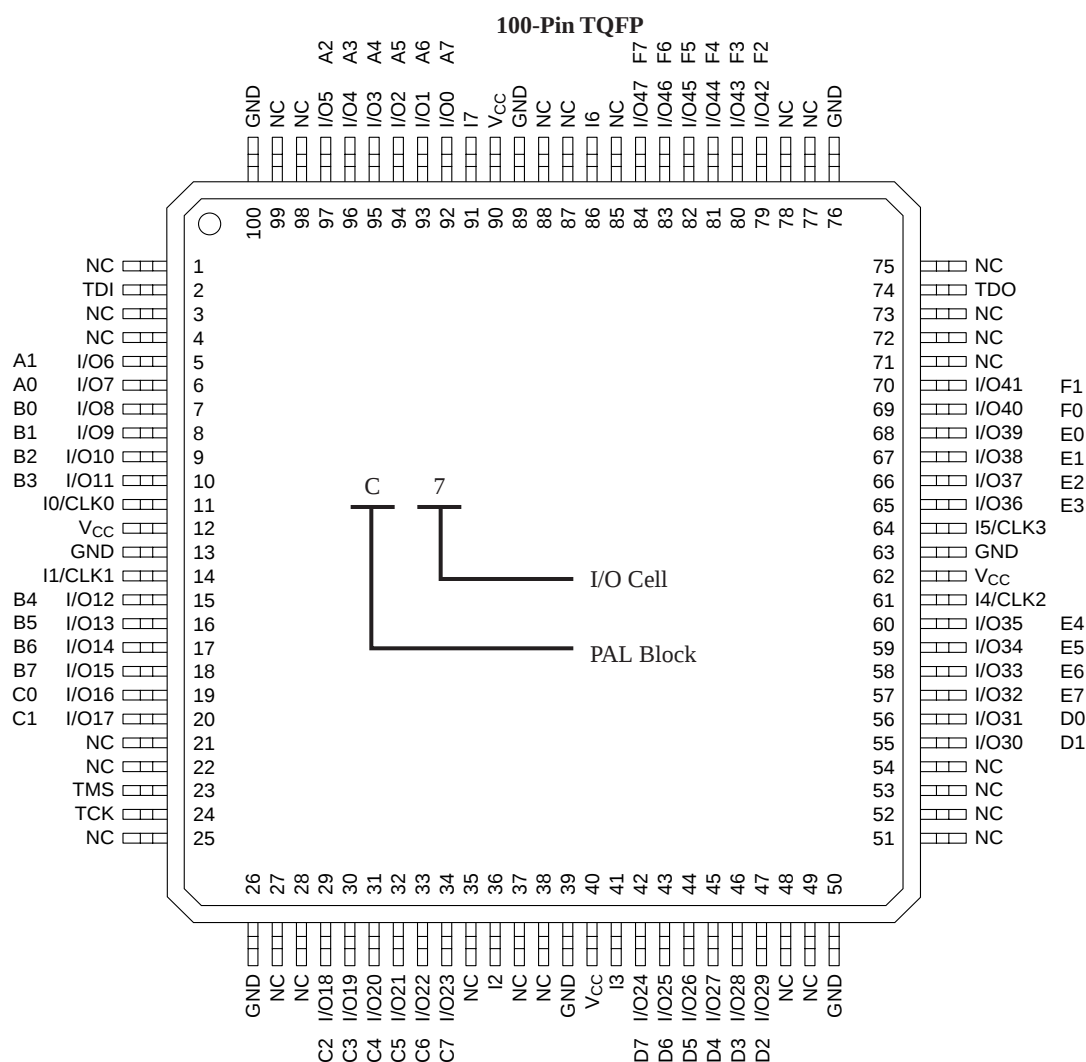
TCK = Test Clock

TMS = Test Mode Select

TDO = Test Data Out

100-PIN TQFP CONNECTION DIAGRAM (M4A(3,5)-96/48)

Top View



17466G-029

PIN DESIGNATIONS

CLK/I = Clock or Input

GND = Ground

I = Input

I/O = Input/Output

V_{CC} = Supply Voltage

NC = No Connect

TDI = Test Data In

TCK = Test Clock

TMS = Test Mode Select

TDO = Test Data Out

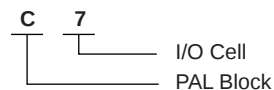
144-BALL FPBGA CONNECTION DIAGRAM (M4A3-192/96)

Bottom View

144-Ball fpBGA													
	12	11	10	9	8	7	6	5	4	3	2	1	
A	GND	I/O72 L7	I/O76 L3	I13	GBCLK3	I0	I/O82 A2	I/O86 A6	I/O88 B0	I/O93 B5	I/O95 B7	GND	A
B	GND	I/O73 L6	I/O77 L2	I/O79 L0	VCC	I1	I/O83 A3	I/O87 A7	I/O90 B2	I/O94 B6	I/O0 D7	TDI	B
C	GND	TD0	I/O74 L5	I14	GND	I/O80 A0	I/O84 A4	GND	I/O92 B4	I/O1 D6	I/O4 D3	I/O3 D4	C
D	I/O67 K4	I/O69 K2	I/O71 K0	I/O75 L4	GBCLK0	I/O81 A1	VCC	I/O91 B3	I/O2 D5	I2	I/O6 D1	I/O7 D0	D
E	I12	I/O64 K7	I/O66 K5	I/O70 K1	I/O78 L1	I/O85 A5	I/O89 B1	I/O5 D2	I/O8 C7	I4	GND	VCC	E
F	I10	I11	GND	I/O65 K6	I/O68 K3	I15	I3	GND	I/O12 C3	I/O11 C4	I/O10 C5	I/O9 C6	F
G	I/O60 J3	I/O61 J2	I/O62 J1	I/O63 J0	VCC	GND	I7	I/O20 E3	I/O17 E6	I/O15 C0	I/O14 C1	I/O13 C2	G
H	I/O56 J7	I/O57 J6	I/O58 J5	I/O59 J4	I/O53 I2	I/O41 H1	I/O37 G5	I/O30 F1	I/O22 E1	I/O18 E5	I/O16 E7	VCC	H
J	I/O55 I0	I/O54 I1	VCC	I/O50 I5	I/O43 H3	VCC	I/O33 G1	GBCLK2	I/O27 F4	I/O23 E0	I/O21 E2	I/O19 E4	J
K	I/O51 I4	I/O52 I3	I/O49 I6	I/O44 H4	GND	I/O36 G4	I/O32 G0	VCC	I6	I/O26 F5	TCK	TMS	K
L	GND	I/O48 I7	I/O46 H6	I/O42 H2	I/O39 G7	I/O35 G3	I9	GND	I/O31 F0	I/O29 F2	I/O25 F6	GND	L
M	GND	I/O47 H7	I/O45 H5	I/O40 H0	I/O38 G6	I/O34 G2	I8	GBCLK1	I5	I/O28 F3	I/O24 F7	GND	M
	12	11	10	9	8	7	6	5	4	3	2	1	

PIN DESIGNATIONS

CLK = Clock
 GND = Ground
 I = Input
 I/O = Input/Output
 N/C = No Connect
 VCC = Supply Voltage
 TDI = Test Data In
 TCK = Test Clock
 TMS = Test Mode Select
 TD0 = Test Data Out

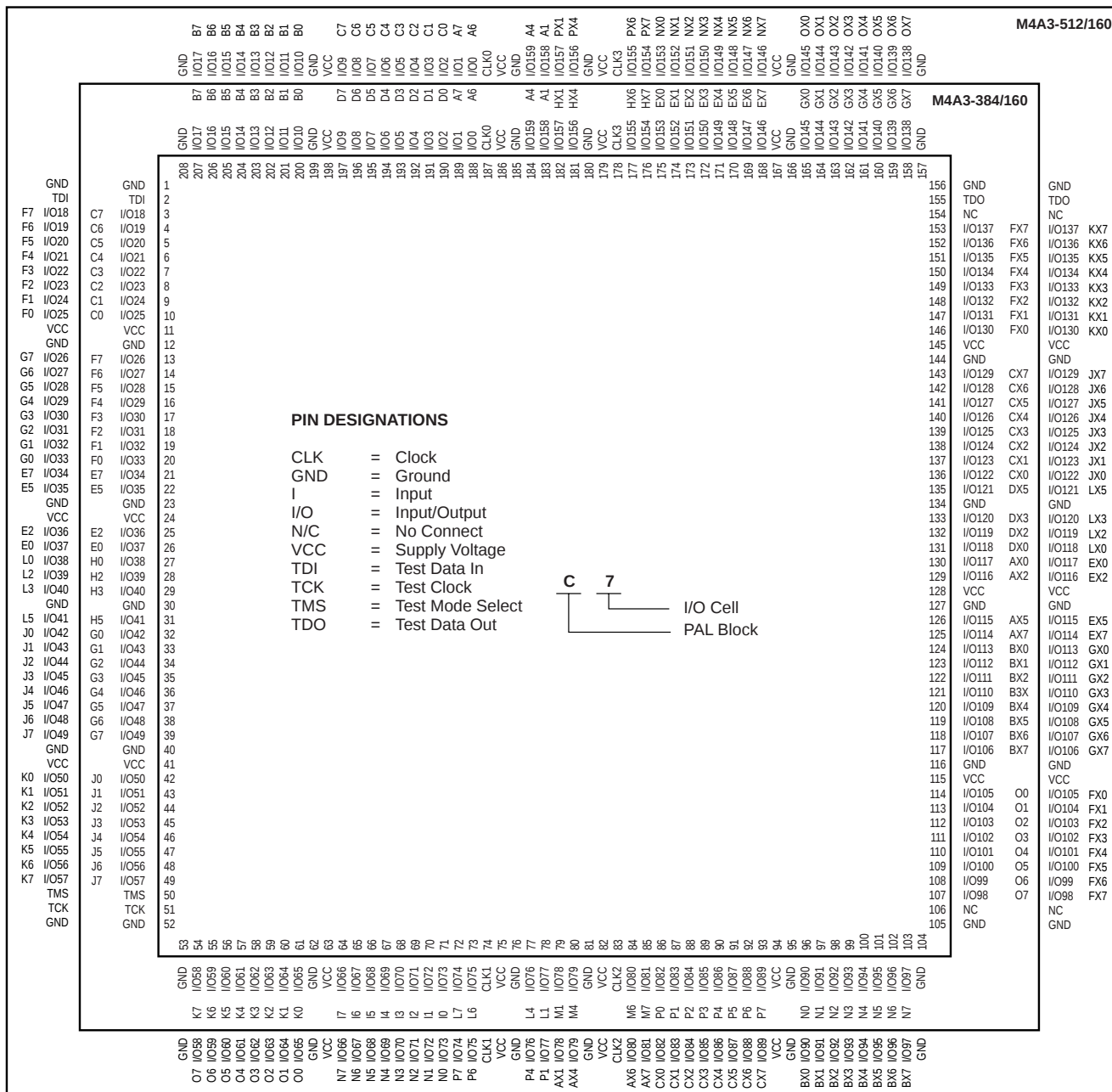


m4a3.192.96_144bga

208-PIN PQFP CONNECTION DIAGRAM (M4A3-384/160 AND M4A3-512/160)

Top View

208-Pin PQFP



17466Ga-044

256-BALL fpBGA CONNECTION DIAGRAM (M4A3-256/192)

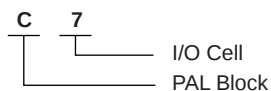
Bottom View

256-Ball fpBGA

	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	I/O167 N15	I/O181 O13	I/O180 O12	I/O177 O9	I/O174 O6	I/O172 O4	I/O191 P14	I/O186 P4	I/O1 A2	I/O3 A6	GCLK0	I/O9 B1	I/O13 B5	I/O15 B7	I/O18 B10	I/O20 B12	A
B	I/O165 N13	I/O166 N14	I/O182 O14	I/O179 O11	I/O175 O7	I/O173 O5	I/O168 O0	I/O187 P6	I/O0 A0	I/O5 A10	I/O7 A14	I/O10 B2	I/O16 B8	I/O19 B11	I/O21 B13	NC	B
C	I/O163 N11	I/O164 N12	NC	I/O183 O15	I/O178 O10	I/O170 O2	I/O171 O3	I/O189 P10	I/O184 P0	I/O6 A12	I/O12 B4	I/O14 B6	I/O23 B15	I/O22 B14	TDI	I/O39 C15	C
D	I/O158 N6	I/O159 N7	TDO	GND	GND	VCC	GND	VCC	GND	GND	VCC	GND	VCC	I/O17 B9	I/O38 C14	I/O37 C13	D
E	I/O156 N4	NC	I/O162 N10	VCC	I/O160 N8	I/O161 N9	I/O190 P12	GCLK3	I/O188 P8	I/O2 A4	I/O8 B0	NC	GND	I/O36 C12	I/O35 C11	I/O31 C7	E
F	I/O152 N0	I/O157 N5	I/O155 N3	GND	I/O154 N2	I/O153 N1	I/O176 O8	I/O169 O1	I/O185 P2	I/O4 A8	I/O11 B3	I/O34 C10	VCC	I/O32 C8	I/O30 C6	I/O29 C5	F
G	I/O147 M6	I/O150 M12	I/O149 M10	VCC	I/O148 M8	I/O151 M14	VCC	GND	GND	VCC	I/O33 C9	I/O28 C4	GND	I/O26 C2	I/O25 C1	I/O47 D14	G
H	I/O144 M0	I/O146 M4	I/O145 OM2	GND	I/O136 L0	I/O137 L2	GND	VCC	VCC	GND	I/O27 C3	I/O24 C0	VCC	I/O44 D8	I/O43 D6	I/O42 D4	H
J	I/O138 L4	I/O139 L6	I/O140 L8	GND	I/O142 L12	I/O141 L10	GND	VCC	VCC	GND	I/O46 D12	I/O45 D10	GND	I/O49 E2	I/O48 E0	I/O50 E4	J
K	I/O143 L14	I/O120 K0	I/O121 K1	VCC	I/O123 K3	I/O122 K2	VCC	GND	GND	VCC	I/O41 D2	I/O40 D0	VCC	I/O55 E14	I/O54 E12	I/O56 F0	K
L	I/O124 K4	I/O125 K5	I/O127 K7	GND	I/O130 K10	I/O126 K6	I/O98 I4	I/O91 H6	I/O75 G3	I/O77 G5	I/O52 E8	I/O51 E6	GND	I/O59 F3	I/O60 F4	I/O57 F1	L
M	I/O128 K8	I/O129 K9	I/O131 K11	GND	I/O107 J3	I/O105 J1	I/O100 I8	I/O90 H4	I/O74 G2	I/O80 G8	I/O83 G11	I/O53 E10	VCC	I/O68 F12	I/O63 F7	I/O58 F2	M
N	I/O132 K12	I/O133 K13	I/O135 K15	VCC	GND	VCC	GND	VCC	GND	GND	VCC	GND	GND	TCK	I/O64 F8	I/O61 F5	N
P	I/O134 K14	I/O117 J13	I/O118 J14	I/O119 J15	I/O108 J4	I/O106 J2	I/O101 I10	I/O89 H2	I/O93 H10	I/O94 H12	I/O79 G7	I/O84 G12	I/O87 G15	TMS	I/O65 F9	I/O62 F6	P
R	I/O116 J12	I/O115 J11	I/O112 J8	I/O111 J7	I/O104 J0	I/O102 I12	I/O99 I6	I/O96 I0	I/O92 H8	I/O72 G0	I/O76 G4	I/O81 G9	I/O85 G13	I/O71 F15	I/O67 F11	I/O66 F10	R
T	I/O114 J10	I/O113 J9	I/O110 J6	I/O109 J5	I/O103 I14	GCLK2	I/O97 I2	I/O88 H0	GCLK1	I/O95 H14	I/O73 G1	I/O78 G6	I/O82 G10	I/O86 G14	I/O70 F14	I/O69 F13	T
	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

PIN DESIGNATIONS

CLK = Clock
 GND = Ground
 I = Input
 I/O = Input/Output
 N/C = No Connect
 VCC = Supply Voltage
 TDI = Test Data In
 TCK = Test Clock
 TMS = Test Mode Select
 TDO = Test Data Out



17466G-047

ispMACH 4A PRODUCT ORDERING INFORMATION

ispMACH 4A Devices Commercial and Industrial - 3.3V and 5V

Lattice programmable logic products are available with several ordering options. The order number (Valid Combination) is formed by a combination of:

M4A3- 256 / 128 -7 Y C		L48	
FAMILY TYPE		= 48-pin TQFP for M4A3-32/32 or M4A3-64/32 M4A5-32/32 or M4A5-64/32	
M4A3- = ispMACH 4A Family Low Voltage Advanced Feature (3.3-V V_{CC})		OPERATING CONDITIONS	
M4A5- = ispMACH 4A Family Advanced Feature (5-V V_{CC})		C = Commercial (0°C to +70°C)	
MACROCELL DENSITY		I = Industrial (-40°C to +85°C)	
32 = 32 Macrocells 192 = 192 Macrocells		PACKAGE TYPE	
64 = 64 Macrocells 256 = 256 Macrocells		SA = Ball Grid Array (BGA)	
96 = 96 Macrocells 384 = 384 Macrocells		J = Plastic Leaded Chip Carrier (PLCC)	
128 = 128 Macrocells 512 = 512 Macrocells		JN = Lead-free Plastic Leaded Chip Carrier (PLCC)	
I/Os		V = Thin Quad Flat Pack (TQFP)	
/32 = 32 I/Os in 44-pin PLCC, 44-pin TQFP or 48-pin TQFP		VN = Lead-free Thin Quad Flat Pack (TQFP)	
/48 = 48 I/Os in 100-pin TQFP		Y = Plastic Quad Flat Pack (PQFP)	
/64 = 64 I/Os in 100-pin TQFP, 100-pin PQFP, or 100-ball caBGA		YN = Lead-free Plastic Quad Flat Pack (PQFP)	
/96 = 96 I/Os in 144-pin TQFP or 144-ball fpBGA		FA = Fine-pitch Ball Grid Array (fpBGA)	
/128 = 128 I/Os in 208-pin PQFP, 256-ball BGA or 256-ball fpBGA		FAN = Lead-free Fine-pitch Ball Grid Array (fpBGA)	
/160 = 160 I/Os in 208-pin PQFP		CA = Chip-array Ball Grid Array (caBGA)	
/192 = 192 I/Os in 256-ball BGA or 256-ball fpBGA		SPEED	
/256 = 256 I/Os in 388-ball fpBGA		-5 = 5.0 ns t_{PD}	
		-55 = 5.5 ns t_{PD}	
		-6 = 6.0 ns t_{PD}	
		-65 = 6.5 ns t_{PD}	
		-7 = 7.5 ns t_{PD}	
		-10 = 10 ns t_{PD}	
		-12 = 12 ns t_{PD}	
		-14 = 14 ns t_{PD}	

*Package obsolete, contact factory.

Conventional Packaging

3.3V Commercial Combinations			3.3V Industrial Combinations		
M4A3-32/32	-5, -7, -10	JC, VC, VC48	M4A3-32/32	-7, -10, -12	JI, VI, VI48
M4A3-64/32	-55, -7, -10	JC, VC, VC48	M4A3-64/32		JI, VI, VI48
M4A3-64/64		VC	M4A3-64/64		VI
M4A3-96/48		VC	M4A3-96/48		VI
M4A3-128/64		YC, VC, CAC	M4A3-128/64		YI, VI, CAI
M4A3-192/96	-6, -7, -10	VC, FAC	M4A3-192/96		VI, FAI
M4A3-256/128	-55, -65 ¹ , -7, -10	YC, FAC, SAC	M4A3-256/128	-10, -12	YI, FAI, SAI
M4A3-256/160	-7, -10	YC	M4A3-256/160		YI
M4A3-256/192		FAC	M4A3-256/192	-10, -12, -14	FAI
M4A3-384/160	-65, -10, -12	YC	M4A3-384/160		YI
M4A3-384/192		SAC, FAC	M4A3-384/192		FAI
M4A3-512/160	-7, -10, -12	YC	M4A3-512/160		YI
M4A3-512/192		FAC	M4A3-512/192		FAI
M4A3-512/256		FAC	M4A3-512/256		FAI

1. Use 5.5ns for new designs.

Revision History

Date	Version	Change Summary
-	K	Previous Lattice release.
August 2006	L	Updated for lead-free package options.
September 2006	M	Revised M4A3-256/160 208-pin PQFP connection diagram.