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Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details

Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	7.5 ns
Voltage Supply - Internal	3V ~ 3.6V
Number of Logic Elements/Blocks	-
Number of Macrocells	64
Number of Gates	-
Number of I/O	32
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/m4a3-64-32-7vi

The ispMACH 4A family offers 20 density-I/O combinations in Thin Quad Flat Pack (TQFP), Plastic Quad Flat Pack (PQFP), Plastic Leaded Chip Carrier (PLCC), Ball Grid Array (BGA), fine-pitch BGA (fpBGA), and chip-array BGA (caBGA) packages ranging from 44 to 388 pins (Table 3). It also offers I/O safety features for mixed-voltage designs so that the 3.3-V devices can accept 5-V inputs, and 5-V devices do not overdrive 3.3-V inputs. Additional features include Bus-Friendly inputs and I/Os, a programmable power-down mode for extra power savings and individual output slew rate control for the highest speed transition or for the lowest noise transition.

Table 3. ispMACH 4A Package and I/O Options (Number of I/Os and dedicated inputs in Table)

3.3 V Devices								
Package	M4A3-32	M4A3-64	M4A3-96	M4A3-128	M4A3-192	M4A3-256	M4A3-384	M4A3-512
44-pin PLCC	32+2	32+2						
44-pin TQFP	32+2	32+2						
48-pin TQFP	32+2	32+2						
100-pin TQFP		64+6	48+8	64+6				
100-pin PQFP				64+6				
100-ball caBGA				64+6				
144-pin TQFP					96+16			
144-ball fpBGA					96+16			
208-pin PQFP						128+14, 160	160	160
256-ball fpBGA						128+14, 192	192	192
256-ball BGA						128+14	192	
388-ball fpBGA								256

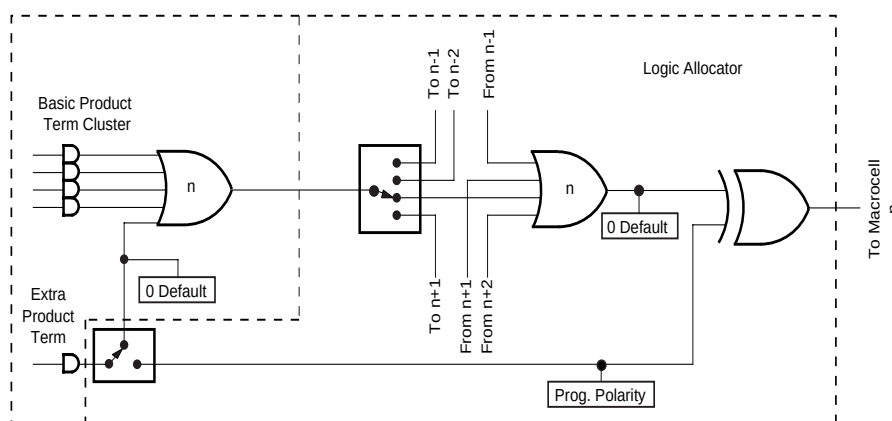
5 V Devices						
Package	M4A5-32	M4A5-64	M4A5-96	M4A5-128	M4A5-192	M4A5-256
44-pin PLCC	32+2	32+2				
44-pin TQFP	32+2	32+2				
48-pin TQFP	32+2	32+2				
100-pin TQFP			48+8	64+6		
100-pin PQFP				64+6		
144-pin TQFP					96+16	
208-pin PQFP						128+14

Table 6. Logic Allocator for All ispMACH 4A Devices (except M4A(3,5)-32/32)

Output Macrocell	Available Clusters	Output Macrocell	Available Clusters
M ₀	C ₀ , C ₁ , C ₂	M ₈	C ₇ , C ₈ , C ₉ , C ₁₀
M ₁	C ₀ , C ₁ , C ₂ , C ₃	M ₉	C ₈ , C ₉ , C ₁₀ , C ₁₁
M ₂	C ₁ , C ₂ , C ₃ , C ₄	M ₁₀	C ₉ , C ₁₀ , C ₁₁ , C ₁₂
M ₃	C ₂ , C ₃ , C ₄ , C ₅	M ₁₁	C ₁₀ , C ₁₁ , C ₁₂ , C ₁₃
M ₄	C ₃ , C ₄ , C ₅ , C ₆	M ₁₂	C ₁₁ , C ₁₂ , C ₁₃ , C ₁₄
M ₅	C ₄ , C ₅ , C ₆ , C ₇	M ₁₃	C ₁₂ , C ₁₃ , C ₁₄ , C ₁₅
M ₆	C ₅ , C ₆ , C ₇ , C ₈	M ₁₄	C ₁₃ , C ₁₄ , C ₁₅
M ₇	C ₆ , C ₇ , C ₈ , C ₉	M ₁₅	C ₁₄ , C ₁₅

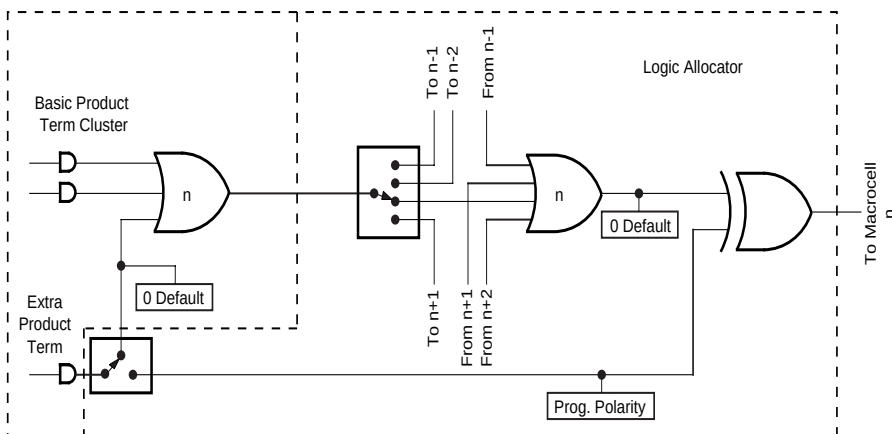
Table 7. Logic Allocator for M4A(3,5)-32/32

Output Macrocell	Available Clusters	Output Macrocell	Available Clusters
M ₀	C ₀ , C ₁ , C ₂	M ₈	C ₈ , C ₉ , C ₁₀
M ₁	C ₀ , C ₁ , C ₂ , C ₃	M ₉	C ₈ , C ₉ , C ₁₀ , C ₁₁
M ₂	C ₁ , C ₂ , C ₃ , C ₄	M ₁₀	C ₉ , C ₁₀ , C ₁₁ , C ₁₂
M ₃	C ₂ , C ₃ , C ₄ , C ₅	M ₁₁	C ₁₀ , C ₁₁ , C ₁₂ , C ₁₃
M ₄	C ₃ , C ₄ , C ₅ , C ₆	M ₁₂	C ₁₁ , C ₁₂ , C ₁₃ , C ₁₄
M ₅	C ₄ , C ₅ , C ₆ , C ₇	M ₁₃	C ₁₂ , C ₁₃ , C ₁₄ , C ₁₅
M ₆	C ₅ , C ₆ , C ₇	M ₁₄	C ₁₃ , C ₁₄ , C ₁₅
M ₇	C ₆ , C ₇	M ₁₅	C ₁₄ , C ₁₅



a. Synchronous Mode

17466G-005



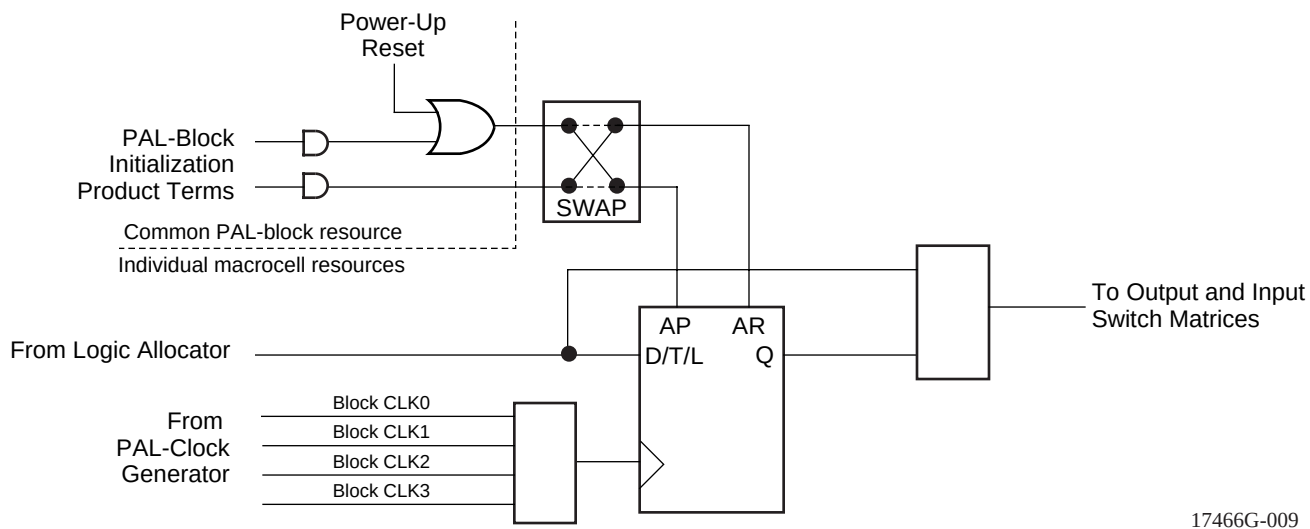
b. Asynchronous Mode

17466G-006

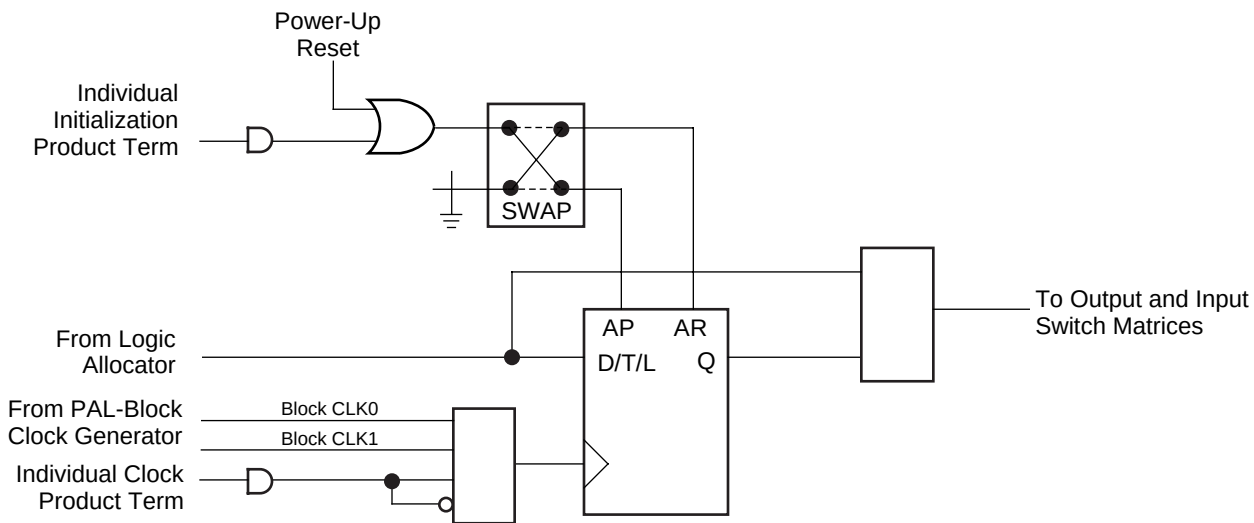
Figure 2. Logic Allocator: Configuration of Cluster “n” Set by Mode of Macrocell “n”

Macrocell

The macrocell consists of a storage element, routing resources, a clock multiplexer, and initialization control. The macrocell has two fundamental modes: synchronous and asynchronous (Figure 5). The mode chosen only affects clocking and initialization in the macrocell.



a. Synchronous mode

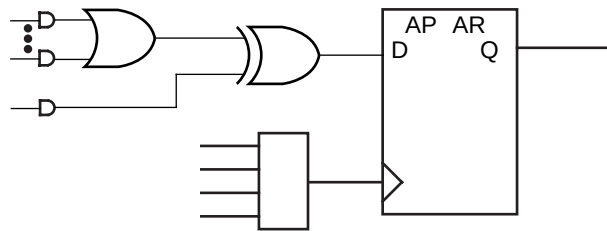


b. Asynchronous mode

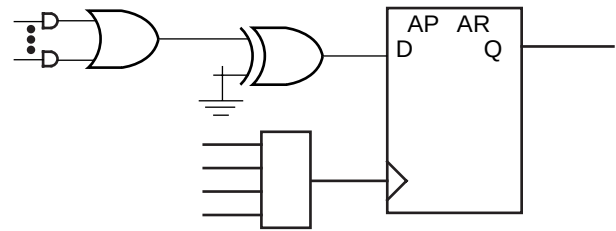
Figure 5. Macrocell

In either mode, a combinatorial path can be used. For combinatorial logic, the synchronous mode will generally be used, since it provides more product terms in the allocator.

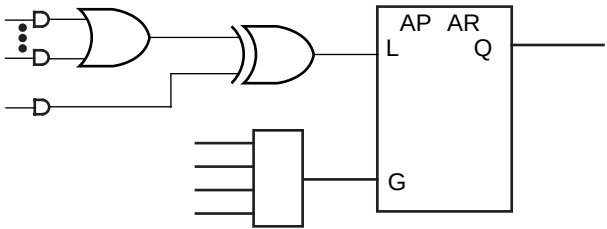
The flip-flop can be configured as a D-type or T-type latch. J-K or S-R registers can be synthesized. The primary flip-flop configurations are shown in Figure 6, although others are possible. Flip-flop functionality is defined in Table 8. Note that a J-K latch is inadvisable as it will cause oscillation if both J and K inputs are HIGH.



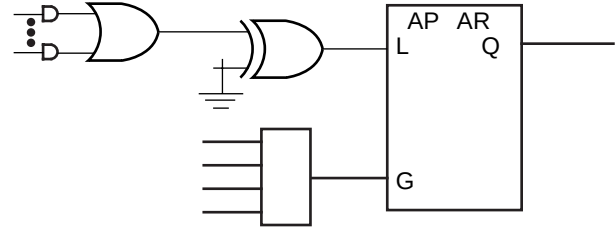
a. D-type with XOR



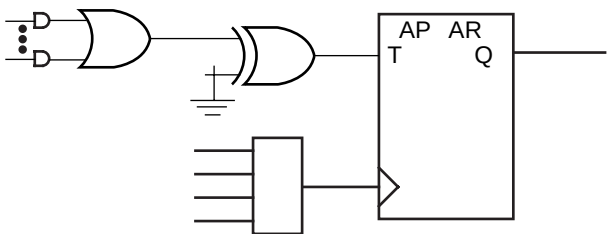
b. D-type with programmable D polarity



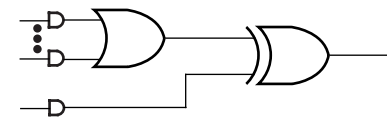
c. Latch with XOR



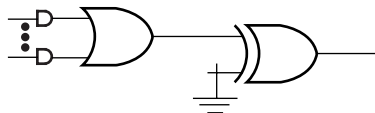
d. Latch with programmable D polarity



e. T-type with programmable T polarity



f. Combinatorial with XOR



g. Combinatorial with programmable polarity

Figure 6. Primary Macrocell Configurations

17466G-011

Table 8. Register/Latch Operation

Configuration	Input(s)	CLK/LE ¹	Q+
D-type Register	D=X	0, 1, ↓ (↑)	Q
	D=0	↑ (↓)	0
	D=1	↑ (↓)	1
T-type Register	T=X	0, 1, ↓ (↑)	Q
	T=0	↑ (↓)	Q
	T=1	↑ (↓)	$\overline{Q}$
D-type Latch	D=X	1(0)	Q
	D=0	0(1)	0
	D=1	0(1)	1

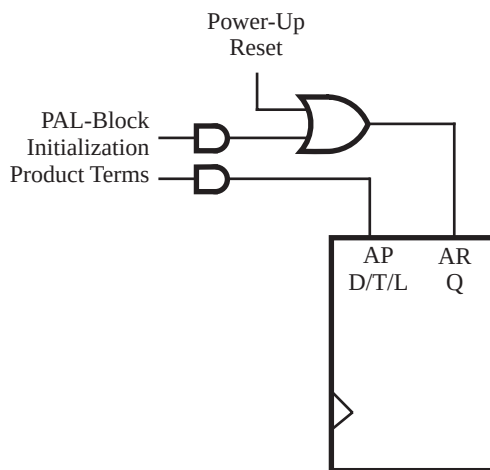
Note:

1. Polarity of CLK/LE can be programmed

Although the macrocell shows only one input to the register, the XOR gate in the logic allocator allows the D-, T-type register to emulate J-K, and S-R behavior. In this case, the available product terms are divided between J and K (or S and R). When configured as J-K, S-R, or T-type, the extra product term must be used on the XOR gate input for flip-flop emulation. In any register type, the polarity of the inputs can be programmed.

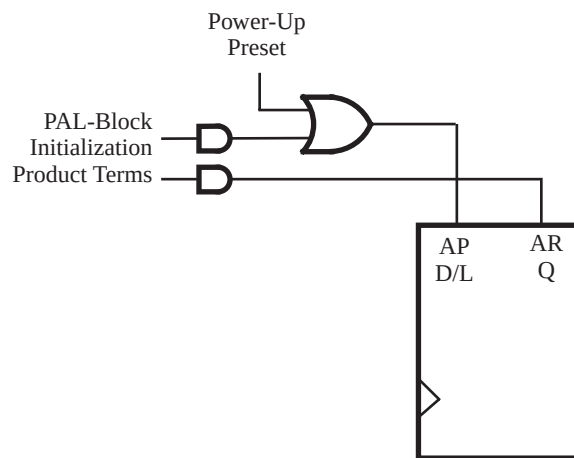
The clock input to the flip-flop can select any of the four PAL block clocks in synchronous mode, with the additional choice of either polarity of an individual product term clock in the asynchronous mode.

The initialization circuit depends on the mode. In synchronous mode (Figure 7), asynchronous reset and preset are provided, each driven by a product term common to the entire PAL block.



a. Power-up reset

17466G-012



b. Power-up preset

17466G-013

Figure 7. Synchronous Mode Initialization Configurations

Table 10. Output Switch Matrix Combinations for ispMACH 4A Devices with 2:1 Macrocell-I/O Cell Ratio

Macrocell	Routable to I/O Cells
M12, M13	I/O3, I/O4, I/O5, I/O6
M14, M15	I/O4, I/O5, I/O6, I/O7

I/O Cell	Available Macrocells
I/O0	M0, M1, M2, M3, M4, M5, M6, M7
I/O1	M2, M3, M4, M5, M6, M7, M8, M9
I/O2	M4, M5, M6, M7, M8, M9, M10, M11
I/O3	M6, M7, M8, M9, M10, M11, M12, M13
I/O4	M8, M9, M10, M11, M12, M13, M14, M15
I/O5	M0, M1, M10, M11, M12, M13, M14, M15
I/O6	M0, M1, M2, M3, M12, M13, M14, M15
I/O7	M0, M1, M2, M3, M4, M5, M14, M15

Table 11. Output Switch Matrix Combinations for M4A3-256/160 and M4A3-256/192

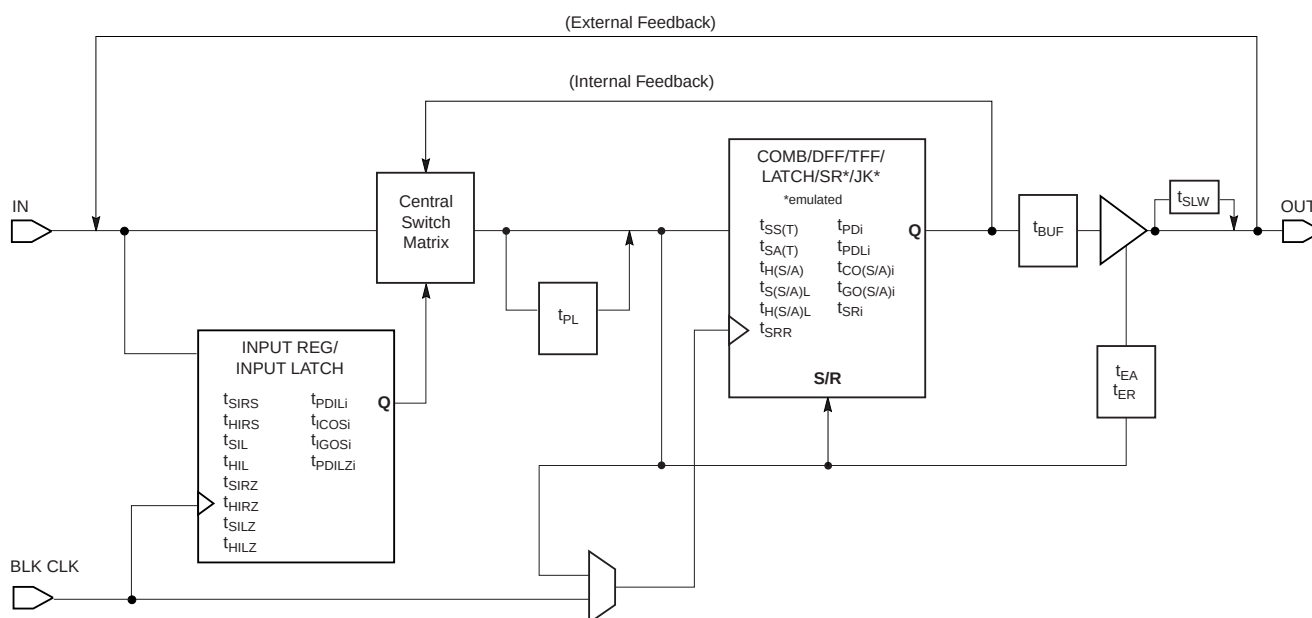
Macrocell	Routable to I/O Cells							
M0	I/O0	I/O1	I/O2	I/O3	I/O4	I/O5	I/O6	I/O7
M1	I/O0	I/O1	I/O2	I/O3	I/O4	I/O5	I/O6	I/O7
M2	I/O0	I/O1	I/O2	I/O3	I/O4	I/O5	I/O6	I/O7
M3	I/O0	I/O1	I/O2	I/O3	I/O4	I/O5	I/O6	I/O7
M4	I/O0	I/O1	I/O2	I/O3	I/O4	I/O5	I/O6	I/O7
M5	I/O0	I/O1	I/O2	I/O3	I/O4	I/O5	I/O6	I/O7
M6	I/O0	I/O1	I/O2	I/O3	I/O4	I/O5	I/O6	I/O7
M7	I/O0	I/O1	I/O2	I/O3	I/O4	I/O5	I/O6	I/O7
M8	I/O8	I/O9	I/O10	I/O11	I/O12	I/O13	I/O14	I/O15
M9	I/O8	I/O9	I/O10	I/O11	I/O12	I/O13	I/O14	I/O15
M10	I/O8	I/O9	I/O10	I/O11	I/O12	I/O13	I/O14	I/O15
M11	I/O8	I/O9	I/O10	I/O11	I/O12	I/O13	I/O14	I/O15
M12	I/O8	I/O9	I/O10	I/O11	I/O12	I/O13	I/O14	I/O15
M13	I/O8	I/O9	I/O10	I/O11	I/O12	I/O13	I/O14	I/O15
M14	I/O8	I/O9	I/O10	I/O11	I/O12	I/O13	I/O14	I/O15
M15	I/O8	I/O9	I/O10	I/O11	I/O12	I/O13	I/O14	I/O15

I/O Cell	Available Macrocells							
I/O0	M0	M1	M2	M3	M4	M5	M6	M7
I/O1	M0	M1	M2	M3	M4	M5	M6	M7
I/O2	M0	M1	M2	M3	M4	M5	M6	M7
I/O3	M0	M1	M2	M3	M4	M5	M6	M7
I/O4	M0	M1	M2	M3	M4	M5	M6	M7
I/O5	M0	M1	M2	M3	M4	M5	M6	M7
I/O6	M0	M1	M2	M3	M4	M5	M6	M7
I/O7	M0	M1	M2	M3	M4	M5	M6	M7

ispMACH 4A TIMING MODEL

The primary focus of the ispMACH 4A timing model is to accurately represent the timing in a ispMACH 4A device, and at the same time, be easy to understand. This model accurately describes all combinatorial and registered paths through the device, making a distinction between internal feedback and external feedback. A signal uses internal feedback when it is fed back into the switch matrix or block without having to go through the output buffer. The input register specifications are also reported as internal feedback. When a signal is fed back into the switch matrix after having gone through the output buffer, it is using external feedback.

The parameter, t_{BUF} , is defined as the time it takes to go from feedback through the output buffer to the I/O pad. If a signal goes to the internal feedback rather than to the I/O pad, the parameter designator is followed by an “i”. By adding t_{BUF} to this internal parameter, the external parameter is derived. For example, $t_{PD} = t_{PDi} + t_{BUF}$. A diagram representing the modularized ispMACH 4A timing model is shown in Figure 15. Refer to the application note entitled *MACH 4 Timing and High Speed Design* for a more detailed discussion about the timing parameters.



17466G-025

Figure 15. ispMACH 4A Timing Model

SPEEDLOCKING FOR GUARANTEED FIXED TIMING

The ispMACH 4A architecture allows allocation of up to 20 product terms to an individual macrocell with the assistance of an XOR gate without incurring additional timing delays.

The design of the switch matrix and PAL blocks guarantee a fixed pin-to-pin delay that is independent of the logic required by the design. Other competitive CPLDs incur serious timing delays as product terms expand beyond their typical 4 or 5 product term limits. Speed and SpeedLocking combine to give designs easy access to the performance required in today's designs.

weakly pulled up. For the circuit diagram, please refer to the document entitled *MACH Endurance Characteristics* on the Lattice Data Book CD-ROM or Lattice web site.

POWER MANAGEMENT

Each individual PAL block in ispMACH 4A devices features a programmable low-power mode, which results in power savings of up to 50%. The signal speed paths in the low-power PAL block will be slower than those in the non-low-power PAL block. This feature allows speed critical paths to run at maximum frequency while the rest of the signal paths operate in the low-power mode.

PROGRAMMABLE SLEW RATE

Each ispMACH 4A device I/O has an individually programmable output slew rate control bit. Each output can be individually configured for the higher speed transition (3 V/ns) or for the lower noise transition (1 V/ns). For high-speed designs with long, unterminated traces, the slow-slew rate will introduce fewer reflections, less noise, and keep ground bounce to a minimum. For designs with short traces or well terminated lines, the fast slew rate can be used to achieve the highest speed. The slew rate is adjusted independent of power.

POWER-UP RESET/SET

All flip-flops power up to a known state for predictable system initialization. If a macrocell is configured to SET on a signal from the control generator, then that macrocell will be SET during device power-up. If a macrocell is configured to RESET on a signal from the control generator or is not configured for set/reset, then that macrocell will RESET on power-up. To guarantee initialization values, the V_{CC} rise must be monotonic, and the clock must be inactive until the reset delay time has elapsed.

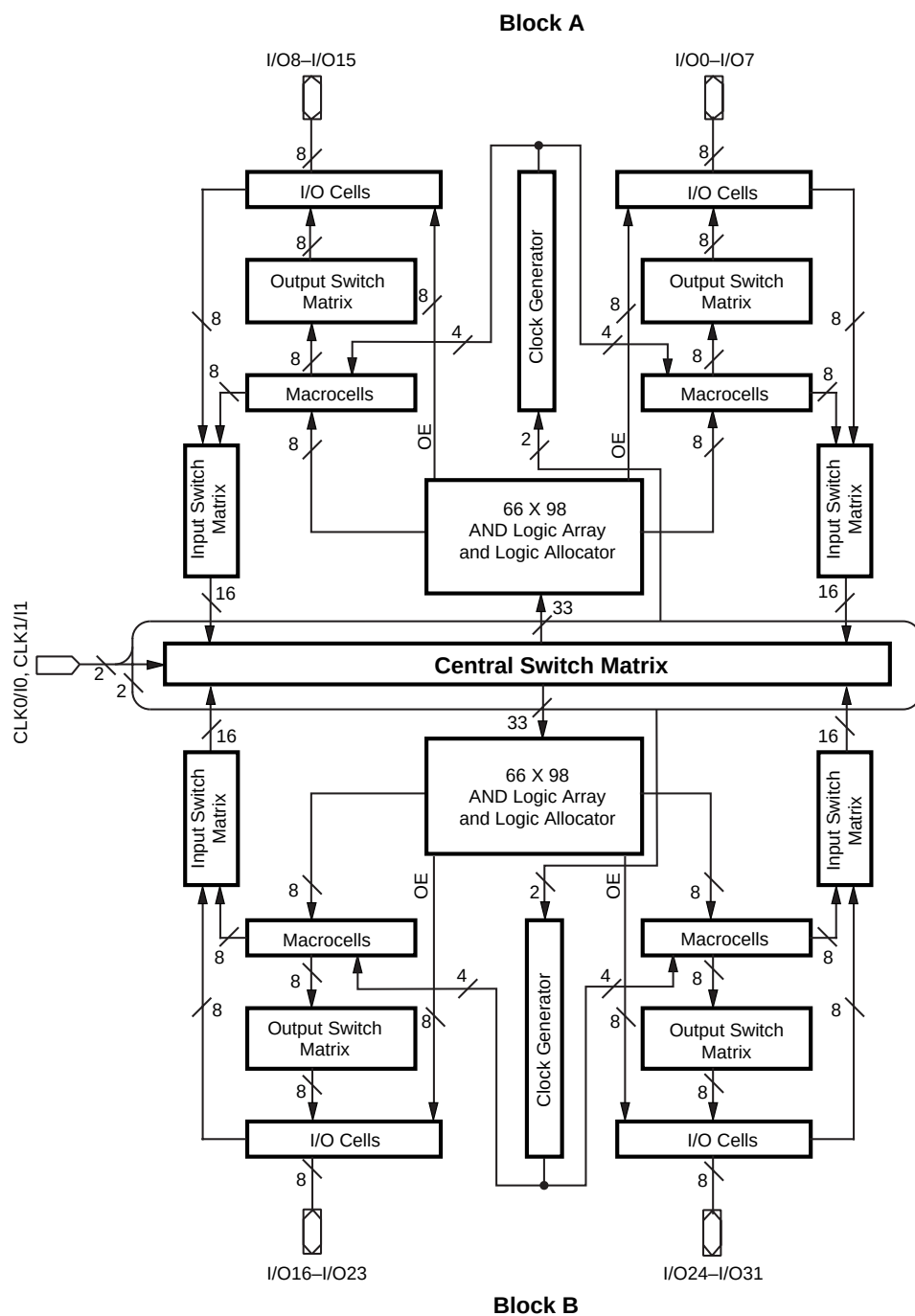
SECURITY BIT

A programmable security bit is provided on the ispMACH 4A devices as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, this bit defeats readback of the programmed pattern by a device programmer, securing proprietary designs from competitors. Programming and verification are also defeated by the security bit. The bit can only be reset by erasing the entire device.

HOT SOCKETING

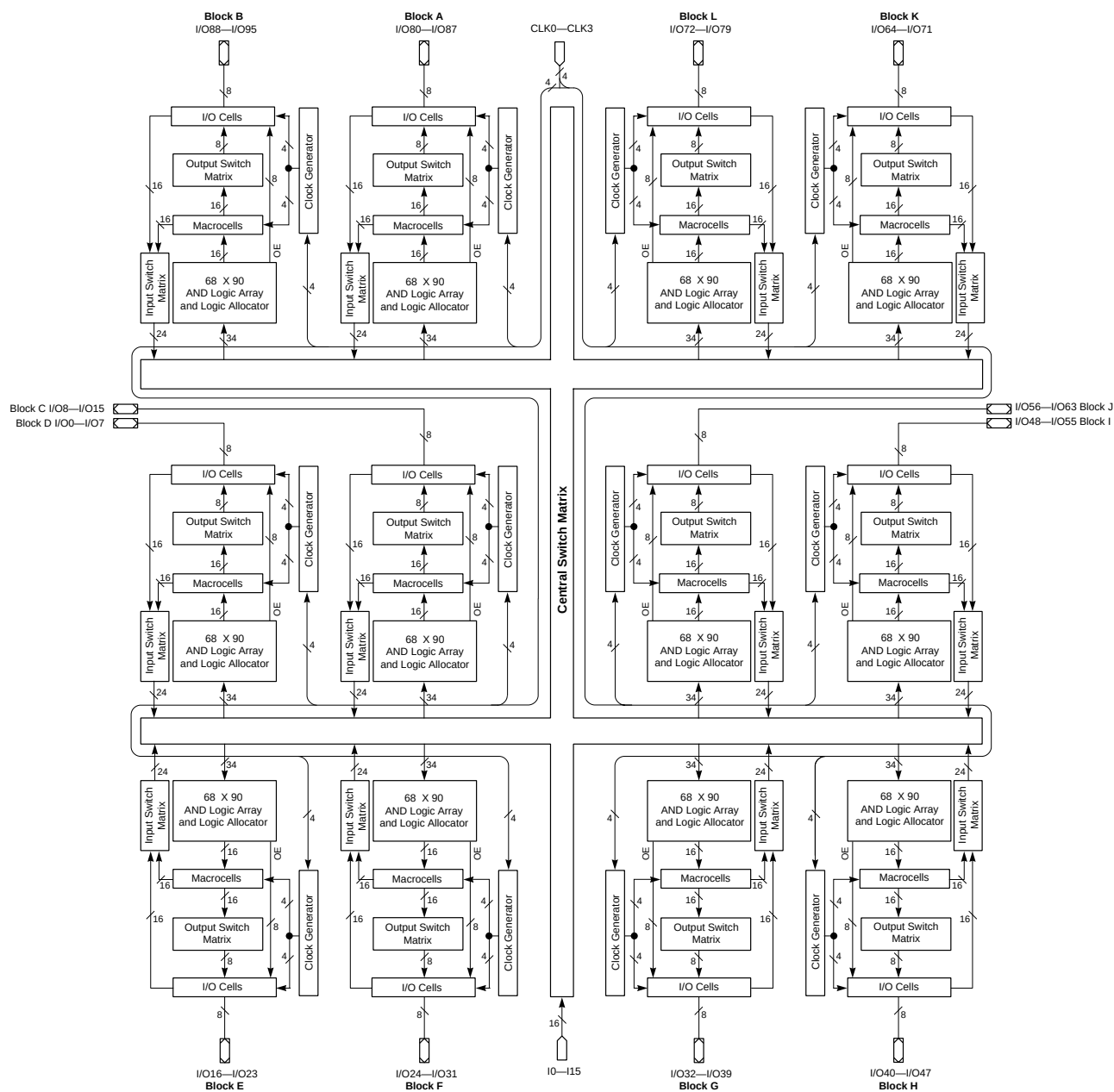
ispMACH 4A devices are well-suited for those applications that require hot socketing capability. Hot socketing a device requires that the device, when powered down, can tolerate active signals on the I/Os and inputs without being damaged. Additionally, it requires that the effects of the powered-down MACH devices be minimal on active signals.

BLOCK DIAGRAM – M4A(3,5)-32/32



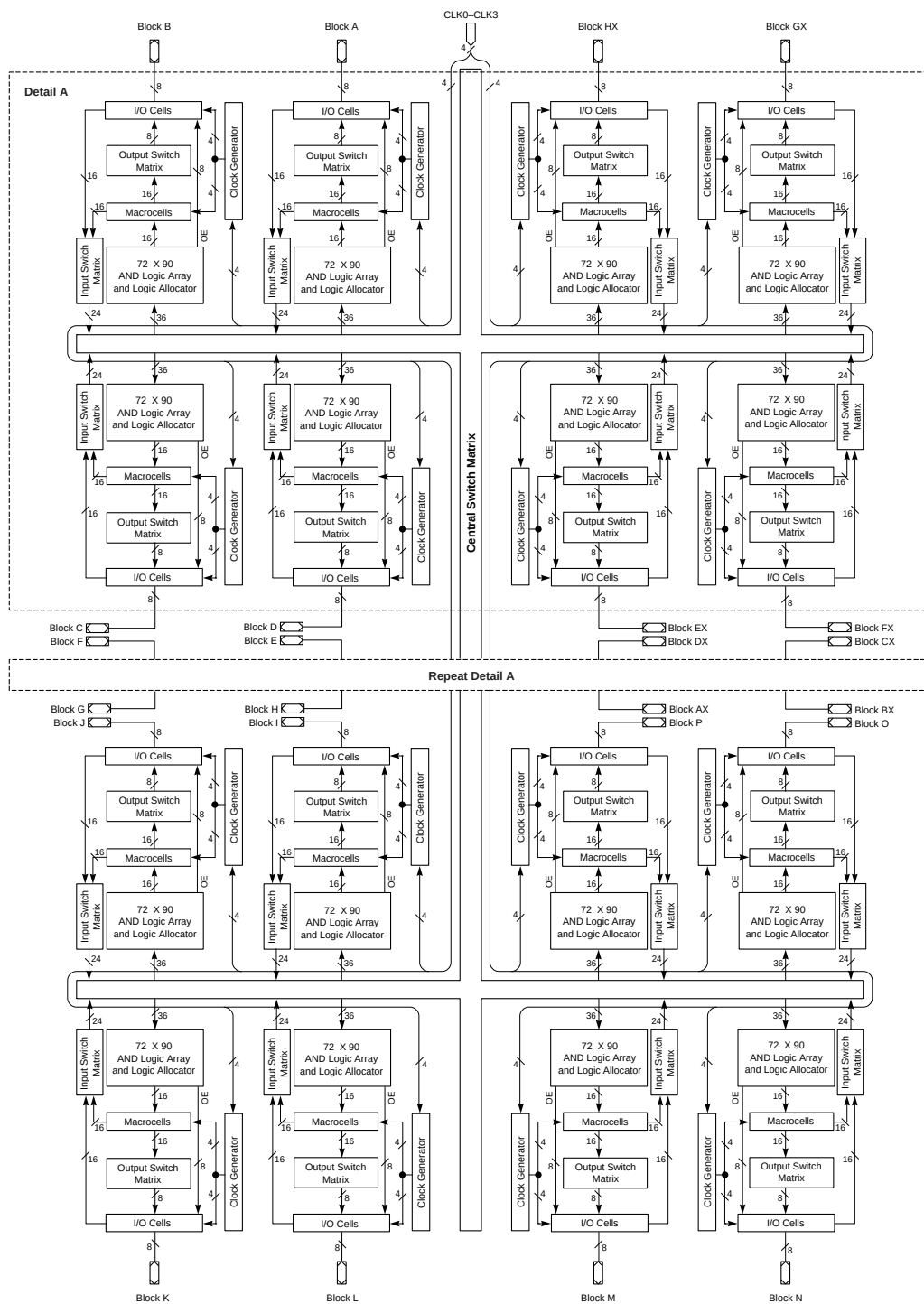
17466H-019

BLOCK DIAGRAM – M4A(3,5)-192/96



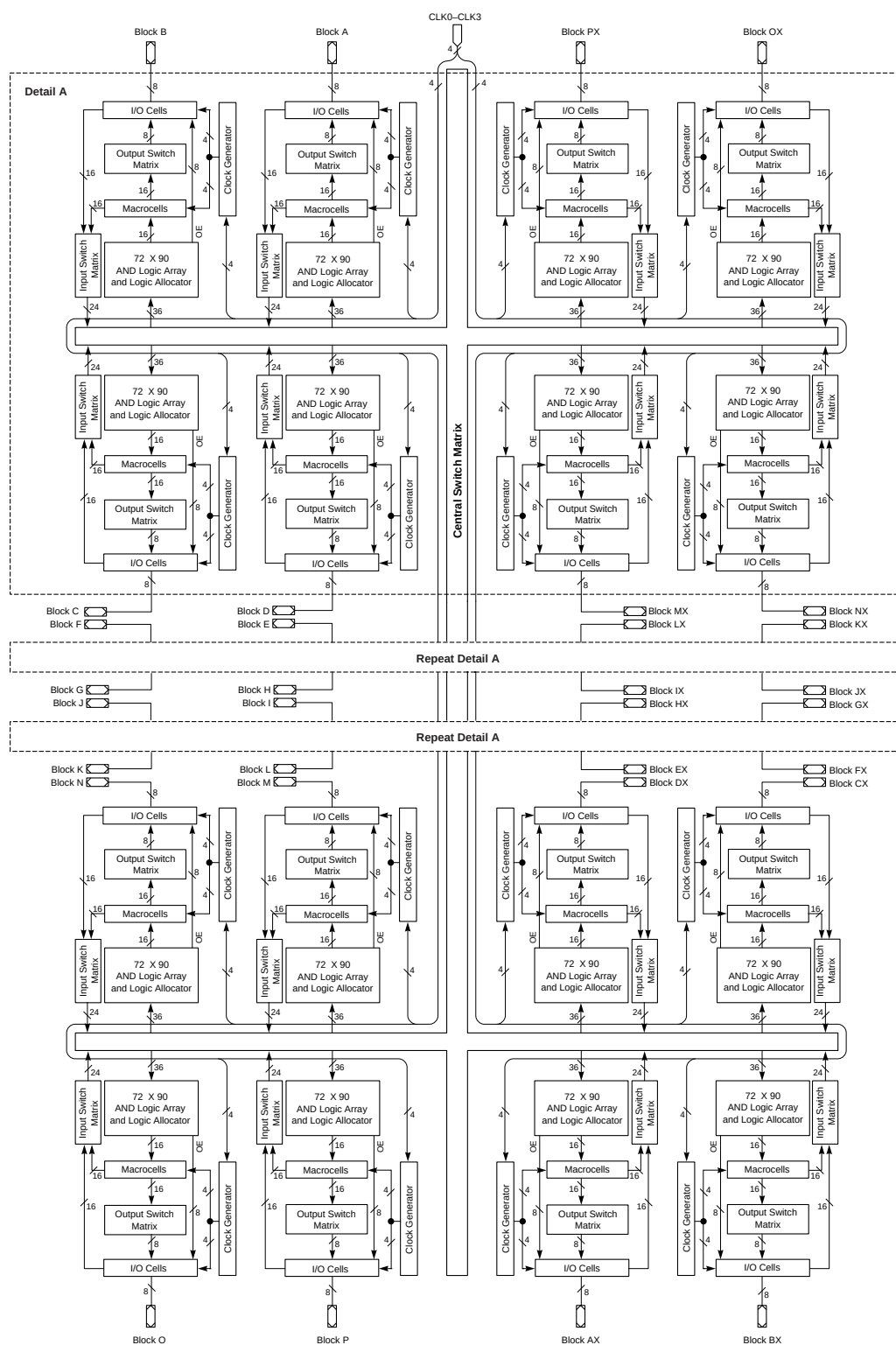
17466G-067

BLOCK DIAGRAM – M4A3-384/160, M4A3-384/192



17466G-067

BLOCK DIAGRAM - M4A3-512/160, M4A3-512/192, M4A3-512/256



17466G-068

ispMACH 4A TIMING PARAMETERS OVER OPERATING RANGES¹

		-5		-55		-6		-65		-7		-10		-12		-14		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Combinatorial Delay:																		
t _{PDi}	Internal combinatorial propagation delay		3.5		4.0		4.3		4.5		5.0		7.0		9.0		11.0	ns
t _{PD}	Combinatorial propagation delay		5.0		5.5		6.0		6.5		7.5		10.0		12.0		14.0	ns
Registered Delays:																		
t _{SS}	Synchronous clock setup time, D-type register	3.0		3.5		3.5		3.5		5.0		5.5		7.0		10.0		ns
t _{SST}	Synchronous clock setup time, T-type register	4.0		4.0		4.0		4.0		6.0		6.5		8.0		11.0		ns
t _{SA}	Asynchronous clock setup time, D-type register	2.5		2.5		2.5		3.0		3.5		4.0		5.0		8.0		ns
t _{SAT}	Asynchronous clock setup time, T-type register	3.0		3.0		3.0		3.5		4.5		5.0		6.0		9.0		ns
t _{HS}	Synchronous clock hold time	0.0		0.0		0.0		0.0		0.0		0.0		0.0		0.0		ns
t _{HA}	Asynchronous clock hold time	2.5		2.5		2.5		3.0		3.5		4.0		5.0		8.0		ns
t _{COSi}	Synchronous clock to internal output		2.5		2.5		2.8		3.0		3.0		3.0		3.5		3.5	ns
t _{COS}	Synchronous clock to output		4.0		4.0		4.5		5.0		5.5		6.0		6.5		6.5	ns
t _{COAi}	Asynchronous clock to internal output		5.0		5.0		5.0		5.0		6.0		8.0		10.0		12.0	ns
t _{COA}	Asynchronous clock to output		6.5		6.5		6.8		7.0		8.5		11.0		13.0		15.0	ns
Latched Delays:																		
t _{SSL}	Synchronous latch setup time	4.0		4.0		4.0		4.5		6.0		7.0		8.0		10.0		ns
t _{SAL}	Asynchronous latch setup time	3.0		3.0		3.5		3.5		4.0		4.0		5.0		8.0		ns
t _{HSL}	Synchronous latch hold time	0.0		0.0		0.0		0.0		0.0		0.0		0.0		0.0		ns
t _{HAL}	Asynchronous latch hold time	3.0		3.0		3.5		3.5		4.0		4.0		5.0		8.0		ns
t _{PDLi}	Transparent latch to internal output		5.5		5.5		5.8		6.0		7.5		9.0		11.0		12.0	ns
t _{PDL}	Propagation delay through transparent latch to output		7.0		7.0		7.5		8.0		10.0		12.0		14.0		15.0	ns
t _{GOSi}	Synchronous gate to internal output		3.0		3.0		3.0		3.0		3.5		4.5		7.0		8.0	ns
t _{GOS}	Synchronous gate to output		4.5		4.5		4.8		5.0		6.0		7.5		10.0		11.0	ns
t _{GOAi}	Asynchronous gate to internal output		6.0		6.0		6.0		6.0		8.5		10.0		13.0		15.0	ns
t _{GOA}	Asynchronous gate to output		7.5		7.5		7.8		8.0		11.0		13.0		16.0		18.0	ns
Input Register Delays:																		
t _{SIRS}	Input register setup time	1.5		1.5		2.0		2.0		2.0		2.0		2.0		2.0		ns
t _{HIRS}	Input register hold time	2.5		2.5		3.0		3.0		3.0		3.0		3.0		4.0		ns
t _{ICOSi}	Input register clock to internal feedback		3.0		3.0		3.0		3.0		3.5		4.5		6.0		6.0	ns
Input Latch Delays:																		
t _{SIL}	Input latch setup time	1.5		1.5		1.5		2.0		2.0		2.0		2.0		2.0		ns
t _{HIL}	Input latch hold time	2.5		2.5		2.5		3.0		3.0		3.0		3.0		4.0		ns
t _{IGOSi}	Input latch gate to internal feedback		3.5		3.5		3.8		4.0		4.0		4.0		4.0		5.0	ns
t _{PDILi}	Transparent input latch to internal feedback		1.5		1.5		1.5		1.5		2.0		2.0		2.0		2.0	ns

ispMACH 4A TIMING PARAMETERS OVER OPERATING RANGES¹

		-5		-55		-6		-65		-7		-10		-12		-14		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Frequency:																		
f _{MAXS}	External feedback, D-type, Min of 1/(t _{WLS} + t _{WHS}) or 1/(t _{SS} + t _{COS})	143		133		125		118		95.2		87.0		74.1		60.6		MHz
	External feedback, T-type, Min of 1/(t _{WLS} + t _{WHS}) or 1/(t _{SST} + t _{COS})	125		125		118		111		87.0		80.0		69.0		57.1		MHz
	Internal feedback (f _{CNT}), D-type, Min of 1/(t _{WLS} + t _{WHS}) or 1/(t _{SS} + t _{COSi})	182		167		160		154		125		118		95.0		74.1		MHz
	Internal feedback (f _{CNT}), T-type, Min of 1/(t _{WLS} + t _{WHS}) or 1/(t _{SST} + t _{COSi})	154		154		148		143		111		105		87.0		69.0		MHz
	No feedback ² , Min of 1/(t _{WLS} + t _{WHS}), 1/(t _{SS} + t _{HS}) or 1/(t _{SST} + t _{HS})	250		250		200		200		154		125		100		83.3		MHz
f _{MAXA}	External feedback, D-type, Min of 1/(t _{WLA} + t _{WHA}) or 1/(t _{SA} + t _{COA})	111		111		108		100		83.3		66.7		55.6		43.5		MHz
	External feedback, T-type, Min of 1/(t _{WLA} + t _{WHA}) or 1/(t _{SAT} + t _{COA})	105		105		102		95.2		76.9		62.5		52.6		41.7		MHz
	Internal feedback (f _{CNTA}), D-type, Min of 1/(t _{WLA} + t _{WHA}) or 1/(t _{SA} + t _{COAi})	133		133		125		125		105		83.3		66.7		50.0		MHz
	Internal feedback (f _{CNTA}), T-type, Min of 1/(t _{WLA} + t _{WHA}) or 1/(t _{SAT} + t _{COAi})	125		125		125		118		95.2		76.9		62.5		47.6		MHz
	No feedback ² , Min of 1/(t _{WLA} + t _{WHA}), 1/(t _{SA} + t _{HA}) or 1/(t _{SAT} + t _{HA})	167		167		143		143		125		100		62.5		55.6		MHz
f _{MAXI}	Maximum input register frequency, Min of 1/(t _{WIRH} + t _{WIRL}) or 1/(t _{SIRS} + t _{HIRS})	167		167		143		143		125		100		83.3		83.3		MHz

Notes:

1. See "Switching Test Circuit" document on the Literature Download page of the Lattice web site.
2. This parameter does not apply to flip-flops in the emulated mode since the feedback path is required for emulation.

CAPACITANCE¹

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input capacitance	$V_{IN}=2.0\text{ V}$	3.3 V or 5 V, 25°C, 1 MHz	6	pF
$C_{I/O}$	Output capacitance	$V_{OUT}=2.0\text{ V}$	3.3 V or 5 V, 25°C, 1 MHz	8	pF

Note:

1. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where this parameter may be affected.

I_{CC} vs. FREQUENCY

These curves represent the typical power consumption for a particular device at system frequency. The selected “typical” pattern is a 16-bit up-down counter. This pattern fills the device and exercises every macrocell. Maximum frequency shown uses internal feedback and a D-type register. Power/Speed are optimized to obtain the highest counter frequency and the lowest power. The highest frequency (LSBs) is placed in common PAL blocks, which are set to high power. The lowest frequency signals (MSBs) are placed in a common PAL block and set to lowest power.

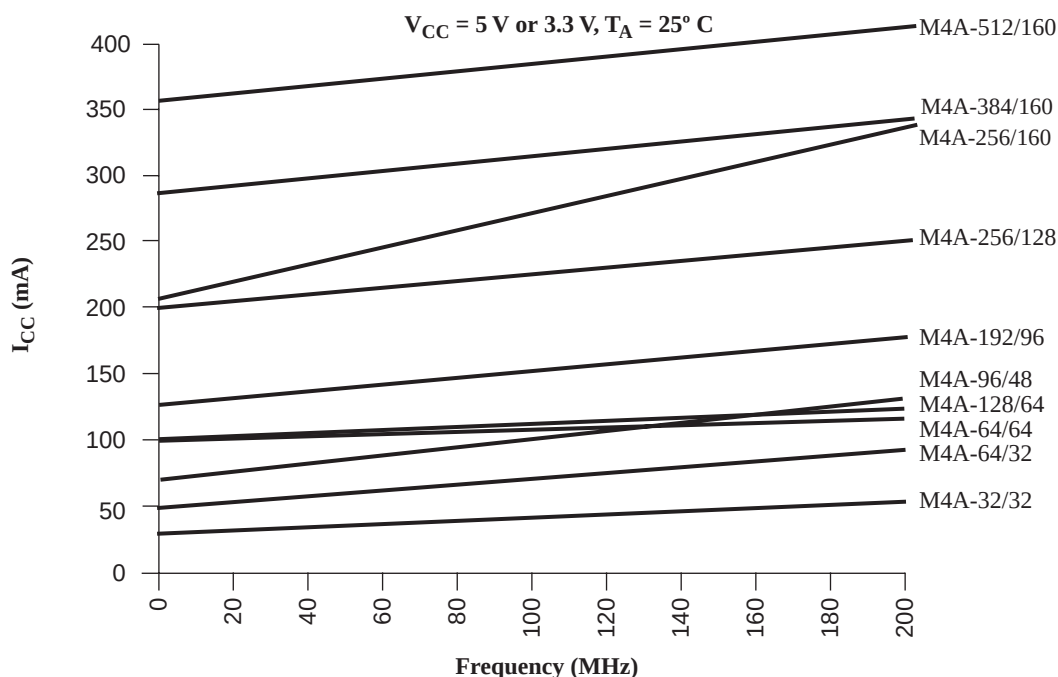


Figure 19. ispMACH 4A I_{CC} Curves at High Speed Mode

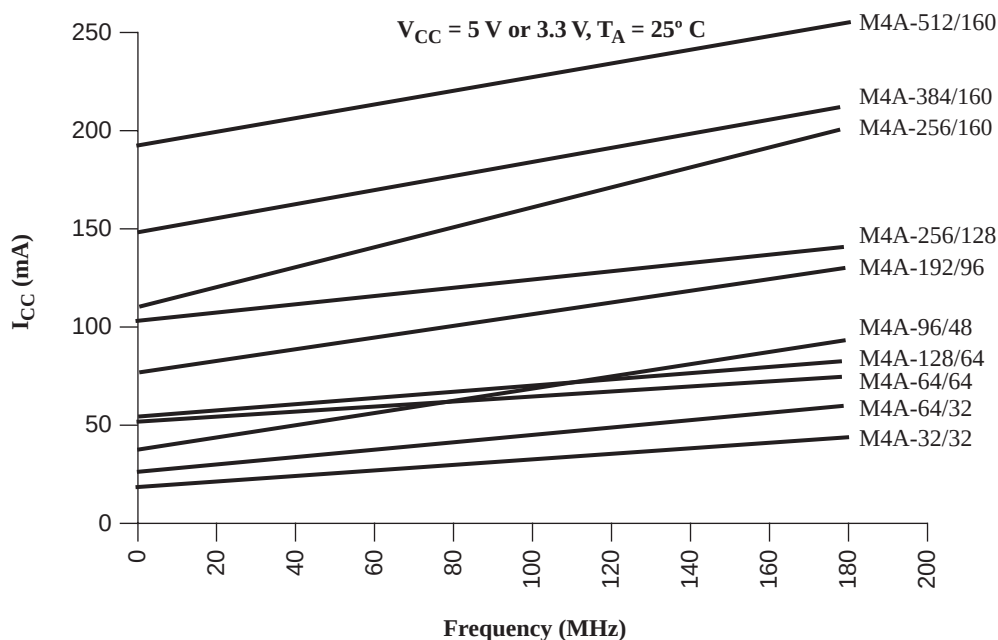


Figure 20. ispMACH 4A I_{CC} Curves at Low Power Mode

100-BALL caBGA CONNECTION DIAGRAM (M4A3-128/64)

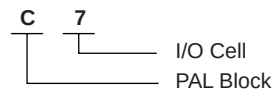
Bottom View

100-Ball caBGA

	10	9	8	7	6	5	4	3	2	1	
A	GND	I/O63 H7	I/O60 H4	I/O57 H1	GND	GND	I/O1 A1	I/O4 A4	I/O7 A7	GND	A
B	TRST	GND	I/O61 H5	I5	VCC	I/O0 A0	I/O6 A6	GND	TDI	I/O15 B7	B
C	I/O53 G5	TDO	I/O62 H6	I/O58 H2	I/O56 H0	I/O2 A2	GND	I/O14 B6	I/O13 B5	I/O12 B4	C
D	I/O50 G2	I/O55 G7	GND	I/O59 H3	I/O3 A3	I/O5 A5	I/O11 B3	I/O10 B2	CLK0/I0	I/O9 B1	D
E	CLK3/I4	I/O49 G1	I/O51 G3	I/O54 G6	VCC	I/O16 C0	I/O20 C4	I/O8 B0	VCC	GND	E
F	GND	VCC	I/O40 F0	I/O52 G4	I/O48 G0	VCC	I/O22 C6	I/O19 C3	I/O17 C1	CLK1/I1	F
G	I/O41 F1	CLK2/I3	I/O42 F2	I/O43 F3	I/O37 E5	I/O35 E3	I/O27 D3	GND	I/O23 C7	I/O18 C2	G
H	I/O44 F4	I/O45 F5	I/O46 F6	GND	I/O34 E2	I/O24 D0	I/O26 D2	I/O30 D6	TCK	I/O21 C5	H
J	I/O47 F7	ENABLE	GND	I/O38 E6	I/O32 E0	VCC	I2	I/O29 D5	GND	TMS	J
K	GND	I/O39 E7	I/O36 E4	I/O33 E1	GND	GND	I/O25 D1	I/O28 D4	I/O31 D7	GND	K
	10	9	8	7	6	5	4	3	2	1	

PIN DESIGNATIONS

CLK = Clock
 GND = Ground
 I = Input
 I/O = Input/Output
 N/C = No Connect
 VCC = Supply Voltage
 TDI = Test Data In
 TCK = Test Clock
 TMS = Test Mode Select
 TDO = Test Data Out
 TRST = Test Reset
 ENABLE = Program

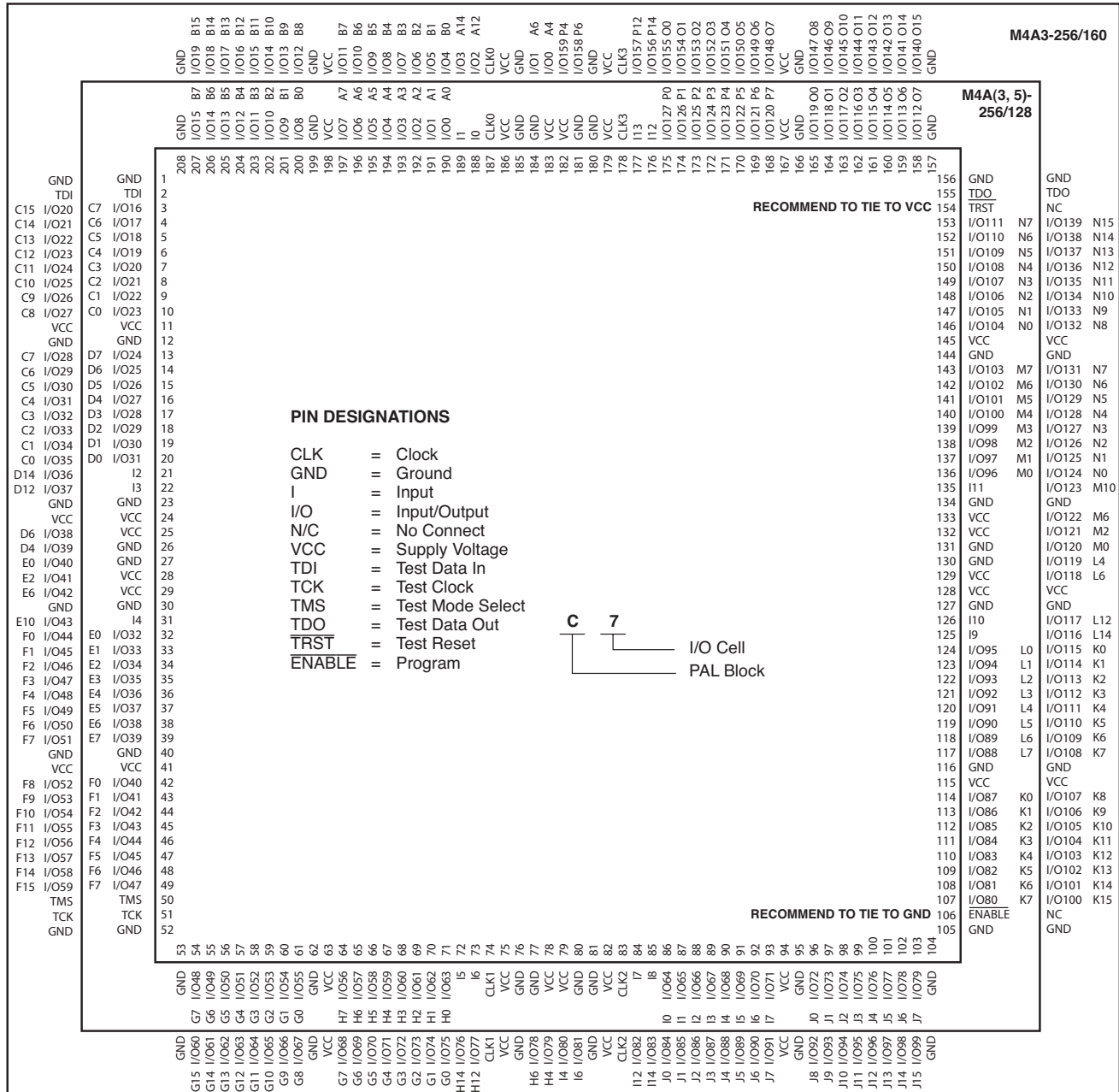


17466G-100cabga

208-PIN PQFP CONNECTION DIAGRAM (M4A(3,5)-256/128 AND M4A3-256/160)

Top View

208-Pin PQFP

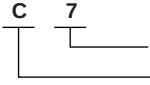


17466G-044

256-BALL BGA CONNECTION DIAGRAM (M4A3-256/128)

Bottom View

256-Ball BGA

	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	GND	N/C	GND	I/O108 N4	I/O105 N1	GND	I/O100 M4	I/O96 M0	GND	GND	GND	GND	I/O95 L0	I/O91 L4	GND	I/O87 K0	N/C	GND	GND	GND	A
B	GND	I/O113 O6	N/C	I/O109 N5	I/O106 N2	I/O103 M7	I/O102 M6	I/O98 M2	N/C	I11	N/C	N/C	I/O93 L2	I/O89 L6	I/O88 L7	I/O85 K2	I/O83 K4	I/O82 K5	N/C	GND	B
C	I/O116 O3	N/C	VCC	TRST	I/O111 N7	I/O107 N3	I/O104 N0	I/O101 M5	I/O97 M1	N/C	I10	I/O94 L1	I/O90 L5	I/O86 K1	I/O84 K3	I/O80 K7	ENABLE	VCC	I/O78 J6	I/O74 J2	C
D	I/O120 P7	I/O117 O2	I/O112 O7	VCC	VCC	I/O110 N6	VCC	N/C	I/O99 M3	N/C	I9	I/O92 L3	N/C	VCC	I/O81 K6	VCC	VCC	I/O79 J7	I/O75 J3	I/O71 I7	D
E	I/O123 P4	I/O119 O0	I/O114 O5	TDI	PIN DESIGNATIONS CLK = Clock GND = Ground I = Input I/O = Input/Output N/C = No Connect VCC = Supply Voltage TDI = Test Data In TCK = Test Clock TMS = Test Mode Select TDO = Test Data Out TRST = Test Reset ENABLE = Program  I/O Cell PAL Block												TDO	I/O77 J5	I/O72 J0	I/O68 I4	E
F	GND	I/O122 P5	I/O118 O1	I/O115 O4													I/O76 J4	I/O73 J1	I/O69 I5	GND	F
G	I12	I/O125 P2	I/O121 P6	VCC													VCC	I/O70 I6	I/O65 I1	I8	G
H	GND	I/O127 P0	I/O126 P1	I/O124 P3													I/O67 I3	I/O66 I2	I/O64 I0	GND	H
J	N/C	N/C	N/C	I13													I7	N/C	N/C	N/C	J
K	GND	CLK3	N/C	N/C													N/C	N/C	CLK2	N/C	K
L	N/C	CLK0	N/C	N/C													N/C	N/C	CLK1	GND	L
M	N/C	N/C	N/C	I0													I6	N/C	I/O63 H0	I/O62 H1	M
N	GND	I/O0 A0	I/O2 A2	I/O3 A3													I/O60 H3	I/O61 H2	I/O59 H4	GND	N
P	I1	I/O1 A1	I/O6 A6	VCC													VCC	I/O57 H6	I/O58 H5	I5	P
R	GND	I/O5 A5	I/O9 B1	N/C													I/O51 G4	I/O54 G1	I/O56 H7	GND	R
T	I/O4 A4	I/O8 B0	I/O12 B4	TCK													TMS	I/O50 G5	I/O55 G0	N/C	T
U	I/O7 A7	I/O11 B3	I/O15 B7	VCC	VCC	I/O18 C5	VCC	I/O24 D7	I/O29 D2	I2	N/C	I/O35 E3	N/C	VCC	N/C	VCC	VCC	I/O48 G7	I/O53 G2	N/C	U
V	I/O10 B2	I/O13 B5	VCC	I/O16 C7	I/O17 C6	I/O21 C2	I/O23 C0	I/O27 D4	I/O31 D0	I3	N/C	I/O33 E1	I/O37 E5	I/O41 F1	I/O43 F3	I/O46 F6	I/O47 F7	VCC	I/O52 G3	N/C	V
W	GND	I/O14 B6	N/C	N/C	I/O19 C4	I/O22 C1	I/O25 D6	I/O28 D3	N/C	N/C	I4	N/C	I/O34 E2	I/O38 E6	I/O39 E7	I/O42 F2	I/O45 F5	N/C	I/O49 G6	GND	W
Y	GND	GND	GND	N/C	I/O20 C3	GND	I/O26 D5	I/O30 D1	GND	GND	GND	GND	I/O32 E0	I/O36 E4	GND	I/O40 F0	I/O44 F4	GND	N/C	GND	Y
	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

17466G-045

388-BALL fpBGA CONNECTION DIAGRAM (M4A3-512/256)

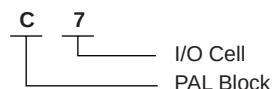
Bottom View

388-Ball fpBGA

	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	GND	I/O243 OX3	I/O240 OX0	I/O241 OX1	I/O236 NX4	I/O231 MX7	I/O228 MX4	I/O226 MX2	I/O255 PX7	I/O251 PX3	I/O248 PX0	I/O0 A0	I/O5 A5	I/O6 A6	I/O27 D3	I/O30 D6	I/O17 C1	I/O22 C6	I/O8 B0	I/O10 B2	N/C	GND	A
B	N/C	GND	I/O245 OX5	I/O242 OX2	I/O238 NX6	I/O234 NX2	I/O232 NX0	I/O229 MX5	I/O224 MX0	I/O253 PX5	I/O249 PX1	I/O2 A2	CLK0	I/O26 D2	I/O29 D5	I/O31 D7	I/O20 C4	I/O9 B1	I/O12 B4	I/O13 B5	GND	TDI	B
C	I/O213 KX5	TDO	GND	I/O247 OX7	I/O244 OX4	I/O239 NX7	I/O235 NX3	I/O230 MX6	I/O227 MX3	CLK3	I/O250 PX2	I/O1 A1	I/O7 A7	I/O25 D1	I/O16 C0	I/O18 C2	I/O23 C7	I/O11 B3	I/O15 B7	GND	I/O47 F7	I/O44 F4	C
D	I/O210 KX2	I/O212 KX4	I/O215 KX7	GND	I/O246 OX6	VCC	I/O237 NX5	I/O233 NX1	VCC	I/O254 PX6	VCC	I/O3 A3	I/O24 D0	VCC	I/O19 C3	I/O21 C5	VCC	I/O14 B6	GND	I/O46 F6	I/O43 F3	I/O41 F1	D
E	I/O207 JX7	I/O209 KX1	I/O211 KX3	I/O214 KX6															I/O45 F5	I/O42 F2	I/O40 F0	I/O54 G6	E
F	I/O203 JX3	I/O205 JX5	I/O208 KX0	VCC															VCC	I/O55 G7	I/O52 G4	I/O50 G2	F
G	I/O200 JX0	I/O202 JX2	I/O204 JX4	I/O206 JX6			VCC	VCC	N/C	I/O225 MX1	I/O252 PX4	I/O4 A4	I/O28 D4	N/C	VCC	VCC			I/O53 G5	I/O51 G3	I/O49 G1	I/O39 E7	G
H	I/O221 LX5	I/O222 LX6	I/O223 LX7	I/O201 JX1			VCC	N/C	GND	GND	GND	GND	GND	GND	N/C	VCC			I/O48 G0	I/O38 E6	I/O37 E5	I/O36 E4	H
J	I/O218 LX2	I/O219 LX3	I/O220 LX4	VCC			N/C	GND	GND	GND	GND	GND	GND	GND	GND	N/C			VCC	I/O35 E3	I/O34 E2	I/O32 E0	J
K	I/O197 IX5	I/O198 IX6	I/O199 IX7	I/O216 LX0			I/O217 LX1	GND	GND	GND	GND	GND	GND	GND	GND	I/O33 E1			I/O63 H7	I/O62 H6	I/O61 H5	I/O60 H4	K
L	I/O192 IX0	I/O194 IX2	I/O195 IX3	I/O196 IX4			I/O193 IX1	GND	GND	GND	GND	GND	GND	GND	GND	I/O58 H2			VCC	I/O59 H3	I/O57 H1	I/O56 H0	L
M	I/O184 HX0	I/O185 HX1	I/O187 HX3	VCC			I/O186 HX2	GND	GND	GND	GND	GND	GND	GND	GND	I/O69 I5			I/O67 I3	I/O65 I1	I/O66 I2	I/O64 I0	M
N	I/O188 HX4	I/O189 HX5	I/O191 HX7	I/O190 HX6			I/O162 EX2	GND	GND	GND	GND	GND	GND	GND	GND	I/O89 L1			I/O88 L0	I/O71 I7	I/O70 I6	I/O68 I4	N
P	I/O160 EX0	I/O161 EX1	I/O163 EX3	VCC			N/C	GND	GND	GND	GND	GND	GND	GND	GND	N/C			VCC	I/O92 L4	I/O91 L3	I/O90 L2	P
R	I/O164 EX4	I/O165 EX5	I/O166 EX6	I/O177 GX1			VCC	N/C	GND	GND	GND	GND	GND	GND	N/C	VCC			I/O74 J2	I/O95 L7	I/O94 L6	I/O93 L5	R
T	I/O167 EX7	I/O176 GX0	I/O179 GX3	I/O181 GX5			VCC	VCC	N/C	I/O152 DX0	I/O131 AX3	I/O122 P2	I/O98 M2	N/C	VCC	VCC			I/O78 J6	I/O76 J4	I/O73 J1	I/O72 J0	T
U	I/O178 GX2	I/O180 GX4	I/O183 GX7	VCC															VCC	I/O80 K0	I/O77 J5	I/O75 J3	U
V	I/O182 GX6	N/C	I/O169 FX1	I/O172 FX4															I/O86 K6	I/O83 K3	I/O81 K1	I/O79 J7	V
W	I/O168 FX0	I/O170 FX2	I/O173 FX5	GND	I/O143 BX7	VCC	I/O150 CX6	I/O145 CX1	VCC	I/O153 DX1	I/O123 P3	VCC	I/O96 M0	VCC	I/O104 N0	I/O111 N7	VCC	I/O119 O7	GND	I/O87 K7	I/O84 K4	I/O82 K2	W
Y	I/O171 FX3	I/O174 FX6	GND	I/O141 BX5	I/O138 BX2	I/O136 BX0	I/O147 CX3	I/O158 DX6	I/O156 DX4	CLK2	I/O132 AX4	I/O121 P1	I/O125 P5	I/O99 M3	I/O101 M5	I/O106 N2	I/O110 N6	I/O115 O3	I/O118 O6	GND	TMS	I/O85 K5	Y
AA	I/O175 FX7	GND	I/O142 BX6	I/O140 BX4	I/O151 CX7	I/O149 CX5	I/O144 CX0	I/O157 DX5	I/O154 DX2	I/O134 AX6	I/O130 AX2	I/O128 AX0	CLK1	I/O127 P7	I/O100 M4	I/O103 M7	I/O108 N4	I/O109 N5	I/O113 O1	I/O116 O4	GND	TCK	AA
AB	GND	N/C	I/O139 BX3	I/O137 BX1	I/O148 CX4	I/O146 CX2	I/O159 DX7	I/O155 DX3	I/O135 AX7	I/O133 AX5	I/O129 AX1	I/O120 P0	I/O124 P4	I/O126 P6	I/O97 M1	I/O102 M6	I/O105 N1	I/O107 N3	I/O112 O0	I/O114 O2	I/O117 O5	GND	AB

PIN DESIGNATIONS

CLK = Clock
 GND = Ground
 I = Input
 I/O = Input/Output
 N/C = No Connect
 VCC = Supply Voltage
 TDI = Test Data In
 TCK = Test Clock
 TMS = Test Mode Select
 TDO = Test Data Out



m4a3.512.256_388bga

5V Commercial Combinations		
M4A5-32/32	-5, -7, -10,	JC, VC, VC48
M4A5-64/32	-55, -7, -10	JC, VC, VC48
M4A5-96/48		VC
M4A5-128/64		YC, VC
M4A5-192/96	-6, -7, -10	VC
M4A5-256/128	-65, -7, -10	YC

5V Industrial Combinations		
M4A5-32/32	-7, -10, -12	JJ, VI, VI48
M4A5-64/32	-7, -10, -12	JJ, VI, VI48
M4A5-96/48		VI
M4A5-128/64		YI, VI
M4A5-192/96	-7, -10, -12	VI
M4A5-256/128	-10, -12	YI

Lead-free Packaging

3.3V Commercial Combinations		
M4A3-32/32	-5, -7, -10	VNC, VNC48, JNC
M4A3-64/32	-55, -7, -10	VNC, VNC48, JNC
M4A3-64/64		VNC
M4A3-128/64		VNC
M4A3-192/96	-6, -7, -10	VNC
M4A3-256/128	-55, -7, -10	FANC, YNC
M4A3-256/160	-7, -10	YNC
M4A3-256/192		FANC
M4A3-384/192	-65, -10, -12	FANC
M4A3-512/192	-7, -10, -12	FANC

3.3V Industrial Combinations		
M4A3-32/32	-7, -10, -12	VNI, VNI48, JNI
M4A3-64/32		VNI, VNI48, JNI
M4A3-64/64		VNI
M4A3-128/64		VNI
M4A3-192/96	-10, -12	VNI
M4A3-256/128		FANI, YNI
M4A3-256/160		YNI
M4A3-256/192	-10, -12, -14	FANI
M4A3-384/192		FANI
M4A3-512/192		FANI

5V Commercial Combinations		
M4A5-32/32	-5, -7, -10	VNC, VNC48, JNC
M4A5-64/32	-55, -7, -10	VNC, VNC48, JNC
M4A5-96/48		VNC
M4A5-128/64		VNC, YNC
M4A5-192/96	-6, -7, -10	VNC
M4A5-256/128	-65, -7, -10	YNC

5V Industrial Combinations		
M4A5-32/32	-7, -10, -12	VNI, VNI48, JNI
M4A5-64/32		VNI, VNI48, JNI
M4A5-96/48		VNI
M4A5-128/64		VNI, YNI
M4A5-192/96		VNI
M4A5-256/128		YNI

Most ispMACH devices are dual-marked with both Commercial and Industrial grades. The Industrial speed grade is slower, i.e., M4A3-256/128-7YC-10YI

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local Lattice sales office to confirm availability of specific valid combinations and to check on newly released combinations.