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Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	7.5 ns
Voltage Supply - Internal	4.5V ~ 5.5V
Number of Logic Elements/Blocks	-
Number of Macrocells	192
Number of Gates	-
Number of I/O	96
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/m4a5-192-96-7vi

Table 1. ispMACH 4A Device Features

3.3 V Devices								
Feature	**M4A3-32**	**M4A3-64**	**M4A3-96**	**M4A3-128**	**M4A3-192**	**M4A3-256**	**M4A3-384**	**M4A3-512**
Macrocells	32	64	96	128	192	256	384	512
User I/O options	32	32/64	48	64	96	128/160/192	160/192	160/192/256
t_{PD} (ns)	5.0	5.5	5.5	5.5	6.0	5.5	6.5	7.5
f_{CNT} (MHz)	182	167	167	167	160	167	154	125
t_{COS} (ns)	4.0	4.0	4.0	4.0	4.5	4.0	4.5	5.5
t_{SS} (ns)	3.0	3.5	3.5	3.5	3.5	3.5	3.5	5.0
Static Power (mA)	20	25/52	40	55	85	110/150	149/155	179
JTAG Compliant	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
PCI Compliant	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes

5 V Devices						
Feature	**M4A5-32**	**M4A5-64**	**M4A5-96**	**M4A5-128**	**M4A5-192**	**M4A5-256**
Macrocells	32	64	96	128	192	256
User I/O options	32	32	48	64	96	128
t_{PD} (ns)	5.0	5.5	5.5	5.5	6.0	6.5
f_{CNT} (MHz)	182	167	167	167	160	154
t_{COS} (ns)	4.0	4.0	4.0	4.0	4.5	5.0
t_{SS} (ns)	3.0	3.5	3.5	3.5	3.5	3.5
Static Power (mA)	20	25	40	55	74	110
JTAG Compliant	Yes	Yes	Yes	Yes	Yes	Yes
PCI Compliant	Yes	Yes	Yes	Yes	Yes	Yes

The ispMACH 4A family offers 20 density-I/O combinations in Thin Quad Flat Pack (TQFP), Plastic Quad Flat Pack (PQFP), Plastic Leaded Chip Carrier (PLCC), Ball Grid Array (BGA), fine-pitch BGA (fpBGA), and chip-array BGA (caBGA) packages ranging from 44 to 388 pins (Table 3). It also offers I/O safety features for mixed-voltage designs so that the 3.3-V devices can accept 5-V inputs, and 5-V devices do not overdrive 3.3-V inputs. Additional features include Bus-Friendly inputs and I/Os, a programmable power-down mode for extra power savings and individual output slew rate control for the highest speed transition or for the lowest noise transition.

Table 3. ispMACH 4A Package and I/O Options (Number of I/Os and dedicated inputs in Table)

3.3 V Devices								
Package	**M4A3-32**	**M4A3-64**	**M4A3-96**	**M4A3-128**	**M4A3-192**	**M4A3-256**	**M4A3-384**	**M4A3-512**
44-pin PLCC	32+2	32+2						
44-pin TQFP	32+2	32+2						
48-pin TQFP	32+2	32+2						
100-pin TQFP		64+6	48+8	64+6				
100-pin PQFP				64+6				
100-ball caBGA				64+6				
144-pin TQFP					96+16			
144-ball fpBGA					96+16			
208-pin PQFP						128+14, 160	160	160
256-ball fpBGA						128+14, 192	192	192
256-ball BGA						128+14	192	
388-ball fpBGA								256

5 V Devices						
Package	**M4A5-32**	**M4A5-64**	**M4A5-96**	**M4A5-128**	**M4A5-192**	**M4A5-256**
44-pin PLCC	32+2	32+2				
44-pin TQFP	32+2	32+2				
48-pin TQFP	32+2	32+2				
100-pin TQFP			48+8	64+6		
100-pin PQFP				64+6		
144-pin TQFP					96+16	
208-pin PQFP						128+14

Product-Term Array

The product-term array consists of a number of product terms that form the basis of the logic being implemented. The inputs to the AND gates come from the central switch matrix (Table 5), and are provided in both true and complement forms for efficient logic implementation.

Table 5. PAL Block Inputs

Device	Number of Inputs to PAL Block
M4A3-32/32 and M4A5-32/32	33
M4A3-64/32 and M4A5-64/32	33
M4A3-64/64	33
M4A3-96/48 and M4A5-96/48	33
M4A3-128/64 and M4A5-128/64	33
M4A3-192/96 and M4A5-192/96	34
M4A3-256/128 and M4A5-256/128	34
M4A3-256/160 and M4A3-256/192	36
M4A3-384	36
M4A3-512	36

Logic Allocator

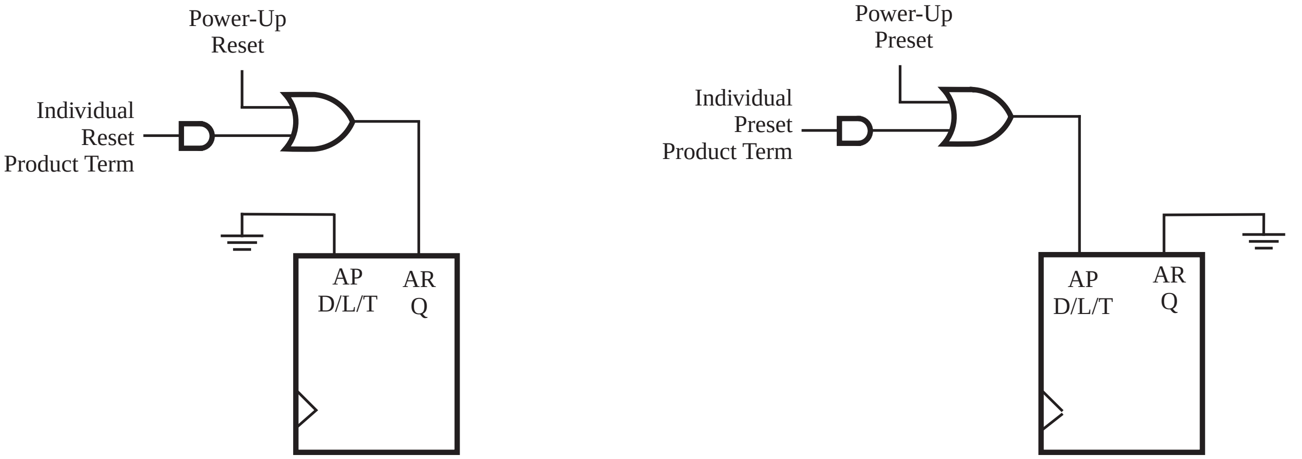
Within the logic allocator, product terms are allocated to macrocells in "product term clusters." The availability and distribution of product term clusters are automatically considered by the software as it fits functions within a PAL block. The size of a product term cluster has been optimized to provide high utilization of product terms, making complex functions using many product terms possible. Yet when few product terms are used, there will be a minimal number of unused—or wasted—product terms left over. The product term clusters available to each macrocell within a PAL block are shown in Tables 6 and 7.

Each product term cluster is associated with a macrocell. The size of a cluster depends on the configuration of the associated macrocell. When the macrocell is used in synchronous mode (Figure 2a), the basic cluster has 4 product terms. When the associated macrocell is used in asynchronous mode (Figure 2b), the cluster has 2 product terms. Note that if the product term cluster is routed to a different macrocell, the allocator configuration is not determined by the mode of the macrocell actually being driven. The configuration is always set by the mode of the macrocell that the cluster will drive if not routed away, regardless of the actual routing.

In addition, there is an extra product term that can either join the basic cluster to give an extended cluster, or drive the second input of an exclusive-OR gate in the signal path. If included with the basic cluster, this provides for up to 20 product terms on a synchronous function that uses four extended 5-product-term clusters. A similar asynchronous function can have up to 18 product terms.

When the extra product term is used to extend the cluster, the value of the second XOR input can be programmed as a 0 or a 1, giving polarity control. The possible configurations of the logic allocator are shown in Figures 3 and 4.

A reset / preset swapping feature in each macrocell allows for reset and preset to be exchanged, providing flexibility. In asynchronous mode (Figure 8), a single individual product term is provided for initialization. It can be selected to control reset or preset.



a. Reset

b. Preset

Figure 8. Asynchronous Mode Initialization Configurations

Note that the reset / preset swapping selection feature effects power-up reset as well. The initialization functionality of the flip-flops is illustrated in Table 9. The macrocell sends its data to the output switch matrix and the input switch matrix. The output switch matrix can route this data to an output if so desired. The input switch matrix can send the signal back to the central switch matrix as feedback.

Table 9. Asynchronous Reset/Preset Operation

AR	AP	CLK/LE[1]	Q+
0	0	X	See Table 8
0	1	X	1
1	0	X	0
1	1	X	0

Note:

1. *Transparent latch is unaffected by AR, AP*

weakly pulled up. For the circuit diagram, please refer to the document entitled *MACH Endurance Characteristics* on the Lattice Data Book CD-ROM or Lattice web site.

POWER MANAGEMENT

Each individual PAL block in ispMACH 4A devices features a programmable low-power mode, which results in power savings of up to 50%. The signal speed paths in the low-power PAL block will be slower than those in the non-low-power PAL block. This feature allows speed critical paths to run at maximum frequency while the rest of the signal paths operate in the low-power mode.

PROGRAMMABLE SLEW RATE

Each ispMACH 4A device I/O has an individually programmable output slew rate control bit. Each output can be individually configured for the higher speed transition (3 V/ns) or for the lower noise transition (1 V/ns). For high-speed designs with long, unterminated traces, the slow-slew rate will introduce fewer reflections, less noise, and keep ground bounce to a minimum. For designs with short traces or well terminated lines, the fast slew rate can be used to achieve the highest speed. The slew rate is adjusted independent of power.

POWER-UP RESET/SET

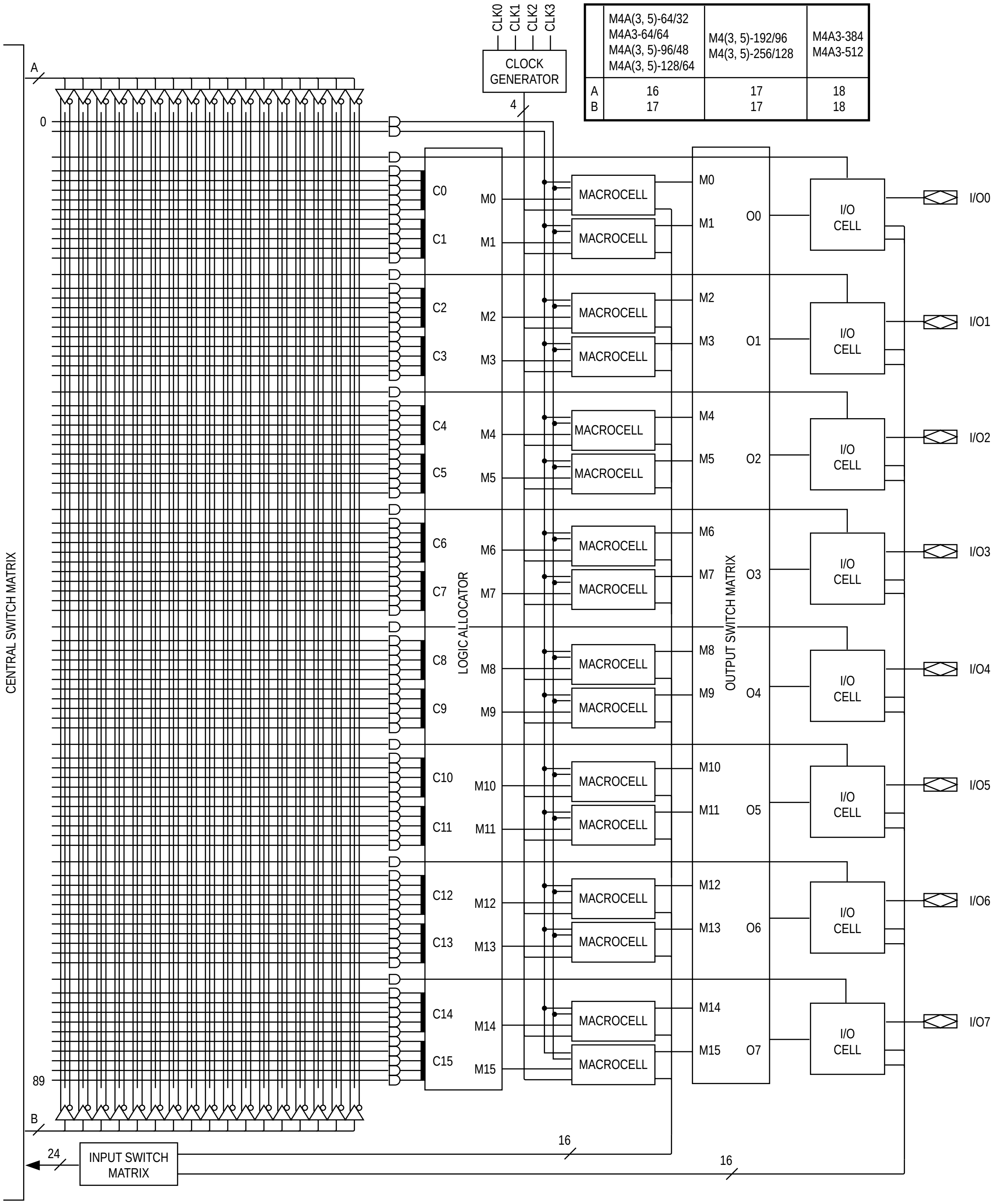
All flip-flops power up to a known state for predictable system initialization. If a macrocell is configured to SET on a signal from the control generator, then that macrocell will be SET during device power-up. If a macrocell is configured to RESET on a signal from the control generator or is not configured for set/reset, then that macrocell will RESET on power-up. To guarantee initialization values, the V_{CC} rise must be monotonic, and the clock must be inactive until the reset delay time has elapsed.

SECURITY BIT

A programmable security bit is provided on the ispMACH 4A devices as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, this bit defeats readback of the programmed pattern by a device programmer, securing proprietary designs from competitors. Programming and verification are also defeated by the security bit. The bit can only be reset by erasing the entire device.

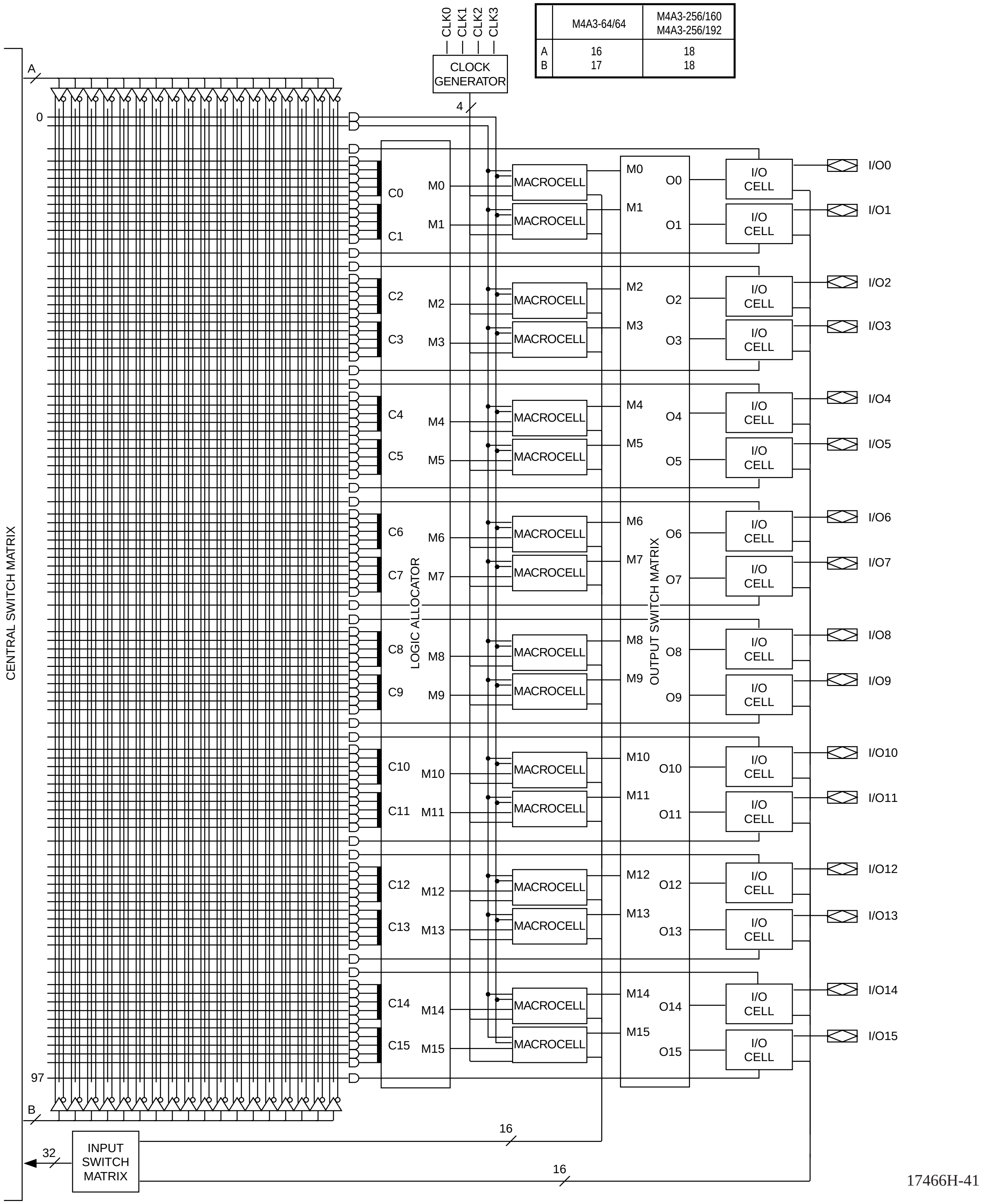
HOT SOCKETING

ispMACH 4A devices are well-suited for those applications that require hot socketing capability. Hot socketing a device requires that the device, when powered down, can tolerate active signals on the I/Os and inputs without being damaged. Additionally, it requires that the effects of the powered-down MACH devices be minimal on active signals.



	M4A(3, 5)-64/32 M4A3-64/64 M4A(3, 5)-96/48 M4A(3, 5)-128/64	M4(3, 5)-192/96 M4(3, 5)-256/128	M4A3-384 M4A3-512
A	16	17	18
B	17	17	18

Figure 16. PAL Block for ispMACH 4A with 2:1 Macrocell - I/O Cell Ratio



	M4A3-64/64	M4A3-256/160 M4A3-256/192
A	16	18
B	17	18

Figure 17. PAL Block for ispMACH 4A Devices with 1:1 Macrocell-I/O Cell Ratio (except M4A (3,5)-32/32)

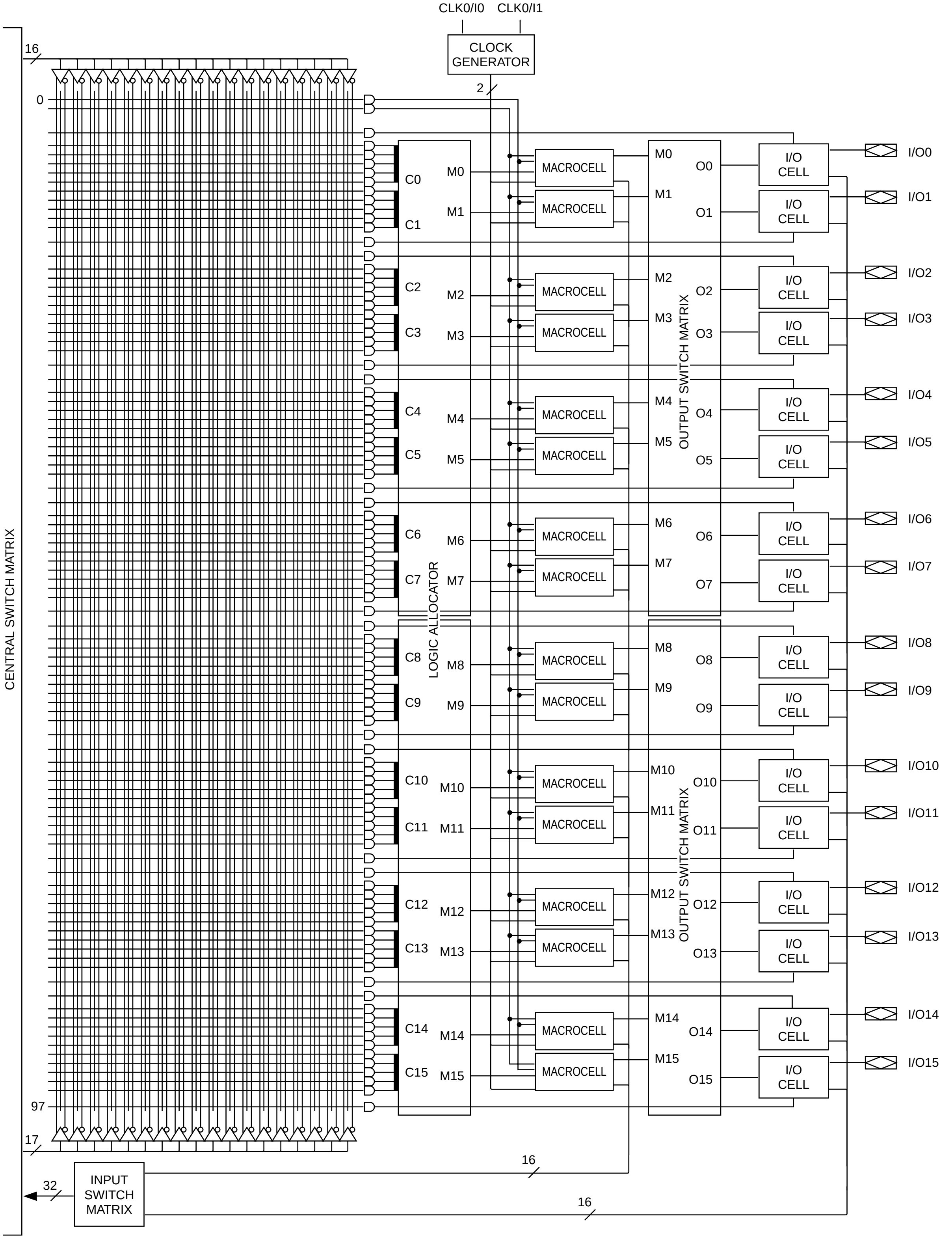
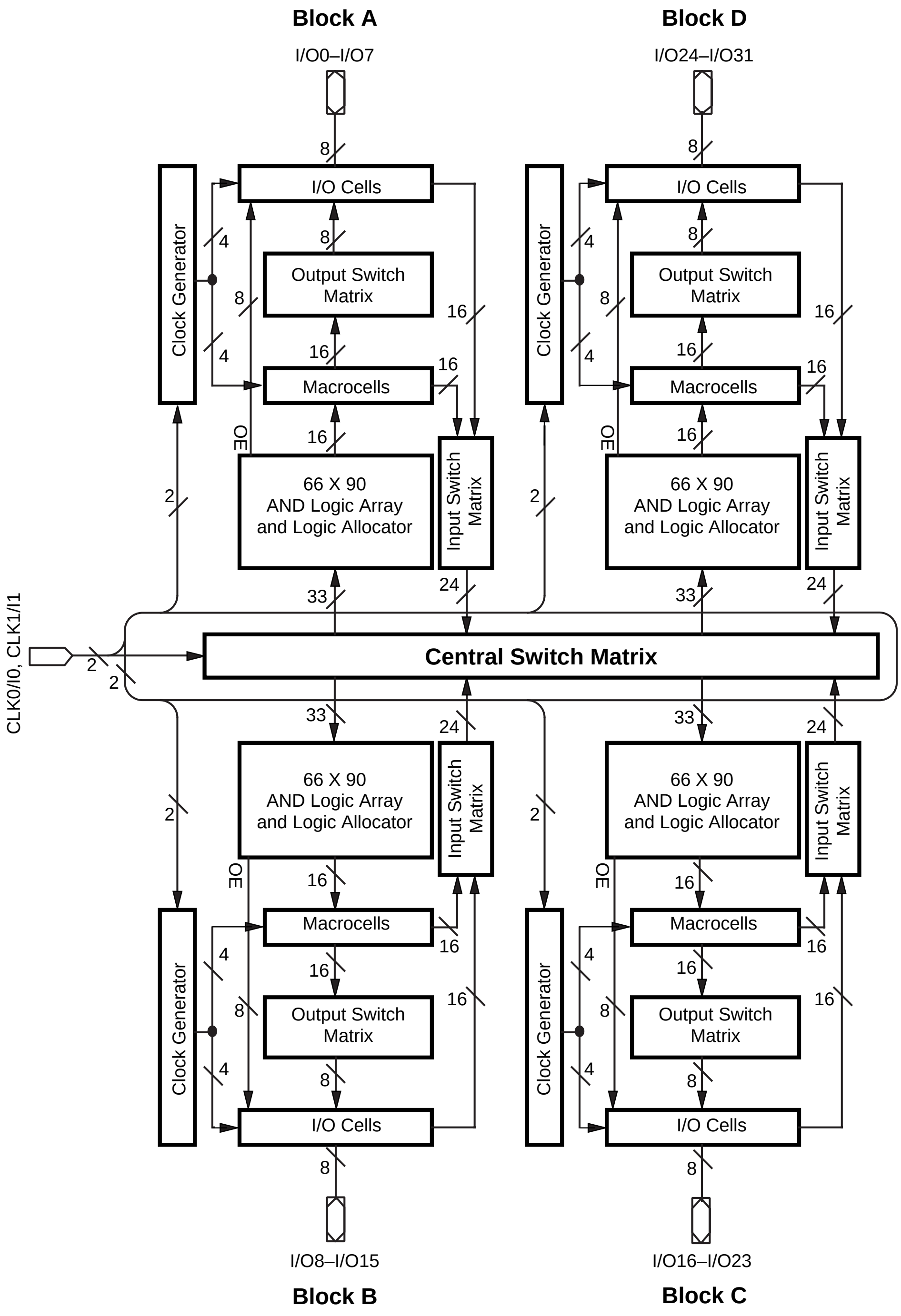


Figure 18. PAL Block for M4A (3,5)-32/32

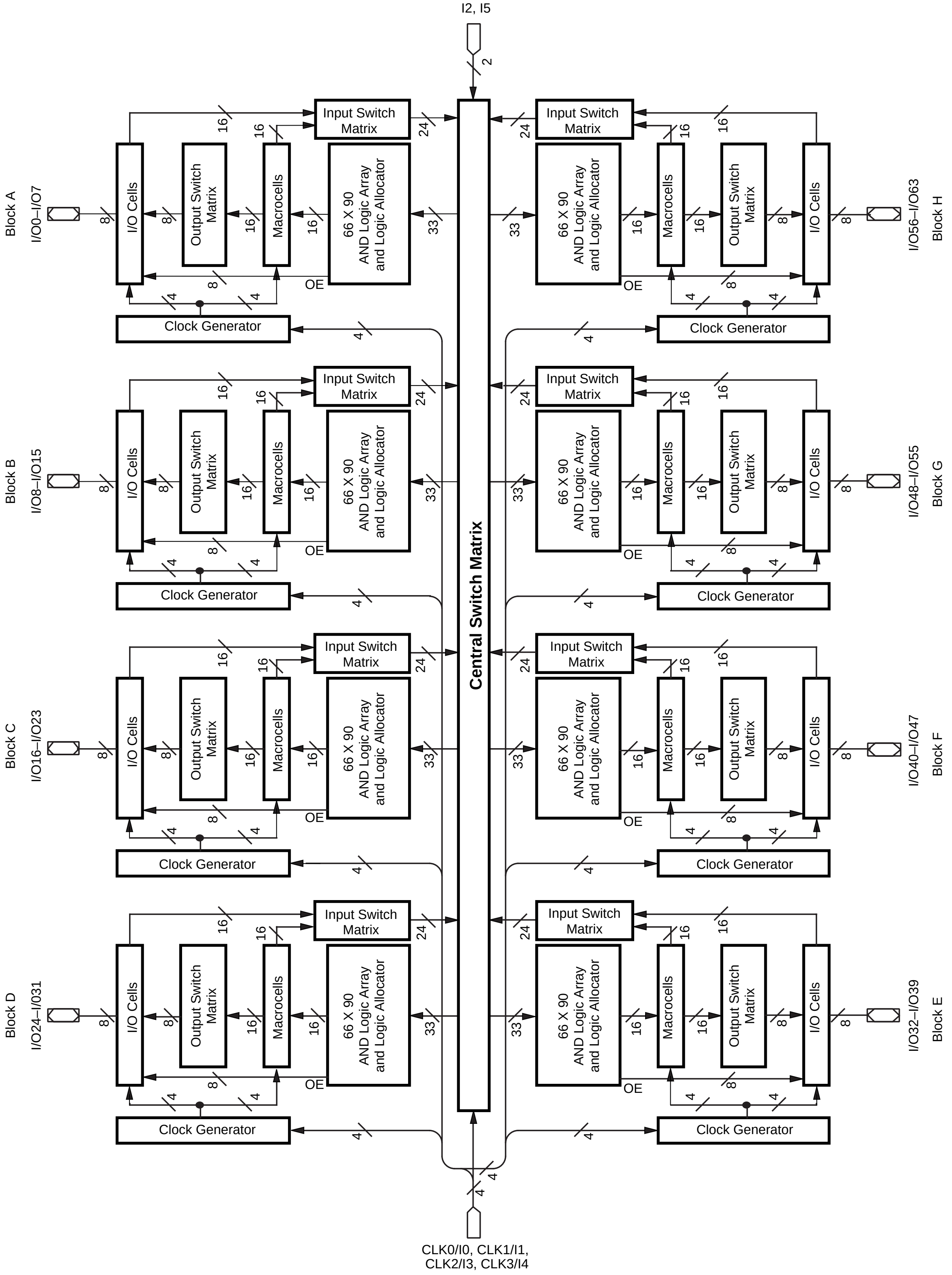
17466H-042

BLOCK DIAGRAM – M4A(3,5)-64/32



17466H-020

BLOCK DIAGRAM – M4A(3,5)-128/64



17466H-022

ABSOLUTE MAXIMUM RATINGS

M4A3

Storage Temperature . . . . -65°C to +150°C

Ambient Temperature
with Power Applied. . . . .-55°C to +100°C

Device Junction Temperature. . . . .+130°C

Supply Voltage
with Respect to Ground . . . .-0.5 V to +4.5 V

DC Input Voltage . . . . -0.5 V to 6.0 V

Static Discharge Voltage . . . . 2000 V

Latchup Current (T_A = -40°C to +85°C) . . . . .200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)
Operating in Free Air . . . . 0°C to +70°C

Supply Voltage (V_{CC})
with Respect to Ground. . . . . +3.0 V to +3.6 V

Industrial (I) Devices

Ambient Temperature (T_A)
Operating in Free Air . . . .-40°C to +85°C

Supply Voltage (V_{CC})
with Respect to Ground. . . . . +3.0 V to +3.6 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

3.3-V DC CHARACTERISTICS OVER OPERATING RANGES

Parameter Symbol	Parameter Description	Test Conditions		Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min $V_{IN} = V_{IH}$ or V_{IL}	I_{OH} = –100 μA	V_{CC} – 0.2			V
			I_{OH} = –3.2 mA	2.4			V
V_{OL}	Output LOW Voltage	V_{CC} = Min $V_{IN} = V_{IH}$ or V_{IL} (Note 1)	I_{OL} = 100 μA			0.2	V
			I_{OL} = 24 mA			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs		2.0		5.5	V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs		–0.3		0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 3.6 V, V_{CC} = Max (Note 2)				5	μA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)				–5	μA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 3.6 V, V_{CC} = Max $V_{IN} = V_{IH}$ or V_{IL} (Note 2)				5	μA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max $V_{IN} = V_{IH}$ or V_{IL} (Note 2)				–5	μA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)		–15		–160	mA

Notes:

1. *Total I_{OL} for one PAL block should not exceed 64 mA.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.*

Notes:

1. *See “MACH Switching Test Circuit” document on the Literature Download page of the Lattice web site.*
2. *This parameter does not apply to flip-flops in the emulated mode since the feedback path is required for emulation.*

I_{CC} vs. FREQUENCY

These curves represent the typical power consumption for a particular device at system frequency. The selected “typical” pattern is a 16-bit up-down counter. This pattern fills the device and exercises every macrocell. Maximum frequency shown uses internal feedback and a D-type register. Power / Speed are optimized to obtain the highest counter frequency and the lowest power. The highest frequency (LSBs) is placed in common PAL blocks, which are set to high power. The lowest frequency signals (MSBs) are placed in a common PAL block and set to lowest power.

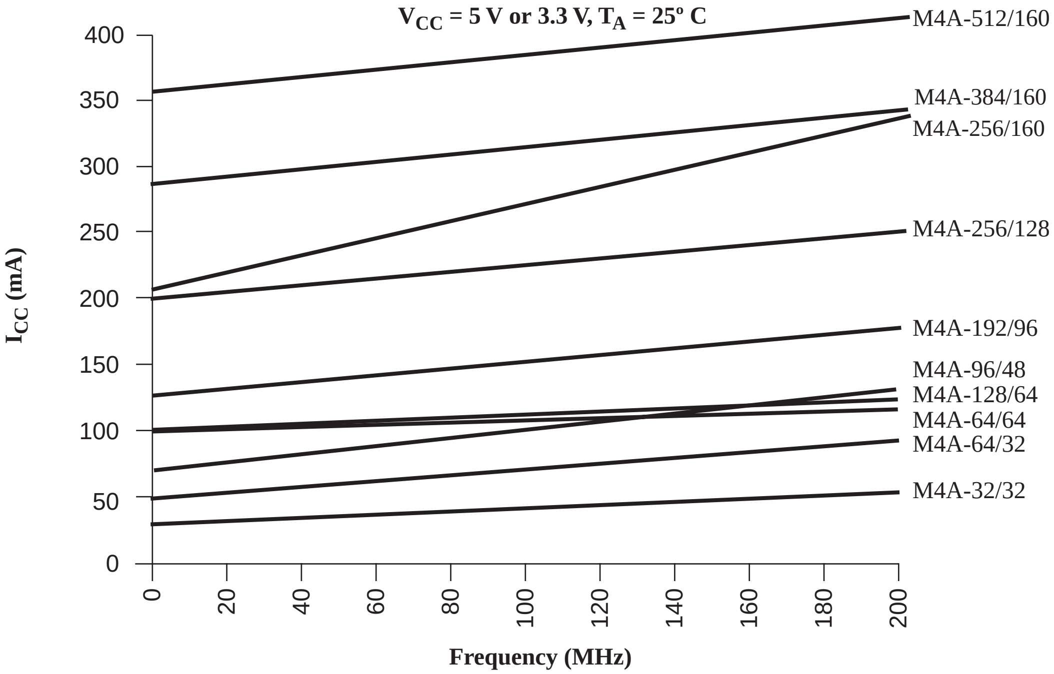


Figure 19. ispMACH 4A I_{CC} Curves at High Speed Mode

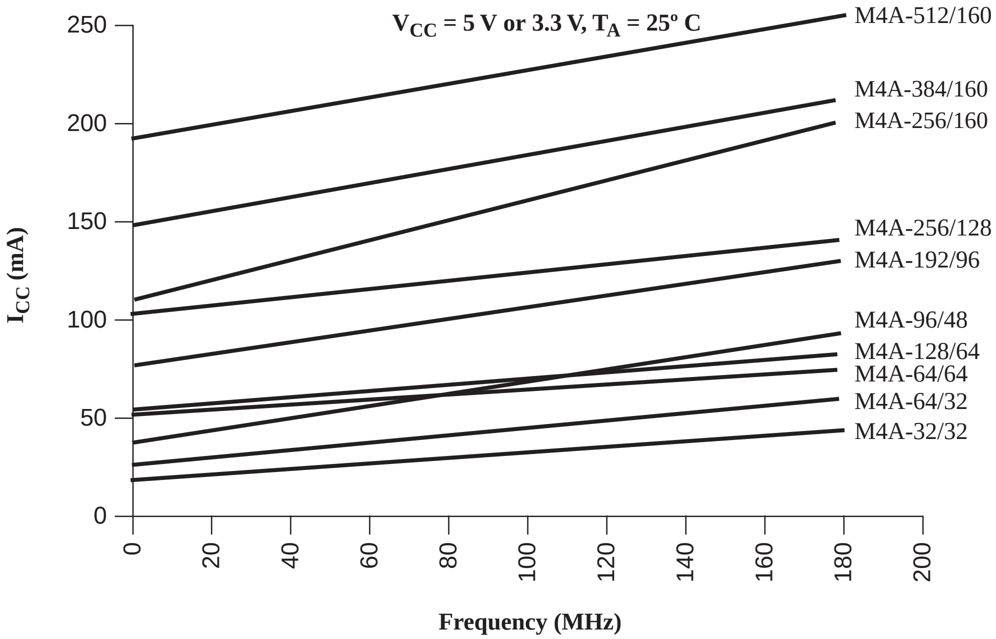
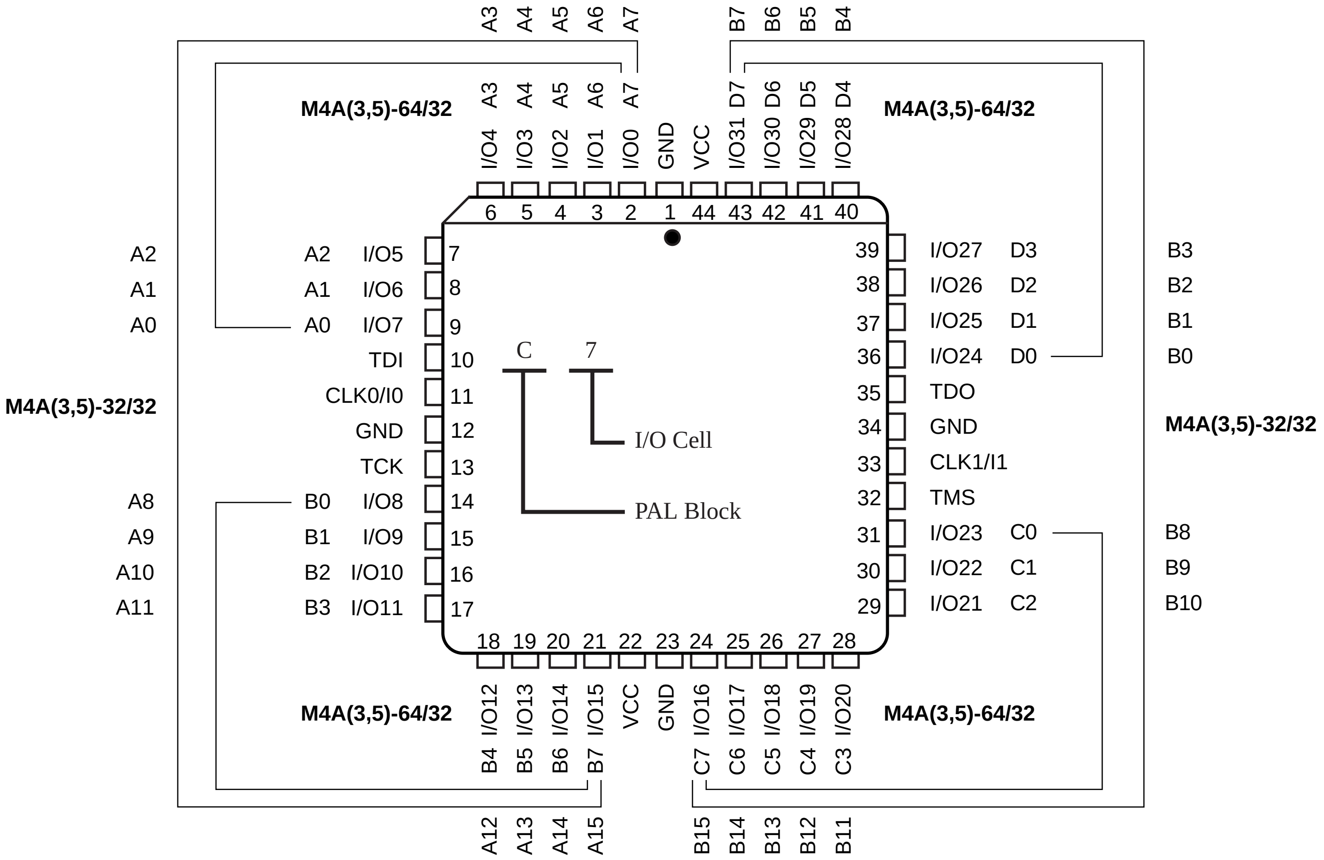


Figure 20. ispMACH 4A I_{CC} Curves at Low Power Mode

44-PIN PLCC CONNECTION DIAGRAM (M4A(3,5)-32/32 AND M4A(3,5)-64/32)

Top View

44-Pin PLCC



17466G-026

PIN DESIGNATIONS

CLK/I = Clock or Input

GND = Ground

I/O = Input/Output

V_{CC} = Supply Voltage

TDI = Test Data In

TCK = Test Clock

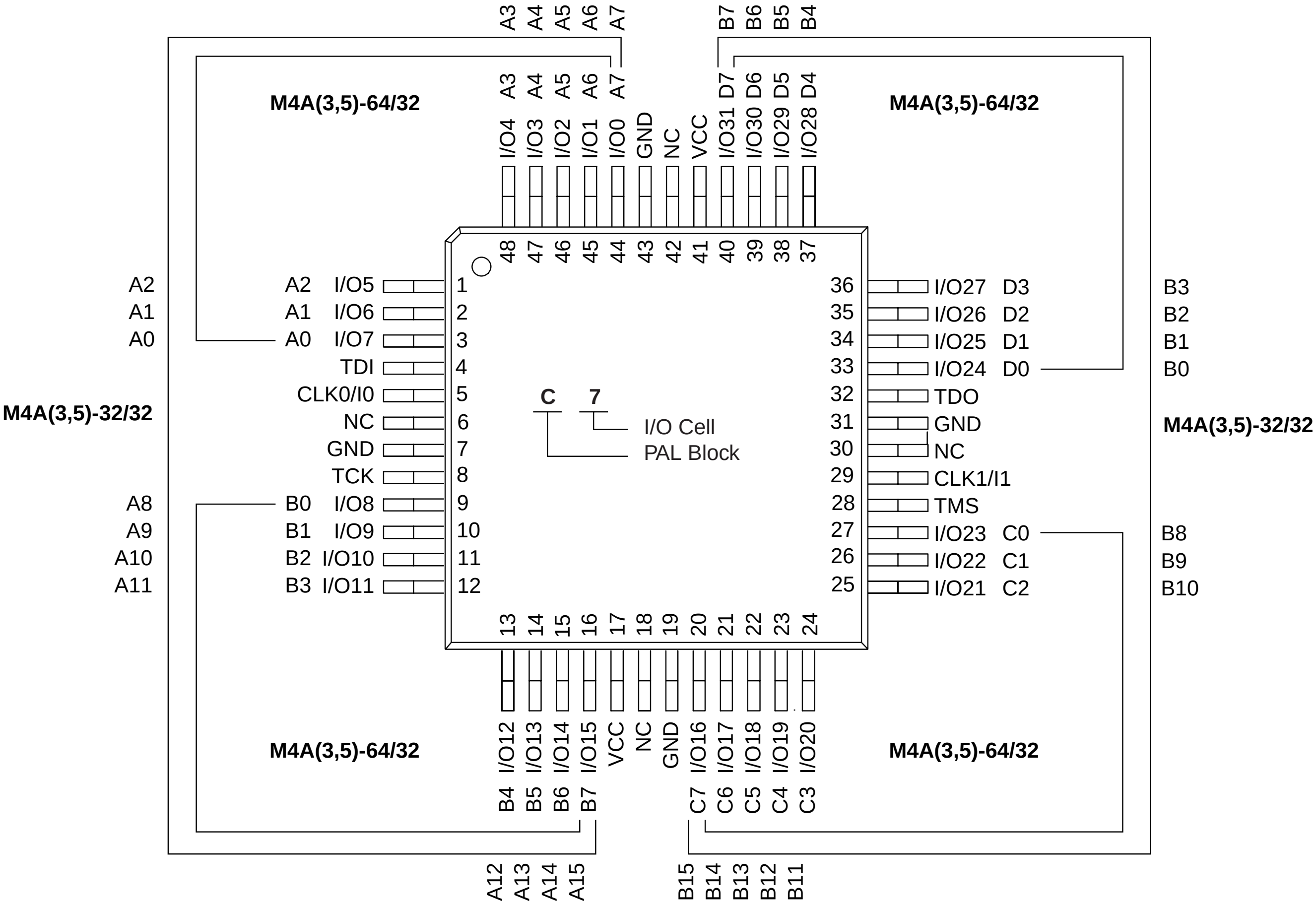
TMS = Test Mode Select

TDO = Test Data Out

48-PIN TQFP CONNECTION DIAGRAM (M4A(3,5)-32/32 AND M4A(3,5)-64/32)

Top View

48-Pin TQFP (1.4mm Thickness)



17466G-028

PIN DESIGNATIONS

CLK/I = Clock or Input

GND = Ground

I/O = Input/Output

V_{CC} = Supply Voltage

NC = No Connect

TDI = Test Data In

TCK = Test Clock

TMS = Test Mode Select

TDO = Test Data Out

144-BALL FPBGA CONNECTION DIAGRAM (M4A3-192/96)

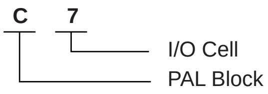
Bottom View

144-Ball fpBGA

	12	11	10	9	8	7	6	5	4	3	2	1	
A	GND	I/O72 L7	I/O76 L3	I13	GBCLK3	I0	I/O82 A2	I/O86 A6	I/O88 B0	I/O93 B5	I/O95 B7	GND	**A**
B	GND	I/O73 L6	I/O77 L2	I/O79 L0	VCC	I1	I/O83 A3	I/O87 A7	I/O90 B2	I/O94 B6	I/O0 D7	TDI	**B**
C	GND	TDO	I/O74 L5	I14	GND	I/O80 A0	I/O84 A4	GND	I/O92 B4	I/O1 D6	I/O4 D3	I/O3 D4	**C**
D	I/O67 K4	I/O69 K2	I/O71 K0	I/O75 L4	GBCLK0	I/O81 A1	VCC	I/O91 B3	I/O2 D5	I2	I/O6 D1	I/O7 D0	**D**
E	I12	I/O64 K7	I/O66 K5	I/O70 K1	I/O78 L1	I/O85 A5	I/O89 B1	I/O5 D2	I/O8 C7	I4	GND	VCC	**E**
F	I10	I11	GND	I/065 K6	I/O68 K3	I15	I3	GND	I/O12 C3	I/O11 C4	I/O10 C5	I/O9 C6	**F**
G	I/O60 J3	I/O61 J2	I/O62 J1	I/O63 J0	VCC	GND	I7	I/O20 E3	I/O17 E6	I/O15 C0	I/O14 C1	I/O13 C2	**G**
H	I/O56 J7	I/O57 J6	I/O58 J5	I/O59 J4	I/O53 I2	I/O41 H1	I/O37 G5	I/O30 F1	I/O22 E1	I/O18 E5	I/O16 E7	VCC	**H**
J	I/O55 I0	I/O54 I1	VCC	I/O50 I5	I/O43 H3	VCC	I/O33 G1	GBCLK2	I/O27 F4	I/O23 E0	I/O21 E2	I/O19 E4	**J**
K	I/O51 I4	I/O52 I3	I/O49 I6	I/O44 H4	GND	I/O36 G4	I/O32 G0	VCC	I6	I/O26 F5	TCK	TMS	**K**
L	GND	I/O48 I7	I/O46 H6	I/O42 H2	I/O39 G7	I/O35 G3	I9	GND	I/O31 F0	I/O29 F2	I/O25 F6	GND	**L**
M	GND	I/O47 H7	I/O45 H5	I/O40 H0	I/O38 G6	I/O34 G2	I8	GBCLK1	I5	I/O28 F3	I/O24 F7	GND	**M**
	12	11	10	9	8	7	6	5	4	3	2	1	

PIN DESIGNATIONS

CLK = Clock
GND = Ground
I = Input
I/O = Input/Output
N/C = No Connect
VCC = Supply Voltage
TDI = Test Data In
TCK = Test Clock
TMS = Test Mode Select
TDO = Test Data Out

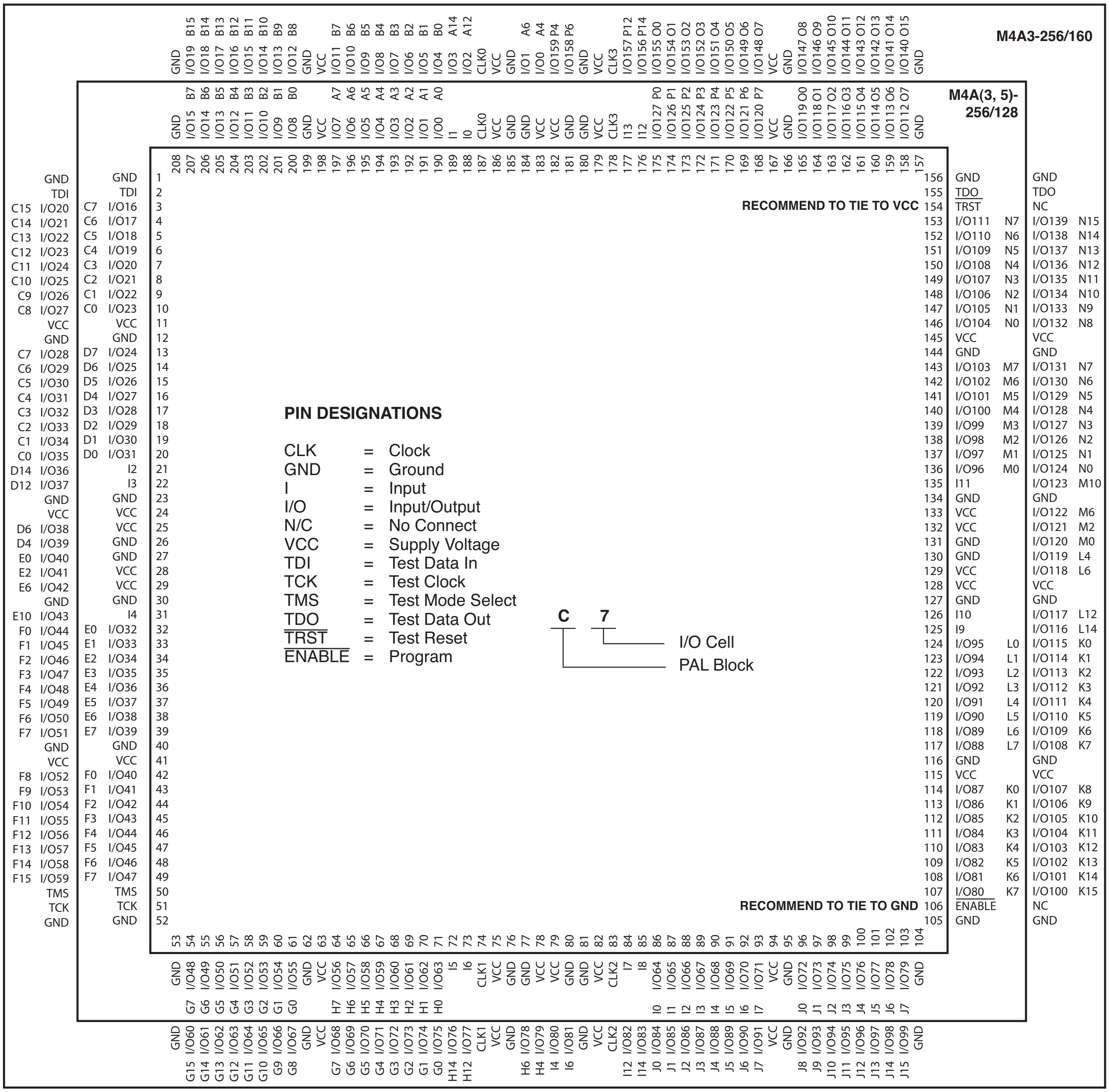


m4a3.192.96_144bga

208-PIN PQFP CONNECTION DIAGRAM (M4A(3,5)-256/128 AND M4A3-256/160)

Top View

208-Pin PQFP



Pin	M4A(3, 5)-256/128	M4A3-256/160
1	GND	GND
2	TDI	TDI
3	C7 I/O16	C15 I/O20
4	C6 I/O17	C14 I/O21
5	C5 I/O18	C13 I/O22
6	C4 I/O19	C12 I/O23
7	C3 I/O20	C11 I/O24
8	C2 I/O21	C10 I/O25
9	C1 I/O22	C9 I/O26
10	C0 I/O23	C8 I/O27
11	VCC	VCC
12	GND	GND
13	D7 I/O24	C7 I/O28
14	D6 I/O25	C6 I/O29
15	D5 I/O26	C5 I/O30
16	D4 I/O27	C4 I/O31
17	D3 I/O28	C3 I/O32
18	D2 I/O29	C2 I/O33
19	D1 I/O30	C1 I/O34
20	D0 I/O31	C0 I/O35
21	I2	D14 I/O36
22	I3	D12 I/O37
23	GND	GND
24	VCC	VCC
25	VCC	D6 I/O38
26	GND	D4 I/O39
27	GND	E0 I/O40
28	VCC	E2 I/O41
29	VCC	E6 I/O42
30	GND	GND
31	I4	E10 I/O43
32	E0 I/O32	F0 I/O44
33	E1 I/O33	F1 I/O45
34	E2 I/O34	F2 I/O46
35	E3 I/O35	F3 I/O47
36	E4 I/O36	F4 I/O48
37	E5 I/O37	F5 I/O49
38	E6 I/O38	F6 I/O50
39	E7 I/O39	F7 I/O51
40	GND	GND
41	VCC	VCC
42	F0 I/O40	F8 I/O52
43	F1 I/O41	F9 I/O53
44	F2 I/O42	F10 I/O54
45	F3 I/O43	F11 I/O55
46	F4 I/O44	F12 I/O56
47	F5 I/O45	F13 I/O57
48	F6 I/O46	F14 I/O58
49	F7 I/O47	F15 I/O59
50	TMS	TMS
51	TCK	TCK
52	GND	GND
53	GND	GND
54	I/O48 G7	I/O60 G15
55	I/O49 G6	I/O61 G14
56	I/O50 G5	I/O62 G13
57	I/O51 G4	I/O63 G12
58	I/O52 G3	I/O64 G11
59	I/O53 G2	I/O65 G10
60	I/O54 G1	I/O66 G9
61	I/O55 G0	I/O67 G8
62	GND	GND
63	VCC	VCC
64	I/O56 H7	I/O68 G7
65	I/O57 H6	I/O69 G6
66	I/O58 H5	I/O70 G5
67	I/O59 H4	I/O71 G4
68	I/O60 H3	I/O72 G3
69	I/O61 H2	I/O73 G2
70	I/O62 H1	I/O74 G1
71	I/O63 H0	I/O75 G0
72	I5	I/O76 H14
73	I6	I/O77 H12
74	CLK1	CLK1
75	VCC	VCC
76	GND	GND
77	GND	I/O78 H6
78	VCC	I/O79 H4
79	VCC	I/O80 I4
80	GND	I/O81 I6
81	GND	GND
82	VCC	VCC
83	CLK2	CLK2
84	I7	I/O82 I12
85	I8	I/O83 I14
86	I/O64 I0	I/O84 J0
87	I/O65 I1	I/O85 J1
88	I/O66 I2	I/O86 J2
89	I/O67 I3	I/O87 J3
90	I/O68 I4	I/O88 J4
91	I/O69 I5	I/O89 J5
92	I/O70 I6	I/O90 J6
93	I/O71 I7	I/O91 J7
94	VCC	VCC
95	GND	GND
96	I/O72 J0	I/O92 J8
97	I/O73 J1	I/O93 J9
98	I/O74 J2	I/O94 J10
99	I/O75 J3	I/O95 J11
100	I/O76 J4	I/O96 J12
101	I/O77 J5	I/O97 J13
102	I/O78 J6	I/O98 J14
103	I/O79 J7	I/O99 J15
104	GND	GND
105	GND	GND
106	ENABLE	NC
107	I/O80 K7	I/O100 K15
108	I/O81 K6	I/O101 K14
109	I/O82 K5	I/O102 K13
110	I/O83 K4	I/O103 K12
111	I/O84 K3	I/O104 K11
112	I/O85 K2	I/O105 K10
113	I/O86 K1	I/O106 K9
114	I/O87 K0	I/O107 K8
115	VCC	VCC
116	GND	GND
117	I/O88 L7	I/O108 K7
118	I/O89 L6	I/O109 K6
119	I/O90 L5	I/O110 K5
120	I/O91 L4	I/O111 K4
121	I/O92 L3	I/O112 K3
122	I/O93 L2	I/O113 K2
123	I/O94 L1	I/O114 K1
124	I/O95 L0	I/O115 K0
125	I9	I/O116 L14
126	I10	I/O117 L12
127	GND	GND
128	VCC	VCC
129	VCC	I/O118 L6
130	GND	I/O119 L4
131	GND	I/O120 M0
132	VCC	I/O121 M2
133	VCC	I/O122 M6
134	GND	GND
135	I11	I/O123 M10
136	I/O96 M0	I/O124 N0
137	I/O97 M1	I/O125 N1
138	I/O98 M2	I/O126 N2
139	I/O99 M3	I/O127 N3
140	I/O100 M4	I/O128 N4
141	I/O101 M5	I/O129 N5
142	I/O102 M6	I/O130 N6
143	I/O103 M7	I/O131 N7
144	GND	GND
145	VCC	VCC
146	I/O104 N0	I/O132 N8
147	I/O105 N1	I/O133 N9
148	I/O106 N2	I/O134 N10
149	I/O107 N3	I/O135 N11
150	I/O108 N4	I/O136 N12
151	I/O109 N5	I/O137 N13
152	I/O110 N6	I/O138 N14
153	I/O111 N7	I/O139 N15
154	TRST	NC
155	TDO	TDO
156	GND	GND
157	GND	GND
158	I/O112 O7	I/O140 O15
159	I/O113 O6	I/O141 O14
160	I/O114 O5	I/O142 O13
161	I/O115 O4	I/O143 O12
162	I/O116 O3	I/O144 O11
163	I/O117 O2	I/O145 O10
164	I/O118 O1	I/O146 O9
165	I/O119 O0	I/O147 O8
166	GND	GND
167	VCC	VCC
168	I/O120 P7	I/O148 O7
169	I/O121 P6	I/O149 O6
170	I/O122 P5	I/O150 O5
171	I/O123 P4	I/O151 O4
172	I/O124 P3	I/O152 O3
173	I/O125 P2	I/O153 O2
174	I/O126 P1	I/O154 O1
175	I/O127 P0	I/O155 O0
176	I12	I/O156 P14
177	I13	I/O157 P12
178	CLK3	CLK3
179	VCC	VCC
180	GND	GND
181	GND	I/O158 P6
182	VCC	I/O159 P4
183	VCC	I/O0 A4
184	GND	I/O1 A6
185	GND	GND
186	VCC	VCC
187	CLK0	CLK0
188	I0	I/O2 A12
189	I1	I/O3 A14
190	I/O0 A0	I/O4 B0
191	I/O1 A1	I/O5 B1
192	I/O2 A2	I/O6 B2
193	I/O3 A3	I/O7 B3
194	I/O4 A4	I/O8 B4
195	I/O5 A5	I/O9 B5
196	I/O6 A6	I/O10 B6
197	I/O7 A7	I/O11 B7
198	VCC	VCC
199	GND	GND
200	I/O8 B0	I/O12 B8
201	I/O9 B1	I/O13 B9
202	I/O10 B2	I/O14 B10
203	I/O11 B3	I/O15 B11
204	I/O12 B4	I/O16 B12
205	I/O13 B5	I/O17 B13
206	I/O14 B6	I/O18 B14
207	I/O15 B7	I/O19 B15
208	GND	GND

RECOMMEND TO TIE TO VCC (154)

RECOMMEND TO TIE TO GND (106)

PIN DESIGNATIONS

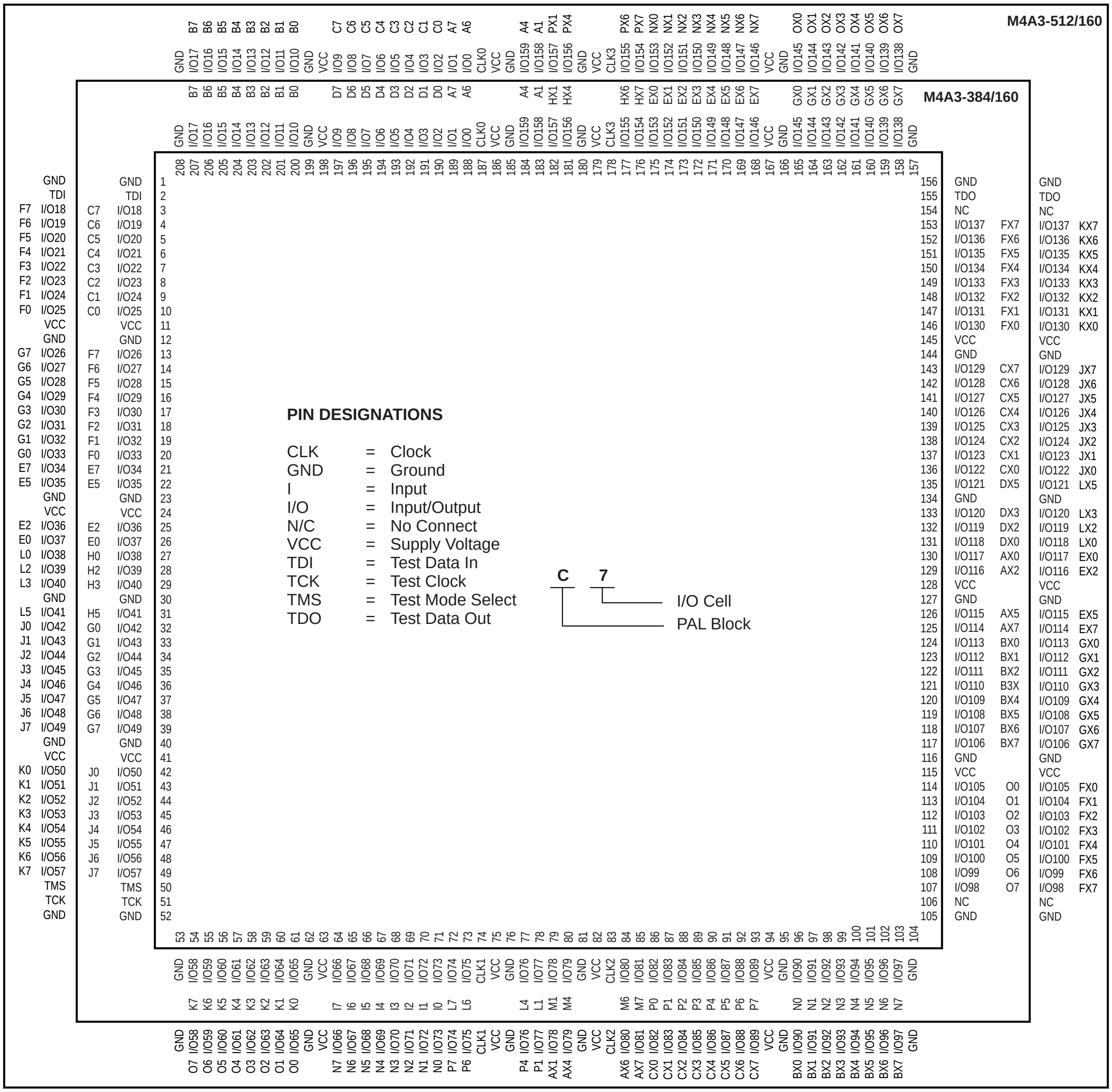
CLK = Clock
GND = Ground
I = Input
I/O = Input/Output
N/C = No Connect
VCC = Supply Voltage
TDI = Test Data In
TCK = Test Clock
TMS = Test Mode Select
TDO = Test Data Out
TRST = Test Reset
ENABLE = Program

17466G-044

208-PIN PQFP CONNECTION DIAGRAM (M4A3-384/160 AND M4A3-512/160)

Top View

208-Pin PQFP



17466Ga-044

256-BALL fpBGA CONNECTION DIAGRAM (M4A3-384/192)

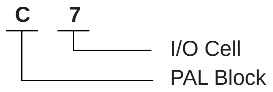
Bottom View

256-Ball fpBGA

	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	I/O175 FX7	I/O181 GX5	I/O180 GX4	I/O177 GX1	I/O166 EX6	I/O164 EX4	I/O191 HX7	I/O186 HX2	I/O1 A1	I/O3 A3	CLK0	I/O25 D1	I/O29 D5	I/O31 D7	I/O10 B2	I/O12 B4	**A**
B	I/O173 FX5	I/O174 FX6	I/O182 GX6	I/O179 GX3	I/O167 EX7	I/O165 EX5	I/O160 EX0	I/O187 HX3	I/O0 A0	I/O5 A5	I/O7 A7	I/O26 D2	I/O8 B0	I/O11 B3	I/O13 B5	N/C	**B**
C	I/O171 FX3	I/O172 FX4	N/C	I/O183 GX7	I/O178 GX2	I/O162 EX2	I/O163 EX3	I/O189 HX5	I/O184 HX0	I/O6 A6	I/O28 D4	I/O30 D6	I/O15 B7	I/O14 B6	TDI	I/O23 C7	**C**
D	I/O150 CX6	I/O151 CX7	TDO	GND	GND	VCC	GND	VCC	GND	GND	VCC	GND	VCC	I/O9 B1	I/O22 C6	I/O21 C5	**D**
E	I/O148 CX4	N/C	I/O170 FX2	VCC	I/O168 FX0	169 FX1	I/O190 HX6	CLK3	I/O188 HX4	I/O2 A2	I/O24 D0	N/C	GND	I/O20 C4	I/O19 C3	I/O47 F7	**E**
F	I/O144 CX0	I/O149 CX5	I/O147 CX3	GND	I/O146 CX2	I/O145 CX1	I/O176 GX0	I/O161 EX1	I/O185 HX1	I/O4 A4	I/O27 D3	I/O18 C2	VCC	I/O16 C0	I/O46 F6	I/O45 F5	**F**
G	I/O155 DX3	I/O158 DX6	I/O157 DX5	VCC	I/O156 DX4	I/O159 DX7	VCC	GND	GND	VCC	I/O17 C1	I/O44 F4	GND	I/O42 F2	I/O41 F1	I/O39 E7	**G**
H	I/O152 DX0	I/O154 DX2	I/O153 DX1	GND	I/O128 AX0	I/O129 AX1	GND	VCC	VCC	GND	I/O43 F3	I/O40 F0	VCC	I/O36 E4	I/O35 E3	I/O34 E2	**H**
J	I/O130 AX2	I/O131 AX3	I/O132 AX4	GND	I/O134 AX6	I/O133 AX5	GND	VCC	VCC	GND	I/O38 E6	I/O37 E5	GND	I/O57 H1	I/O56 H0	I/O58 H2	**J**
K	I/O135 AX7	I/O136 BX0	I/O137 BX1	VCC	I/O139 BX3	I/O138 BX2	VCC	GND	GND	VCC	I/O33 E1	I/O32 E0	VCC	I/O63 H7	I/O62 H6	I/O48 G0	**K**
L	I/O140 BX4	I/O141 BX5	I/O143 BX7	GND	I/O114 O2	I/O142 BX6	I/O98 M2	I/O91 L3	I/O67 I3	I/O69 I5	I/O60 H4	I/O59 H3	GND	I/O51 G3	I/O52 G4	I/O49 G1	**L**
M	I/O112 O0	I/O113 O1	I/O115 O3	GND	I/O123 P3	I/O121 P1	I/O100 M4	I/O90 L2	I/O66 I2	I/O80 K0	I/O83 K3	I/O61 H5	VCC	I/O76 J4	I/O55 G7	I/O50 G2	**M**
N	I/O116 O4	I/O117 O5	I/O119 O7	VCC	GND	VCC	GND	VCC	GND	GND	VCC	GND	GND	TCK	I/O72 J0	I/O53 G5	**N**
P	I/O118 O6	I/O109 N5	I/O110 N6	I/O111 N7	I/O124 P4	I/O122 P2	I/O101 M5	I/O89 L1	I/O93 L5	I/O94 L6	I/O71 I7	I/O84 K4	I/O87 K7	TMS	I/O73 J1	I/O54 G6	**P**
R	I/O108 N4	I/O107 N3	I/O104 N0	I/O127 P7	I/O120 P0	I/O102 M6	I/O99 M3	I/O96 M0	I/O92 L4	I/O64 I0	I/O68 I4	I/O81 K1	I/O85 K5	I/O79 J7	I/O75 J3	I/O74 J2	**R**
T	I/O106 N2	I/O105 N1	I/O126 P6	I/O125 P5	I/O103 M7	CLK2	I/O97 M1	I/O88 L0	CLK1	I/O95 L7	I/O65 I1	I/O70 I6	I/O82 K2	I/O86 K6	I/O78 J6	I/O77 J5	**T**
	16	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	

PIN DESIGNATIONS

CLK = Clock
GND = Ground
I = Input
I/O = Input/Output
N/C = No Connect
VCC = Supply Voltage
TDI = Test Data In
TCK = Test Clock
TMS = Test Mode Select
TDO = Test Data Out



m4a3.384.192_256bga

256-BALL fpBGA CONNECTION DIAGRAM (M4A3-512/192)

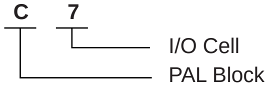
Bottom View

256-Ball fpBGA

	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	I/O159 KX7	I/O181 OX5	I/O180 OX4	I/O177 OX1	I/O174 NX6	I/O172 NX4	I/O191 PX7	I/O186 PX2	I/O1 A1	I/O3 A3	CLK0	I/O17 C1	I/O21 C5	I/O23 C7	I/O10 B2	I/O12 B4	A
B	I/O157 KX5	I/O158 KX6	I/O182 OX6	I/O179 OX3	I/O175 NX7	I/O173 NX5	I/O168 NX0	I/O187 PX3	I/O0 A0	I/O5 A5	I/O7 A7	I/O18 C2	I/O8 B0	I/O11 B3	I/O13 B5	N/C	B
C	I/O155 KX3	I/O156 KX4	N/C	I/O183 OX7	I/O178 OX2	I/O170 NX2	I/O171 NX3	I/O189 PX5	I/O184 PX0	I/O6 A6	I/O20 C4	I/O22 C6	I/O15 B7	I/O14 B6	TDI	I/O39 F7	C
D	I/O150 JX6	I/O151 JX7	TDO	GND	GND	VCC	GND	VCC	GND	GND	VCC	GND	VCC	I/O9 B1	I/O38 F6	I/O37 F5	D
E	I/O148 JX4	N/C	I/O154 KX2	VCC	I/O152 KX0	I/O153 KX1	I/O190 PX6	CLK3	I/O188 PX4	I/O2 A2	I/O16 C0	N/C	GND	I/O36 F4	I/O35 F3	I/O47 G7	E
F	I/O144 JX0	I/O149 JX5	I/O147 JX3	GND	I/O146 JX2	I/O145 JX1	I/O176 OX0	I/O169 NX1	I/O185 PX1	I/O4 A4	I/O19 C3	I/O34 F2	VCC	I/O32 F0	I/O46 G6	I/O45 G5	F
G	I/O163 LX3	I/O166 LX6	I/O165 LX5	VCC	I/O164 LX4	I/O167 LX7	VCC	GND	GND	VCC	I/O33 F1	I/O44 G4	GND	I/O42 G2	I/O41 G1	I/O31 E7	G
H	I/O160 LX0	I/O162 LX2	I/O161 LX1	GND	I/O120 EX0	I/O121 EX1	GND	VCC	VCC	GND	I/O43 G3	I/O40 G0	VCC	I/O28 E4	I/O27 E3	I/O26 E2	H
J	I/O122 EX2	I/O123 EX3	I/O124 EX4	GND	I/O126 EX6	I/O125 EX5	GND	VCC	VCC	GND	I/O30 E6	I/O29 E5	GND	I/O65 L1	I/O64 L0	I/O66 L2	J
K	I/O127 EX7	I/O136 GX0	I/O137 GX1	VCC	I/O139 GX3	I/O138 GX2	VCC	GND	GND	VCC	I/O25 E1	I/O24 E0	VCC	I/O71 L7	I/O70 L6	I/O48 J0	K
L	I/O140 GX4	I/O141 GX5	I/O143 GX7	GND	I/O130 FX2	I/O142 GX6	I/O98 AX2	I/O91 P3	I/O75 N3	I/O77 N5	I/O68 L4	I/O67 L3	GND	I/O51 J3	I/O52 J4	I/O49 J1	L
M	I/O128 FX0	I/O129 FX1	I/O131 FX3	GND	I/O115 CX3	I/O113 CX1	I/O100 AX4	I/O90 P2	I/O74 N2	I/O80 O0	I/O83 O3	I/O69 L5	VCC	I/O60 K4	I/O55 J7	I/O50 J2	M
N	I/O132 FX4	I/O133 FX5	I/O135 FX7	VCC	GND	VCC	GND	VCC	GND	GND	VCC	GND	GND	TCK	I/O56 K0	I/O53 J5	N
P	I/O134 FX6	I/O109 BX5	I/O110 BX6	I/O111 BX7	I/O116 CX4	I/O114 CX2	I/O101 AX5	I/O89 P1	I/O93 P5	I/O94 P6	I/O79 N7	I/O84 O4	I/O87 O7	TMS	I/O57 K1	I/O54 J6	P
R	I/O108 BX4	I/O107 BX3	I/O104 BX0	I/O119 CX7	I/O112 CX0	I/O102 AX6	I/O99 AX3	I/O96 AX0	I/O92 P4	I/O72 N0	I/O76 N4	I/O81 O1	I/O85 O5	I/O63 K7	I/O59 K3	I/O58 K2	R
T	I/O106 BX2	I/O105 BX1	I/O118 CX6	I/O117 CX5	I/O103 AX7	CLK2	I/O97 AX1	I/O88 P0	CLK1	I/O95 P7	I/O73 N1	I/O78 N6	I/O82 O2	I/O86 O6	I/O62 K6	I/O61 K5	T
	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

PIN DESIGNATIONS

CLK = Clock
GND = Ground
I = Input
I/O = Input/Output
N/C = No Connect
VCC = Supply Voltage
TDI = Test Data In
TCK = Test Clock
TMS = Test Mode Select
TDO = Test Data Out



m4a3.512.192_256bga

ispMACH 4A PRODUCT ORDERING INFORMATION

ispMACH 4A Devices Commercial and Industrial - 3.3V and 5V

Lattice programmable logic products are available with several ordering options. The order number (Valid Combination) is formed by a combination of:

M4A3- 256 / 128 -7 Y C

FAMILY TYPE

M4A3- = ispMACH 4A Family Low Voltage Advanced Feature (3.3-V V_{CC})
M4A5- = ispMACH 4A Family Advanced Feature (5-V V_{CC})

MACROCELL DENSITY

32 = 32 Macrocells
64 = 64 Macrocells
96 = 96 Macrocells
128 = 128 Macrocells
192 = 192 Macrocells
256 = 256 Macrocells
384 = 384 Macrocells
512 = 512 Macrocells

I/Os

/32 = 32 I/Os in 44-pin PLCC, 44-pin TQFP or 48-pin TQFP
/48 = 48 I/Os in 100-pin TQFP
/64 = 64 I/Os in 100-pin TQFP, 100-pin PQFP, or 100-ball caBGA
/96 = 96 I/Os in 144-pin TQFP or 144-ball fpBGA
/128 = 128 I/Os in 208-pin PQFP, 256-ball BGA or 256-ball fpBGA
/160 = 160 I/Os in 208-pin PQFP
/192 = 192 I/Os in 256-ball BGA or 256-ball fpBGA
/256 = 256 I/Os in 388-ball fpBGA

48 = 48-pin TQFP for M4A3-32/32 or M4A3-64/32 M4A5-32/32 or M4A5-64/32

OPERATING CONDITIONS

C = Commercial (0°C to +70°C)
I = Industrial (-40°C to +85°C)

PACKAGE TYPE

SA = Ball Grid Array (BGA)
J = Plastic Leaded Chip Carrier (PLCC)
JN = Lead-free Plastic Leaded Chip Carrier (PLCC)
V = Thin Quad Flat Pack (TQFP)
VN = Lead-free Thin Quad Flat Pack (TQFP)
Y = Plastic Quad Flat Pack (PQFP)
YN = Lead-fee Plastic Quad Flat Pack (PQFP)
FA = Fine-pitch Ball Grid Array (fpBGA)
FAN = Lead-free Fine-pitch Ball Grid Array (fpBGA)
CA = Chip-array Ball Grid Array (caBGA)

SPEED

-5 = 5.0 ns t_{PD}
-55 = 5.5 ns t_{PD}
-6 = 6.0 ns t_{PD}
-65 = 6.5 ns t_{PD}
-7 = 7.5 ns t_{PD}
-10 = 10 ns t_{PD}
-12 = 12 ns t_{PD}
-14 = 14 ns t_{PD}

*Package obsolete, contact factory.

Conventional Packaging

3.3V Commercial Combinations		
M4A3-32/32	-5, -7, -10	JC, VC, VC48
M4A3-64/32	-55, -7, -10	JC, VC, VC48
M4A3-64/64		VC
M4A3-96/48		VC
M4A3-128/64		YC, VC, CAC
M4A3-192/96	-6, -7, -10	VC, FAC
M4A3-256/128	-55, -65[1], -7, -10	YC, FAC, SAC
M4A3-256/160	-7, -10	YC
M4A3-256/192		FAC
M4A3-384/160	-65, -10, -12	YC
M4A3-384/192		SAC, FAC
M4A3-512/160	-7, -10, -12	YC
M4A3-512/192		FAC
M4A3-512/256		FAC

3.3V Industrial Combinations		
M4A3-32/32	-7, -10, -12	JI, VI, VI48
M4A3-64/32		JI, VI, VI48
M4A3-64/64		VI
M4A3-96/48		VI
M4A3-128/64		YI, VI, CAI
M4A3-192/96		VI, FAI
M4A3-256/128		YI, FAI, SAI
M4A3-256/160	-10, -12	YI
M4A3-256/192		FAI
M4A3-384/160	-10, -12, -14	YI
M4A3-384/192		FAI
M4A3-512/160		YI
M4A3-512/192		FAI
M4A3-512/256		FAI

1. *Use 5.5ns for new designs.*