Lattice Semiconductor Corporation - M4A5-256/128-10YNC Datasheet

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Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Not For New Designs
Programmable Type	In System Programmable
Delay Time tpd(1) Max	10 ns
Voltage Supply - Internal	4.75V ~ 5.25V
Number of Logic Elements/Blocks	-
Number of Macrocells	256
Number of Gates	-
Number of I/O	128
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/m4a5-256-128-10ync

FUNCTIONAL DESCRIPTION

The fundamental architecture of ispMACH 4A devices (Figure 1) consists of multiple, optimized PAL® blocks interconnected by a central switch matrix. The central switch matrix allows communication between PAL blocks and routes inputs to the PAL blocks. Together, the PAL blocks and central switch matrix allow the logic designer to create large designs in a single device instead of having to use multiple devices.

The key to being able to make effective use of these devices lies in the interconnect schemes. In the ispMACH 4A architecture, the macrocells are flexibly coupled to the product terms through the logic allocator, and the I/O pins are flexibly coupled to the macrocells due to the output switch matrix. In addition, more input routing options are provided by the input switch matrix. These resources provide the flexibility needed to fit designs efficiently.

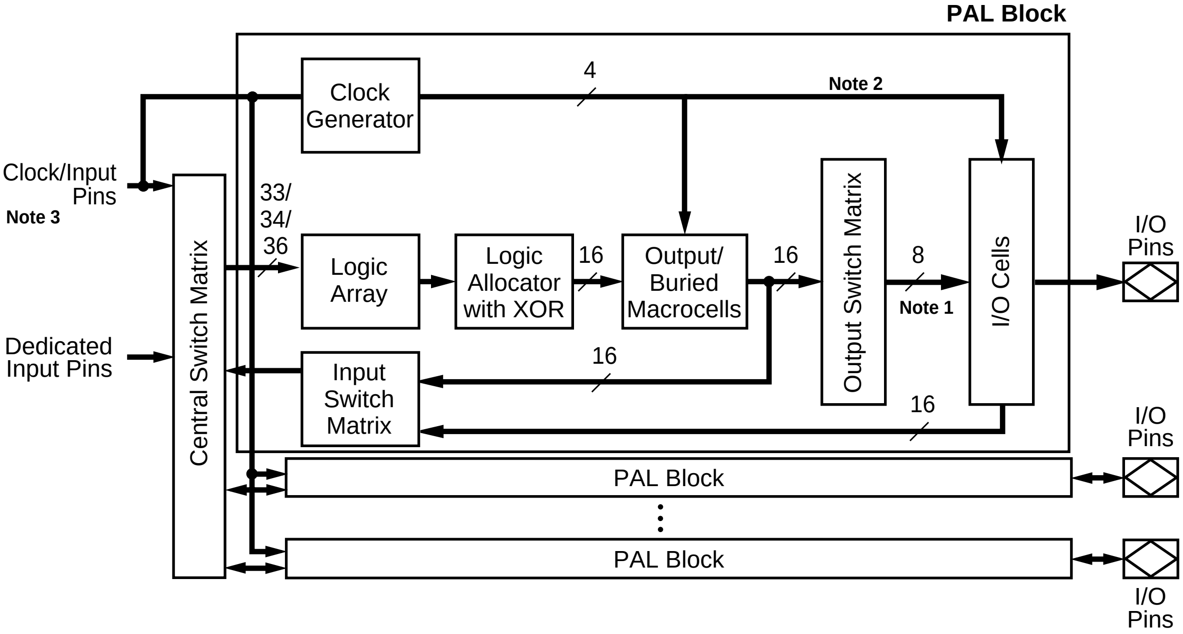

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Figure 1. ispMACH 4A Block Diagram and PAL Block Structure

Notes:

1. *16 for ispMACH 4A devices with 1:1 macrocell-I/O cell ratio (see next page).*
2. *Block clocks do not go to I/O cells in M4A(3,5)-32/32.*
3. *M4A(3,5)-192, M4A(3,5)-256, M4A3-384, and M4A3-512 have dedicated clock pins which cannot be used as inputs and do not connect to the central switch matrix.*

Table 4. Architectural Summary of ispMACH 4A devices

	ispMACH 4A Devices	
	M4A3-64/32, M4A5-64/32 M4A3-96/48, M4A5-96/48 M4A3-128/64, M4A5-128/64 M4A3-192/96, M4A5-192/96 M4A3-256/128, M4A5-256/128 M4A3-384 M4A3-512	M4A3-32/32 M4A5-32/32 M4A3-64/64 M4A3-256/160 M4A3-256/192
Macrocell-I/O Cell Ratio	2:1	1:1
Input Switch Matrix	Yes	Yes[1]
Input Registers	Yes	No
Central Switch Matrix	Yes	Yes
Output Switch Matrix	Yes	Yes

The Macrocell-I/O cell ratio is defined as the number of macrocells versus the number of I/O cells internally in a PAL block (Table 4).

The central switch matrix takes all dedicated inputs and signals from the input switch matrices and routes them as needed to the PAL blocks. Feedback signals that return to the same PAL block still must go through the central switch matrix. This mechanism ensures that PAL blocks in ispMACH 4A devices communicate with each other with consistent, predictable delays.

The central switch matrix makes a ispMACH 4A device more advanced than simply several PAL devices on a single chip. It allows the designer to think of the device not as a collection of blocks, but as a single programmable device; the software partitions the design into PAL blocks through the central switch matrix so that the designer does not have to be concerned with the internal architecture of the device.

Each PAL block consists of:

- Product-term array
- Logic allocator
- Macrocells
- Output switch matrix
- I/O cells
- Input switch matrix
- Clock generator

Notes:

1. *M4A3-64/64 internal switch matrix functionality embedded in central switch matrix.*

Product-Term Array

The product-term array consists of a number of product terms that form the basis of the logic being implemented. The inputs to the AND gates come from the central switch matrix (Table 5), and are provided in both true and complement forms for efficient logic implementation.

Table 5. PAL Block Inputs

Device	Number of Inputs to PAL Block
M4A3-32/32 and M4A5-32/32	33
M4A3-64/32 and M4A5-64/32	33
M4A3-64/64	33
M4A3-96/48 and M4A5-96/48	33
M4A3-128/64 and M4A5-128/64	33
M4A3-192/96 and M4A5-192/96	34
M4A3-256/128 and M4A5-256/128	34
M4A3-256/160 and M4A3-256/192	36
M4A3-384	36
M4A3-512	36

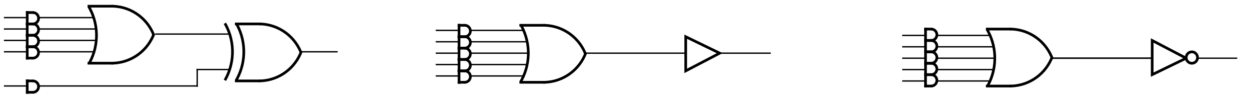
Logic Allocator

Within the logic allocator, product terms are allocated to macrocells in “product term clusters.” The availability and distribution of product term clusters are automatically considered by the software as it fits functions within a PAL block. The size of a product term cluster has been optimized to provide high utilization of product terms, making complex functions using many product terms possible. Yet when few product terms are used, there will be a minimal number of unused—or wasted—product terms left over. The product term clusters available to each macrocell within a PAL block are shown in Tables 6 and 7.

Each product term cluster is associated with a macrocell. The size of a cluster depends on the configuration of the associated macrocell. When the macrocell is used in synchronous mode (Figure 2a), the basic cluster has 4 product terms. When the associated macrocell is used in asynchronous mode (Figure 2b), the cluster has 2 product terms. Note that if the product term cluster is routed to a different macrocell, the allocator configuration is not determined by the mode of the macrocell actually being driven. The configuration is always set by the mode of the macrocell that the cluster will drive if not routed away, regardless of the actual routing.

In addition, there is an extra product term that can either join the basic cluster to give an extended cluster, or drive the second input of an exclusive-OR gate in the signal path. If included with the basic cluster, this provides for up to 20 product terms on a synchronous function that uses four extended 5-product-term clusters. A similar asynchronous function can have up to 18 product terms.

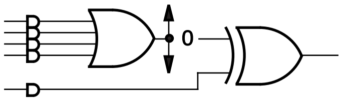
When the extra product term is used to extend the cluster, the value of the second XOR input can be programmed as a 0 or a 1, giving polarity control. The possible configurations of the logic allocator are shown in Figures 3 and 4.



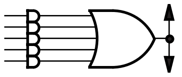
a. Basic cluster with XOR

b. Extended cluster, active high

c. Extended cluster, active low



d. Basic cluster routed away; single-product-term, active high



e. Extended cluster routed away

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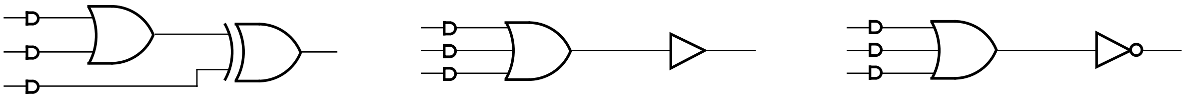
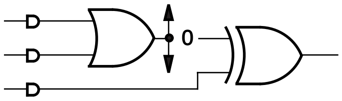
Figure 3. Logic Allocator Configurations: Synchronous Mode



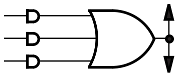
a. Basic cluster with XOR

b. Extended cluster, active high

c. Extended cluster, active low



d. Basic cluster routed away; single-product-term, active high



e. Extended cluster routed away

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Figure 4. Logic Allocator Configurations: Asynchronous Mode

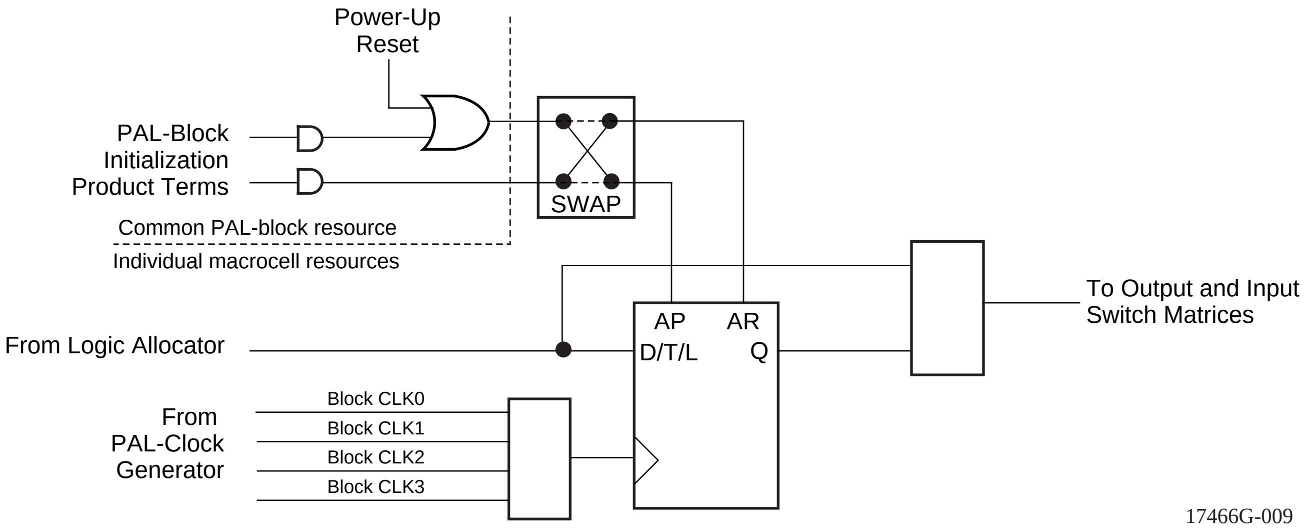
Note that the configuration of the logic allocator has absolutely no impact on the speed of the signal. All configurations have the same delay. This means that designers do not have to decide between optimizing resources or speed; both can be optimized.

If not used in the cluster, the extra product term can act in conjunction with the basic cluster to provide XOR logic for such functions as data comparison, or it can work with the D-,T-type flip-flop to provide for J-K, and S-R register operation. In addition, if the basic cluster is routed to another macrocell, the extra product term is still available for logic. In this case, the first XOR input will be a logic 0. This circuit has the flexibility to route product terms elsewhere without giving up the use of the macrocell.

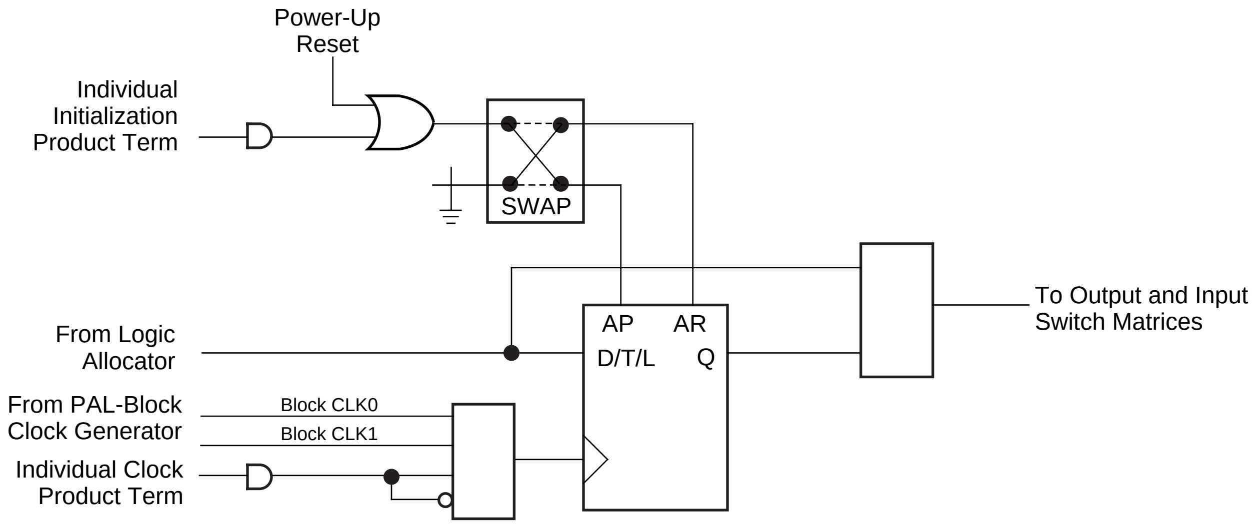
Product term clusters do not “wrap” around a PAL block. This means that the macrocells at the ends of the block have fewer product terms available.

Macrocell

The macrocell consists of a storage element, routing resources, a clock multiplexer, and initialization control. The macrocell has two fundamental modes: synchronous and asynchronous (Figure 5). The mode chosen only affects clocking and initialization in the macrocell.



a. Synchronous mode



b. Asynchronous mode

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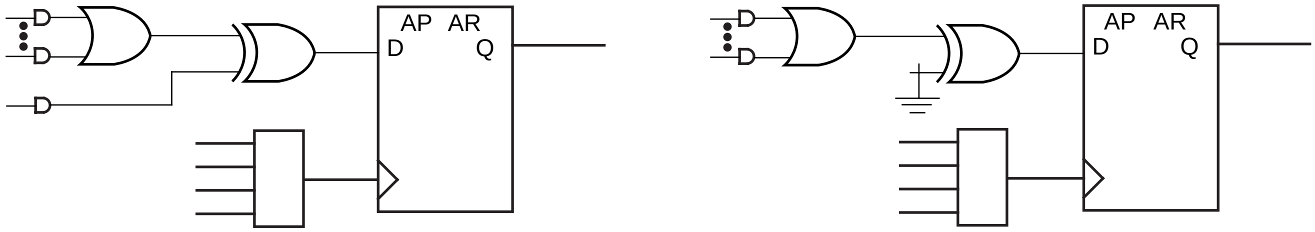
Figure 5. Macrocell

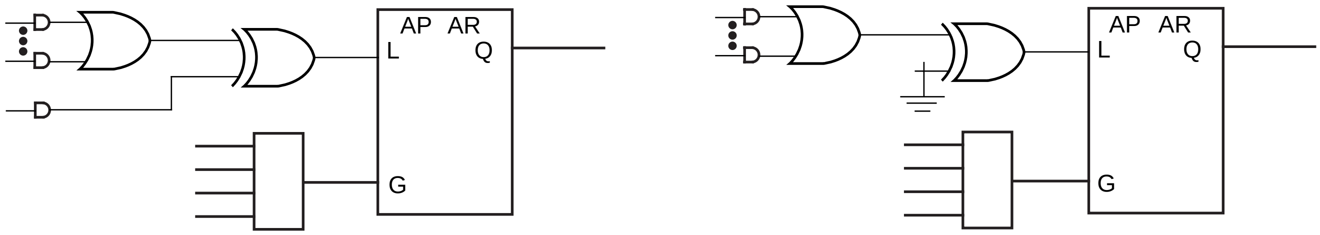
In either mode, a combinatorial path can be used. For combinatorial logic, the synchronous mode will generally be used, since it provides more product terms in the allocator.

The flip-flop can be configured as a D-type or T-type latch. J-K or S-R registers can be synthesized. The primary flip-flop configurations are shown in Figure 6, although others are possible. Flip-flop functionality is defined in Table 8. Note that a J-K latch is inadvisable as it will cause oscillation if both J and K inputs are HIGH.



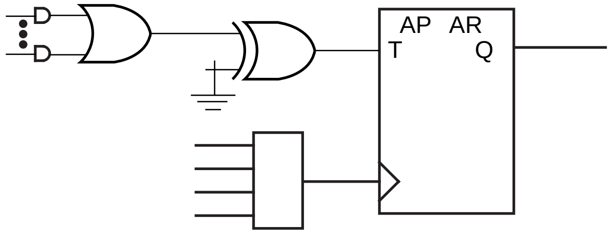
a. D-type with XOR

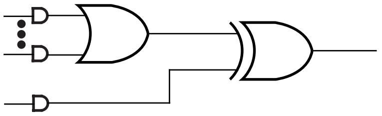
b. D-type with programmable D polarity



c. Latch with XOR

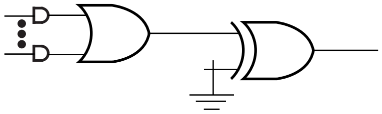
d. Latch with programmable D polarity





f. Combinatorial with XOR

e. T-type with programmable T polarity



g. Combinatorial with programmable polarity

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Figure 6. Primary Macrocell Configurations

Table 8. Register/Latch Operation

Configuration	Input(s)	CLK/LE [1]	Q+
D-type Register	D=X	0,1, ↓ (↑)	Q
	D=0	↑ (↓)	0
	D=1	↑ (↓)	1
T-type Register	T=X	0, 1, ↓ (↑)	Q
	T=0	↑ (↓)	Q
	T=1	↑ (↓)	$\overline{Q}$
D-type Latch	D=X	1(0)	Q
	D=0	0(1)	0
	D=1	0(1)	1

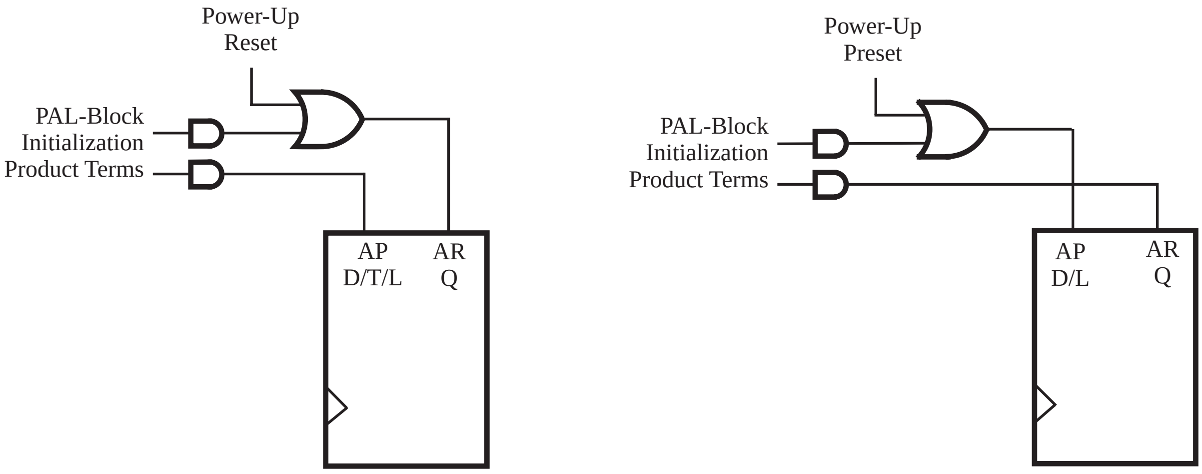
Note:

1. *Polarity of CLK/LE can be programmed*

Although the macrocell shows only one input to the register, the XOR gate in the logic allocator allows the D-, T-type register to emulate J-K, and S-R behavior. In this case, the available product terms are divided between J and K (or S and R). When configured as J-K, S-R, or T-type, the extra product term must be used on the XOR gate input for flip-flop emulation. In any register type, the polarity of the inputs can be programmed.

The clock input to the flip-flop can select any of the four PAL block clocks in synchronous mode, with the additional choice of either polarity of an individual product term clock in the asynchronous mode.

The initialization circuit depends on the mode. In synchronous mode (Figure 7), asynchronous reset and preset are provided, each driven by a product term common to the entire PAL block.



a. Power-up reset

b. Power-up preset

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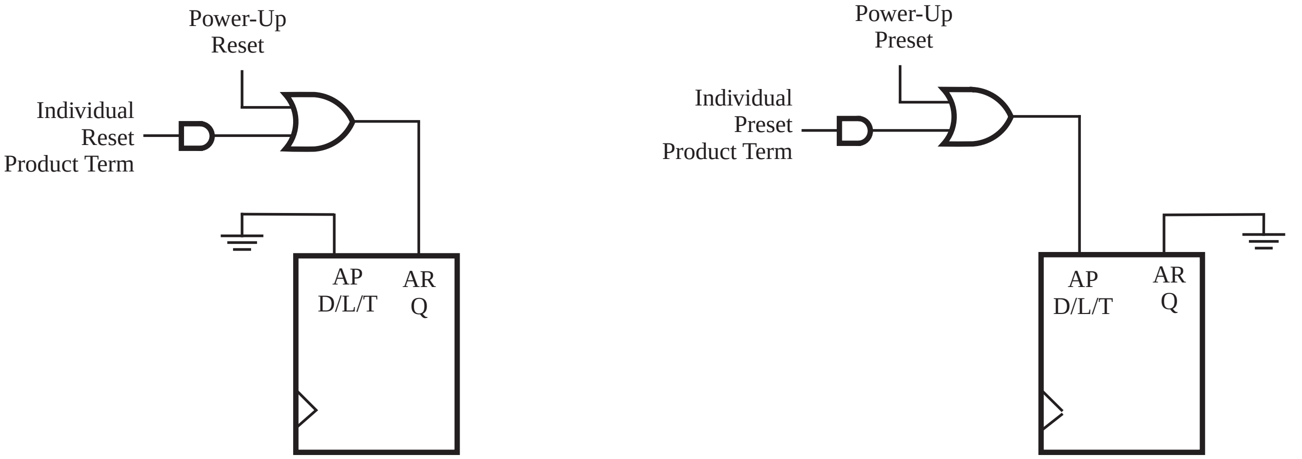
Figure 7. Synchronous Mode Initialization Configurations

A reset/preset swapping feature in each macrocell allows for reset and preset to be exchanged, providing flexibility. In asynchronous mode (Figure 8), a single individual product term is provided for initialization. It can be selected to control reset or preset.



a. Reset

b. Preset

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Figure 8. Asynchronous Mode Initialization Configurations

Note that the reset/preset swapping selection feature effects power-up reset as well. The initialization functionality of the flip-flops is illustrated in Table 9. The macrocell sends its data to the output switch matrix and the input switch matrix. The output switch matrix can route this data to an output if so desired. The input switch matrix can send the signal back to the central switch matrix as feedback.

Table 9. Asynchronous Reset/Preset Operation

AR	AP	CLK/LE[1]	Q+
0	0	X	See Table 8
0	1	X	1
1	0	X	0
1	1	X	0

Note:

1. *Transparent latch is unaffected by AR, AP*

Input Switch Matrix

The input switch matrix (Figures 12 and 13) optimizes routing of inputs to the central switch matrix. Without the input switch matrix, each input and feedback signal has only one way to enter the central switch matrix. The input switch matrix provides additional ways for these signals to enter the central switch matrix.

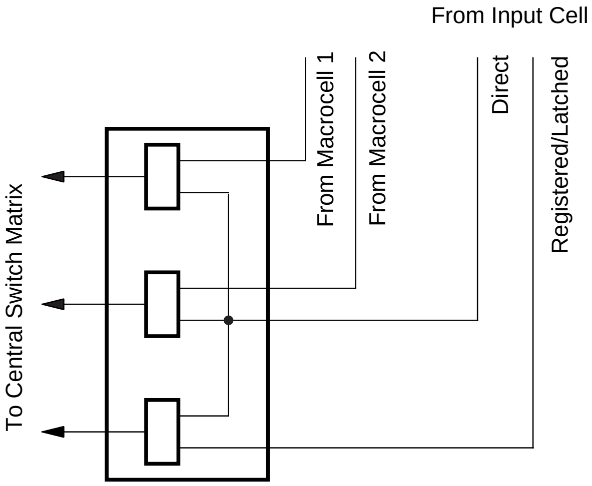

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Figure 12. ispMACH 4A with 2:1 Macrocell-I/O Cell Ratio - Input Switch Matrix

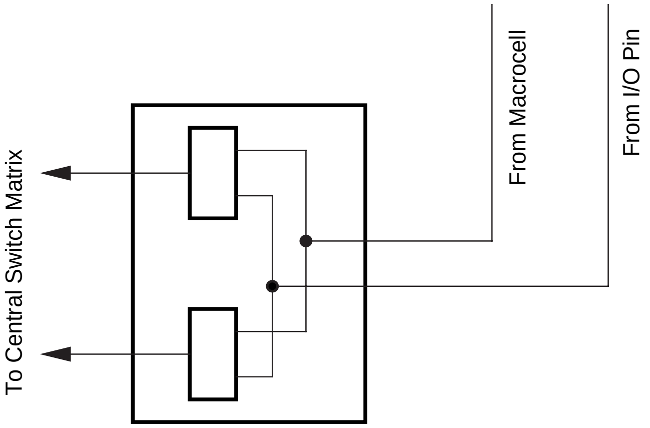

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Figure 13. ispMACH 4A with 1:1 Macrocell-I/O Cell Ratio - Input Switch Matrix

IEEE 1149.1-COMPLIANT BOUNDARY SCAN TESTABILITY

All ispMACH 4A devices have boundary scan cells and are compliant to the IEEE 1149.1 standard. This allows functional testing of the circuit board on which the device is mounted through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test node data to be captured and shifted out for verification. In addition, these devices can be linked into a board-level serial scan path for more complete board-level testing.

IEEE 1149.1-COMPLIANT IN-SYSTEM PROGRAMMING

Programming devices in-system provides a number of significant benefits including: rapid prototyping, lower inventory levels, higher quality, and the ability to make in-field modifications. All ispMACH 4A devices provide In-System Programming (ISP) capability through their Boundary ScanTest Access Ports. This capability has been implemented in a manner that ensures that the port remains compliant to the IEEE 1149.1 standard. By using IEEE 1149.1 as the communication interface through which ISP is achieved, customers get the benefit of a standard, well-defined interface.

ispMACH 4A devices can be programmed across the commercial temperature and voltage range. The PC-based ispVM™ software facilitates in-system programming of ispMACH 4A devices. ispVM takes the JEDEC file output produced by the design implementation software, along with information about the JTAG chain, and creates a set of vectors that are used to drive the JTAG chain. ispVM software can use these vectors to drive a JTAG chain via the parallel port of a PC. Alternatively, ispVM software can output files in formats understood by common automated test equipment. This equpment can then be used to program ispMACH 4A devices during the testing of a circuit board.

PCI COMPLIANT

ispMACH 4A devices in the -5/-55/-6/-65/-7/-10/-12 speed grades are compliant with the *PCI Local Bus Specification* version 2.1, published by the PCI Special Interest Group (SIG). The 5-V devices are fully PCI-compliant. The 3.3-V devices are mostly compliant but do not meet the PCI condition to clamp the inputs as they rise above V_{CC} because of their 5-V input tolerant feature.

SAFE FOR MIXED SUPPLY VOLTAGE SYSTEM DESIGNS

Both the 3.3-V and 5-V V_{CC} ispMACH 4A devices are safe for mixed supply voltage system designs. The 5-V devices will not overdrive 3.3-V devices above the output voltage of 3.3 V, while they accept inputs from other 3.3-V devices. The 3.3-V device will accept inputs up to 5.5 V. Both the 5-V and 3.3-V versions have the same high-speed performance and provide easy-to-use mixed-voltage design capability.

PULL UP OR BUS-FRIENDLY INPUTS AND I/Os

All ispMACH 4A devices have inputs and I/Os which feature the Bus-Friendly circuitry incorporating two inverters in series which loop back to the input. This double inversion weakly holds the input at its last driven logic state. While it is good design practice to tie unused pins to a known state, the Bus-Friendly input structure pulls pins away from the input threshold voltage where noise can cause high-frequency switching. At power-up, the Bus-Friendly latches are reset to a logic level "1." For the circuit diagram, please refer to the document entitled *MACH Endurance Characteristics* on the Lattice Data Book CD-ROM or Lattice web site.

All ispMACH 4A devices have a programmable bit that configures all inputs and I/Os with either pull-up or Bus-Friendly characteristics. If the device is configured in pull-up mode, all inputs and I/O pins are weakly pulled up. For the circuit diagram, please refer to the document entitled *MACH Endurance Characteristics* on the Lattice Data Book CD-ROM or Lattice web site.

POWER MANAGEMENT

Each individual PAL block in ispMACH 4A devices features a programmable low-power mode, which results in power savings of up to 50%. The signal speed paths in the low-power PAL block will be slower than those in the non-low-power PAL block. This feature allows speed critical paths to run at maximum frequency while the rest of the signal paths operate in the low-power mode.

PROGRAMMABLE SLEW RATE

Each ispMACH 4A device I/O has an individually programmable output slew rate control bit. Each output can be individually configured for the higher speed transition (3 V/ns) or for the lower noise transition (1 V/ns). For high-speed designs with long, unterminated traces, the slow-slew rate will introduce fewer reflections, less noise, and keep ground bounce to a minimum. For designs with short traces or well terminated lines, the fast slew rate can be used to achieve the highest speed. The slew rate is adjusted independent of power.

POWER-UP RESET/SET

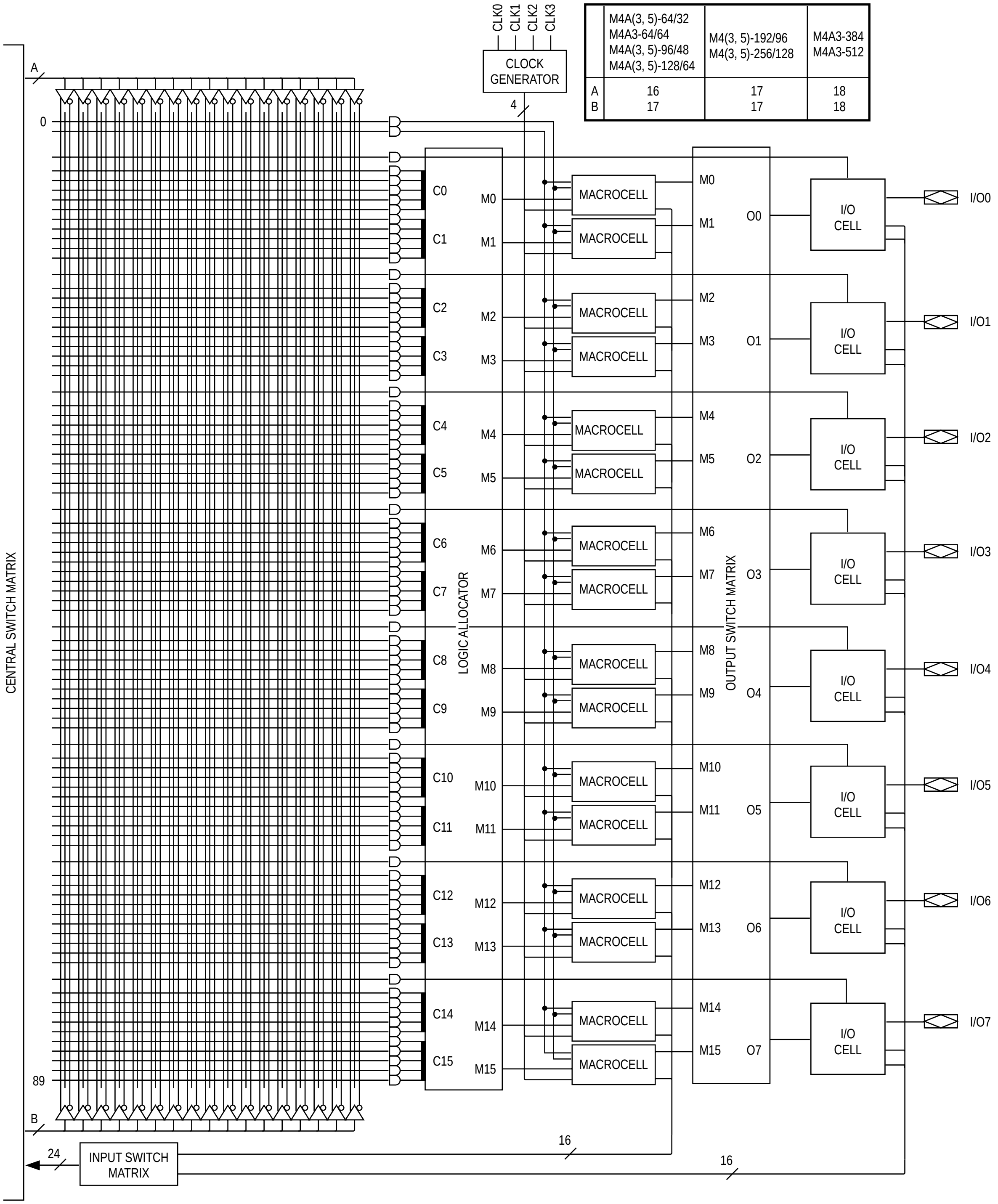
All flip-flops power up to a known state for predictable system initialization. If a macrocell is configured to SET on a signal from the control generator, then that macrocell will be SET during device power-up. If a macrocell is configured to RESET on a signal from the control generator or is not configured for set/reset, then that macrocell will RESET on power-up. To guarantee initialization values, the V_{CC} rise must be monotonic, and the clock must be inactive until the reset delay time has elapsed.

SECURITY BIT

A programmable security bit is provided on the ispMACH 4A devices as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, this bit defeats readback of the programmed pattern by a device programmer, securing proprietary designs from competitors. Programming and verification are also defeated by the security bit. The bit can only be reset by erasing the entire device.

HOT SOCKETING

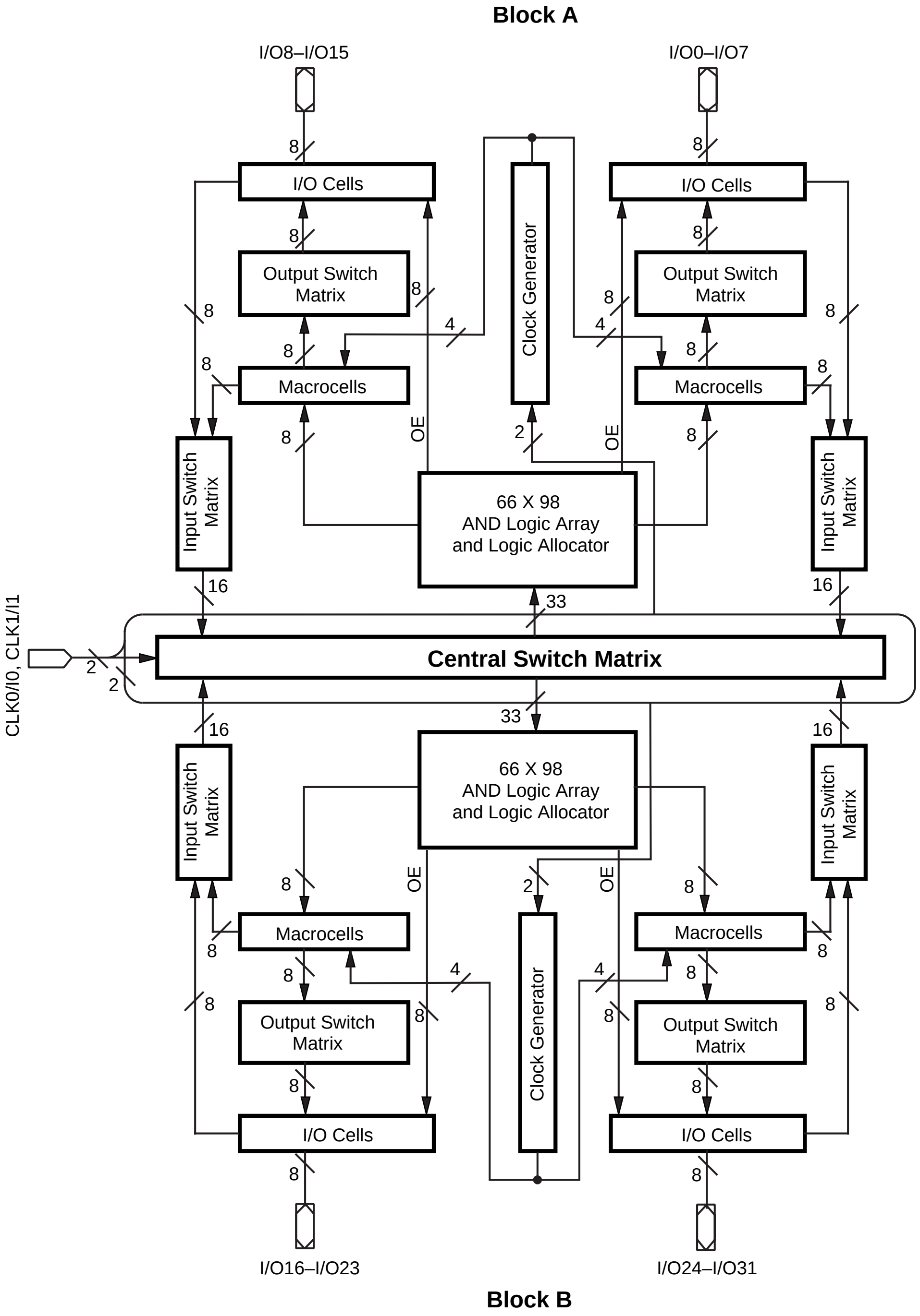
ispMACH 4A devices are well-suited for those applications that require hot socketing capability. Hot socketing a device requires that the device, when powered down, can tolerate active signals on the I/Os and inputs without being damaged. Additionally, it requires that the effects of the powered-down MACH devices be minimal on active signals.



	M4A(3, 5)-64/32 M4A3-64/64 M4A(3, 5)-96/48 M4A(3, 5)-128/64	M4(3, 5)-192/96 M4(3, 5)-256/128	M4A3-384 M4A3-512
A	16	17	18
B	17	17	18

Figure 16. PAL Block for ispMACH 4A with 2:1 Macrocell - I/O Cell Ratio

BLOCK DIAGRAM – M4A(3,5)-32/32



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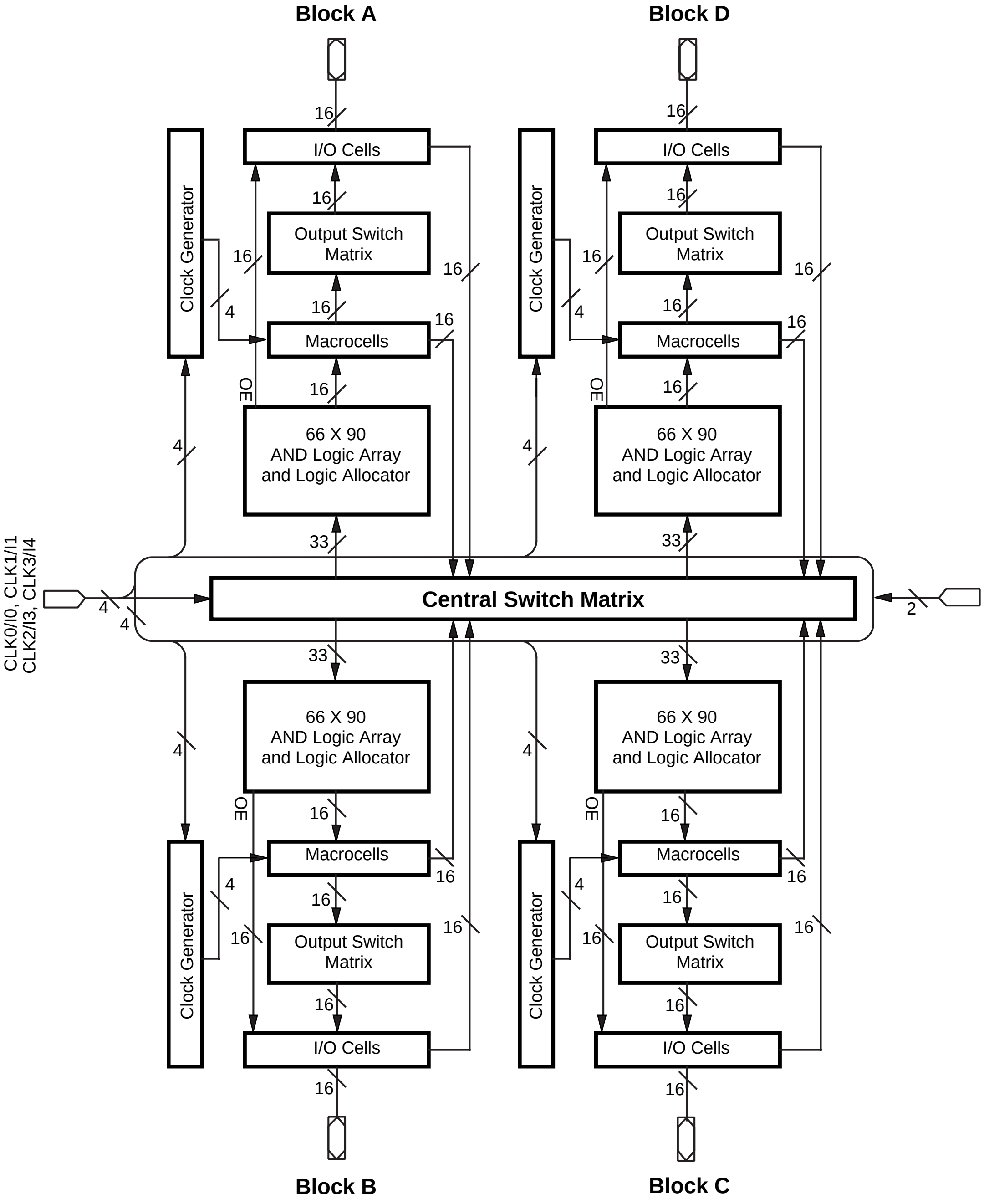
BLOCK DIAGRAM – M4A3-64/64



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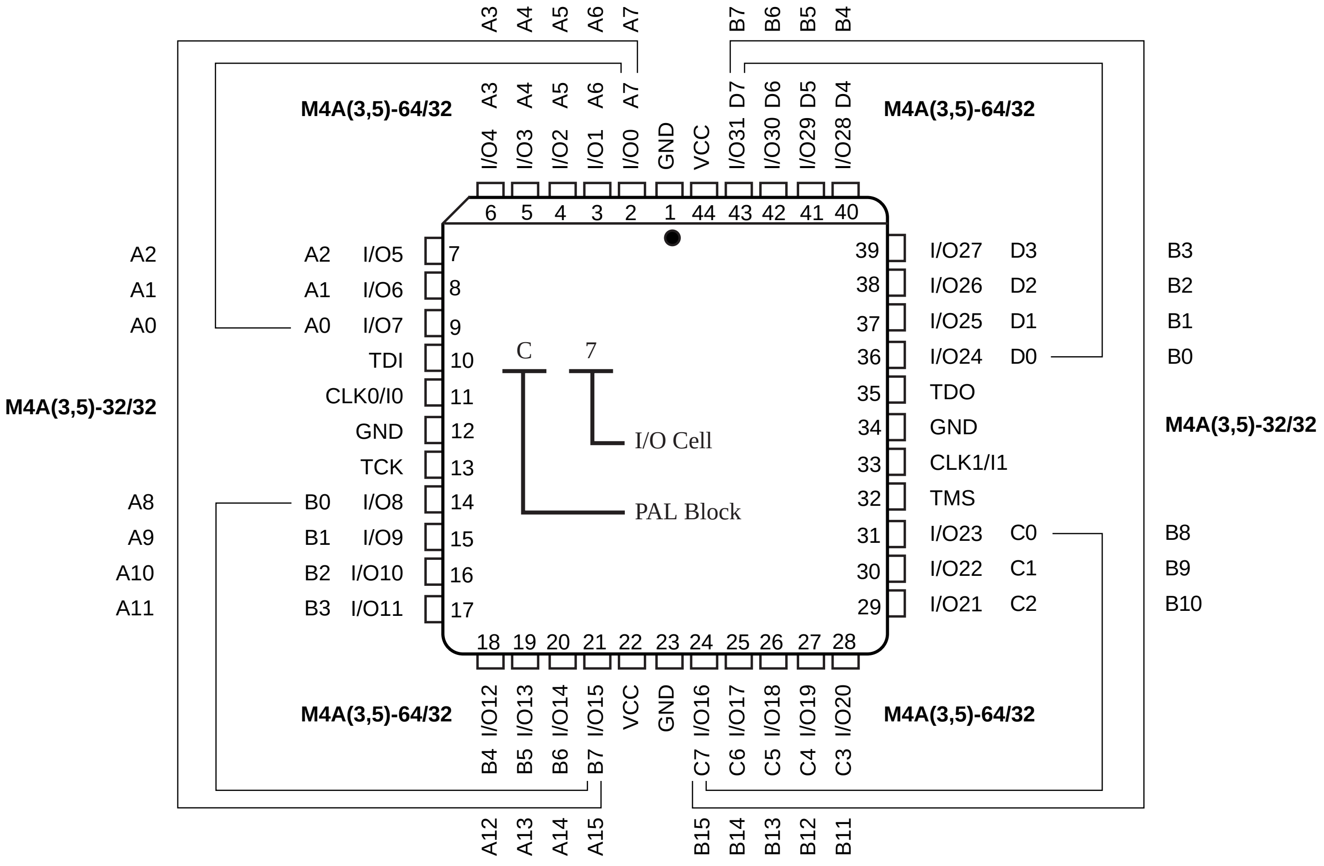
44-PIN PLCC CONNECTION DIAGRAM (M4A(3,5)-32/32 AND M4A(3,5)-64/32)

Top View

44-Pin PLCC



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PIN DESIGNATIONS

CLK/I = Clock or Input

GND = Ground

I/O = Input/Output

V_{CC} = Supply Voltage

TDI = Test Data In

TCK = Test Clock

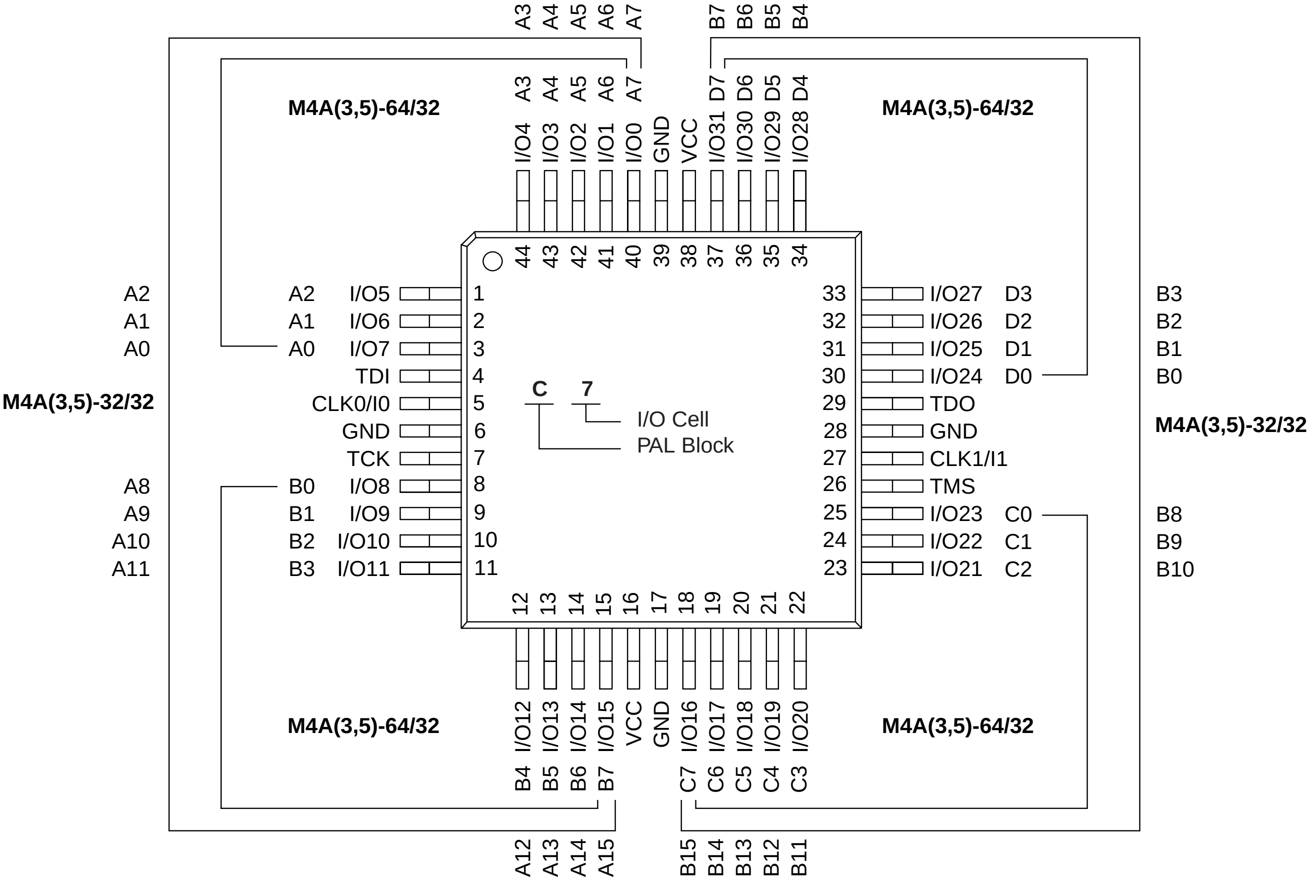
TMS = Test Mode Select

TDO = Test Data Out

44-PIN TQFP CONNECTION DIAGRAM (M4A(3,5)-32/32 AND M4A(3,5)-64/32)

Top View

44-Pin TQFP (1.0mm Thickness)



PIN DESIGNATIONS

CLK / I = Clock or Input

GND = Ground

I / O = Input / Output

V_{CC} = Supply Voltage

TDI = Test Data In

TCK = Test Clock

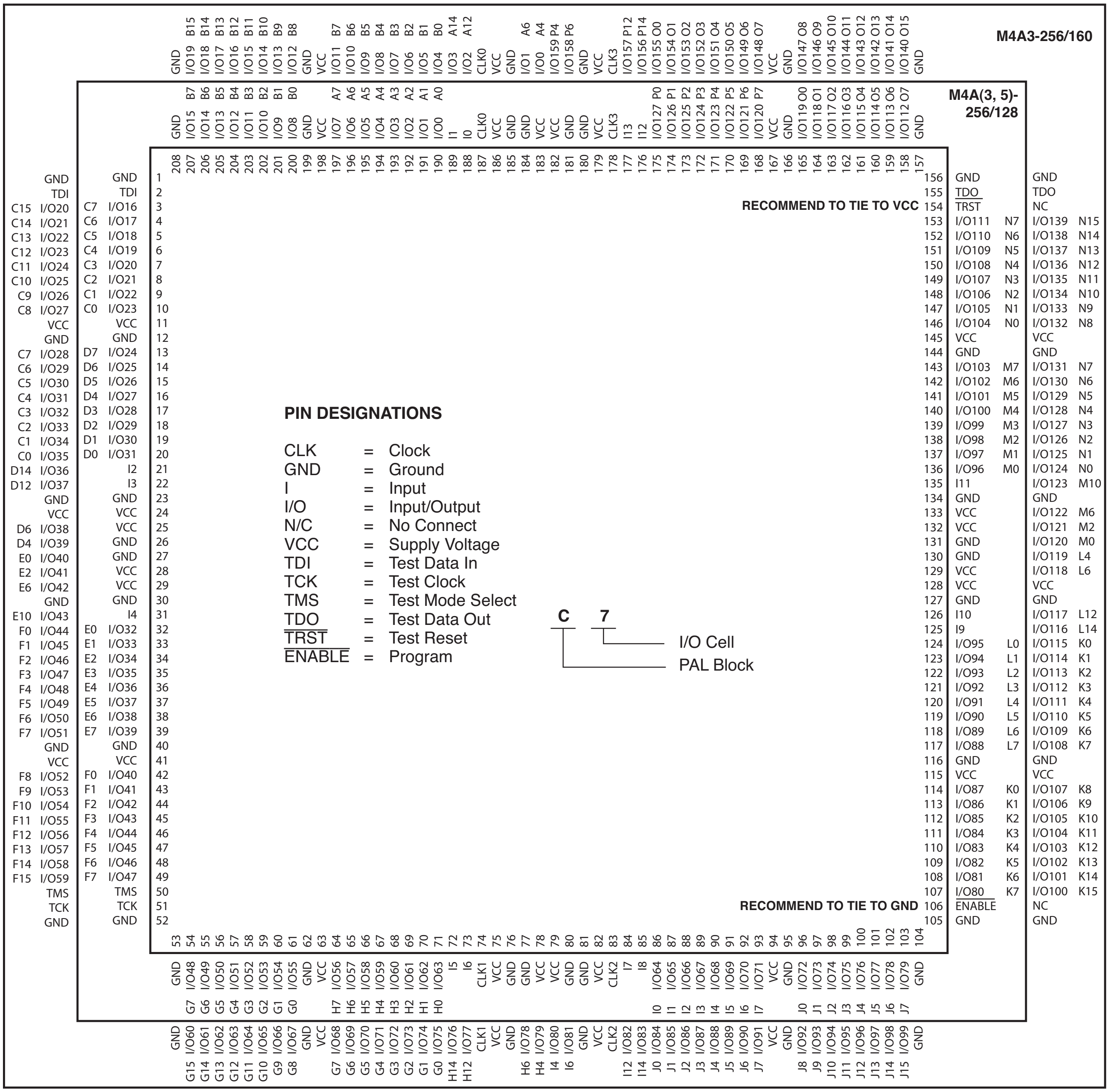
TMS = Test Mode Select

TDO = Test Data Out

208-PIN PQFP CONNECTION DIAGRAM (M4A(3,5)-256/128 AND M4A3-256/160)

Top View

208-Pin PQFP



PIN DESIGNATIONS

CLK = Clock
GND = Ground
I = Input
I/O = Input/Output
N/C = No Connect
VCC = Supply Voltage
TDI = Test Data In
TCK = Test Clock
TMS = Test Mode Select
TDO = Test Data Out
$\overline{\text{TRST}}$ = Test Reset
$\overline{\text{ENABLE}}$ = Program

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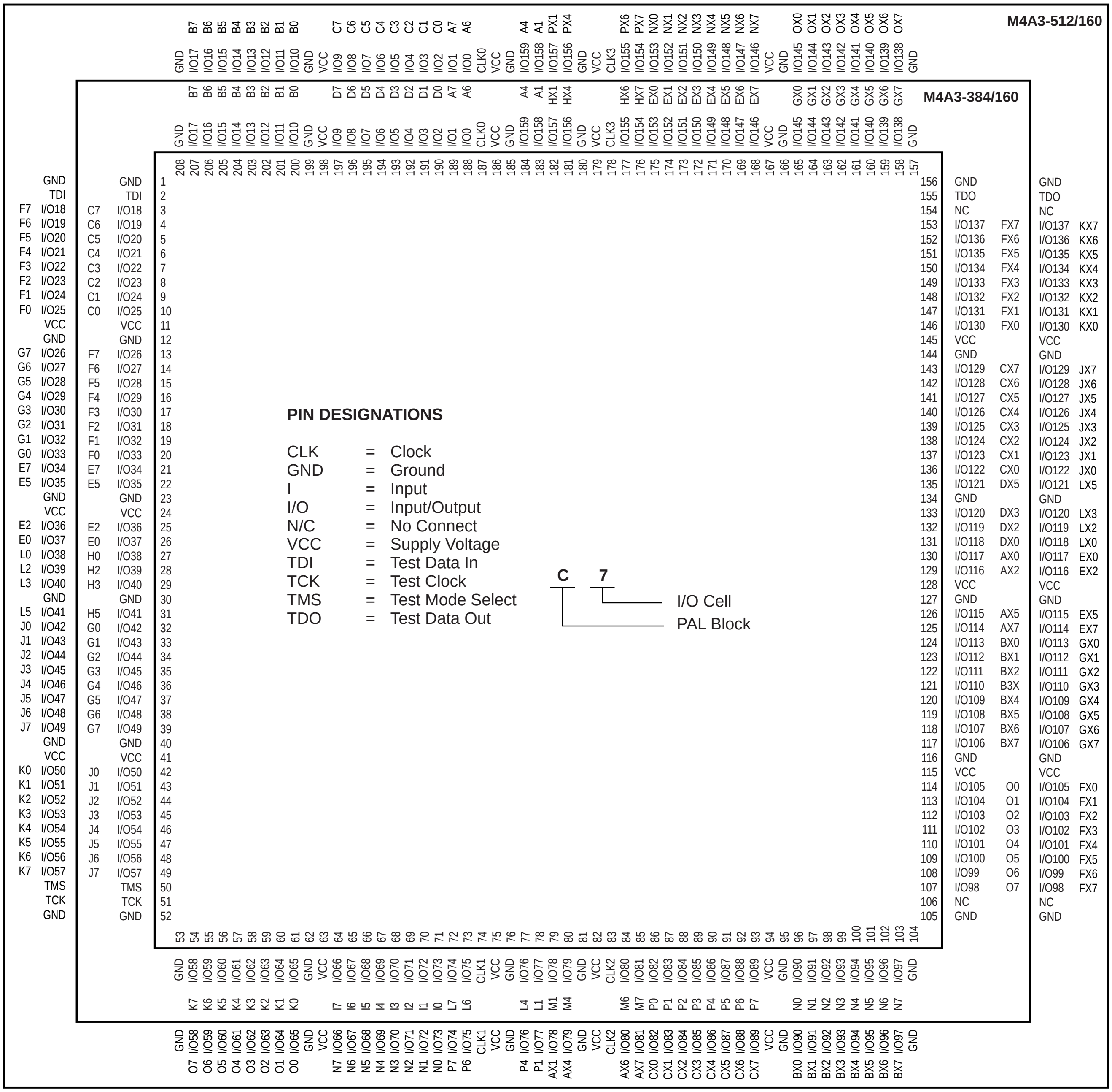
208-PIN PQFP CONNECTION DIAGRAM (M4A3-384/160 AND M4A3-512/160)

Top View

208-Pin PQFP



PIN DESIGNATIONS

CLK = Clock
GND = Ground
I = Input
I/O = Input/Output
N/C = No Connect
VCC = Supply Voltage
TDI = Test Data In
TCK = Test Clock
TMS = Test Mode Select
TDO = Test Data Out

	M4A3-384/160		M4A3-512/160	
1	GND		GND	
2	TDI		TDI	
3	I/O18	C7	I/O18	F7
4	I/O19	C6	I/O19	F6
5	I/O20	C5	I/O20	F5
6	I/O21	C4	I/O21	F4
7	I/O22	C3	I/O22	F3
8	I/O23	C2	I/O23	F2
9	I/O24	C1	I/O24	F1
10	I/O25	C0	I/O25	F0
11	VCC		VCC	
12	GND		GND	
13	I/O26	F7	I/O26	G7
14	I/O27	F6	I/O27	G6
15	I/O28	F5	I/O28	G5
16	I/O29	F4	I/O29	G4
17	I/O30	F3	I/O30	G3
18	I/O31	F2	I/O31	G2
19	I/O32	F1	I/O32	G1
20	I/O33	F0	I/O33	G0
21	I/O34	E7	I/O34	E7
22	I/O35	E5	I/O35	E5
23	GND		GND	
24	VCC		VCC	
25	I/O36	E2	I/O36	E2
26	I/O37	E0	I/O37	E0
27	I/O38	H0	I/O38	L0
28	I/O39	H2	I/O39	L2
29	I/O40	H3	I/O40	L3
30	GND		GND	
31	I/O41	H5	I/O41	L5
32	I/O42	G0	I/O42	J0
33	I/O43	G1	I/O43	J1
34	I/O44	G2	I/O44	J2
35	I/O45	G3	I/O45	J3
36	I/O46	G4	I/O46	J4
37	I/O47	G5	I/O47	J5
38	I/O48	G6	I/O48	J6
39	I/O49	G7	I/O49	J7
40	GND		GND	
41	VCC		VCC	
42	I/O50	J0	I/O50	K0
43	I/O51	J1	I/O51	K1
44	I/O52	J2	I/O52	K2
45	I/O53	J3	I/O53	K3
46	I/O54	J4	I/O54	K4
47	I/O55	J5	I/O55	K5
48	I/O56	J6	I/O56	K6
49	I/O57	J7	I/O57	K7
50	TMS		TMS	
51	TCK		TCK	
52	GND		GND	
53	GND		GND	
54	I/O58	K7	I/O58	O7
55	I/O59	K6	I/O59	O6
56	I/O60	K5	I/O60	O5
57	I/O61	K4	I/O61	O4
58	I/O62	K3	I/O62	O3
59	I/O63	K2	I/O63	O2
60	I/O64	K1	I/O64	O1
61	I/O65	K0	I/O65	O0
62	GND		GND	
63	VCC		VCC	
64	I/O66	I7	I/O66	N7
65	I/O67	I6	I/O67	N6
66	I/O68	I5	I/O68	N5
67	I/O69	I4	I/O69	N4
68	I/O70	I3	I/O70	N3
69	I/O71	I2	I/O71	N2
70	I/O72	I1	I/O72	N1
71	I/O73	I0	I/O73	N0
72	I/O74	L7	I/O74	P7
73	I/O75	L6	I/O75	P6
74	CLK1		CLK1	
75	VCC		VCC	
76	GND		GND	
77	I/O76	L4	I/O76	P4
78	I/O77	L1	I/O77	P1
79	I/O78	M1	I/O78	AX1
80	I/O79	M4	I/O79	AX4
81	GND		GND	
82	VCC		VCC	
83	CLK2		CLK2	
84	I/O80	M6	I/O80	AX6
85	I/O81	M7	I/O81	AX7
86	I/O82	P0	I/O82	CX0
87	I/O83	P1	I/O83	CX1
88	I/O84	P2	I/O84	CX2
89	I/O85	P3	I/O85	CX3
90	I/O86	P4	I/O86	CX4
91	I/O87	P5	I/O87	CX5
92	I/O88	P6	I/O88	CX6
93	I/O89	P7	I/O89	CX7
94	VCC		VCC	
95	GND		GND	
96	I/O90	N0	I/O90	BX0
97	I/O91	N1	I/O91	BX1
98	I/O92	N2	I/O92	BX2
99	I/O93	N3	I/O93	BX3
100	I/O94	N4	I/O94	BX4
101	I/O95	N5	I/O95	BX5
102	I/O96	N6	I/O96	BX6
103	I/O97	N7	I/O97	BX7
104	GND		GND	
105	GND		GND	
106	NC		NC	
107	I/O98	O7	I/O98	FX7
108	I/O99	O6	I/O99	FX6
109	I/O100	O5	I/O100	FX5
110	I/O101	O4	I/O101	FX4
111	I/O102	O3	I/O102	FX3
112	I/O103	O2	I/O103	FX2
113	I/O104	O1	I/O104	FX1
114	I/O105	O0	I/O105	FX0
115	VCC		VCC	
116	GND		GND	
117	I/O106	BX7	I/O106	GX7
118	I/O107	BX6	I/O107	GX6
119	I/O108	BX5	I/O108	GX5
120	I/O109	BX4	I/O109	GX4
121	I/O110	B3X	I/O110	GX3
122	I/O111	BX2	I/O111	GX2
123	I/O112	BX1	I/O112	GX1
124	I/O113	BX0	I/O113	GX0
125	I/O114	AX7	I/O114	EX7
126	I/O115	AX5	I/O115	EX5
127	GND		GND	
128	VCC		VCC	
129	I/O116	AX2	I/O116	EX2
130	I/O117	AX0	I/O117	EX0
131	I/O118	DX0	I/O118	LX0
132	I/O119	DX2	I/O119	LX2
133	I/O120	DX3	I/O120	LX3
134	GND		GND	
135	I/O121	DX5	I/O121	LX5
136	I/O122	CX0	I/O122	JX0
137	I/O123	CX1	I/O123	JX1
138	I/O124	CX2	I/O124	JX2
139	I/O125	CX3	I/O125	JX3
140	I/O126	CX4	I/O126	JX4
141	I/O127	CX5	I/O127	JX5
142	I/O128	CX6	I/O128	JX6
143	I/O129	CX7	I/O129	JX7
144	GND		GND	
145	VCC		VCC	
146	I/O130	FX0	I/O130	KX0
147	I/O131	FX1	I/O131	KX1
148	I/O132	FX2	I/O132	KX2
149	I/O133	FX3	I/O133	KX3
150	I/O134	FX4	I/O134	KX4
151	I/O135	FX5	I/O135	KX5
152	I/O136	FX6	I/O136	KX6
153	I/O137	FX7	I/O137	KX7
154	NC		NC	
155	TDO		TDO	
156	GND		GND	
157	GND		GND	
158	I/O138	GX7	I/O138	OX7
159	I/O139	GX6	I/O139	OX6
160	I/O140	GX5	I/O140	OX5
161	I/O141	GX4	I/O141	OX4
162	I/O142	GX3	I/O142	OX3
163	I/O143	GX2	I/O143	OX2
164	I/O144	GX1	I/O144	OX1
165	I/O145	GX0	I/O145	OX0
166	GND		GND	
167	VCC		VCC	
168	I/O146	EX7	I/O146	NX7
169	I/O147	EX6	I/O147	NX6
170	I/O148	EX5	I/O148	NX5
171	I/O149	EX4	I/O149	NX4
172	I/O150	EX3	I/O150	NX3
173	I/O151	EX2	I/O151	NX2
174	I/O152	EX1	I/O152	NX1
175	I/O153	EX0	I/O153	NX0
176	I/O154	HX7	I/O154	PX7
177	I/O155	HX6	I/O155	PX6
178	CLK3		CLK3	
179	VCC		VCC	
180	GND		GND	
181	I/O156	HX4	I/O156	PX4
182	I/O157	HX1	I/O157	PX1
183	I/O158	A1	I/O158	A1
184	I/O159	A4	I/O159	A4
185	GND		GND	
186	VCC		VCC	
187	CLK0		CLK0	
188	I/O0	A6	I/O0	A6
189	I/O1	A7	I/O1	A7
190	I/O2	D0	I/O2	C0
191	I/O3	D1	I/O3	C1
192	I/O4	D2	I/O4	C2
193	I/O5	D3	I/O5	C3
194	I/O6	D4	I/O6	C4
195	I/O7	D5	I/O7	C5
196	I/O8	D6	I/O8	C6
197	I/O9	D7	I/O9	C7
198	VCC		VCC	
199	GND		GND	
200	I/O10	B0	I/O10	B0
201	I/O11	B1	I/O11	B1
202	I/O12	B2	I/O12	B2
203	I/O13	B3	I/O13	B3
204	I/O14	B4	I/O14	B4
205	I/O15	B5	I/O15	B5
206	I/O16	B6	I/O16	B6
207	I/O17	B7	I/O17	B7
208	GND		GND	

17466Ga-044

256-BALL fpBGA CONNECTION DIAGRAM (M4A3-256/128)

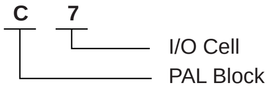
Bottom View

256-Ball fpBGA

	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	$\overline{\text{TRST}}$	I/O117 O5	I/O116 O4	I/O113 O1	I/O126 P6	I/O124 P4	I12	NC	NC	NC	CLK0	I/O1 A1	I/O5 A5	I/O7 A7	I/O10 B2	I/O12 B4	**A**
B	I/O110 N6	I/O111 N7	I/O118 O6	I/O115 O3	I/O127 P7	I/O125 P5	I/O120 P0	NC	NC	NC	I1	I/O2 A2	I/O8 B0	I/O11 B3	I/O13 B5	NC	**B**
C	I/O108 N4	I/O109 N5	NC	I/O119 O7	I/O114 O2	I/O122 P2	I/O123 P3	NC	NC	I0	I/O4 A4	I/O6 A6	I/O15 B7	I/O14 B6	TDI	I/O23 C7	**C**
D	NC	I/O104 N0	TDO	GND	GND	VCC	GND	VCC	GND	GND	VCC	GND	VCC	I/O9 B1	I/O22 C6	I/O21 C5	**D**
E	I/O102 M6	NC	I/O107 N3	VCC	I/O105 N1	I/O106 N2	I13	CLK3	NC	NC	I/O0 A0	NC	GND	I/O20 C4	I/O19 C3	I/O31 D7	**E**
F	I/O98 M2	I/O103 M7	I/O101 M5	GND	I/O100 M4	I/O99 M3	I/O112 O0	I/O121 P1	NC	NC	I/O3 A3	I/O18 C2	VCC	I/O16 C0	I/O30 D6	I/O29 D5	**F**
G	NC	I/O96 M0	I11	VCC	NC	I/O97 M1	VCC	GND	GND	VCC	I/O17 C1	I/O28 D4	GND	I/O26 D2	I/O25 D1	I2	**G**
H	I/O88 L0	I10	I9	GND	I/O89 L1	I/O90 L2	GND	VCC	VCC	GND	I/O27 D3	I/O24 D0	VCC	NC	NC	NC	**H**
J	I/O91 L3	I/O92 L4	I/O93 L5	GND	I/O95 L7	I/O94 L6	GND	VCC	VCC	GND	I3	NC	GND	NC	NC	NC	**J**
K	NC	NC	NC	VCC	NC	NC	VCC	GND	GND	VCC	NC	NC	VCC	I4	NC	I/O32 E0	**K**
L	NC	NC	I/O80 K0	GND	I/O83 K3	NC	NC	NC	I/O59 H3	I/O61 H5	NC	NC	GND	I/O35 E3	I/O36 E4	I/O33 E1	**L**
M	I/O81 K1	I/O82 K2	I/O84 K4	GND	I/O67 I3	I/O65 I1	NC	NC	I/O58 H2	I/O48 G0	I/O51 G3	NC	VCC	I/O44 F4	I/O39 E7	I/O34 E2	**M**
N	I/O85 K5	I/O86 K6	$\overline{\text{ENABLE}}$	VCC	GND	VCC	GND	VCC	GND	GND	VCC	GND	GND	TCK	I/O40 F0	I/O37 E5	**N**
P	I/O87 K7	I/O77 J5	I/O78 J6	I/O79 J7	I/O68 I4	I/O66 I2	NC	NC	NC	I6	I/O63 H7	I/O52 G4	I/O55 G7	TMS	I/O41 F1	I/O38 E6	**P**
R	I/O76 J4	I/O75 J3	I/O72 J0	I/O71 I7	I/O64 I0	I7	NC	NC	NC	I/O56 H0	I/O60 H4	I/O49 G1	I/O53 G5	I/O47 F7	I/O43 F3	I/O42 F2	**R**
T	I/O74 J2	I/O73 J1	I/O70 I6	I/O69 I5	I8	CLK2	NC	NC	CLK1	I5	I/O57 H1	I/O62 H6	I/O50 G2	I/O54 G6	I/O46 F6	I/O45 F5	**T**
	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

PIN DESIGNATIONS

CLK = Clock
GND = Ground
I = Input
I/O = Input/Output
N/C = No Connect
VCC = Supply Voltage
TDI = Test Data In
TCK = Test Clock
TMS = Test Mode Select
TDO = Test Data Out
$\overline{\text{TRST}}$ = Test Reset
$\overline{\text{ENABLE}}$ = Program



m4a3.256.128_256bga

ispMACH 4A PRODUCT ORDERING INFORMATION

ispMACH 4A Devices Commercial and Industrial - 3.3V and 5V

Lattice programmable logic products are available with several ordering options. The order number (Valid Combination) is formed by a combination of:

M4A3- 256 / 128 -7 Y C

48 = 48-pin TQFP for
M4A3-32/32 or M4A3-64/32
M4A5-32/32 or M4A5-64/32

FAMILY TYPE

M4A3- = ispMACH 4A Family Low Voltage Advanced Feature (3.3-V V_{CC})
M4A5- = ispMACH 4A Family Advanced Feature (5-V V_{CC})

MACROCELL DENSITY

32 = 32 Macrocells
64 = 64 Macrocells
96 = 96 Macrocells
128 = 128 Macrocells
192 = 192 Macrocells
256 = 256 Macrocells
384 = 384 Macrocells
512 = 512 Macrocells

I/Os

/32 = 32 I/Os in 44-pin PLCC, 44-pin TQFP or 48-pin TQFP
/48 = 48 I/Os in 100-pin TQFP
/64 = 64 I/Os in 100-pin TQFP, 100-pin PQFP, or 100-ball caBGA
/96 = 96 I/Os in 144-pin TQFP or 144-ball fpBGA
/128 = 128 I/Os in 208-pin PQFP, 256-ball BGA or 256-ball fpBGA
/160 = 160 I/Os in 208-pin PQFP
/192 = 192 I/Os in 256-ball BGA or 256-ball fpBGA
/256 = 256 I/Os in 388-ball fpBGA

*Package obsolete, contact factory.

OPERATING CONDITIONS

C = Commercial (0°C to +70°C)
I = Industrial (-40°C to +85°C)

PACKAGE TYPE

SA = Ball Grid Array (BGA)
J = Plastic Leaded Chip Carrier (PLCC)
JN = Lead-free Plastic Leaded Chip Carrier (PLCC)
V = Thin Quad Flat Pack (TQFP)
VN = Lead-free Thin Quad Flat Pack (TQFP)
Y = Plastic Quad Flat Pack (PQFP)
YN = Lead-fee Plastic Quad Flat Pack (PQFP)
FA = Fine-pitch Ball Grid Array (fpBGA)
FAN = Lead-free Fine-pitch Ball Grid Array (fpBGA)
CA = Chip-array Ball Grid Array (caBGA)

SPEED

-5 = 5.0 ns t_{PD}
-55 = 5.5 ns t_{PD}
-6 = 6.0 ns t_{PD}
-65 = 6.5 ns t_{PD}
-7 = 7.5 ns t_{PD}
-10 = 10 ns t_{PD}
-12 = 12 ns t_{PD}
-14 = 14 ns t_{PD}

Conventional Packaging

3.3V Commercial Combinations		
M4A3-32/32	-5, -7, -10	JC, VC, VC48
M4A3-64/32	-55, -7, -10	JC, VC, VC48
M4A3-64/64		VC
M4A3-96/48		VC
M4A3-128/64		YC, VC, CAC
M4A3-192/96	-6, -7, -10	VC, FAC
M4A3-256/128	-55, -65[1], -7, -10	YC, FAC, SAC
M4A3-256/160	-7, -10	YC
M4A3-256/192		FAC
M4A3-384/160	-65, -10, -12	YC
M4A3-384/192		SAC, FAC
M4A3-512/160	-7, -10, -12	YC
M4A3-512/192		FAC
M4A3-512/256		FAC

3.3V Industrial Combinations		
M4A3-32/32	-7, -10, -12	JI, VI, VI48
M4A3-64/32		JI, VI, VI48
M4A3-64/64		VI
M4A3-96/48		VI
M4A3-128/64		YI, VI, CAI
M4A3-192/96		VI, FAI
M4A3-256/128		YI, FAI, SAI
M4A3-256/160	-10, -12	YI
M4A3-256/192		FAI
M4A3-384/160	-10, -12, -14	YI
M4A3-384/192		FAI
M4A3-512/160		YI
M4A3-512/192		FAI
M4A3-512/256		FAI

[1] *Use 5.5ns for new designs.*