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Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details

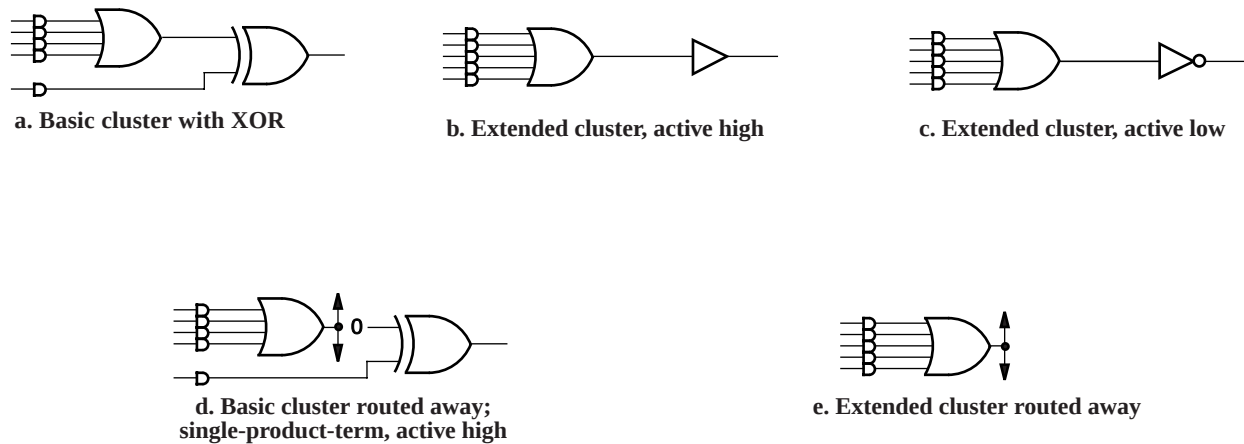
Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	7.5 ns
Voltage Supply - Internal	4.5V ~ 5.5V
Number of Logic Elements/Blocks	-
Number of Macrocells	32
Number of Gates	-
Number of I/O	32
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-TQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/m4a5-32-32-7vi48

The ispMACH 4A family offers 20 density-I/O combinations in Thin Quad Flat Pack (TQFP), Plastic Quad Flat Pack (PQFP), Plastic Leaded Chip Carrier (PLCC), Ball Grid Array (BGA), fine-pitch BGA (fpBGA), and chip-array BGA (caBGA) packages ranging from 44 to 388 pins (Table 3). It also offers I/O safety features for mixed-voltage designs so that the 3.3-V devices can accept 5-V inputs, and 5-V devices do not overdrive 3.3-V inputs. Additional features include Bus-Friendly inputs and I/Os, a programmable power-down mode for extra power savings and individual output slew rate control for the highest speed transition or for the lowest noise transition.

Table 3. ispMACH 4A Package and I/O Options (Number of I/Os and dedicated inputs in Table)

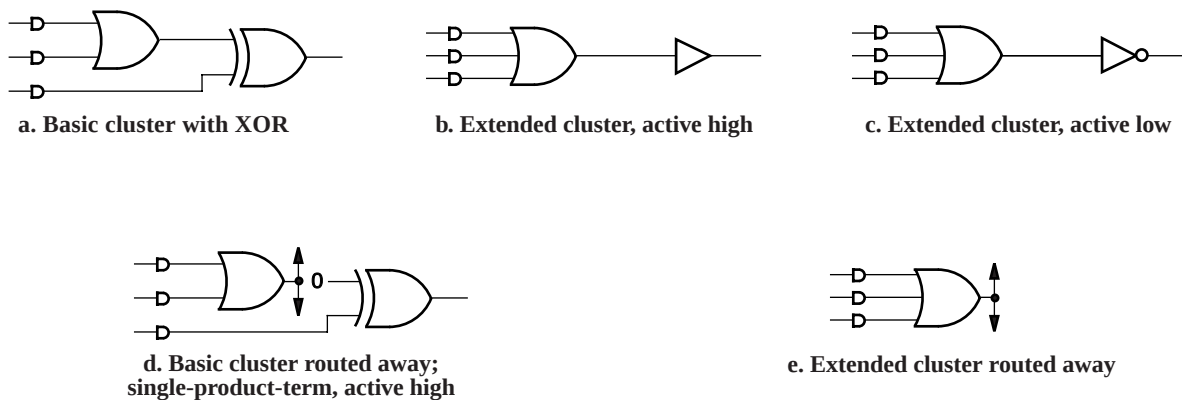
3.3 V Devices								
Package	M4A3-32	M4A3-64	M4A3-96	M4A3-128	M4A3-192	M4A3-256	M4A3-384	M4A3-512
44-pin PLCC	32+2	32+2						
44-pin TQFP	32+2	32+2						
48-pin TQFP	32+2	32+2						
100-pin TQFP		64+6	48+8	64+6				
100-pin PQFP				64+6				
100-ball caBGA				64+6				
144-pin TQFP					96+16			
144-ball fpBGA					96+16			
208-pin PQFP						128+14, 160	160	160
256-ball fpBGA						128+14, 192	192	192
256-ball BGA						128+14	192	
388-ball fpBGA								256

5 V Devices						
Package	M4A5-32	M4A5-64	M4A5-96	M4A5-128	M4A5-192	M4A5-256
44-pin PLCC	32+2	32+2				
44-pin TQFP	32+2	32+2				
48-pin TQFP	32+2	32+2				
100-pin TQFP			48+8	64+6		
100-pin PQFP				64+6		
144-pin TQFP					96+16	
208-pin PQFP						128+14



17466G-007

Figure 3. Logic Allocator Configurations: Synchronous Mode



17466G-008

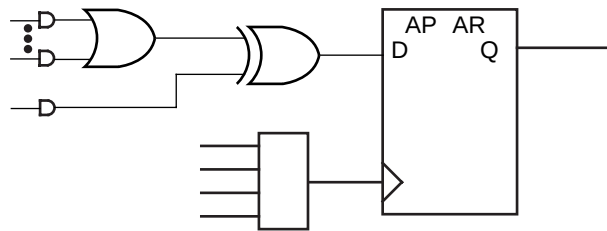
Figure 4. Logic Allocator Configurations: Asynchronous Mode

Note that the configuration of the logic allocator has absolutely no impact on the speed of the signal. All configurations have the same delay. This means that designers do not have to decide between optimizing resources or speed; both can be optimized.

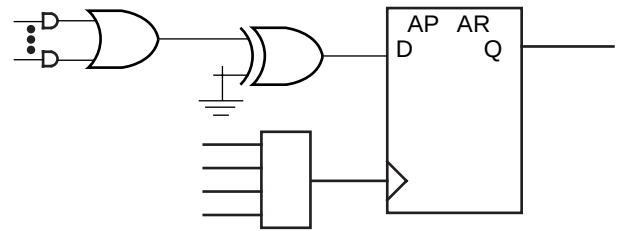
If not used in the cluster, the extra product term can act in conjunction with the basic cluster to provide XOR logic for such functions as data comparison, or it can work with the D-,T-type flip-flop to provide for J-K, and S-R register operation. In addition, if the basic cluster is routed to another macrocell, the extra product term is still available for logic. In this case, the first XOR input will be a logic 0. This circuit has the flexibility to route product terms elsewhere without giving up the use of the macrocell.

Product term clusters do not “wrap” around a PAL block. This means that the macrocells at the ends of the block have fewer product terms available.

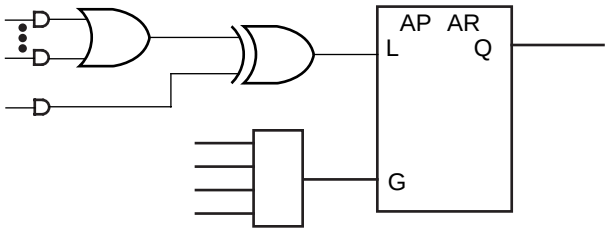
The flip-flop can be configured as a D-type or T-type latch. J-K or S-R registers can be synthesized. The primary flip-flop configurations are shown in Figure 6, although others are possible. Flip-flop functionality is defined in Table 8. Note that a J-K latch is inadvisable as it will cause oscillation if both J and K inputs are HIGH.



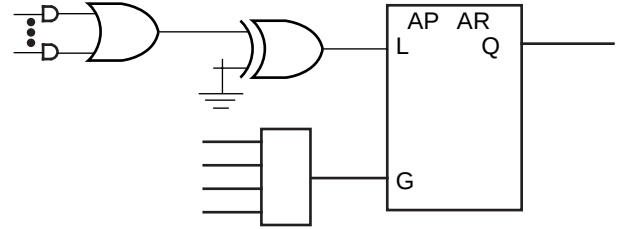
a. D-type with XOR



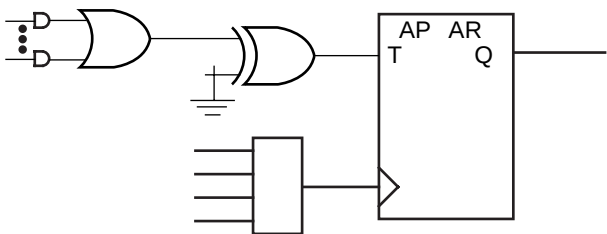
b. D-type with programmable D polarity



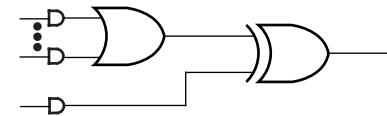
c. Latch with XOR



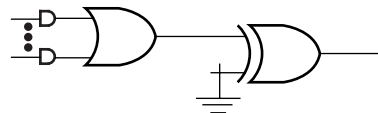
d. Latch with programmable D polarity



e. T-type with programmable T polarity



f. Combinatorial with XOR



g. Combinatorial with programmable polarity

Figure 6. Primary Macrocell Configurations

17466G-011

Output Switch Matrix

The output switch matrix allows macrocells to be connected to any of several I/O cells within a PAL block. This provides high flexibility in determining pinout and allows design changes to occur without effecting pinout.

In ispMACH 4A devices with 2:1 Macrocell-I/O cell ratio, each PAL block has twice as many macrocells as I/O cells. The ispMACH 4A output switch matrix allows for half of the macrocells to drive I/O cells within a PAL block, in combinations according to Figure 9. Each I/O cell can choose from eight macrocells; each macrocell has a choice of four I/O cells. The ispMACH 4A devices with 1:1 Macrocell-I/O cell ratio allow each macrocell to drive one of eight I/O cells (Figure 9).

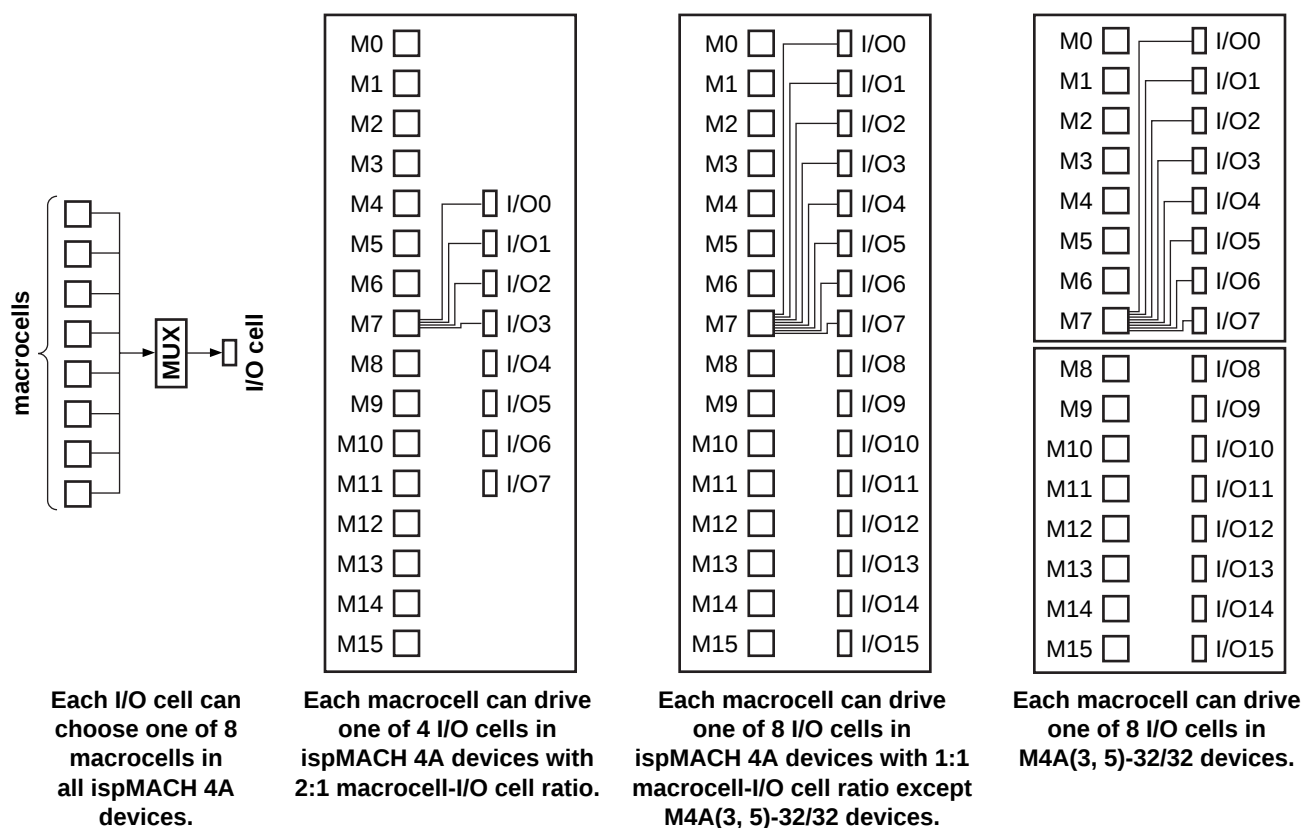


Figure 9. ispMACH 4A Output Switch Matrix

Table 10. Output Switch Matrix Combinations for ispMACH 4A Devices with 2:1 Macrocell-I/O Cell Ratio

Macrocell	Routeable to I/O Cells
M0, M1	I/O0, I/O5, I/O6, I/O7
M2, M3	I/O0, I/O1, I/O6, I/O7
M4, M5	I/O0, I/O1, I/O2, I/O7
M6, M7	I/O0, I/O1, I/O2, I/O3
M8, M9	I/O1, I/O2, I/O3, I/O4
M10, M11	I/O2, I/O3, I/O4, I/O5

Table 11. Output Switch Matrix Combinations for M4A3-256/160 and M4A3-256/192

Macrocell	Routable to I/O Cells							
I/O8	M8	M9	M10	M11	M12	M13	M14	M15
I/O9	M8	M9	M10	M11	M12	M13	M14	M15
I/O10	M8	M9	M10	M11	M12	M13	M14	M15
I/O11	M8	M9	M10	M11	M12	M13	M14	M15
I/O12	M8	M9	M10	M11	M12	M13	M14	M15
I/O13	M8	M9	M10	M11	M12	M13	M14	M15
I/O14	M8	M9	M10	M11	M12	M13	M14	M15
I/O15	M8	M9	M10	M11	M12	M13	M14	M15

Table 12. Output Switch Matrix Combinations for M4A(3,5)-32/32

Macrocell	Routable to I/O Cells
M0, M1, M2, M3, M4, M5, M6, M7	I/O0, I/O1, I/O2, I/O3, I/O4, I/O5, I/O6, I/O7
M8, M9, M10, M11, M12, M13, M14, M15	I/O8, I/O9, I/O10, I/O11, I/O12, I/O13, I/O14, I/O15

I/O Cell	Available Macrocells
I/O0, I/O1, I/O2, I/O3, I/O4, I/O5, I/O6, I/O7	M0, M1, M2, M3, M4, M5, M6, M7
I/O8, I/O9, I/O10, I/O11, I/O12, I/O13, I/O14, I/O15	M8, M9, M10, M11, M12, M13, M14, M15

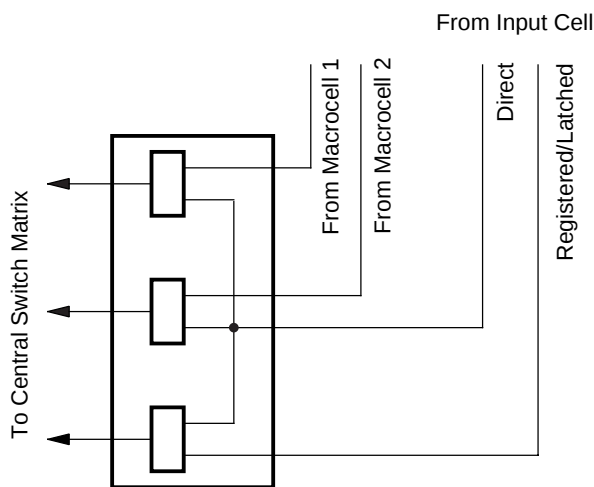
Table 13. Output Switch Matrix Combinations for M4A3-64/64

Macrocell	Routable to I/O Cells
M0, M1	I/O0, I/O1, I/O10, I/O11, I/O12, I/O13, I/O14, I/O15
M2, M3	I/O0, I/O1, I/O2, I/O3, I/O12, I/O13, I/O14, I/O15
M4, M5	I/O0, I/O1, I/O2, I/O3, I/O4, I/O5, I/O14, I/O15
M6, M7	I/O0, I/O1, I/O2, I/O3, I/O4, I/O5, I/O6, I/O7
M8, M9	I/O2, I/O3, I/O4, I/O5, I/O6, I/O7, I/O8, I/O9
M10, M11	I/O4, I/O5, I/O6, I/O7, I/O8, I/O9, I/O10, I/O11
M12, M13	I/O6, I/O7, I/O8, I/O9, I/O10, I/O11, I/O12, I/O13
M14, M15	I/O8, I/O9, I/O10, I/O11, I/O12, I/O13, I/O14, I/O15

I/O Cell	Available Macrocells
I/O0, I/O1	M0, M1, M2, M3, M4, M5, M6, M7
I/O2, I/O3	M2, M3, M4, M5, M6, M7, M8, M9
I/O4, I/O5	M4, M5, M6, M7, M8, M9, M10, M11
I/O6, I/O7	M6, M7, M8, M9, M10, M11, M12, M13
I/O8, I/O9	M8, M9, M10, M11, M12, M13, M14, M15
I/O10, I/O11	M0, M1, M10, M11, M12, M13, M14, M15
I/O12, I/O13	M0, M1, M2, M3, M12, M13, M14, M15
I/O14, I/O15	M0, M1, M2, M3, M4, M5, M14, M15

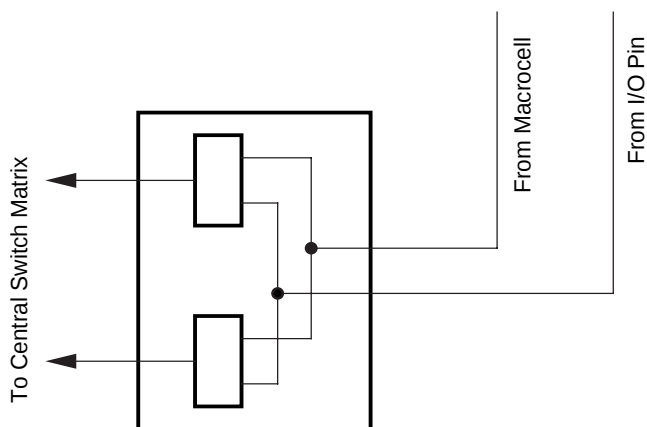
Input Switch Matrix

The input switch matrix (Figures 12 and 13) optimizes routing of inputs to the central switch matrix. Without the input switch matrix, each input and feedback signal has only one way to enter the central switch matrix. The input switch matrix provides additional ways for these signals to enter the central switch matrix.



17466G-002

Figure 12. ispMACH 4A with 2:1 Macrocell-I/O Cell Ratio - Input Switch Matrix



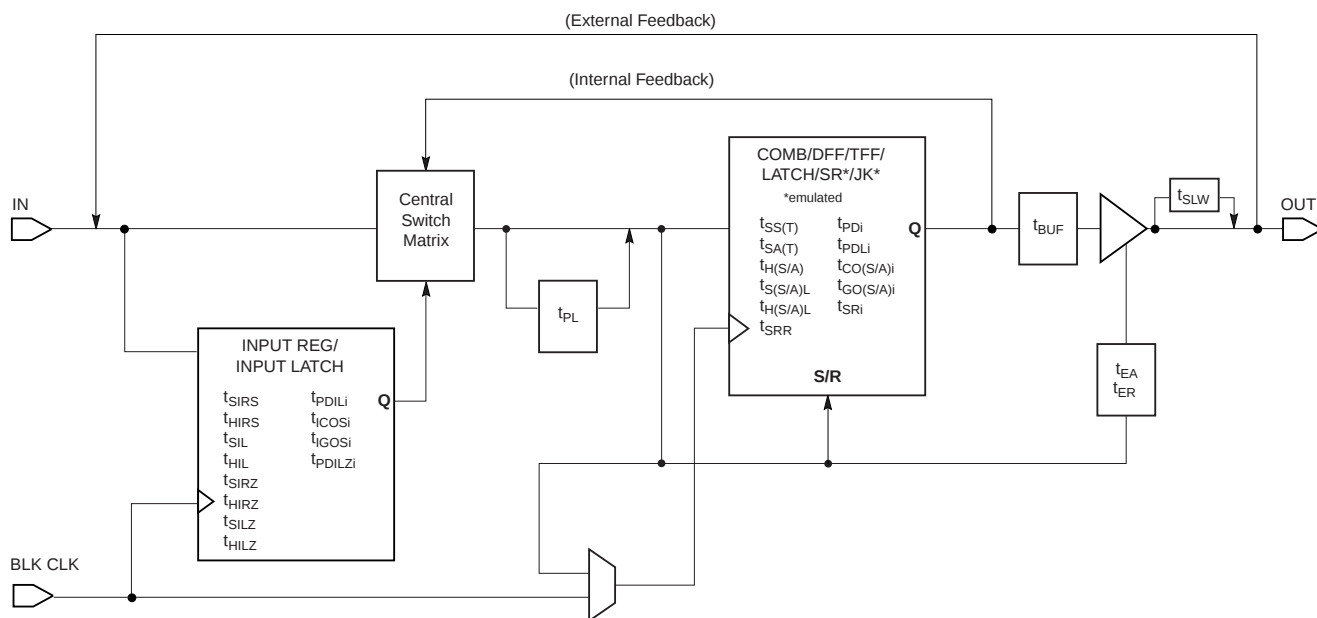
17466G-003

Figure 13. ispMACH 4A with 1:1 Macrocell-I/O Cell Ratio - Input Switch Matrix

ispMACH 4A TIMING MODEL

The primary focus of the ispMACH 4A timing model is to accurately represent the timing in a ispMACH 4A device, and at the same time, be easy to understand. This model accurately describes all combinatorial and registered paths through the device, making a distinction between internal feedback and external feedback. A signal uses internal feedback when it is fed back into the switch matrix or block without having to go through the output buffer. The input register specifications are also reported as internal feedback. When a signal is fed back into the switch matrix after having gone through the output buffer, it is using external feedback.

The parameter, t_{BUF} , is defined as the time it takes to go from feedback through the output buffer to the I/O pad. If a signal goes to the internal feedback rather than to the I/O pad, the parameter designator is followed by an “i”. By adding t_{BUF} to this internal parameter, the external parameter is derived. For example, $t_{PD} = t_{PDi} + t_{BUF}$. A diagram representing the modularized ispMACH 4A timing model is shown in Figure 15. Refer to the application note entitled *MACH 4 Timing and High Speed Design* for a more detailed discussion about the timing parameters.



17466G-025

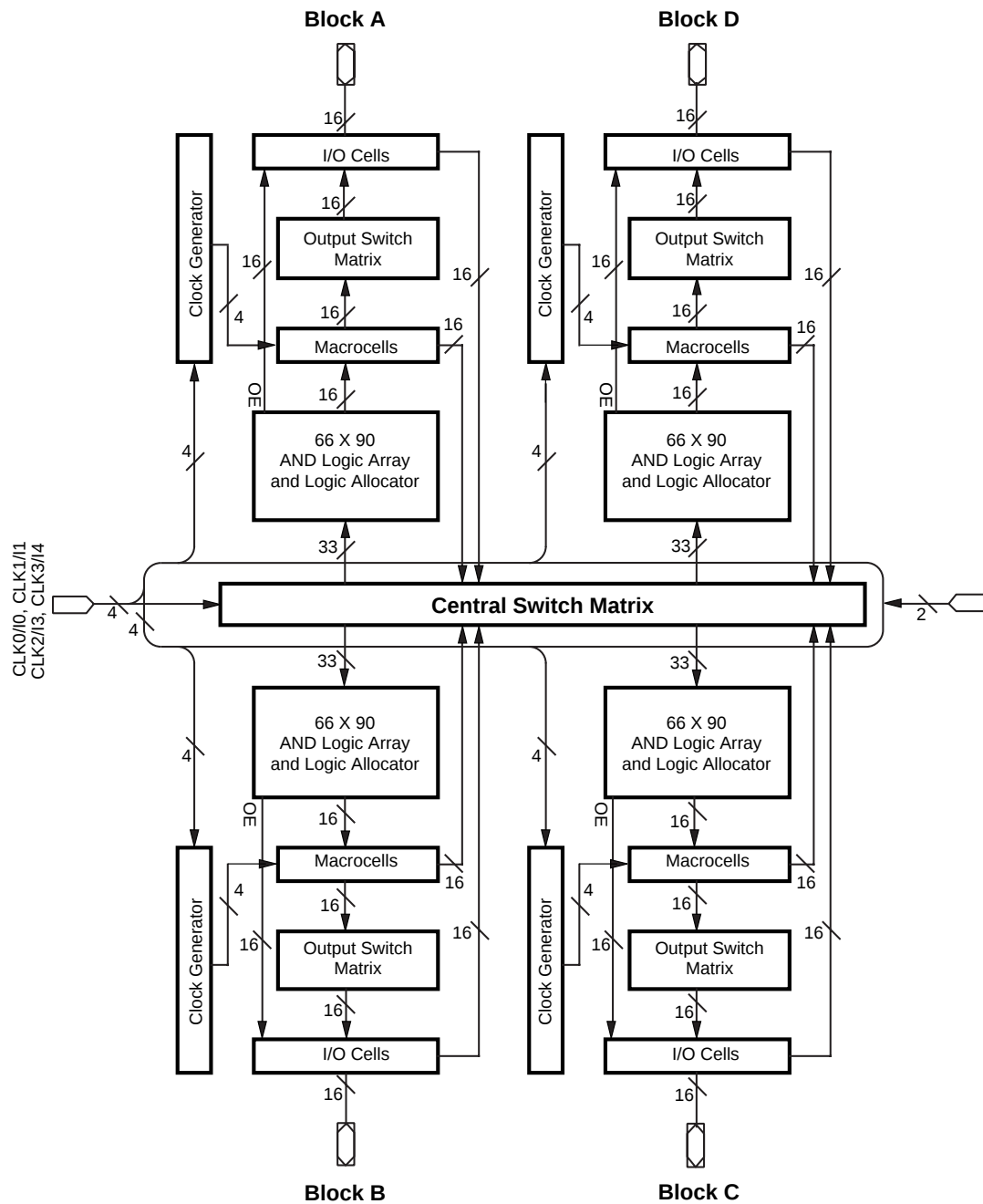
Figure 15. ispMACH 4A Timing Model

SPEEDLOCKING FOR GUARANTEED FIXED TIMING

The ispMACH 4A architecture allows allocation of up to 20 product terms to an individual macrocell with the assistance of an XOR gate without incurring additional timing delays.

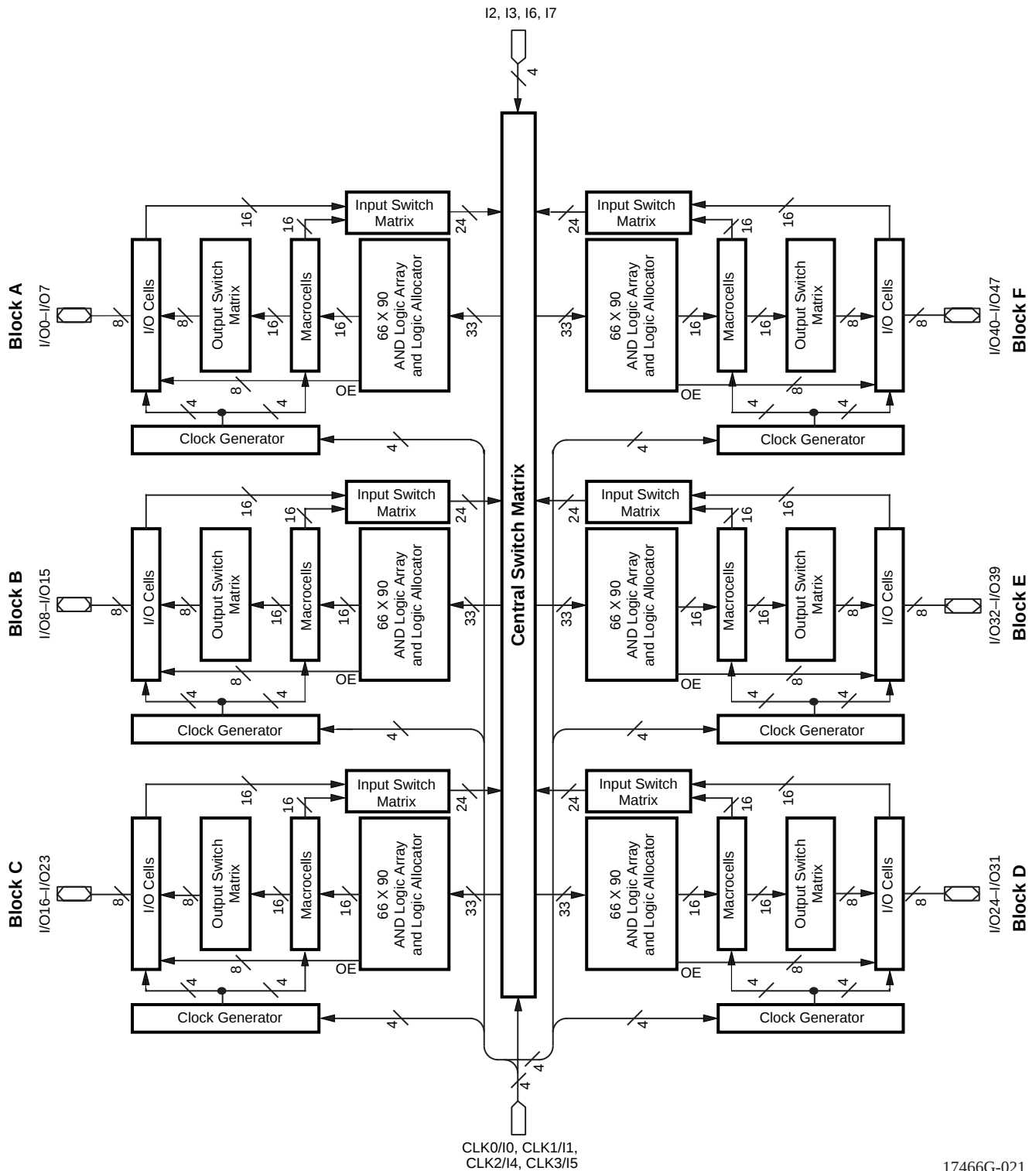
The design of the switch matrix and PAL blocks guarantee a fixed pin-to-pin delay that is independent of the logic required by the design. Other competitive CPLDs incur serious timing delays as product terms expand beyond their typical 4 or 5 product term limits. Speed and SpeedLocking combine to give designs easy access to the performance required in today's designs.

BLOCK DIAGRAM – M4A3-64/64



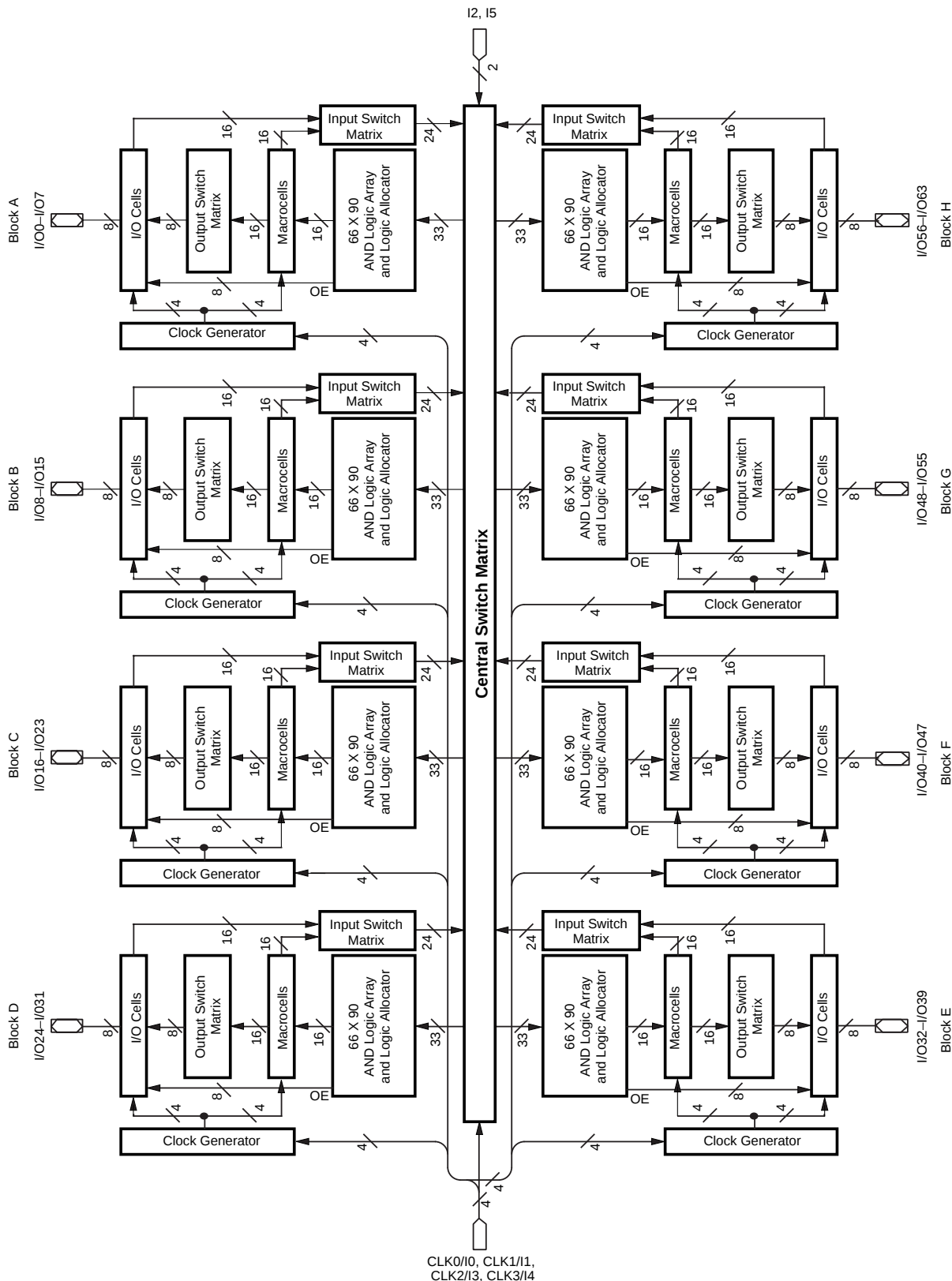
17466H-020A

BLOCK DIAGRAM – M4A(3,5)-96/48



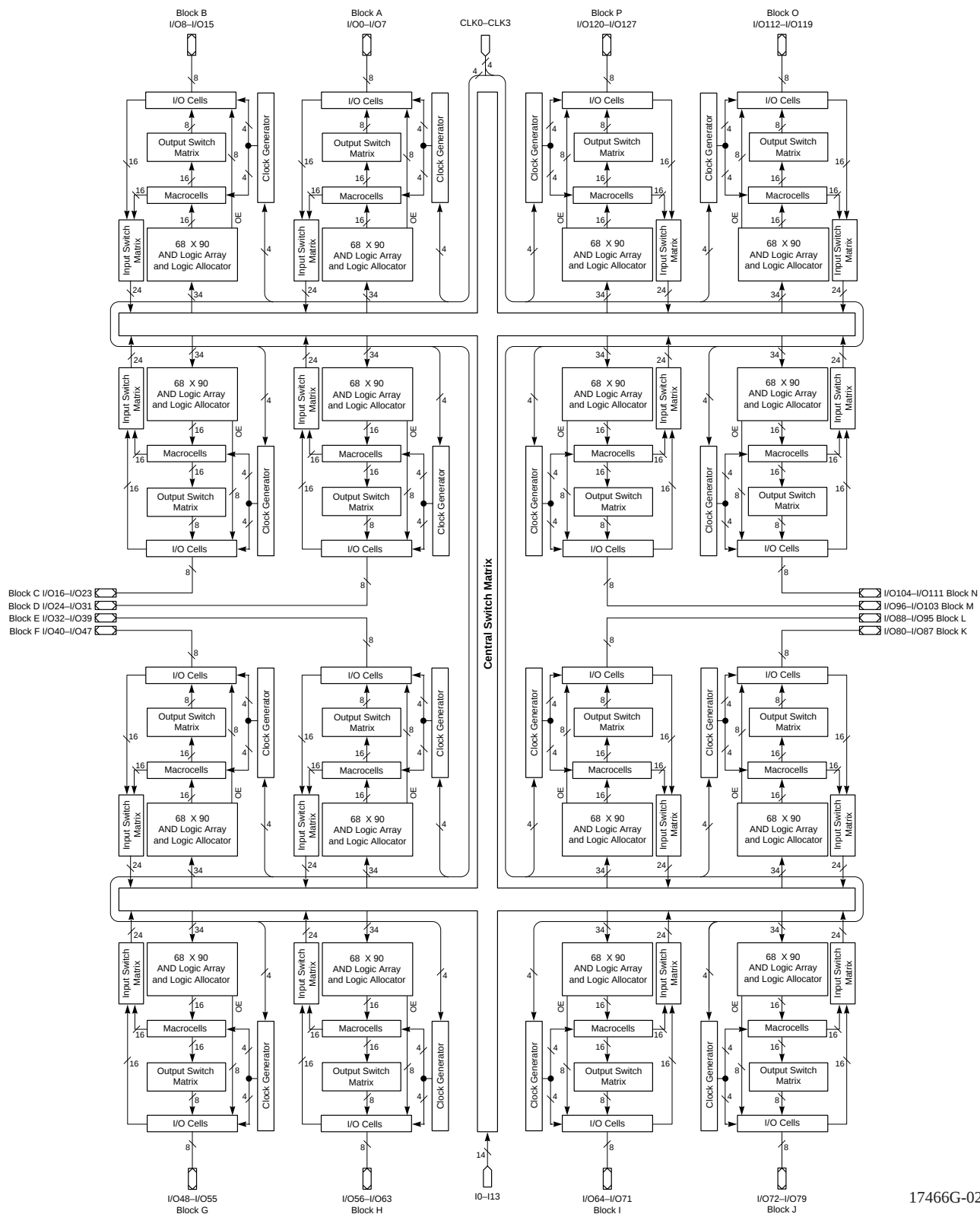
17466G-021

BLOCK DIAGRAM – M4A(3,5)-128/64



17466H-022

BLOCK DIAGRAM – M4A(3,5)-256/128



17466G-024

ispMACH 4A TIMING PARAMETERS OVER OPERATING RANGES¹

		-5		-55		-6		-65		-7		-10		-12		-14		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Frequency:																		
f _{MAXS}	External feedback, D-type, Min of 1/(t _{WLS} + t _{WHS}) or 1/(t _{SS} + t _{COS})	143		133		125		118		95.2		87.0		74.1		60.6		MHz
	External feedback, T-type, Min of 1/(t _{WLS} + t _{WHS}) or 1/(t _{SST} + t _{COS})	125		125		118		111		87.0		80.0		69.0		57.1		MHz
	Internal feedback (f _{CNT}), D-type, Min of 1/(t _{WLS} + t _{WHS}) or 1/(t _{SS} + t _{COSi})	182		167		160		154		125		118		95.0		74.1		MHz
	Internal feedback (f _{CNT}), T-type, Min of 1/(t _{WLS} + t _{WHS}) or 1/(t _{SST} + t _{COSi})	154		154		148		143		111		105		87.0		69.0		MHz
	No feedback ² , Min of 1/(t _{WLS} + t _{WHS}), 1/(t _{SS} + t _{HS}) or 1/(t _{SST} + t _{HS})	250		250		200		200		154		125		100		83.3		MHz
f _{MAXA}	External feedback, D-type, Min of 1/(t _{WLA} + t _{WHA}) or 1/(t _{SA} + t _{COA})	111		111		108		100		83.3		66.7		55.6		43.5		MHz
	External feedback, T-type, Min of 1/(t _{WLA} + t _{WHA}) or 1/(t _{SAT} + t _{COA})	105		105		102		95.2		76.9		62.5		52.6		41.7		MHz
	Internal feedback (f _{CNTA}), D-type, Min of 1/(t _{WLA} + t _{WHA}) or 1/(t _{SA} + t _{COAi})	133		133		125		125		105		83.3		66.7		50.0		MHz
	Internal feedback (f _{CNTA}), T-type, Min of 1/(t _{WLA} + t _{WHA}) or 1/(t _{SAT} + t _{COAi})	125		125		125		118		95.2		76.9		62.5		47.6		MHz
	No feedback ² , Min of 1/(t _{WLA} + t _{WHA}), 1/(t _{SA} + t _{HA}) or 1/(t _{SAT} + t _{HA})	167		167		143		143		125		100		62.5		55.6		MHz
f _{MAXI}	Maximum input register frequency, Min of 1/(t _{WIRH} + t _{WIRL}) or 1/(t _{SIRS} + t _{HIRS})	167		167		143		143		125		100		83.3		83.3		MHz

Notes:

- See "Switching Test Circuit" document on the Literature Download page of the Lattice web site.
- This parameter does not apply to flip-flops in the emulated mode since the feedback path is required for emulation.

CAPACITANCE¹

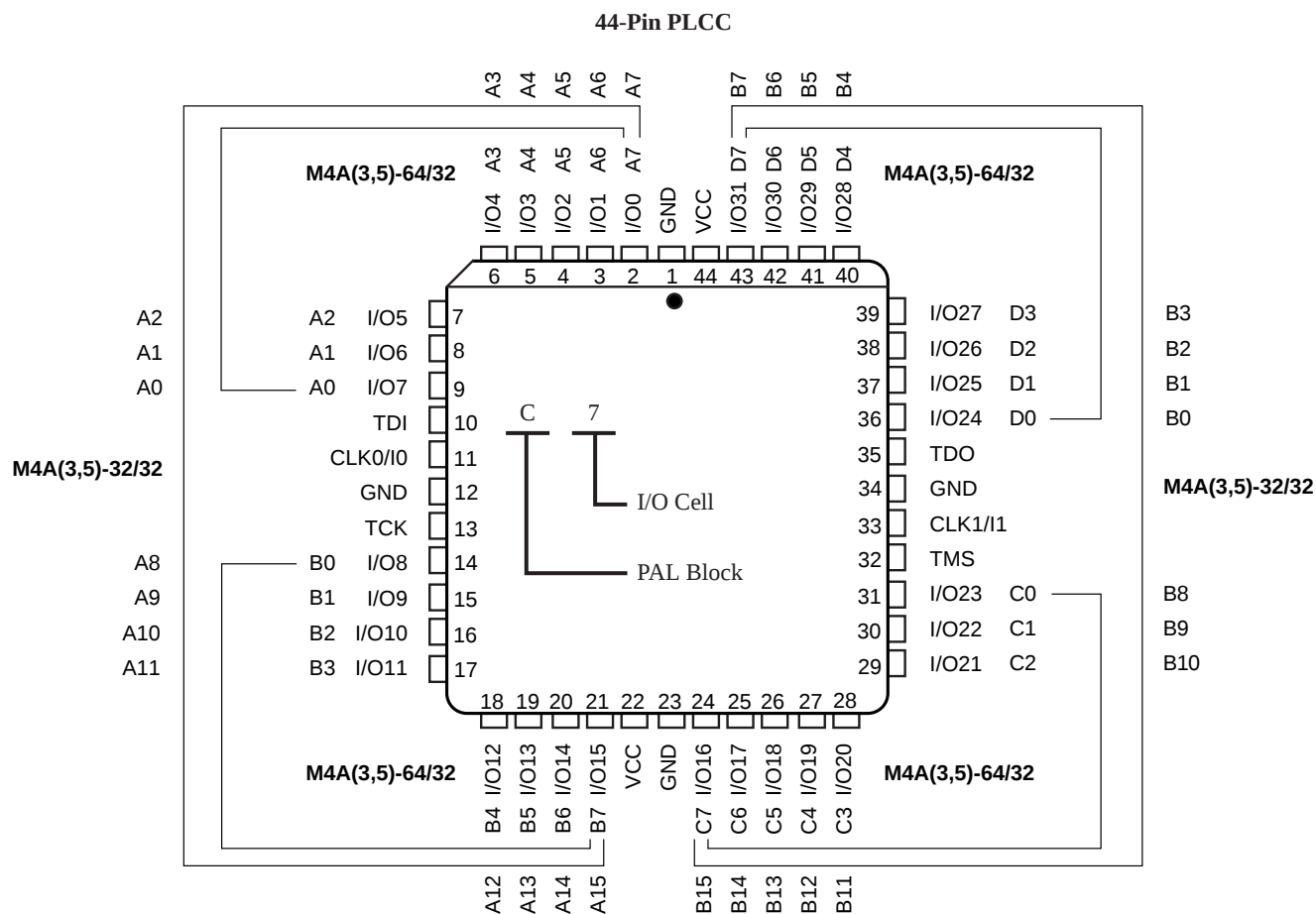
Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input capacitance	$V_{IN}=2.0\text{ V}$	3.3 V or 5 V, 25°C, 1 MHz	6	pF
$C_{I/O}$	Output capacitance	$V_{OUT}=2.0\text{ V}$	3.3 V or 5 V, 25°C, 1 MHz	8	pF

Note:

- These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where this parameter may be affected.

44-PIN PLCC CONNECTION DIAGRAM (M4A(3,5)-32/32 AND M4A(3,5)-64/32)

Top View



17466G-026

PIN DESIGNATIONS

CLK/I = Clock or Input

GND = Ground

I/O = Input/Output

V_{CC} = Supply Voltage

TDI = Test Data In

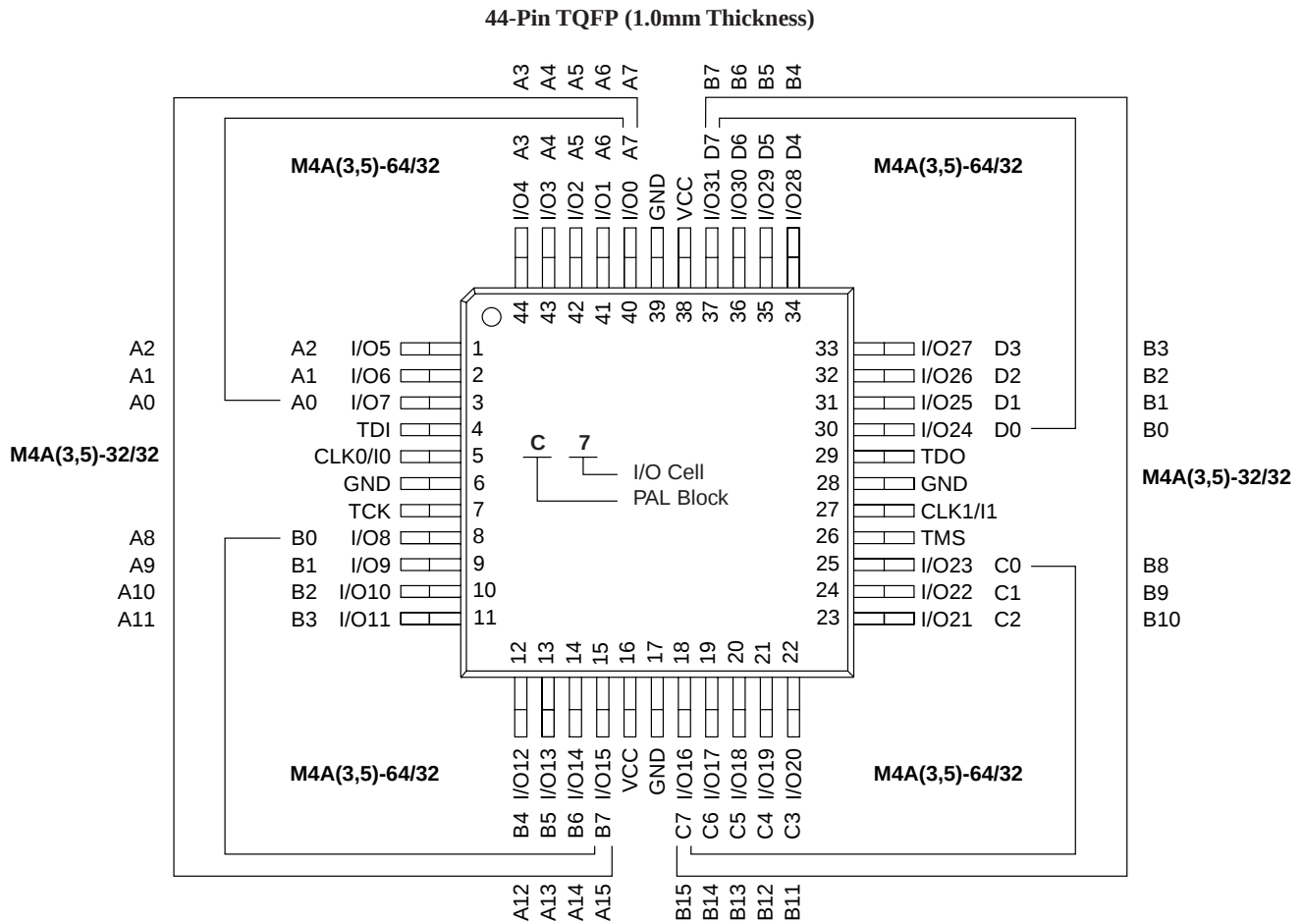
TCK = Test Clock

TMS = Test Mode Select

TDO = Test Data Out

44-PIN TQFP CONNECTION DIAGRAM (M4A(3,5)-32/32 AND M4A(3,5)-64/32)

Top View



PIN DESIGNATIONS

CLK/I = Clock or Input

GND = Ground

I/O = Input/Output

V_{CC} = Supply Voltage

TDI = Test Data In

TCK = Test Clock

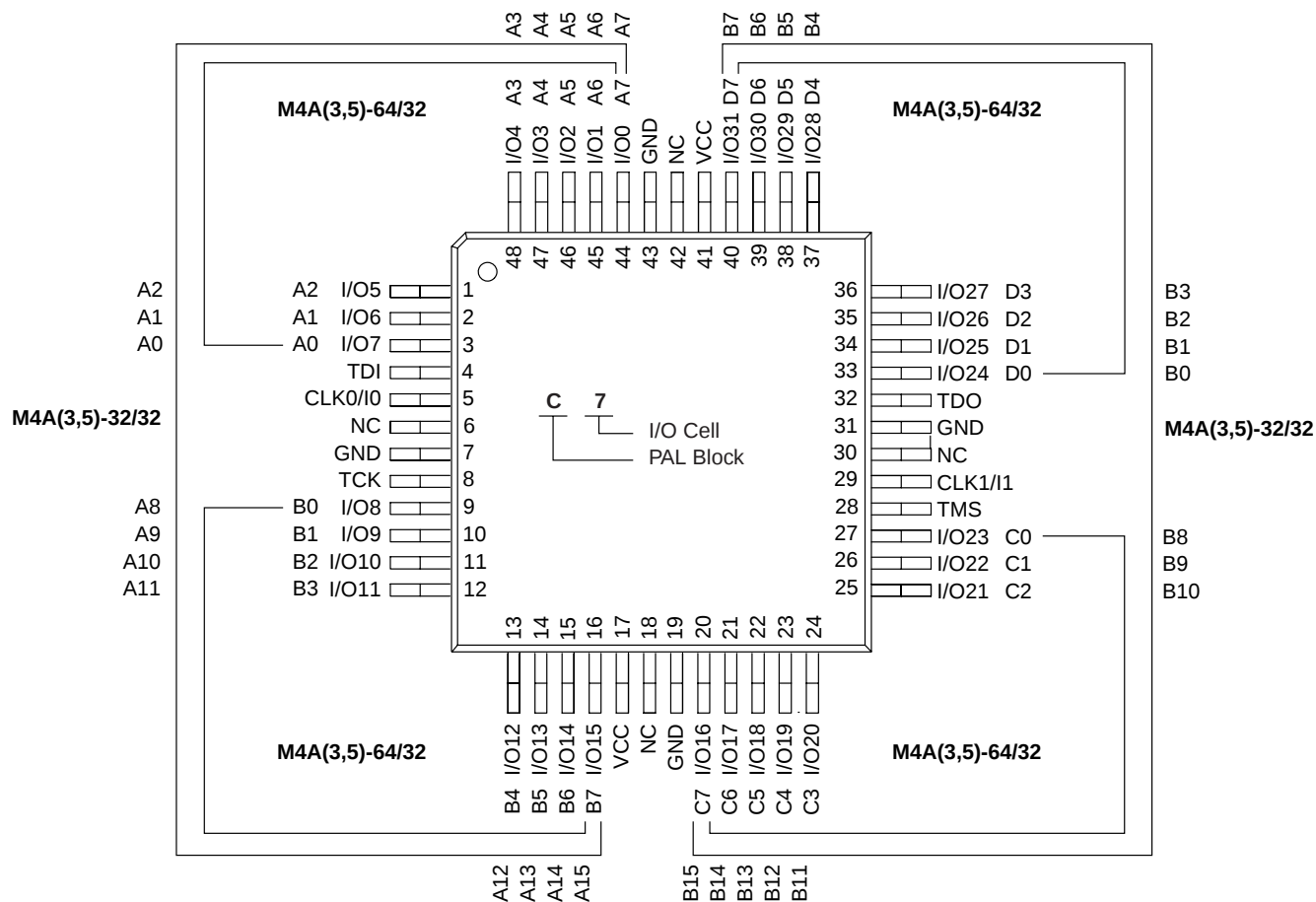
TMS = Test Mode Select

TDO = Test Data Out

48-PIN TQFP CONNECTION DIAGRAM (M4A(3,5)-32/32 AND M4A(3,5)-64/32)

Top View

48-Pin TQFP (1.4mm Thickness)



17466G-028

PIN DESIGNATIONS

CLK/I = Clock or Input

GND = Ground

I/O = Input/Output

V_{CC} = Supply Voltage

NC = No Connect

TDI = Test Data In

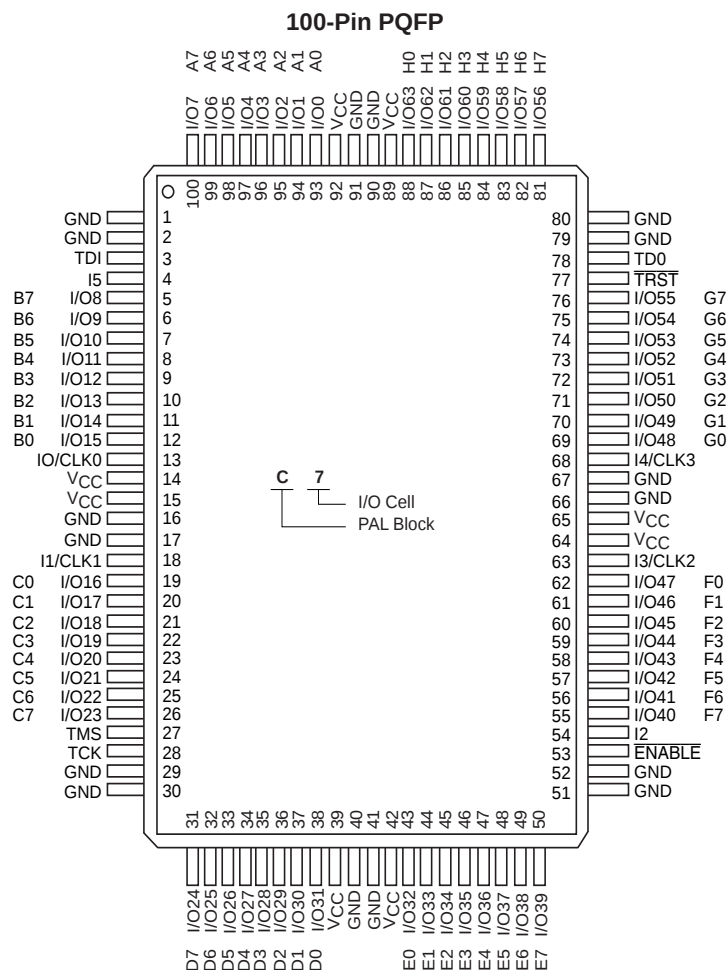
TCK = Test Clock

TMS = Test Mode Select

TDO = Test Data Out

100-PIN PQFP CONNECTION DIAGRAM (M4A(3,5)-128/64)

Top View



17466G-031

PIN DESIGNATIONS

I/CLK = Input or Clock

GND = Ground

I = Input

I/O = Input/Output

V_{CC} = Supply Voltage

TDI = Test Data In

TCK = Test Clock

TMS = Test Mode Select

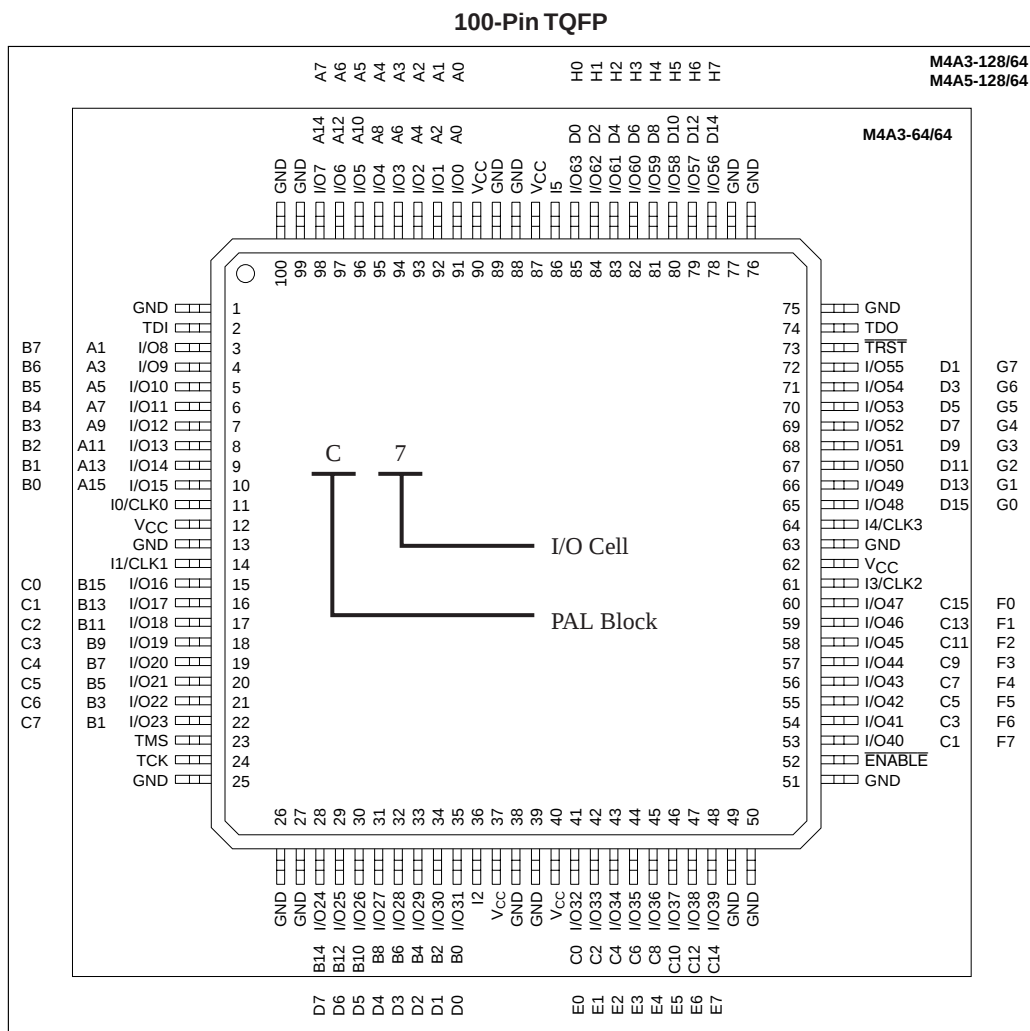
TDO = Test Data Out

TRST = Test Reset

ENABLE = Program

100-PIN TQFP CONNECTION DIAGRAM (M4A3-64/64 AND M4A(3,5)-128/64)

Top View



PIN DESIGNATIONS

CLK/I = Clock or Input

GND = Ground

I = Input

I/O = Input/Output

V_{CC} = Supply Voltage

TDI = Test Data In

TCK = Test Clock

TMS = Test Mode Select

TDO = Test Data Out

TRST = Test Reset

ENABLE = Program

256-BALL fpBGA CONNECTION DIAGRAM (M4A3-256/192)

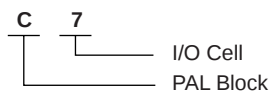
Bottom View

256-Ball fpBGA

	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	I/O167 N15	I/O181 O13	I/O180 O12	I/O177 O9	I/O174 O6	I/O172 O4	I/O191 P14	I/O186 P4	I/O1 A2	I/O3 A6	GCLK0	I/O9 B1	I/O13 B5	I/O15 B7	I/O18 B10	I/O20 B12	A
B	I/O165 N13	I/O166 N14	I/O182 O14	I/O179 O11	I/O175 O7	I/O173 O5	I/O168 O0	I/O187 P6	I/O0 A0	I/O5 A10	I/O7 A14	I/O10 B2	I/O16 B8	I/O19 B11	I/O21 B13	NC	B
C	I/O163 N11	I/O164 N12	NC	I/O183 O15	I/O178 O10	I/O170 O2	I/O171 O3	I/O189 P10	I/O184 P0	I/O6 A12	I/O12 B4	I/O14 B6	I/O23 B15	I/O22 B14	TDI	I/O39 C15	C
D	I/O158 N6	I/O159 N7	TDO	GND	GND	VCC	GND	VCC	GND	GND	VCC	GND	VCC	I/O17 B9	I/O38 C14	I/O37 C13	D
E	I/O156 N4	NC	I/O162 N10	VCC	I/O160 N8	I/O161 N9	I/O190 P12	GCLK3	I/O188 P8	I/O2 A4	I/O8 B0	NC	GND	I/O36 C12	I/O35 C11	I/O31 C7	E
F	I/O152 N0	I/O157 N5	I/O155 N3	GND	I/O154 N2	I/O153 N1	I/O176 O8	I/O169 O1	I/O185 P2	I/O4 A8	I/O11 B3	I/O34 C10	VCC	I/O32 C8	I/O30 C6	I/O29 C5	F
G	I/O147 M6	I/O150 M12	I/O149 M10	VCC	I/O148 M8	I/O151 M14	VCC	GND	GND	VCC	I/O33 C9	I/O28 C4	GND	I/O26 C2	I/O25 C1	I/O47 D14	G
H	I/O144 M0	I/O146 M4	I/O145 OM2	GND	I/O136 L0	I/O137 L2	GND	VCC	VCC	GND	I/O27 C3	I/O24 C0	VCC	I/O44 D8	I/O43 D6	I/O42 D4	H
J	I/O138 L4	I/O139 L6	I/O140 L8	GND	I/O142 L12	I/O141 L10	GND	VCC	VCC	GND	I/O46 D12	I/O45 D10	GND	I/O49 E2	I/O48 E0	I/O50 E4	J
K	I/O143 L14	I/O120 K0	I/O121 K1	VCC	I/O123 K3	I/O122 K2	VCC	GND	GND	VCC	I/O41 D2	I/O40 D0	VCC	I/O55 E14	I/O54 E12	I/O56 F0	K
L	I/O124 K4	I/O125 K5	I/O127 K7	GND	I/O130 K10	I/O126 K6	I/O98 I4	I/O91 H6	I/O75 G3	I/O77 G5	I/O52 E8	I/O51 E6	GND	I/O59 F3	I/O60 F4	I/O57 F1	L
M	I/O128 K8	I/O129 K9	I/O131 K11	GND	I/O107 J3	I/O105 J1	I/O100 I8	I/O90 H4	I/O74 G2	I/O80 G8	I/O83 G11	I/O53 E10	VCC	I/O68 F12	I/O63 F7	I/O58 F2	M
N	I/O132 K12	I/O133 K13	I/O135 K15	VCC	GND	VCC	GND	VCC	GND	GND	VCC	GND	GND	TCK	I/O64 F8	I/O61 F5	N
P	I/O134 K14	I/O117 J13	I/O118 J14	I/O119 J15	I/O108 J4	I/O106 J2	I/O101 I10	I/O89 H2	I/O93 H10	I/O94 H12	I/O79 G7	I/O84 G12	I/O87 G15	TMS	I/O65 F9	I/O62 F6	P
R	I/O116 J12	I/O115 J11	I/O112 J8	I/O111 J7	I/O104 J0	I/O102 I12	I/O99 I6	I/O96 I0	I/O92 H8	I/O72 G0	I/O76 G4	I/O81 G9	I/O85 G13	I/O71 F15	I/O67 F11	I/O66 F10	R
T	I/O114 J10	I/O113 J9	I/O110 J6	I/O109 J5	I/O103 I14	GCLK2	I/O97 I2	I/O88 H0	GCLK1	I/O95 H14	I/O73 G1	I/O78 G6	I/O82 G10	I/O86 G14	I/O70 F14	I/O69 F13	T
	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

PIN DESIGNATIONS

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17466G-047

256-BALL fpBGA CONNECTION DIAGRAM (M4A3-512/192)

Bottom View

256-Ball fpBGA

	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	I/O159 KX7	I/O181 OX5	I/O180 OX4	I/O177 OX1	I/O174 NX6	I/O172 NX4	I/O191 PX7	I/O186 PX2	I/O1 A1	I/O3 A3	CLK0	I/O17 C1	I/O21 C5	I/O23 C7	I/O10 B2	I/O12 B4	A
B	I/O157 KX5	I/O158 KX6	I/O182 OX6	I/O179 OX3	I/O175 NX7	I/O173 NX5	I/O168 NX0	I/O187 PX3	I/O0 A0	I/O5 A5	I/O7 A7	I/O18 C2	I/O8 B0	I/O11 B3	I/O13 B5	N/C	B
C	I/O155 KX3	I/O156 KX4	N/C	I/O183 OX7	I/O178 OX2	I/O170 NX2	I/O171 NX3	I/O189 PX5	I/O184 PX0	I/O6 A6	I/O20 C4	I/O22 C6	I/O15 B7	I/O14 B6	TDI	I/O39 F7	C
D	I/O150 JX6	I/O151 JX7	TDO	GND	GND	VCC	GND	VCC	GND	GND	VCC	GND	VCC	I/O9 B1	I/O38 F6	I/O37 F5	D
E	I/O148 JX4	N/C	I/O154 KX2	VCC	I/O152 KX0	I/O153 KX1	I/O190 PX6	CLK3	I/O188 PX4	I/O2 A2	I/O16 C0	N/C	GND	I/O36 F4	I/O35 F3	I/O47 G7	E
F	I/O144 JX0	I/O149 JX5	I/O147 JX3	GND	I/O146 JX2	I/O145 JX1	I/O176 OX0	I/O169 NX1	I/O185 PX1	I/O4 A4	I/O19 C3	I/O34 F2	VCC	I/O32 F0	I/O46 G6	I/O45 G5	F
G	I/O163 LX3	I/O166 LX6	I/O165 LX5	VCC	I/O164 LX4	I/O167 LX7	VCC	GND	GND	VCC	I/O33 F1	I/O44 G4	GND	I/O42 G2	I/O41 G1	I/O31 E7	G
H	I/O160 LX0	I/O162 LX2	I/O161 LX1	GND	I/O120 EX0	I/O121 EX1	GND	VCC	VCC	GND	I/O43 G3	I/O40 G0	VCC	I/O28 E4	I/O27 E3	I/O26 E2	H
J	I/O122 EX2	I/O123 EX3	I/O124 EX4	GND	I/O126 EX6	I/O125 EX5	GND	VCC	VCC	GND	I/O30 E6	I/O29 E5	GND	I/O65 L1	I/O64 L0	I/O66 L2	J
K	I/O127 EX7	I/O136 GX0	I/O137 GX1	VCC	I/O139 GX3	I/O138 GX2	VCC	GND	GND	VCC	I/O25 E1	I/O24 E0	VCC	I/O71 L7	I/O70 L6	I/O48 J0	K
L	I/O140 GX4	I/O141 GX5	I/O143 GX7	GND	I/O130 FX2	I/O142 GX6	I/O98 AX2	I/O91 P3	I/O75 N3	I/O77 N5	I/O68 L4	I/O67 L3	GND	I/O51 J3	I/O52 J4	I/O49 J1	L
M	I/O128 FX0	I/O129 FX1	I/O131 FX3	GND	I/O115 CX3	I/O113 CX1	I/O100 AX4	I/O90 P2	I/O74 N2	I/O80 O0	I/O83 O3	I/O69 L5	VCC	I/O60 K4	I/O55 J7	I/O50 J2	M
N	I/O132 FX4	I/O133 FX5	I/O135 FX7	VCC	GND	VCC	GND	VCC	GND	GND	VCC	GND	GND	TCK	I/O56 K0	I/O53 J5	N
P	I/O134 FX6	I/O109 BX5	I/O110 BX6	I/O111 BX7	I/O116 CX4	I/O114 CX2	I/O101 AX5	I/O89 P1	I/O93 P5	I/O94 P6	I/O79 N7	I/O84 O4	I/O87 O7	TMS	I/O57 K1	I/O54 J6	P
R	I/O108 BX4	I/O107 BX3	I/O104 BX0	I/O119 CX7	I/O112 CX0	I/O102 AX6	I/O99 AX3	I/O96 AX0	I/O92 P4	I/O72 N0	I/O76 N4	I/O81 O1	I/O85 O5	I/O63 K7	I/O59 K3	I/O58 K2	R
T	I/O106 BX2	I/O105 BX1	I/O118 CX6	I/O117 CX5	I/O103 AX7	CLK2	I/O97 AX1	I/O88 P0	CLK1	I/O95 P7	I/O73 N1	I/O78 N6	I/O82 O2	I/O86 O6	I/O62 K6	I/O61 K5	T
	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

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m4a3.512.192_256bga

388-BALL fpBGA CONNECTION DIAGRAM (M4A3-512/256)

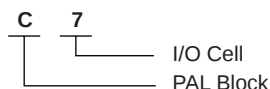
Bottom View

388-Ball fpBGA

	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	GND	I/O243 OX3	I/O240 OX0	I/O241 OX1	I/O236 NX4	I/O231 MX7	I/O228 MX4	I/O226 MX2	I/O255 PX7	I/O251 PX3	I/O248 PX0	I/O0 A0	I/O5 A5	I/O6 A6	I/O27 D3	I/O30 D6	I/O17 C1	I/O22 C6	I/O8 B0	I/O10 B2	N/C	GND	A
B	N/C	GND	I/O245 OX5	I/O242 OX2	I/O238 NX6	I/O234 NX2	I/O232 NX0	I/O229 MX5	I/O224 MX0	I/O253 PX5	I/O249 PX1	I/O2 A2	CLK0	I/O26 D2	I/O29 D5	I/O31 D7	I/O20 C4	I/O9 B1	I/O12 B4	I/O13 B5	GND	TDI	B
C	I/O213 KX5	TDO	GND	I/O247 OX7	I/O244 OX4	I/O239 NX7	I/O235 NX3	I/O230 MX6	I/O227 MX3	CLK3	I/O250 PX2	I/O1 A1	I/O7 A7	I/O25 D1	I/O16 C0	I/O18 C2	I/O23 C7	I/O11 B3	I/O15 B7	GND	I/O47 F7	I/O44 F4	C
D	I/O210 KX2	I/O212 KX4	I/O215 KX7	GND	I/O246 OX6	VCC	I/O237 NX5	I/O233 NX1	VCC	I/O254 PX6	VCC	I/O3 A3	I/O24 D0	VCC	I/O19 C3	I/O21 C5	VCC	I/O14 B6	GND	I/O46 F6	I/O43 F3	I/O41 F1	D
E	I/O207 JX7	I/O209 KX1	I/O211 KX3	I/O214 KX6															I/O45 F5	I/O42 F2	I/O40 F0	I/O54 G6	E
F	I/O203 JX3	I/O205 JX5	I/O208 KX0	VCC															VCC	I/O55 G7	I/O52 G4	I/O50 G2	F
G	I/O200 JX0	I/O202 JX2	I/O204 JX4	I/O206 JX6			VCC	VCC	N/C	I/O225 MX1	I/O252 PX4	I/O4 A4	I/O28 D4	N/C	VCC	VCC			I/O53 G5	I/O51 G3	I/O49 G1	I/O39 E7	G
H	I/O221 LX5	I/O222 LX6	I/O223 LX7	I/O201 JX1			VCC	N/C	GND	GND	GND	GND	GND	GND	N/C	VCC			I/O48 G0	I/O38 E6	I/O37 E5	I/O36 E4	H
J	I/O218 LX2	I/O219 LX3	I/O220 LX4	VCC			N/C	GND	GND	GND	GND	GND	GND	GND	GND	N/C			VCC	I/O35 E3	I/O34 E2	I/O32 E0	J
K	I/O197 IX5	I/O198 IX6	I/O199 IX7	I/O216 LX0			I/O217 LX1	GND	GND	GND	GND	GND	GND	GND	GND	I/O33 E1			I/O63 H7	I/O62 H6	I/O61 H5	I/O60 H4	K
L	I/O192 IX0	I/O194 IX2	I/O195 IX3	I/O196 IX4			I/O193 IX1	GND	GND	GND	GND	GND	GND	GND	GND	I/O58 H2			VCC	I/O59 H3	I/O57 H1	I/O56 H0	L
M	I/O184 HX0	I/O185 HX1	I/O187 HX3	VCC			I/O186 HX2	GND	GND	GND	GND	GND	GND	GND	GND	I/O69 I5			I/O67 I3	I/O65 I1	I/O66 I2	I/O64 I0	M
N	I/O188 HX4	I/O189 HX5	I/O191 HX7	I/O190 HX6			I/O162 EX2	GND	GND	GND	GND	GND	GND	GND	GND	I/O89 L1			I/O88 L0	I/O71 I7	I/O70 I6	I/O68 I4	N
P	I/O160 EX0	I/O161 EX1	I/O163 EX3	VCC			N/C	GND	GND	GND	GND	GND	GND	GND	GND	N/C			VCC	I/O92 L4	I/O91 L3	I/O90 L2	P
R	I/O164 EX4	I/O165 EX5	I/O166 EX6	I/O177 GX1			VCC	N/C	GND	GND	GND	GND	GND	GND	N/C	VCC			I/O74 J2	I/O95 L7	I/O94 L6	I/O93 L5	R
T	I/O167 EX7	I/O176 GX0	I/O179 GX3	I/O181 GX5			VCC	VCC	N/C	I/O152 DX0	I/O131 AX3	I/O122 P2	I/O98 M2	N/C	VCC	VCC			I/O78 J6	I/O76 J4	I/O73 J1	I/O72 J0	T
U	I/O178 GX2	I/O180 GX4	I/O183 GX7	VCC															VCC	I/O80 K0	I/O77 J5	I/O75 J3	U
V	I/O182 GX6	N/C	I/O169 FX1	I/O172 FX4															I/O86 K6	I/O83 K3	I/O81 K1	I/O79 J7	V
W	I/O168 FX0	I/O170 FX2	I/O173 FX5	GND	I/O143 BX7	VCC	I/O150 CX6	I/O145 CX1	VCC	I/O153 DX1	I/O123 P3	VCC	I/O96 M0	VCC	I/O104 N0	I/O111 N7	VCC	I/O119 O7	GND	I/O87 K7	I/O84 K4	I/O82 K2	W
Y	I/O171 FX3	I/O174 FX6	GND	I/O141 BX5	I/O138 BX2	I/O136 BX0	I/O147 CX3	I/O158 DX6	I/O156 DX4	CLK2	I/O132 AX4	I/O121 P1	I/O125 P5	I/O99 M3	I/O101 M5	I/O106 N2	I/O110 N6	I/O115 O3	I/O118 O6	GND	TMS	I/O85 K5	Y
AA	I/O175 FX7	GND	I/O142 BX6	I/O140 BX4	I/O151 CX7	I/O149 CX5	I/O144 CX0	I/O157 DX5	I/O154 DX2	I/O134 AX6	I/O130 AX2	I/O128 AX0	CLK1	I/O127 P7	I/O100 M4	I/O103 M7	I/O108 N4	I/O109 N5	I/O113 O1	I/O116 O4	GND	TCK	AA
AB	GND	N/C	I/O139 BX3	I/O137 BX1	I/O148 CX4	I/O146 CX2	I/O159 DX7	I/O155 DX3	I/O135 AX7	I/O133 AX5	I/O129 AX1	I/O120 P0	I/O124 P4	I/O126 P6	I/O97 M1	I/O102 M6	I/O105 N1	I/O107 N3	I/O112 O0	I/O114 O2	I/O117 O5	GND	AB

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