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Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details

Product Status	Not For New Designs
Programmable Type	In System Programmable
Delay Time tpd(1) Max	7.5 ns
Voltage Supply - Internal	4.75V ~ 5.25V
Number of Logic Elements/Blocks	-
Number of Macrocells	32
Number of Gates	-
Number of I/O	32
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/m4a5-32-32-7vnc

Product-Term Array

The product-term array consists of a number of product terms that form the basis of the logic being implemented. The inputs to the AND gates come from the central switch matrix (Table 5), and are provided in both true and complement forms for efficient logic implementation.

Table 5. PAL Block Inputs

Device	Number of Inputs to PAL Block
M4A3-32/32 and M4A5-32/32	33
M4A3-64/32 and M4A5-64/32	33
M4A3-64/64	33
M4A3-96/48 and M4A5-96/48	33
M4A3-128/64 and M4A5-128/64	33
M4A3-192/96 and M4A5-192/96	34
M4A3-256/128 and M4A5-256/128	34
M4A3-256/160 and M4A3-256/192	36
M4A3-384	36
M4A3-512	36

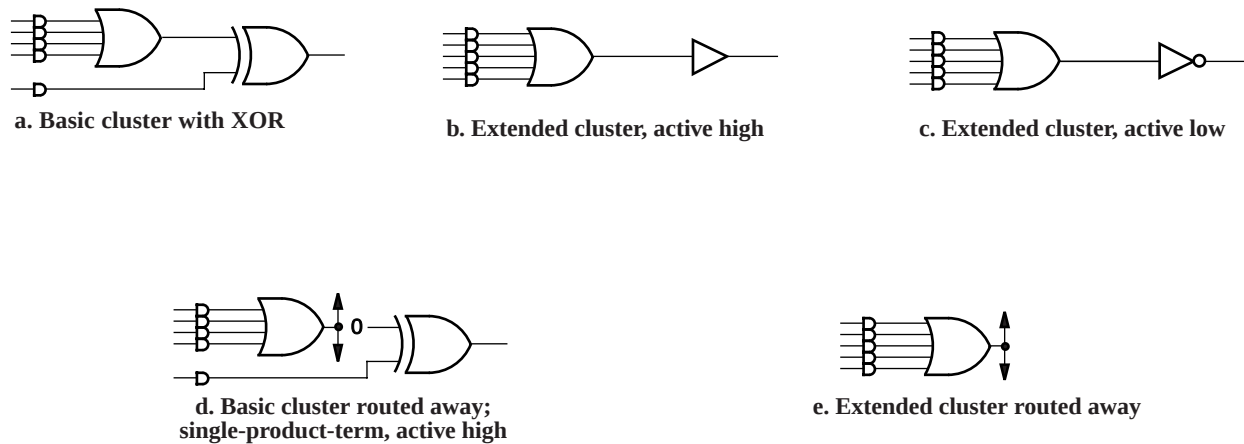
Logic Allocator

Within the logic allocator, product terms are allocated to macrocells in “product term clusters.” The availability and distribution of product term clusters are automatically considered by the software as it fits functions within a PAL block. The size of a product term cluster has been optimized to provide high utilization of product terms, making complex functions using many product terms possible. Yet when few product terms are used, there will be a minimal number of unused—or wasted—product terms left over. The product term clusters available to each macrocell within a PAL block are shown in Tables 6 and 7.

Each product term cluster is associated with a macrocell. The size of a cluster depends on the configuration of the associated macrocell. When the macrocell is used in synchronous mode (Figure 2a), the basic cluster has 4 product terms. When the associated macrocell is used in asynchronous mode (Figure 2b), the cluster has 2 product terms. Note that if the product term cluster is routed to a different macrocell, the allocator configuration is not determined by the mode of the macrocell actually being driven. The configuration is always set by the mode of the macrocell that the cluster will drive if not routed away, regardless of the actual routing.

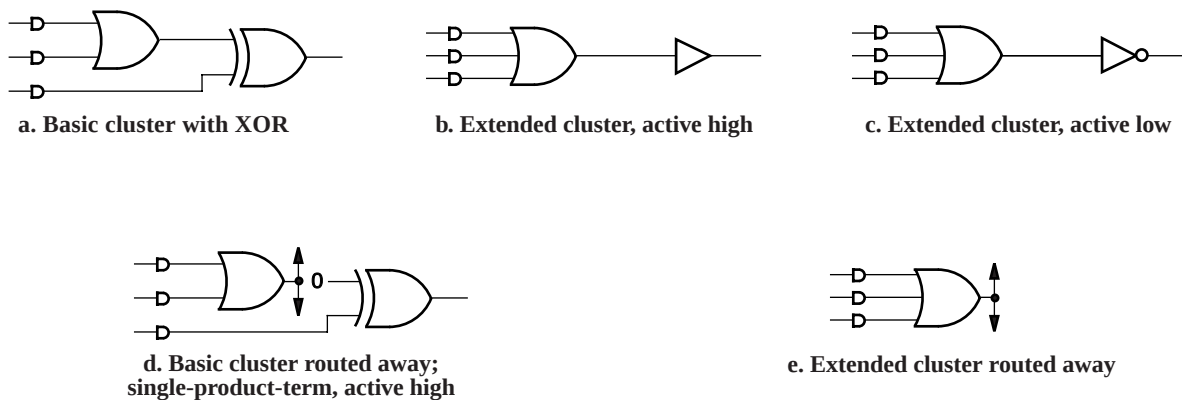
In addition, there is an extra product term that can either join the basic cluster to give an extended cluster, or drive the second input of an exclusive-OR gate in the signal path. If included with the basic cluster, this provides for up to 20 product terms on a synchronous function that uses four extended 5-product-term clusters. A similar asynchronous function can have up to 18 product terms.

When the extra product term is used to extend the cluster, the value of the second XOR input can be programmed as a 0 or a 1, giving polarity control. The possible configurations of the logic allocator are shown in Figures 3 and 4.



17466G-007

Figure 3. Logic Allocator Configurations: Synchronous Mode



17466G-008

Figure 4. Logic Allocator Configurations: Asynchronous Mode

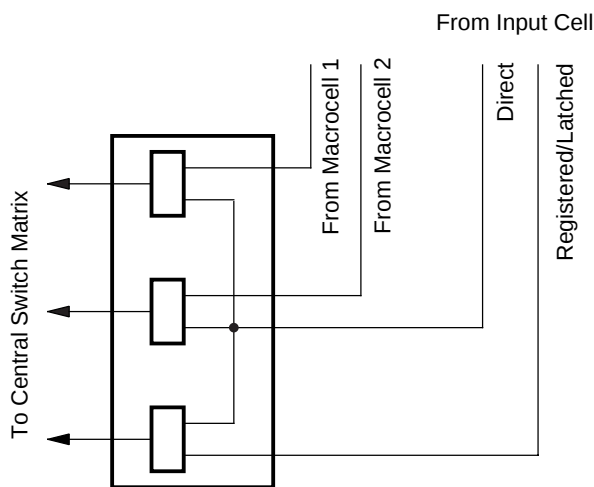
Note that the configuration of the logic allocator has absolutely no impact on the speed of the signal. All configurations have the same delay. This means that designers do not have to decide between optimizing resources or speed; both can be optimized.

If not used in the cluster, the extra product term can act in conjunction with the basic cluster to provide XOR logic for such functions as data comparison, or it can work with the D-,T-type flip-flop to provide for J-K, and S-R register operation. In addition, if the basic cluster is routed to another macrocell, the extra product term is still available for logic. In this case, the first XOR input will be a logic 0. This circuit has the flexibility to route product terms elsewhere without giving up the use of the macrocell.

Product term clusters do not “wrap” around a PAL block. This means that the macrocells at the ends of the block have fewer product terms available.

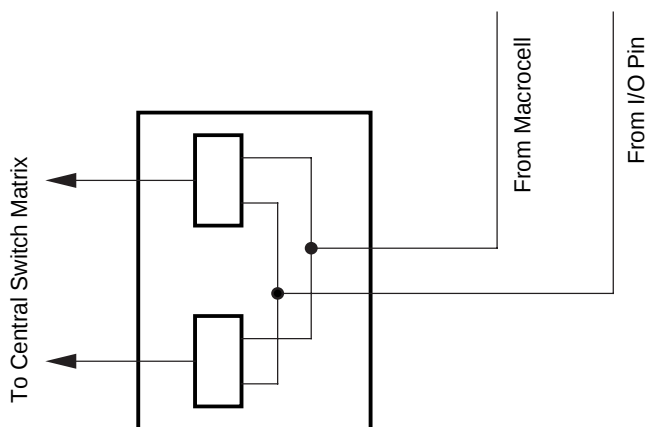
Input Switch Matrix

The input switch matrix (Figures 12 and 13) optimizes routing of inputs to the central switch matrix. Without the input switch matrix, each input and feedback signal has only one way to enter the central switch matrix. The input switch matrix provides additional ways for these signals to enter the central switch matrix.



17466G-002

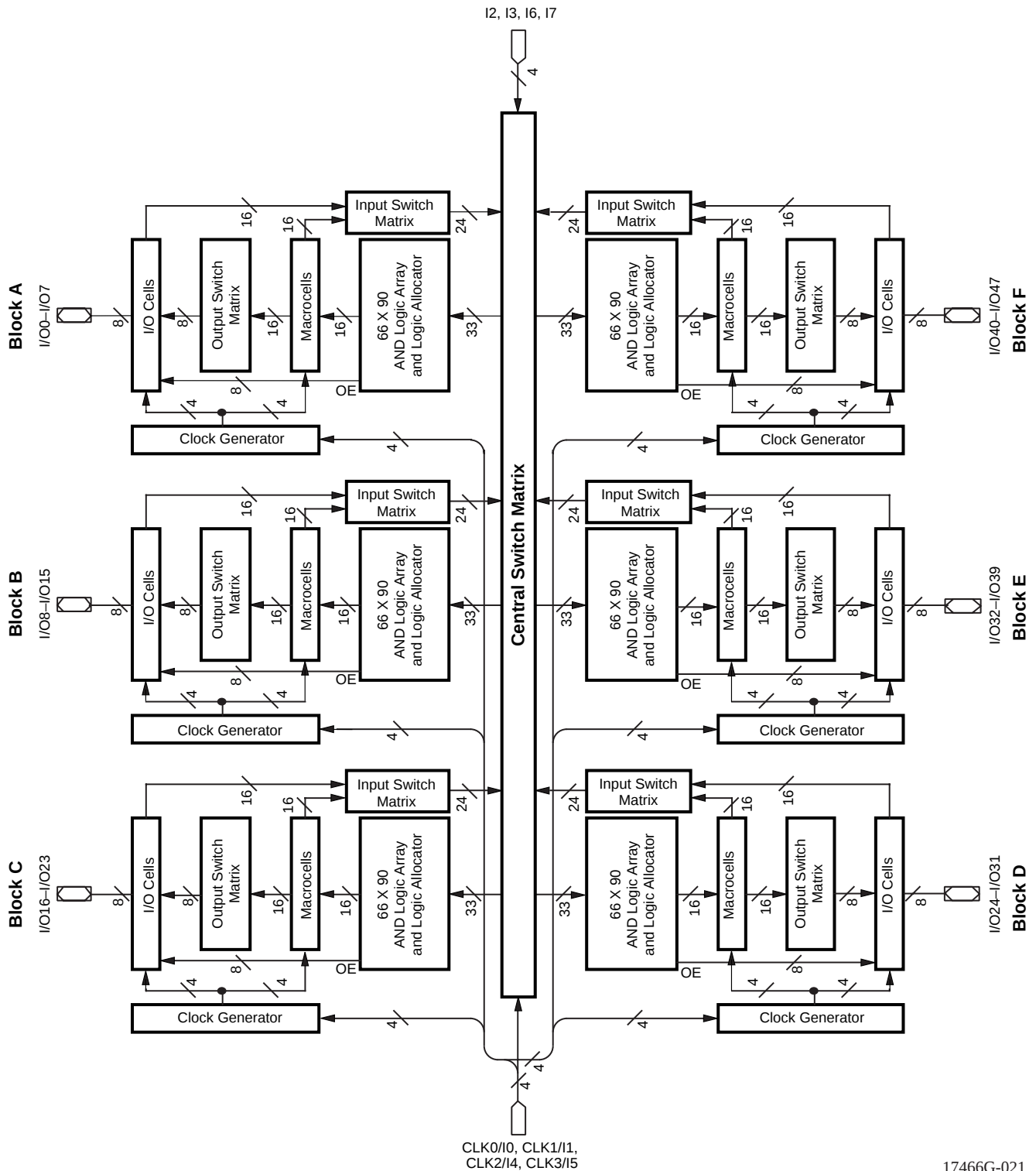
Figure 12. ispMACH 4A with 2:1 Macrocell-I/O Cell Ratio - Input Switch Matrix



17466G-003

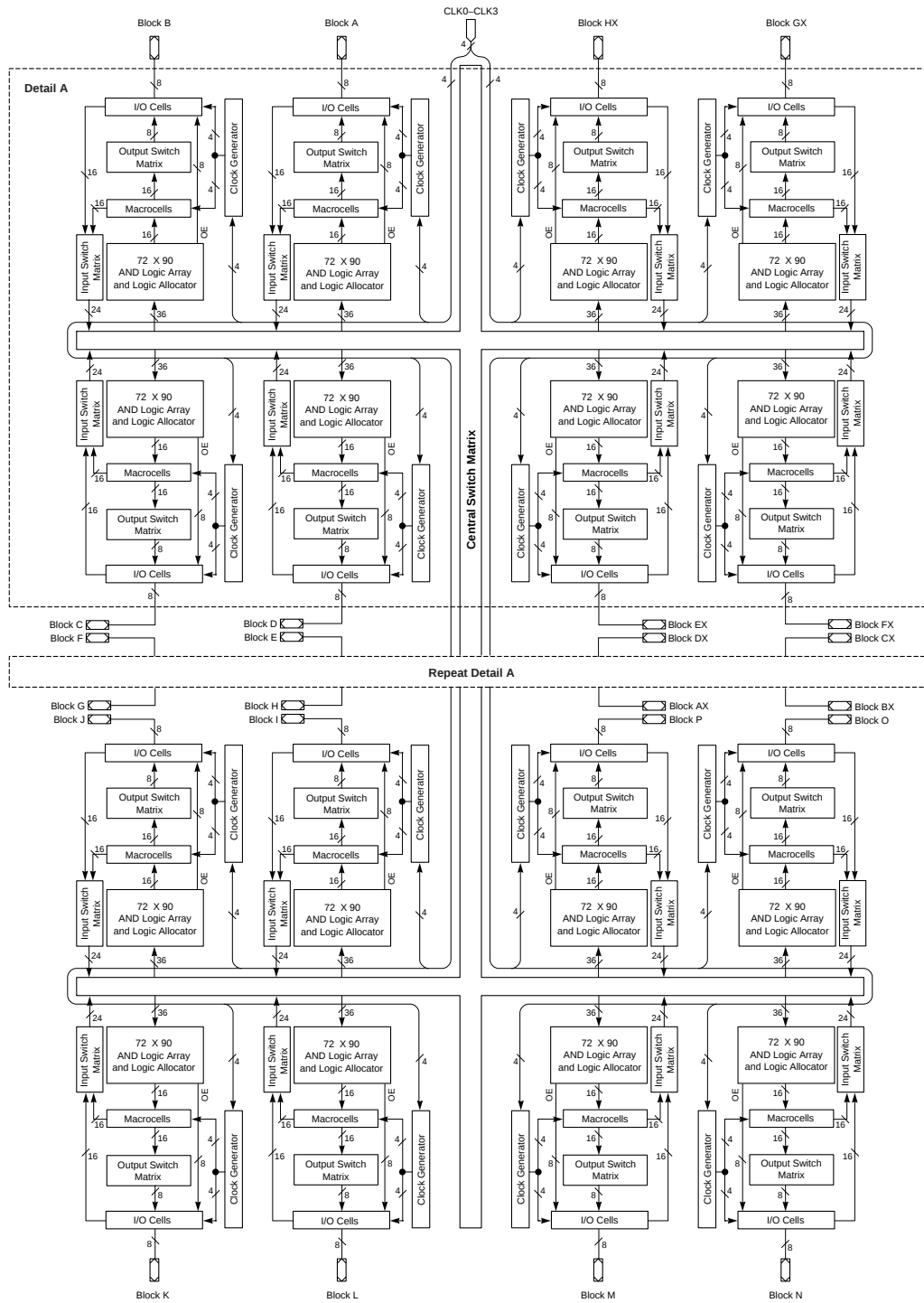
Figure 13. ispMACH 4A with 1:1 Macrocell-I/O Cell Ratio - Input Switch Matrix

BLOCK DIAGRAM – M4A(3,5)-96/48



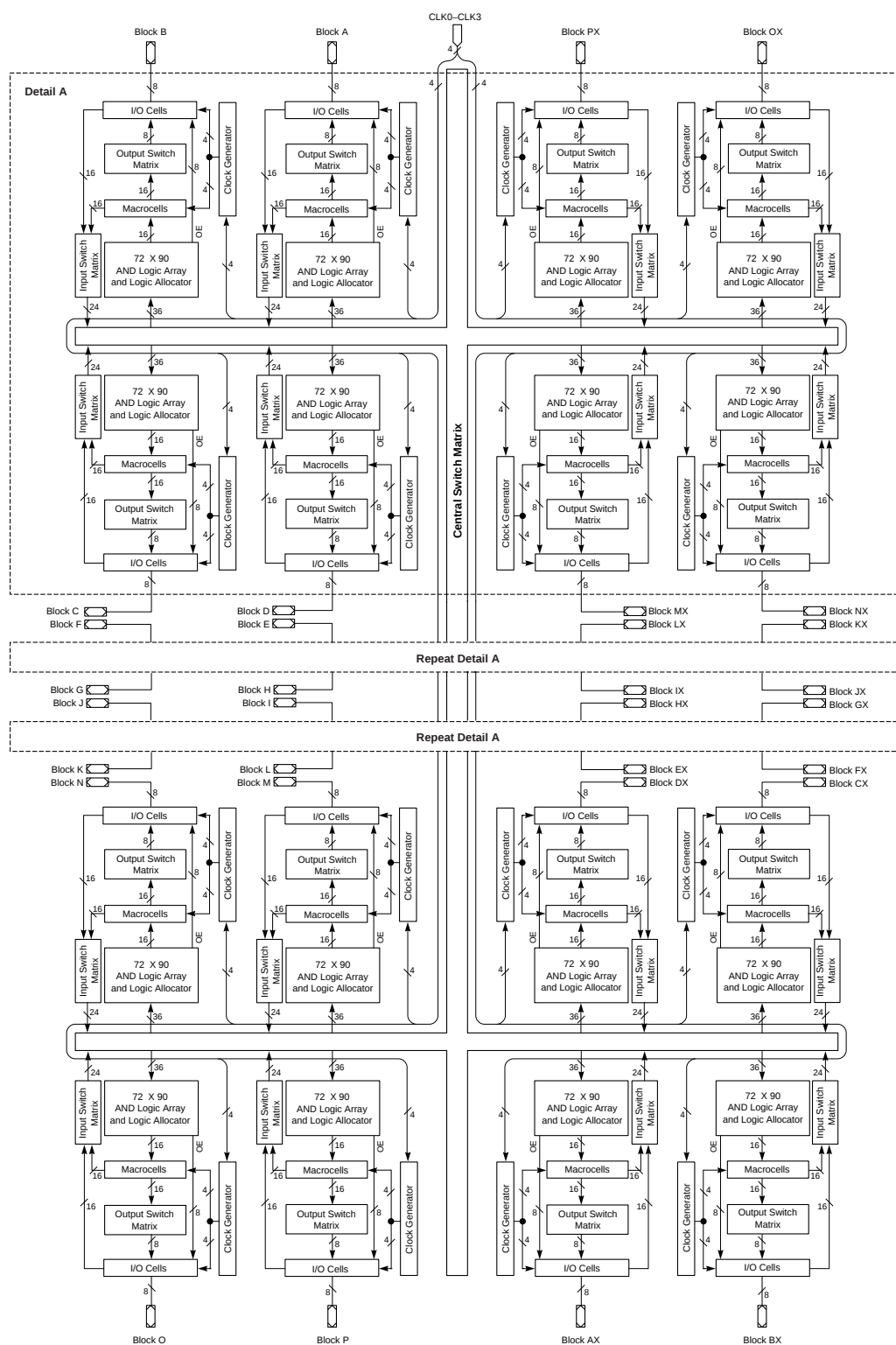
17466G-021

BLOCK DIAGRAM – M4A3-384/160, M4A3-384/192



17466G-067

BLOCK DIAGRAM - M4A3-512/160, M4A3-512/192, M4A3-512/256



17466G-068

ABSOLUTE MAXIMUM RATINGS

M4A5

Storage Temperature. -65°C to +150°C
 Ambient Temperature
 with Power Applied. -55°C to +100°C
 Device Junction Temperature. +130°C
 Supply Voltage
 with Respect to Ground -0.5 V to +7.0 V
 DC Input Voltage -0.5 V to $V_{CC} + 0.5$ V
 Static Discharge Voltage 2000 V
 Latchup Current ($T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$) 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)
 Operating in Free Air. 0°C to $+70^\circ\text{C}$
 Supply Voltage (V_{CC})
 with Respect to Ground. +4.75 V to +5.25 V

Industrial (I) Devices

Ambient Temperature (T_A)
 Operating in Free Air. -40°C to $+85^\circ\text{C}$
 Supply Voltage (V_{CC})
 with Respect to Ground. +4.50 V to +5.5 V
Operating ranges define those limits between which the functionality of the device is guaranteed.

5-V DC CHARACTERISTICS OVER OPERATING RANGES

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	$I_{OH} = -3.2$ mA, $V_{CC} = \text{Min}$, $V_{IN} = V_{IH}$ or V_{IL}	2.4			V
		$I_{OH} = -100$ μA , $V_{CC} = \text{Max}$, $V_{IN} = V_{IH}$ or V_{IL}		3.3	3.6	V
V_{OL}	Output LOW Voltage	$I_{OL} = 24$ mA, $V_{CC} = \text{Min}$, $V_{IN} = V_{IH}$ or V_{IL} (Note 1)			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 2)	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 2)			0.8	V
I_{IH}	Input HIGH Leakage Current	$V_{IN} = 5.25$ V, $V_{CC} = \text{Max}$ (Note 3)			10	μA
I_{IL}	Input LOW Leakage Current	$V_{IN} = 0$ V, $V_{CC} = \text{Max}$ (Note 3)			-10	μA
I_{OZH}	Off-State Output Leakage Current HIGH	$V_{OUT} = 5.25$ V, $V_{CC} = \text{Max}$, $V_{IN} = V_{IH}$ or V_{IL} (Note 3)			10	μA
I_{OZL}	Off-State Output Leakage Current LOW	$V_{OUT} = 0$ V, $V_{CC} = \text{Max}$, $V_{IN} = V_{IH}$ or V_{IL} (Note 3)			-10	μA
I_{SC}	Output Short-Circuit Current	$V_{OUT} = 0.5$ V, $V_{CC} = \text{Max}$ (Note 4)	-30		-160	mA

Notes:

1. Total I_{OL} for one PAL block should not exceed 64 mA.
2. These are absolute values with respect to device ground, and all overshoots due to system or tester noise are included.
3. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
4. Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
 $V_{OUT} = 0.5$ V has been chosen to avoid test problems caused by tester ground degradation.

ispMACH 4A TIMING PARAMETERS OVER OPERATING RANGES¹

		-5		-55		-6		-65		-7		-10		-12		-14		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Input Register Delays with ZHT Option:																		
t _{SIRZ}	Input register setup time - ZHT	6.0		6.0		6.0		6.0		6.0		6.0		6.0		6.0		ns
t _{HIRZ}	Input register hold time - ZHT	0.0		0.0		0.0		0.0		0.0		0.0		0.0		0.0		ns
Input Latch Delays with ZHT Option:																		
t _{SILZ}	Input latch setup time - ZHT	6.0		6.0		6.0		6.0		6.0		6.0		6.0		6.0		ns
t _{HILZ}	Input latch hold time - ZHT	0.0		0.0		0.0		0.0		0.0		0.0		0.0		0.0		ns
t _{PDIL} Z _i	Transparent input latch to internal feedback - ZHT		6.0		6.0		6.0		6.0		6.0		6.0		6.0		6.0	ns
Output Delays:																		
t _{BUF}	Output buffer delay		1.5		1.5		1.8		2.0		2.5		3.0		3.0		3.0	ns
t _{SLW}	Slow slew rate delay adder		2.5		2.5		2.5		2.5		2.5		2.5		2.5		2.5	ns
t _{EA}	Output enable time		7.5		7.5		8.5		8.5		9.5		10.0		12.0		15.0	ns
t _{ER}	Output disable time		7.5		7.5		8.5		8.5		9.5		10.0		12.0		15.0	ns
Power Delay:																		
t _{PL}	Power-down mode delay adder		2.5		2.5		2.5		2.5		2.5		2.5		2.5		2.5	ns
Reset and Preset Delays:																		
t _{SRI}	Asynchronous reset or preset to internal register output		7.5		7.7		8.0		8.0		9.5		11.0		13.0		16.0	ns
t _{SR}	Asynchronous reset or preset to register output		9.0		9.2		10.0		10.0		12.0		14.0		16.0		19.0	ns
t _{SRR}	Asynchronous reset and preset register recovery time	7.0		7.0		7.5		7.5		8.0		8.0		10.0		15.0		ns
t _{SRW}	Asynchronous reset or preset width	7.0		7.0		8.0		8.0		10.0		10.0		12.0		15.0		ns
Clock/LE Width:																		
t _{WLS}	Global clock width low	2.0		2.0		2.5		2.5		3.0		4.0		5.0		6.0		ns
t _{WHS}	Global clock width high	2.0		2.0		2.5		2.5		3.0		4.0		5.0		6.0		ns
t _{WLA}	Product term clock width low	3.0		3.0		3.5		3.5		4.0		5.0		8.0		9.0		ns
t _{WHA}	Product term clock width high	3.0		3.0		3.5		3.5		4.0		5.0		8.0		9.0		ns
t _{GWS}	Global gate width low (for low transparent) or high (for high transparent)	4.0		4.0		4.5		4.5		5.0		5.0		6.0		6.0		ns
t _{GWA}	Product term gate width low (for low transparent) or high (for high transparent)	4.0		4.0		4.5		4.5		5.0		5.0		6.0		9.0		ns
t _{WIRL}	Input register clock width low	3.0		3.0		3.5		3.5		4.0		5.0		6.0		6.0		ns
t _{WIRH}	Input register clock width high	3.0		3.0		3.5		3.5		4.0		5.0		6.0		6.0		ns
t _{WIL}	Input latch gate width	4.0		4.0		4.5		4.5		5.0		5.0		6.0		6.0		ns

I_{CC} vs. FREQUENCY

These curves represent the typical power consumption for a particular device at system frequency. The selected “typical” pattern is a 16-bit up-down counter. This pattern fills the device and exercises every macrocell. Maximum frequency shown uses internal feedback and a D-type register. Power/Speed are optimized to obtain the highest counter frequency and the lowest power. The highest frequency (LSBs) is placed in common PAL blocks, which are set to high power. The lowest frequency signals (MSBs) are placed in a common PAL block and set to lowest power.

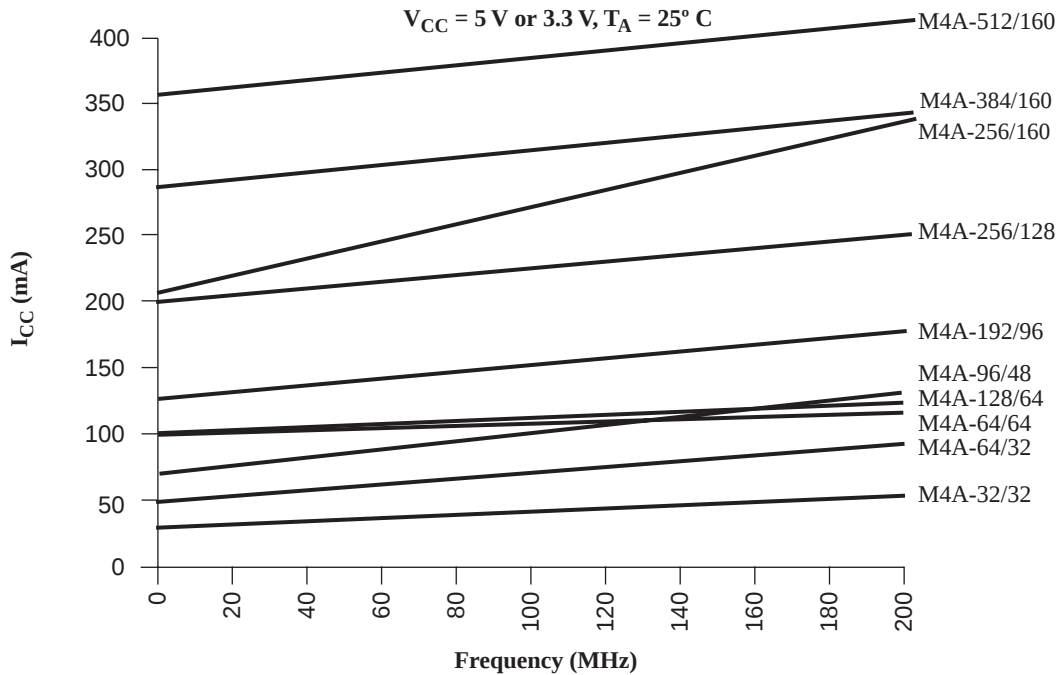


Figure 19. ispMACH 4A I_{CC} Curves at High Speed Mode

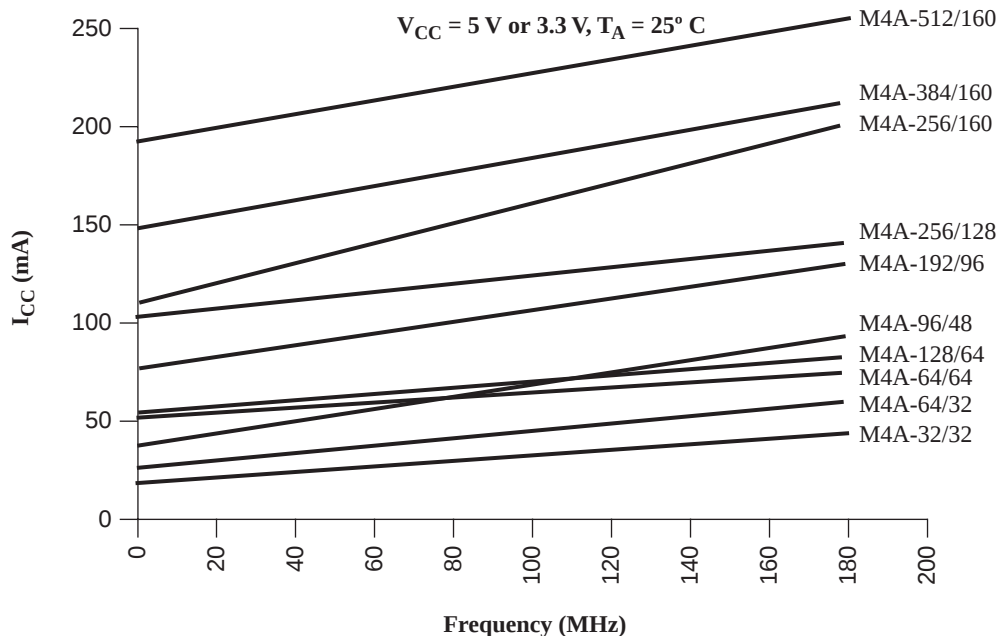
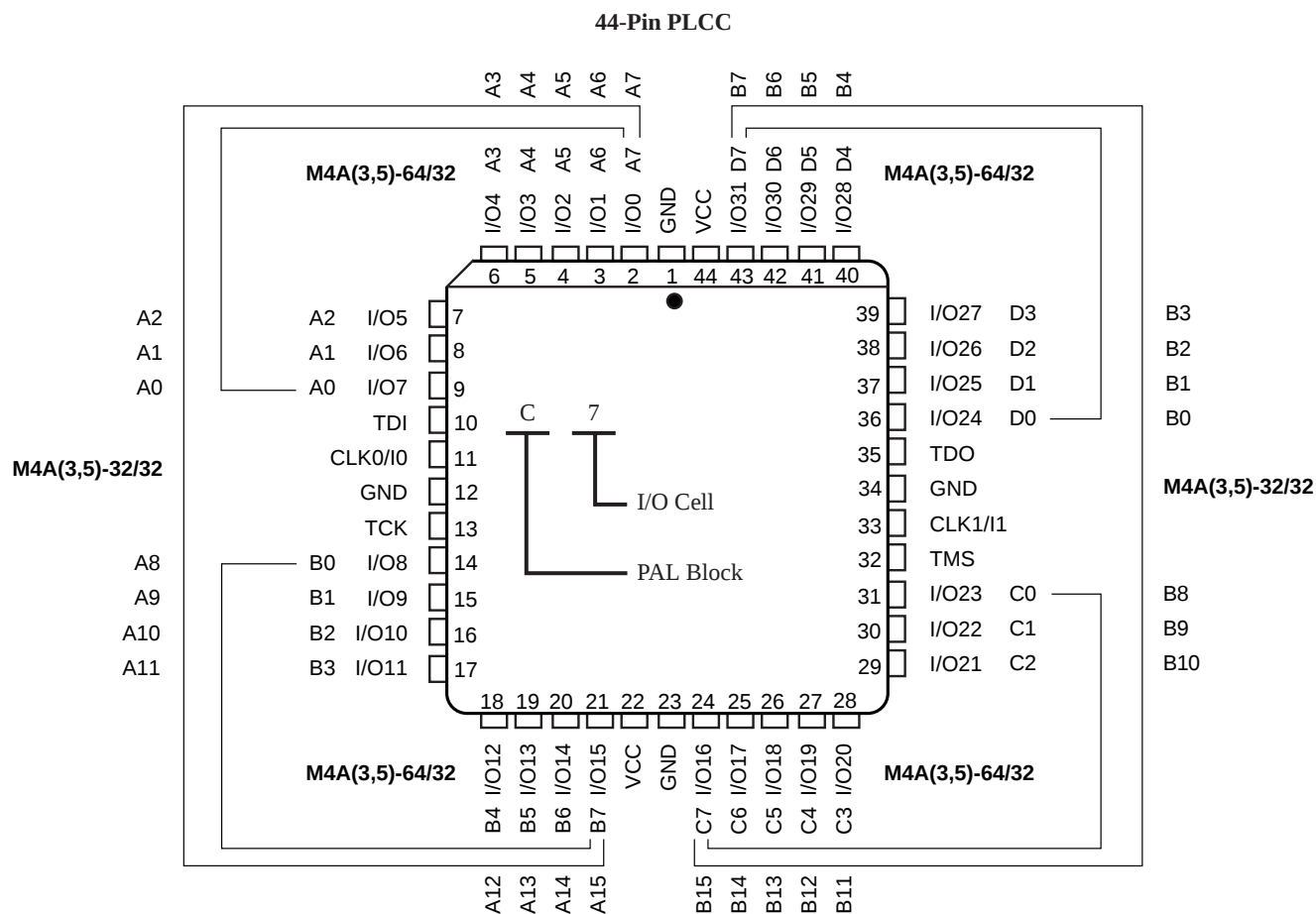


Figure 20. ispMACH 4A I_{CC} Curves at Low Power Mode

44-PIN PLCC CONNECTION DIAGRAM (M4A(3,5)-32/32 AND M4A(3,5)-64/32)

Top View



17466G-026

PIN DESIGNATIONS

CLK/I = Clock or Input

GND = Ground

I/O = Input/Output

V_{CC} = Supply Voltage

TDI = Test Data In

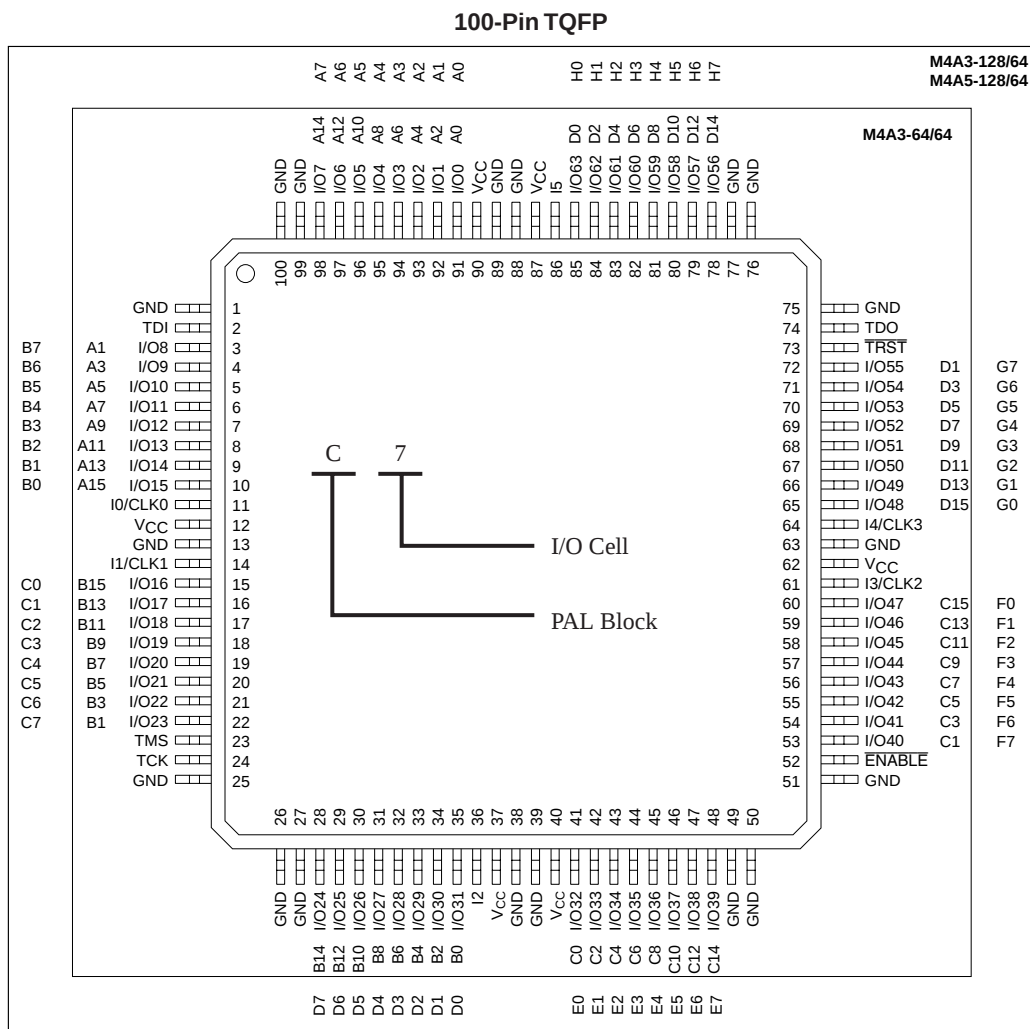
TCK = Test Clock

TMS = Test Mode Select

TDO = Test Data Out

100-PIN TQFP CONNECTION DIAGRAM (M4A3-64/64 AND M4A(3,5)-128/64)

Top View



PIN DESIGNATIONS

CLK/I = Clock or Input

GND = Ground

I = Input

I/O = Input/Output

V_{CC} = Supply Voltage

TDI = Test Data In

TCK = Test Clock

TMS = Test Mode Select

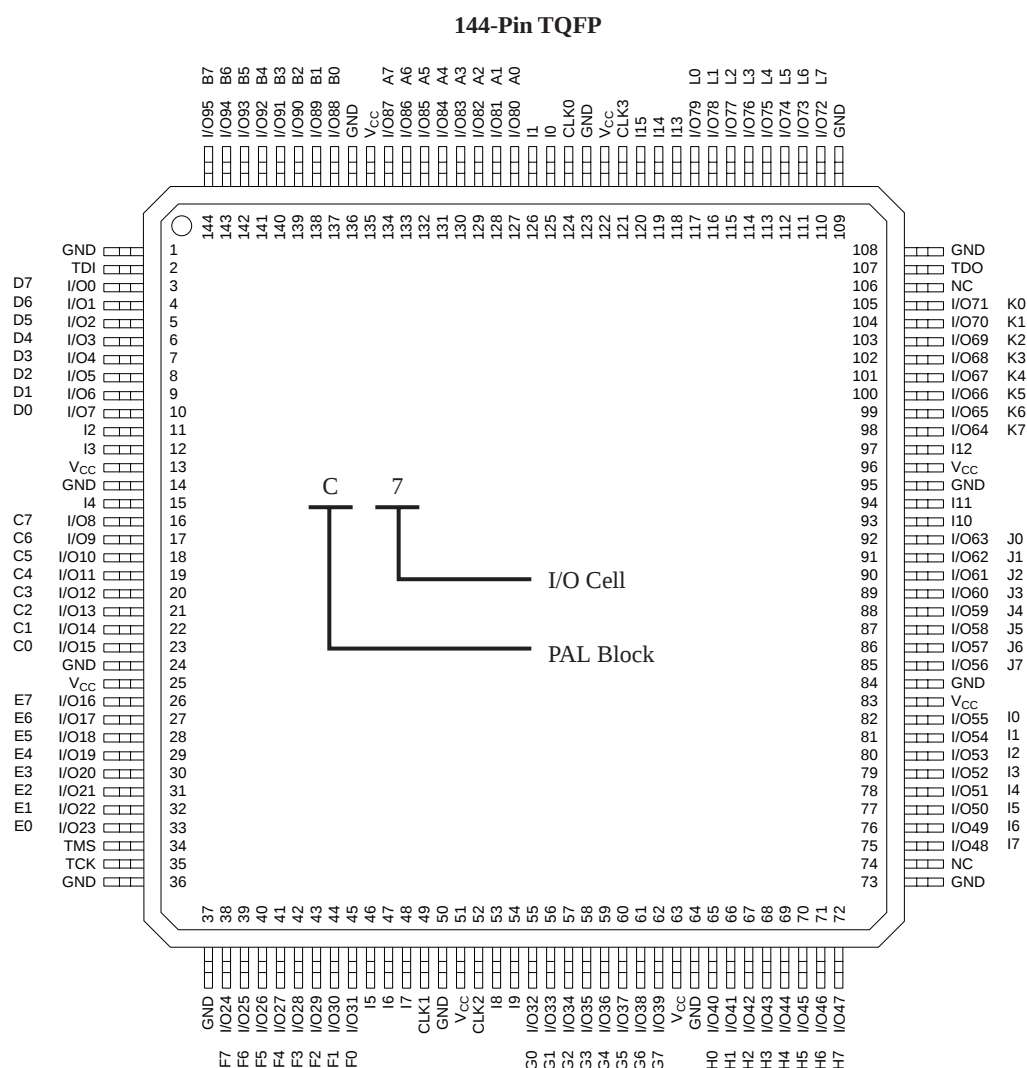
TDO = Test Data Out

TRST = Test Reset

ENABLE = Program

144-PIN TQFP CONNECTION DIAGRAM (M4A(3,5)-192/96)

Top View



17466G-033

PIN DESIGNATIONS

- CLK = Clock
- GND = Ground
- I = Input
- I/O = Input/Output
- V_{CC} = Supply Voltage
- TDI = Test Data In
- TCK = Test Clock
- TMS = Test Mode Select
- TDO = Test Data Out

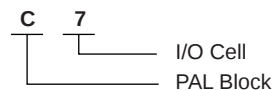
144-BALL FPBGA CONNECTION DIAGRAM (M4A3-192/96)

Bottom View

144-Ball fpBGA													
	12	11	10	9	8	7	6	5	4	3	2	1	
A	GND	I/O72 L7	I/O76 L3	I13	GBCLK3	I0	I/O82 A2	I/O86 A6	I/O88 B0	I/O93 B5	I/O95 B7	GND	A
B	GND	I/O73 L6	I/O77 L2	I/O79 L0	VCC	I1	I/O83 A3	I/O87 A7	I/O90 B2	I/O94 B6	I/O0 D7	TDI	B
C	GND	TD0	I/O74 L5	I14	GND	I/O80 A0	I/O84 A4	GND	I/O92 B4	I/O1 D6	I/O4 D3	I/O3 D4	C
D	I/O67 K4	I/O69 K2	I/O71 K0	I/O75 L4	GBCLK0	I/O81 A1	VCC	I/O91 B3	I/O2 D5	I2	I/O6 D1	I/O7 D0	D
E	I12	I/O64 K7	I/O66 K5	I/O70 K1	I/O78 L1	I/O85 A5	I/O89 B1	I/O5 D2	I/O8 C7	I4	GND	VCC	E
F	I10	I11	GND	I/O65 K6	I/O68 K3	I15	I3	GND	I/O12 C3	I/O11 C4	I/O10 C5	I/O9 C6	F
G	I/O60 J3	I/O61 J2	I/O62 J1	I/O63 J0	VCC	GND	I7	I/O20 E3	I/O17 E6	I/O15 C0	I/O14 C1	I/O13 C2	G
H	I/O56 J7	I/O57 J6	I/O58 J5	I/O59 J4	I/O53 I2	I/O41 H1	I/O37 G5	I/O30 F1	I/O22 E1	I/O18 E5	I/O16 E7	VCC	H
J	I/O55 I0	I/O54 I1	VCC	I/O50 I5	I/O43 H3	VCC	I/O33 G1	GBCLK2	I/O27 F4	I/O23 E0	I/O21 E2	I/O19 E4	J
K	I/O51 I4	I/O52 I3	I/O49 I6	I/O44 H4	GND	I/O36 G4	I/O32 G0	VCC	I6	I/O26 F5	TCK	TMS	K
L	GND	I/O48 I7	I/O46 H6	I/O42 H2	I/O39 G7	I/O35 G3	I9	GND	I/O31 F0	I/O29 F2	I/O25 F6	GND	L
M	GND	I/O47 H7	I/O45 H5	I/O40 H0	I/O38 G6	I/O34 G2	I8	GBCLK1	I5	I/O28 F3	I/O24 F7	GND	M
	12	11	10	9	8	7	6	5	4	3	2	1	

PIN DESIGNATIONS

CLK = Clock
 GND = Ground
 I = Input
 I/O = Input/Output
 N/C = No Connect
 VCC = Supply Voltage
 TDI = Test Data In
 TCK = Test Clock
 TMS = Test Mode Select
 TD0 = Test Data Out

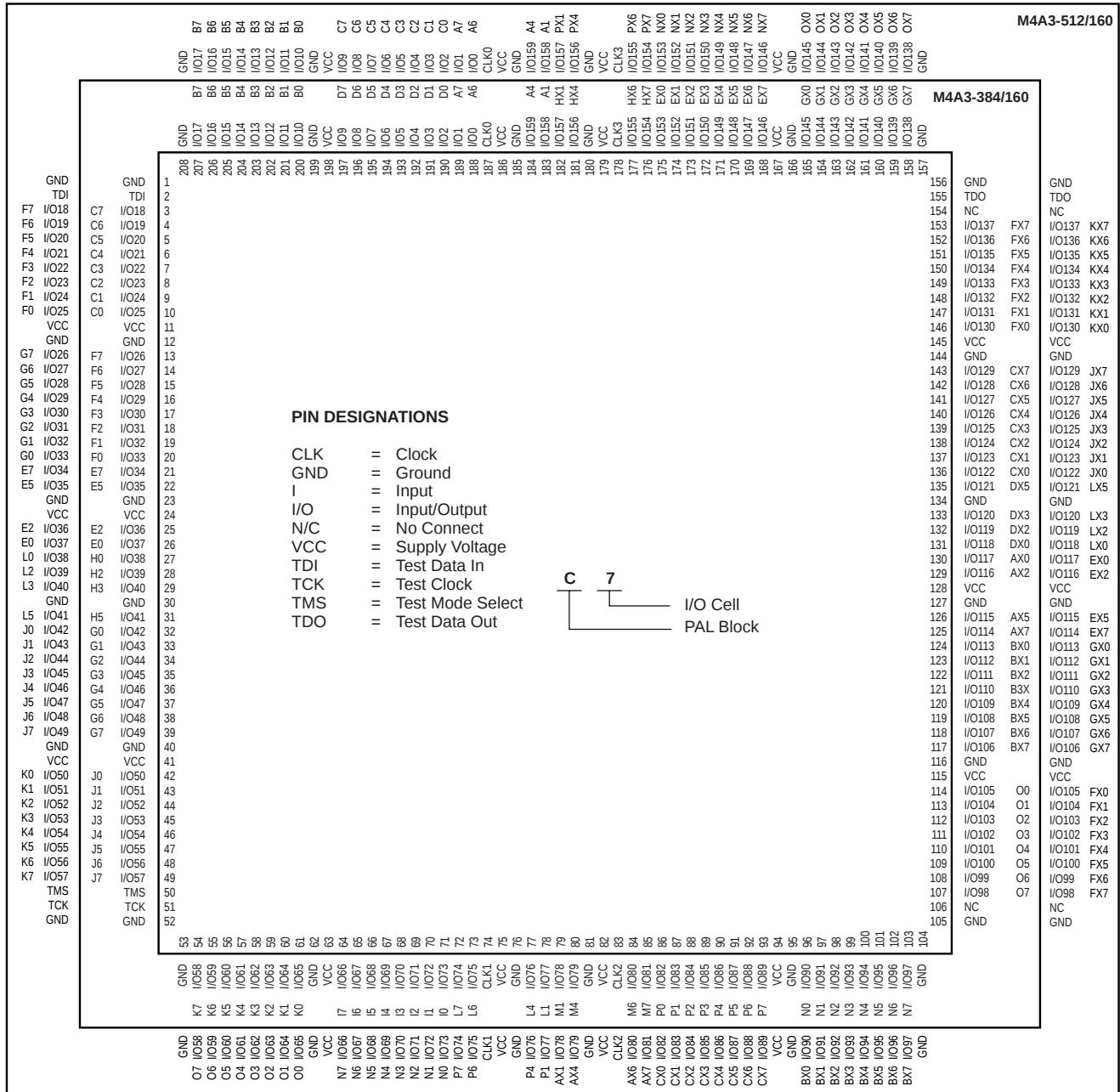


m4a3.192.96_144bga

208-PIN PQFP CONNECTION DIAGRAM (M4A3-384/160 AND M4A3-512/160)

Top View

208-Pin PQFP



17466Ga-044

256-BALL BGA CONNECTION DIAGRAM (M4A3-256/128)

Bottom View

256-Ball BGA

	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	GND	N/C	GND	I/O108 N4	I/O105 N1	GND	I/O100 M4	I/O96 M0	GND	GND	GND	GND	I/O95 L0	I/O91 L4	GND	I/O87 K0	N/C	GND	GND	GND	A
B	GND	I/O113 O6	N/C	I/O109 N5	I/O106 N2	I/O103 M7	I/O102 M6	I/O98 M2	N/C	I11	N/C	N/C	I/O93 L2	I/O89 L6	I/O88 L7	I/O85 K2	I/O83 K4	I/O82 K5	N/C	GND	B
C	I/O116 O3	N/C	VCC	TRST	I/O111 N7	I/O107 N3	I/O104 N0	I/O101 M5	I/O97 M1	N/C	I10	I/O94 L1	I/O90 L5	I/O86 K1	I/O84 K3	I/O80 K7	ENABLE	VCC	I/O78 J6	I/O74 J2	C
D	I/O120 P7	I/O117 O2	I/O112 O7	VCC	VCC	I/O110 N6	VCC	N/C	I/O99 M3	N/C	I9	I/O92 L3	N/C	VCC	I/O81 K6	VCC	VCC	I/O79 J7	I/O75 J3	I/O71 I7	D
E	I/O123 P4	I/O119 O0	I/O114 O5	TDI	PIN DESIGNATIONS CLK = Clock GND = Ground I = Input I/O = Input/Output N/C = No Connect VCC = Supply Voltage TDI = Test Data In TCK = Test Clock TMS = Test Mode Select TDO = Test Data Out TRST = Test Reset ENABLE = Program C7 I/O Cell PAL Block												TDO	I/O77 J5	I/O72 J0	I/O68 I4	E
F	GND	I/O122 P5	I/O118 O1	I/O115 O4													I/O76 J4	I/O73 J1	I/O69 I5	GND	F
G	I12	I/O125 P2	I/O121 P6	VCC													VCC	I/O70 I6	I/O65 I1	I8	G
H	GND	I/O127 P0	I/O126 P1	I/O124 P3													I/O67 I3	I/O66 I2	I/O64 I0	GND	H
J	N/C	N/C	N/C	I13													I7	N/C	N/C	N/C	J
K	GND	CLK3	N/C	N/C													N/C	N/C	CLK2	N/C	K
L	N/C	CLK0	N/C	N/C													N/C	N/C	CLK1	GND	L
M	N/C	N/C	N/C	I0													I6	N/C	I/O63 H0	I/O62 H1	M
N	GND	I/O0 A0	I/O2 A2	I/O3 A3	I/O60 H3	I/O61 H2	I/O59 H4	GND	N												
P	I1	I/O1 A1	I/O6 A6	VCC	VCC	I/O57 H6	I/O58 H5	I5	P												
R	GND	I/O5 A5	I/O9 B1	N/C	I/O51 G4	I/O54 G1	I/O56 H7	GND	R												
T	I/O4 A4	I/O8 B0	I/O12 B4	TCK	TMS	I/O50 G5	I/O55 G0	N/C	T												
U	I/O7 A7	I/O11 B3	I/O15 B7	VCC	VCC	I/O18 C5	VCC	I/O24 D7	I/O29 D2	I2	N/C	I/O35 E3	N/C	VCC	N/C	VCC	VCC	I/O48 G7	I/O53 G2	N/C	U
V	I/O10 B2	I/O13 B5	VCC	I/O16 C7	I/O17 C6	I/O21 C2	I/O23 C0	I/O27 D4	I/O31 D0	I3	N/C	I/O33 E1	I/O37 E5	I/O41 F1	I/O43 F3	I/O46 F6	I/O47 F7	VCC	I/O52 G3	N/C	V
W	GND	I/O14 B6	N/C	N/C	I/O19 C4	I/O22 C1	I/O25 D6	I/O28 D3	N/C	N/C	I4	N/C	I/O34 E2	I/O38 E6	I/O39 E7	I/O42 F2	I/O45 F5	N/C	I/O49 G6	GND	W
Y	GND	GND	GND	N/C	I/O20 C3	GND	I/O26 D5	I/O30 D1	GND	GND	GND	GND	I/O32 E0	I/O36 E4	GND	I/O40 F0	I/O44 F4	GND	N/C	GND	Y
	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

17466G-045

256-BALL fpBGA CONNECTION DIAGRAM (M4A3-256/192)

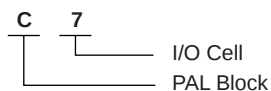
Bottom View

256-Ball fpBGA

	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	I/O167 N15	I/O181 O13	I/O180 O12	I/O177 O9	I/O174 O6	I/O172 O4	I/O191 P14	I/O186 P4	I/O1 A2	I/O3 A6	GCLK0	I/O9 B1	I/O13 B5	I/O15 B7	I/O18 B10	I/O20 B12	A
B	I/O165 N13	I/O166 N14	I/O182 O14	I/O179 O11	I/O175 O7	I/O173 O5	I/O168 O0	I/O187 P6	I/O0 A0	I/O5 A10	I/O7 A14	I/O10 B2	I/O16 B8	I/O19 B11	I/O21 B13	NC	B
C	I/O163 N11	I/O164 N12	NC	I/O183 O15	I/O178 O10	I/O170 O2	I/O171 O3	I/O189 P10	I/O184 P0	I/O6 A12	I/O12 B4	I/O14 B6	I/O23 B15	I/O22 B14	TDI	I/O39 C15	C
D	I/O158 N6	I/O159 N7	TDO	GND	GND	VCC	GND	VCC	GND	GND	VCC	GND	VCC	I/O17 B9	I/O38 C14	I/O37 C13	D
E	I/O156 N4	NC	I/O162 N10	VCC	I/O160 N8	I/O161 N9	I/O190 P12	GCLK3	I/O188 P8	I/O2 A4	I/O8 B0	NC	GND	I/O36 C12	I/O35 C11	I/O31 C7	E
F	I/O152 N0	I/O157 N5	I/O155 N3	GND	I/O154 N2	I/O153 N1	I/O176 O8	I/O169 O1	I/O185 P2	I/O4 A8	I/O11 B3	I/O34 C10	VCC	I/O32 C8	I/O30 C6	I/O29 C5	F
G	I/O147 M6	I/O150 M12	I/O149 M10	VCC	I/O148 M8	I/O151 M14	VCC	GND	GND	VCC	I/O33 C9	I/O28 C4	GND	I/O26 C2	I/O25 C1	I/O47 D14	G
H	I/O144 M0	I/O146 M4	I/O145 OM2	GND	I/O136 L0	I/O137 L2	GND	VCC	VCC	GND	I/O27 C3	I/O24 C0	VCC	I/O44 D8	I/O43 D6	I/O42 D4	H
J	I/O138 L4	I/O139 L6	I/O140 L8	GND	I/O142 L12	I/O141 L10	GND	VCC	VCC	GND	I/O46 D12	I/O45 D10	GND	I/O49 E2	I/O48 E0	I/O50 E4	J
K	I/O143 L14	I/O120 K0	I/O121 K1	VCC	I/O123 K3	I/O122 K2	VCC	GND	GND	VCC	I/O41 D2	I/O40 D0	VCC	I/O55 E14	I/O54 E12	I/O56 F0	K
L	I/O124 K4	I/O125 K5	I/O127 K7	GND	I/O130 K10	I/O126 K6	I/O98 I4	I/O91 H6	I/O75 G3	I/O77 G5	I/O52 E8	I/O51 E6	GND	I/O59 F3	I/O60 F4	I/O57 F1	L
M	I/O128 K8	I/O129 K9	I/O131 K11	GND	I/O107 J3	I/O105 J1	I/O100 I8	I/O90 H4	I/O74 G2	I/O80 G8	I/O83 G11	I/O53 E10	VCC	I/O68 F12	I/O63 F7	I/O58 F2	M
N	I/O132 K12	I/O133 K13	I/O135 K15	VCC	GND	VCC	GND	VCC	GND	GND	VCC	GND	GND	TCK	I/O64 F8	I/O61 F5	N
P	I/O134 K14	I/O117 J13	I/O118 J14	I/O119 J15	I/O108 J4	I/O106 J2	I/O101 I10	I/O89 H2	I/O93 H10	I/O94 H12	I/O79 G7	I/O84 G12	I/O87 G15	TMS	I/O65 F9	I/O62 F6	P
R	I/O116 J12	I/O115 J11	I/O112 J8	I/O111 J7	I/O104 J0	I/O102 I12	I/O99 I6	I/O96 I0	I/O92 H8	I/O72 G0	I/O76 G4	I/O81 G9	I/O85 G13	I/O71 F15	I/O67 F11	I/O66 F10	R
T	I/O114 J10	I/O113 J9	I/O110 J6	I/O109 J5	I/O103 I14	GCLK2	I/O97 I2	I/O88 H0	GCLK1	I/O95 H14	I/O73 G1	I/O78 G6	I/O82 G10	I/O86 G14	I/O70 F14	I/O69 F13	T
	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

PIN DESIGNATIONS

CLK = Clock
 GND = Ground
 I = Input
 I/O = Input/Output
 N/C = No Connect
 VCC = Supply Voltage
 TDI = Test Data In
 TCK = Test Clock
 TMS = Test Mode Select
 TDO = Test Data Out



17466G-047

256-BALL BGA CONNECTION DIAGRAM - (M4A3-384/192)

Bottom View

256-Ball BGA

	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	GND	I/O11 FX7	GND	I/O44 FX6	I/O58 CX6	GND	I/O70 CX2	I/O76 DX6	GND	GND	GND	GND	I/O108 AX5	I/O116 BX0	GND	I/O128 BX7	I/O134 O3	GND	GND	GND	A
B	GND	I/O12 GX7	I/O28 FX5	I/O45 FX3	I/O59 CX7	I/O64 CX5	I/O71 CX3	I/O77 DX7	I/O84 DX5	I/O90 DX2	I/O96 AX0	I/O102 AX3	I/O109 AX6	I/O117 BX1	I/O122 BX4	I/O129 BX6	I/O135 O4	I/O148 O6	I/O164 O7	GND	B
C	I/O0 GX6	I/O13 GX5	VCC	I/O46 FX4	I/O60 FX2	I/O65 FX1	I/O72 CX4	I/O78 CX0	I/O85 DX4	I/O91 DX1	I/O97 AX1	I/O103 AX4	I/O110 BX2	I/O118 BX5	I/O123 O0	I/O130 O1	I/O136 O5	VCC	I/O165 N7	I/O181 N6	C
D	I/O1 EX7	I/O14 GX3	I/O29 GX4	VCC	VCC	I/O66 FX0	VCC	I/O79 CX1	I/O86 DX3	I/O92 DX0	I/O98 AX2	I/O104 AX7	I/O111 BX3	VCC	I/O124 O2	VCC	VCC	I/O149 N4	I/O166 N5	I/O182 P7	D
E	I/O2 EX0	I/O15 GX0	I/O30 GX1	TDI	PIN DESIGNATIONS CLK = Clock GND = Ground I = Input I/O = Input/Output N/C = No Connect VCC = Supply Voltage TDI = Test Data In TCK = Test Clock TMS = Test Mode Select TDO = Test Data Out												TDO	I/O150 N2	I/O167 N3	I/O183 P6	E
F	GND	I/O16 EX1	I/O31 EX6	I/O47 GX2													I/O137 N1	I/O151 N0	I/O168 P5	GND	F
G	I/O3 HX6	I/O17 EX4	I/O32 EX5	VCC													VCC	I/O152 P4	I/O169 P3	I/O184 M7	G
H	GND	I/O18 HX5	I/O33 EX2	I/O48 EX3													I/O138 P2	I/O153 P1	I/O170 P0	GND	H
J	I/O4 HX0	I/O19 HX1	I/O34 HX4	I/O49 HX7													I/O139 M6	I/O154 M5	I/O171 M4	I/O185 M3	J
K	GND	CLK3	I/O35 HX2	I/O50 HX3													I/O140 M0	I/O155 M1	CLK2	I/O186 M2	K
L	I/O5 A2	CLK0	I/O36 A0	I/O51 A1													I/O141 L3	I/O156 L4	CLK1	GND	L
M	I/O6 A4	I/O20 A3	I/O37 A5	I/O52 A6													I/O142 L6	I/O157 L5	I/O172 L0	I/O187 L1	M
N	GND	I/O21 A7	I/O38 D0	I/O53 D1													I/O143 I5	I/O158 I0	I/O173 L7	GND	N
P	I/O7 D2	I/O22 D3	I/O39 D4	VCC													VCC	I/O159 I4	I/O174 I1	I/O188 L2	P
R	GND	I/O23 D5	I/O40 D6	I/O54 D7													I/O144 K5	I/O160 K0	I/O175 I3	GND	R
T	I/O8 B3	I/O24 B0	I/O41 B7	TCK													TMS	I/O161 K4	I/O176 K1	I/O189 I2	T
U	I/O9 B4	I/O25 B1	I/O42 B6	VCC	VCC	I/O67 C0	VCC	I/O80 F0	I/O87 E5	I/O93 E2	I/O99 H2	I/O105 H5	I/O112 G0	VCC	I/O125 J1	VCC	VCC	I/O162 K7	I/O177 K2	I/O190 I6	U
V	I/O10 B5	I/O26 B2	VCC	I/O55 C5	I/O61 C2	I/O68 C1	I/O73 F4	I/O81 F1	I/O88 E4	I/O94 E1	I/O100 H1	I/O106 H4	I/O113 G1	I/O119 G4	I/O126 J0	I/O131 J2	I/O145 J5	VCC	I/O178 K3	I/O191 I7	V
W	GND	I/O27 C7	I/O43 C6	I/O56 C3	I/O62 F7	I/O69 F5	I/O74 F3	I/O82 E7	I/O89 E3	I/O95 E0	I/O101 H0	I/O107 H3	I/O114 H7	I/O120 G3	I/O127 G5	I/O132 G7	I/O146 J4	I/O163 J6	I/O179 J7	GND	W
Y	GND	GND	GND	I/O57 C4	I/O63 F6	GND	I/O75 F2	I/O83 E6	GND	GND	GND	GND	I/O115 H6	I/O121 G2	GND	I/O133 G6	I/O147 J3	GND	I/O180 K6	GND	Y
	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

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256-BALL fpBGA CONNECTION DIAGRAM (M4A3-384/192)

Bottom View

256-Ball fpBGA

	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	I/O175 FX7	I/O181 GX5	I/O180 GX4	I/O177 GX1	I/O166 EX6	I/O164 EX4	I/O191 HX7	I/O186 HX2	I/O1 A1	I/O3 A3	CLK0	I/O25 D1	I/O29 D5	I/O31 D7	I/O10 B2	I/O12 B4	A
B	I/O173 FX5	I/O174 FX6	I/O182 GX6	I/O179 GX3	I/O167 EX7	I/O165 EX5	I/O160 EX0	I/O187 HX3	I/O0 A0	I/O5 A5	I/O7 A7	I/O26 D2	I/O8 B0	I/O11 B3	I/O13 B5	N/C	B
C	I/O171 FX3	I/O172 FX4	N/C	I/O183 GX7	I/O178 GX2	I/O162 EX2	I/O163 EX3	I/O189 HX5	I/O184 HX0	I/O6 A6	I/O28 D4	I/O30 D6	I/O15 B7	I/O14 B6	TDI	I/O23 C7	C
D	I/O150 CX6	I/O151 CX7	TDO	GND	GND	VCC	GND	VCC	GND	GND	VCC	GND	VCC	I/O9 B1	I/O22 C6	I/O21 C5	D
E	I/O148 CX4	N/C	I/O170 FX2	VCC	I/O168 FX0	169 FX1	I/O190 HX6	CLK3	I/O188 HX4	I/O2 A2	I/O24 D0	N/C	GND	I/O20 C4	I/O19 C3	I/O47 F7	E
F	I/O144 CX0	I/O149 CX5	I/O147 CX3	GND	I/O146 CX2	I/O145 CX1	I/O176 GX0	I/O161 EX1	I/O185 HX1	I/O4 A4	I/O27 D3	I/O18 C2	VCC	I/O16 C0	I/O46 F6	I/O45 F5	F
G	I/O155 DX3	I/O158 DX6	I/O157 DX5	VCC	I/O156 DX4	I/O159 DX7	VCC	GND	GND	VCC	I/O17 C1	I/O44 F4	GND	I/O42 F2	I/O41 F1	I/O39 E7	G
H	I/O152 DX0	I/O154 DX2	I/O153 DX1	GND	I/O128 AX0	I/O129 AX1	GND	VCC	VCC	GND	I/O43 F3	I/O40 F0	VCC	I/O36 E4	I/O35 E3	I/O34 E2	H
J	I/O130 AX2	I/O131 AX3	I/O132 AX4	GND	I/O134 AX6	I/O133 AX5	GND	VCC	VCC	GND	I/O38 E6	I/O37 E5	GND	I/O57 H1	I/O56 H0	I/O58 H2	J
K	I/O135 AX7	I/O136 BX0	I/O137 BX1	VCC	I/O139 BX3	I/O138 BX2	VCC	GND	GND	VCC	I/O33 E1	I/O32 E0	VCC	I/O63 H7	I/O62 H6	I/O48 G0	K
L	I/O140 BX4	I/O141 BX5	I/O143 BX7	GND	I/O114 O2	I/O142 BX6	I/O98 M2	I/O91 L3	I/O67 I3	I/O69 I5	I/O60 H4	I/O59 H3	GND	I/O51 G3	I/O52 G4	I/O49 G1	L
M	I/O112 O0	I/O113 O1	I/O115 O3	GND	I/O123 P3	I/O121 P1	I/O100 M4	I/O90 L2	I/O66 I2	I/O80 K0	I/O83 K3	I/O61 H5	VCC	I/O76 J4	I/O55 G7	I/O50 G2	M
N	I/O116 O4	I/O117 O5	I/O119 O7	VCC	GND	VCC	GND	VCC	GND	GND	VCC	GND	GND	TCK	I/O72 J0	I/O53 G5	N
P	I/O118 O6	I/O109 N5	I/O110 N6	I/O111 N7	I/O124 P4	I/O122 P2	I/O101 M5	I/O89 L1	I/O93 L5	I/O94 L6	I/O71 I7	I/O84 K4	I/O87 K7	TMS	I/O73 J1	I/O54 G6	P
R	I/O108 N4	I/O107 N3	I/O104 N0	I/O127 P7	I/O120 P0	I/O102 M6	I/O99 M3	I/O96 M0	I/O92 L4	I/O64 I0	I/O68 I4	I/O81 K1	I/O85 K5	I/O79 J7	I/O75 J3	I/O74 J2	R
T	I/O106 N2	I/O105 N1	I/O126 P6	I/O125 P5	I/O103 M7	CLK2	I/O97 M1	I/O88 L0	CLK1	I/O95 L7	I/O65 I1	I/O70 I6	I/O82 K2	I/O86 K6	I/O78 J6	I/O77 J5	T
	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

PIN DESIGNATIONS

CLK = Clock
 GND = Ground
 I = Input
 I/O = Input/Output
 N/C = No Connect
 VCC = Supply Voltage
 TDI = Test Data In
 TCK = Test Clock
 TMS = Test Mode Select
 TDO = Test Data Out



m4a3.384.192_256bga

256-BALL fpBGA CONNECTION DIAGRAM (M4A3-512/192)

Bottom View

256-Ball fpBGA

	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	I/O159 KX7	I/O181 OX5	I/O180 OX4	I/O177 OX1	I/O174 NX6	I/O172 NX4	I/O191 PX7	I/O186 PX2	I/O1 A1	I/O3 A3	CLK0	I/O17 C1	I/O21 C5	I/O23 C7	I/O10 B2	I/O12 B4	A
B	I/O157 KX5	I/O158 KX6	I/O182 OX6	I/O179 OX3	I/O175 NX7	I/O173 NX5	I/O168 NX0	I/O187 PX3	I/O0 A0	I/O5 A5	I/O7 A7	I/O18 C2	I/O8 B0	I/O11 B3	I/O13 B5	N/C	B
C	I/O155 KX3	I/O156 KX4	N/C	I/O183 OX7	I/O178 OX2	I/O170 NX2	I/O171 NX3	I/O189 PX5	I/O184 PX0	I/O6 A6	I/O20 C4	I/O22 C6	I/O15 B7	I/O14 B6	TDI	I/O39 F7	C
D	I/O150 JX6	I/O151 JX7	TDO	GND	GND	VCC	GND	VCC	GND	GND	VCC	GND	VCC	I/O9 B1	I/O38 F6	I/O37 F5	D
E	I/O148 JX4	N/C	I/O154 KX2	VCC	I/O152 KX0	I/O153 KX1	I/O190 PX6	CLK3	I/O188 PX4	I/O2 A2	I/O16 C0	N/C	GND	I/O36 F4	I/O35 F3	I/O47 G7	E
F	I/O144 JX0	I/O149 JX5	I/O147 JX3	GND	I/O146 JX2	I/O145 JX1	I/O176 OX0	I/O169 NX1	I/O185 PX1	I/O4 A4	I/O19 C3	I/O34 F2	VCC	I/O32 F0	I/O46 G6	I/O45 G5	F
G	I/O163 LX3	I/O166 LX6	I/O165 LX5	VCC	I/O164 LX4	I/O167 LX7	VCC	GND	GND	VCC	I/O33 F1	I/O44 G4	GND	I/O42 G2	I/O41 G1	I/O31 E7	G
H	I/O160 LX0	I/O162 LX2	I/O161 LX1	GND	I/O120 EX0	I/O121 EX1	GND	VCC	VCC	GND	I/O43 G3	I/O40 G0	VCC	I/O28 E4	I/O27 E3	I/O26 E2	H
J	I/O122 EX2	I/O123 EX3	I/O124 EX4	GND	I/O126 EX6	I/O125 EX5	GND	VCC	VCC	GND	I/O30 E6	I/O29 E5	GND	I/O65 L1	I/O64 L0	I/O66 L2	J
K	I/O127 EX7	I/O136 GX0	I/O137 GX1	VCC	I/O139 GX3	I/O138 GX2	VCC	GND	GND	VCC	I/O25 E1	I/O24 E0	VCC	I/O71 L7	I/O70 L6	I/O48 J0	K
L	I/O140 GX4	I/O141 GX5	I/O143 GX7	GND	I/O130 FX2	I/O142 GX6	I/O98 AX2	I/O91 P3	I/O75 N3	I/O77 N5	I/O68 L4	I/O67 L3	GND	I/O51 J3	I/O52 J4	I/O49 J1	L
M	I/O128 FX0	I/O129 FX1	I/O131 FX3	GND	I/O115 CX3	I/O113 CX1	I/O100 AX4	I/O90 P2	I/O74 N2	I/O80 O0	I/O83 O3	I/O69 L5	VCC	I/O60 K4	I/O55 J7	I/O50 J2	M
N	I/O132 FX4	I/O133 FX5	I/O135 FX7	VCC	GND	VCC	GND	VCC	GND	GND	VCC	GND	GND	TCK	I/O56 K0	I/O53 J5	N
P	I/O134 FX6	I/O109 BX5	I/O110 BX6	I/O111 BX7	I/O116 CX4	I/O114 CX2	I/O101 AX5	I/O89 P1	I/O93 P5	I/O94 P6	I/O79 N7	I/O84 O4	I/O87 O7	TMS	I/O57 K1	I/O54 J6	P
R	I/O108 BX4	I/O107 BX3	I/O104 BX0	I/O119 CX7	I/O112 CX0	I/O102 AX6	I/O99 AX3	I/O96 AX0	I/O92 P4	I/O72 N0	I/O76 N4	I/O81 O1	I/O85 O5	I/O63 K7	I/O59 K3	I/O58 K2	R
T	I/O106 BX2	I/O105 BX1	I/O118 CX6	I/O117 CX5	I/O103 AX7	CLK2	I/O97 AX1	I/O88 P0	CLK1	I/O95 P7	I/O73 N1	I/O78 N6	I/O82 O2	I/O86 O6	I/O62 K6	I/O61 K5	T
	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

PIN DESIGNATIONS

CLK = Clock
 GND = Ground
 I = Input
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 VCC = Supply Voltage
 TDI = Test Data In
 TCK = Test Clock
 TMS = Test Mode Select
 TDO = Test Data Out



m4a3.512.192_256bga

5V Commercial Combinations		
M4A5-32/32	-5, -7, -10,	JC, VC, VC48
M4A5-64/32	-55, -7, -10	JC, VC, VC48
M4A5-96/48		VC
M4A5-128/64		YC, VC
M4A5-192/96	-6, -7, -10	VC
M4A5-256/128	-65, -7, -10	YC

5V Industrial Combinations		
M4A5-32/32	-7, -10, -12	JJ, VI, VI48
M4A5-64/32	-7, -10, -12	JJ, VI, VI48
M4A5-96/48		VI
M4A5-128/64		YI, VI
M4A5-192/96	-7, -10, -12	VI
M4A5-256/128	-10, -12	YI

Lead-free Packaging

3.3V Commercial Combinations		
M4A3-32/32	-5, -7, -10	VNC, VNC48, JNC
M4A3-64/32	-55, -7, -10	VNC, VNC48, JNC
M4A3-64/64		VNC
M4A3-128/64		VNC
M4A3-192/96	-6, -7, -10	VNC
M4A3-256/128	-55, -7, -10	FANC, YNC
M4A3-256/160	-7, -10	YNC
M4A3-256/192		FANC
M4A3-384/192	-65, -10, -12	FANC
M4A3-512/192	-7, -10, -12	FANC

3.3V Industrial Combinations		
M4A3-32/32	-7, -10, -12	VNI, VNI48, JNI
M4A3-64/32		VNI, VNI48, JNI
M4A3-64/64		VNI
M4A3-128/64		VNI
M4A3-192/96	-10, -12	VNI
M4A3-256/128		FANI, YNI
M4A3-256/160		YNI
M4A3-256/192	-10, -12, -14	FANI
M4A3-384/192		FANI
M4A3-512/192		FANI

5V Commercial Combinations		
M4A5-32/32	-5, -7, -10	VNC, VNC48, JNC
M4A5-64/32	-55, -7, -10	VNC, VNC48, JNC
M4A5-96/48		VNC
M4A5-128/64		VNC, YNC
M4A5-192/96	-6, -7, -10	VNC
M4A5-256/128	-65, -7, -10	YNC

5V Industrial Combinations		
M4A5-32/32	-7, -10, -12	VNI, VNI48, JNI
M4A5-64/32		VNI, VNI48, JNI
M4A5-96/48		VNI
M4A5-128/64		VNI, YNI
M4A5-192/96		VNI
M4A5-256/128		YNI

Most ispMACH devices are dual-marked with both Commercial and Industrial grades. The Industrial speed grade is slower, i.e., M4A3-256/128-7YC-10YI

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local Lattice sales office to confirm availability of specific valid combinations and to check on newly released combinations.