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## Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

## Applications of Embedded - CPLDs

### Details

Product Status	Not For New Designs
Programmable Type	In System Programmable
Delay Time tpd(1) Max	10 ns
Voltage Supply - Internal	4.75V ~ 5.25V
Number of Logic Elements/Blocks	-
Number of Macrocells	64
Number of Gates	-
Number of I/O	32
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-TQFP (7x7)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/lattice-semiconductor/m4a5-64-32-10vnc48">https://www.e-xfl.com/product-detail/lattice-semiconductor/m4a5-64-32-10vnc48</a>

**Table 1. ispMACH 4A Device Features**

<b>3.3 V Devices</b>								
<b>Feature</b>	<b>M4A3-32</b>	<b>M4A3-64</b>	<b>M4A3-96</b>	<b>M4A3-128</b>	<b>M4A3-192</b>	<b>M4A3-256</b>	<b>M4A3-384</b>	<b>M4A3-512</b>
Macrocells	32	64	96	128	192	256	384	512
User I/O options	32	32/64	48	64	96	128/160/192	160/192	160/192/256
$t_{PD}$ (ns)	5.0	5.5	5.5	5.5	6.0	5.5	6.5	7.5
$f_{CNT}$ (MHz)	182	167	167	167	160	167	154	125
$t_{COS}$ (ns)	4.0	4.0	4.0	4.0	4.5	4.0	4.5	5.5
$t_{SS}$ (ns)	3.0	3.5	3.5	3.5	3.5	3.5	3.5	5.0
Static Power (mA)	20	25/52	40	55	85	110/150	149/155	179
JTAG Compliant	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
PCI Compliant	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes

<b>5 V Devices</b>						
<b>Feature</b>	<b>M4A5-32</b>	<b>M4A5-64</b>	<b>M4A5-96</b>	<b>M4A5-128</b>	<b>M4A5-192</b>	<b>M4A5-256</b>
Macrocells	32	64	96	128	192	256
User I/O options	32	32	48	64	96	128
$t_{PD}$ (ns)	5.0	5.5	5.5	5.5	6.0	6.5
$f_{CNT}$ (MHz)	182	167	167	167	160	154
$t_{COS}$ (ns)	4.0	4.0	4.0	4.0	4.5	5.0
$t_{SS}$ (ns)	3.0	3.5	3.5	3.5	3.5	3.5
Static Power (mA)	20	25	40	55	74	110
JTAG Compliant	Yes	Yes	Yes	Yes	Yes	Yes
PCI Compliant	Yes	Yes	Yes	Yes	Yes	Yes

The ispMACH 4A family offers 20 density-I/O combinations in Thin Quad Flat Pack (TQFP), Plastic Quad Flat Pack (PQFP), Plastic Leaded Chip Carrier (PLCC), Ball Grid Array (BGA), fine-pitch BGA (fpBGA), and chip-array BGA (caBGA) packages ranging from 44 to 388 pins (Table 3). It also offers I/O safety features for mixed-voltage designs so that the 3.3-V devices can accept 5-V inputs, and 5-V devices do not overdrive 3.3-V inputs. Additional features include Bus-Friendly inputs and I/Os, a programmable power-down mode for extra power savings and individual output slew rate control for the highest speed transition or for the lowest noise transition.

**Table 3. ispMACH 4A Package and I/O Options (Number of I/Os and dedicated inputs in Table)**

3.3 V Devices								
Package	M4A3-32	M4A3-64	M4A3-96	M4A3-128	M4A3-192	M4A3-256	M4A3-384	M4A3-512
44-pin PLCC	32+2	32+2						
44-pin TQFP	32+2	32+2						
48-pin TQFP	32+2	32+2						
100-pin TQFP		64+6	48+8	64+6				
100-pin PQFP				64+6				
100-ball caBGA				64+6				
144-pin TQFP					96+16			
144-ball fpBGA					96+16			
208-pin PQFP						128+14, 160	160	160
256-ball fpBGA						128+14, 192	192	192
256-ball BGA						128+14	192	
388-ball fpBGA								256

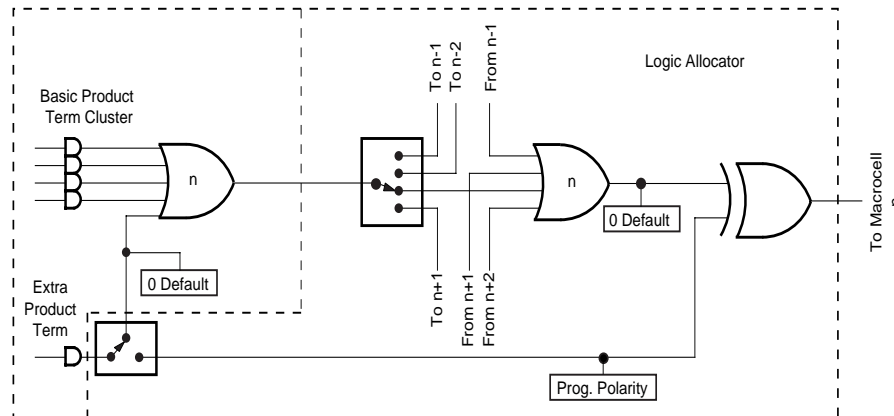
5 V Devices						
Package	M4A5-32	M4A5-64	M4A5-96	M4A5-128	M4A5-192	M4A5-256
44-pin PLCC	32+2	32+2				
44-pin TQFP	32+2	32+2				
48-pin TQFP	32+2	32+2				
100-pin TQFP			48+8	64+6		
100-pin PQFP				64+6		
144-pin TQFP					96+16	
208-pin PQFP						128+14

**Table 6. Logic Allocator for All ispMACH 4A Devices (except M4A(3,5)-32/32)**

Output Macrocell	Available Clusters	Output Macrocell	Available Clusters
M <sub>0</sub>	C <sub>0</sub> , C <sub>1</sub> , C <sub>2</sub>	M <sub>8</sub>	C <sub>7</sub> , C <sub>8</sub> , C <sub>9</sub> , C <sub>10</sub>
M <sub>1</sub>	C <sub>0</sub> , C <sub>1</sub> , C <sub>2</sub> , C <sub>3</sub>	M <sub>9</sub>	C <sub>8</sub> , C <sub>9</sub> , C <sub>10</sub> , C <sub>11</sub>
M <sub>2</sub>	C <sub>1</sub> , C <sub>2</sub> , C <sub>3</sub> , C <sub>4</sub>	M <sub>10</sub>	C <sub>9</sub> , C <sub>10</sub> , C <sub>11</sub> , C <sub>12</sub>
M <sub>3</sub>	C <sub>2</sub> , C <sub>3</sub> , C <sub>4</sub> , C <sub>5</sub>	M <sub>11</sub>	C <sub>10</sub> , C <sub>11</sub> , C <sub>12</sub> , C <sub>13</sub>
M <sub>4</sub>	C <sub>3</sub> , C <sub>4</sub> , C <sub>5</sub> , C <sub>6</sub>	M <sub>12</sub>	C <sub>11</sub> , C <sub>12</sub> , C <sub>13</sub> , C <sub>14</sub>
M <sub>5</sub>	C <sub>4</sub> , C <sub>5</sub> , C <sub>6</sub> , C <sub>7</sub>	M <sub>13</sub>	C <sub>12</sub> , C <sub>13</sub> , C <sub>14</sub> , C <sub>15</sub>
M <sub>6</sub>	C <sub>5</sub> , C <sub>6</sub> , C <sub>7</sub> , C <sub>8</sub>	M <sub>14</sub>	C <sub>13</sub> , C <sub>14</sub> , C <sub>15</sub>
M <sub>7</sub>	C <sub>6</sub> , C <sub>7</sub> , C <sub>8</sub> , C <sub>9</sub>	M <sub>15</sub>	C <sub>14</sub> , C <sub>15</sub>

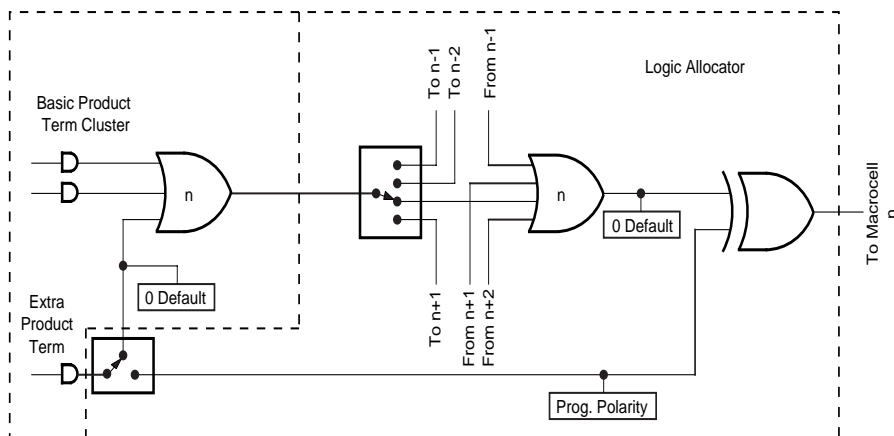
**Table 7. Logic Allocator for M4A(3,5)-32/32**

Output Macrocell	Available Clusters	Output Macrocell	Available Clusters
M <sub>0</sub>	C <sub>0</sub> , C <sub>1</sub> , C <sub>2</sub>	M <sub>8</sub>	C <sub>8</sub> , C <sub>9</sub> , C <sub>10</sub>
M <sub>1</sub>	C <sub>0</sub> , C <sub>1</sub> , C <sub>2</sub> , C <sub>3</sub>	M <sub>9</sub>	C <sub>8</sub> , C <sub>9</sub> , C <sub>10</sub> , C <sub>11</sub>
M <sub>2</sub>	C <sub>1</sub> , C <sub>2</sub> , C <sub>3</sub> , C <sub>4</sub>	M <sub>10</sub>	C <sub>9</sub> , C <sub>10</sub> , C <sub>11</sub> , C <sub>12</sub>
M <sub>3</sub>	C <sub>2</sub> , C <sub>3</sub> , C <sub>4</sub> , C <sub>5</sub>	M <sub>11</sub>	C <sub>10</sub> , C <sub>11</sub> , C <sub>12</sub> , C <sub>13</sub>
M <sub>4</sub>	C <sub>3</sub> , C <sub>4</sub> , C <sub>5</sub> , C <sub>6</sub>	M <sub>12</sub>	C <sub>11</sub> , C <sub>12</sub> , C <sub>13</sub> , C <sub>14</sub>
M <sub>5</sub>	C <sub>4</sub> , C <sub>5</sub> , C <sub>6</sub> , C <sub>7</sub>	M <sub>13</sub>	C <sub>12</sub> , C <sub>13</sub> , C <sub>14</sub> , C <sub>15</sub>
M <sub>6</sub>	C <sub>5</sub> , C <sub>6</sub> , C <sub>7</sub>	M <sub>14</sub>	C <sub>13</sub> , C <sub>14</sub> , C <sub>15</sub>
M <sub>7</sub>	C <sub>6</sub> , C <sub>7</sub>	M <sub>15</sub>	C <sub>14</sub> , C <sub>15</sub>



**a. Synchronous Mode**

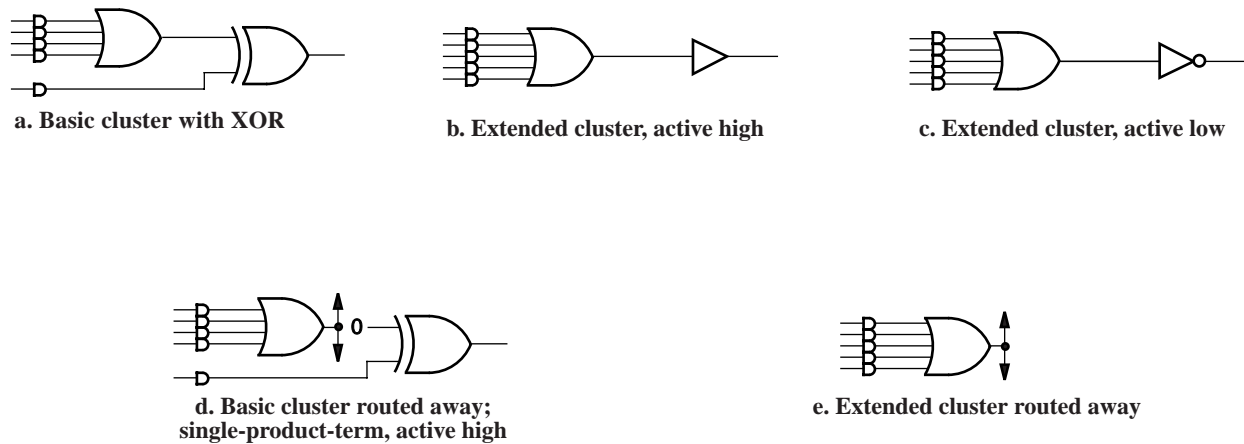
17466G-005



**b. Asynchronous Mode**

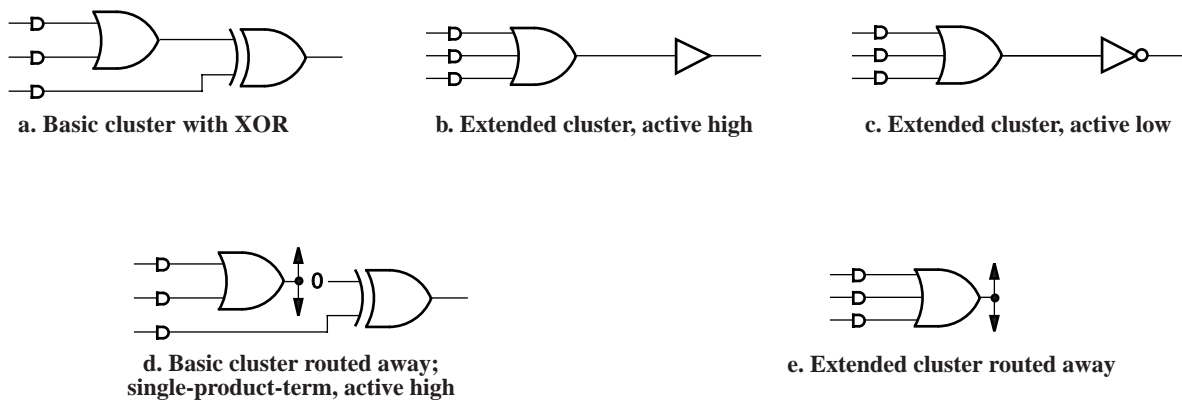
17466G-006

**Figure 2. Logic Allocator: Configuration of Cluster “n” Set by Mode of Macrocell “n”**



17466G-007

**Figure 3. Logic Allocator Configurations: Synchronous Mode**



17466G-008

**Figure 4. Logic Allocator Configurations: Asynchronous Mode**

Note that the configuration of the logic allocator has absolutely no impact on the speed of the signal. All configurations have the same delay. This means that designers do not have to decide between optimizing resources or speed; both can be optimized.

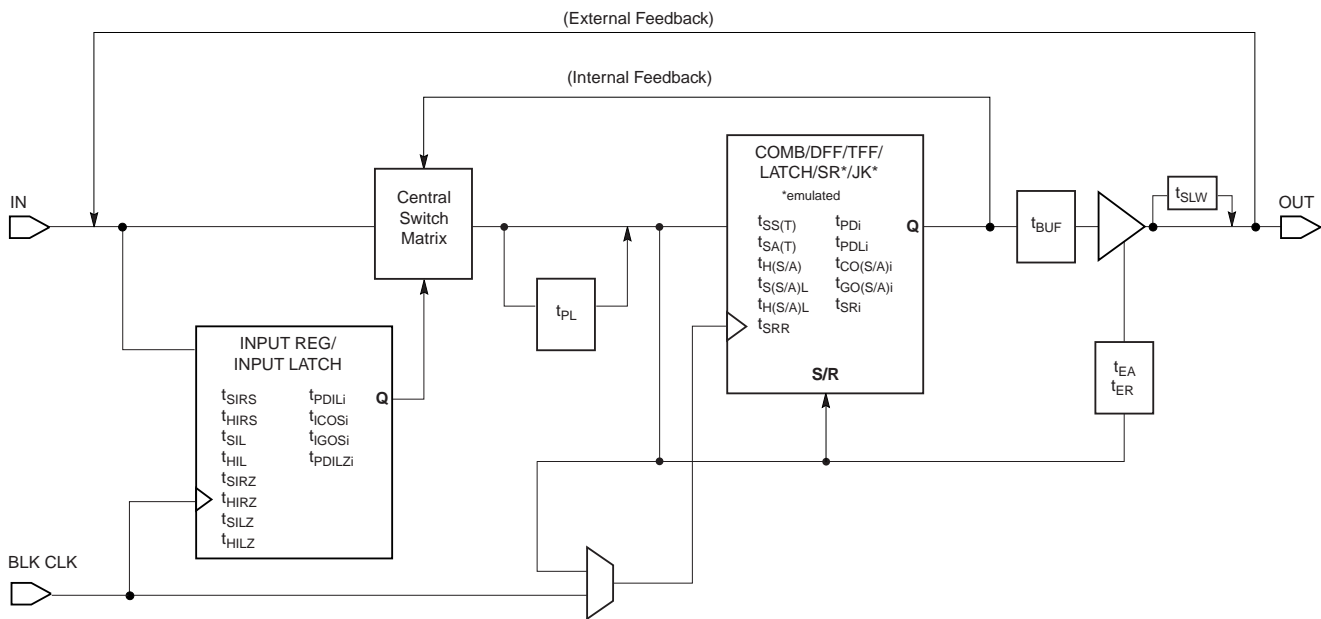
If not used in the cluster, the extra product term can act in conjunction with the basic cluster to provide XOR logic for such functions as data comparison, or it can work with the D-,T-type flip-flop to provide for J-K, and S-R register operation. In addition, if the basic cluster is routed to another macrocell, the extra product term is still available for logic. In this case, the first XOR input will be a logic 0. This circuit has the flexibility to route product terms elsewhere without giving up the use of the macrocell.

Product term clusters do not “wrap” around a PAL block. This means that the macrocells at the ends of the block have fewer product terms available.

## ispMACH 4A TIMING MODEL

The primary focus of the ispMACH 4A timing model is to accurately represent the timing in a ispMACH 4A device, and at the same time, be easy to understand. This model accurately describes all combinatorial and registered paths through the device, making a distinction between internal feedback and external feedback. A signal uses internal feedback when it is fed back into the switch matrix or block without having to go through the output buffer. The input register specifications are also reported as internal feedback. When a signal is fed back into the switch matrix after having gone through the output buffer, it is using external feedback.

The parameter,  $t_{BUF}$ , is defined as the time it takes to go from feedback through the output buffer to the I/O pad. If a signal goes to the internal feedback rather than to the I/O pad, the parameter designator is followed by an “i”. By adding  $t_{BUF}$  to this internal parameter, the external parameter is derived. For example,  $t_{PD} = t_{PDi} + t_{BUF}$ . A diagram representing the modularized ispMACH 4A timing model is shown in Figure 15. Refer to the application note entitled *MACH 4 Timing and High Speed Design* for a more detailed discussion about the timing parameters.



17466G-025

Figure 15. ispMACH 4A Timing Model

## SPEEDLOCKING FOR GUARANTEED FIXED TIMING

The ispMACH 4A architecture allows allocation of up to 20 product terms to an individual macrocell with the assistance of an XOR gate without incurring additional timing delays.

The design of the switch matrix and PAL blocks guarantee a fixed pin-to-pin delay that is independent of the logic required by the design. Other competitive CPLDs incur serious timing delays as product terms expand beyond their typical 4 or 5 product term limits. Speed *and* SpeedLocking combine to give designs easy access to the performance required in today's designs.

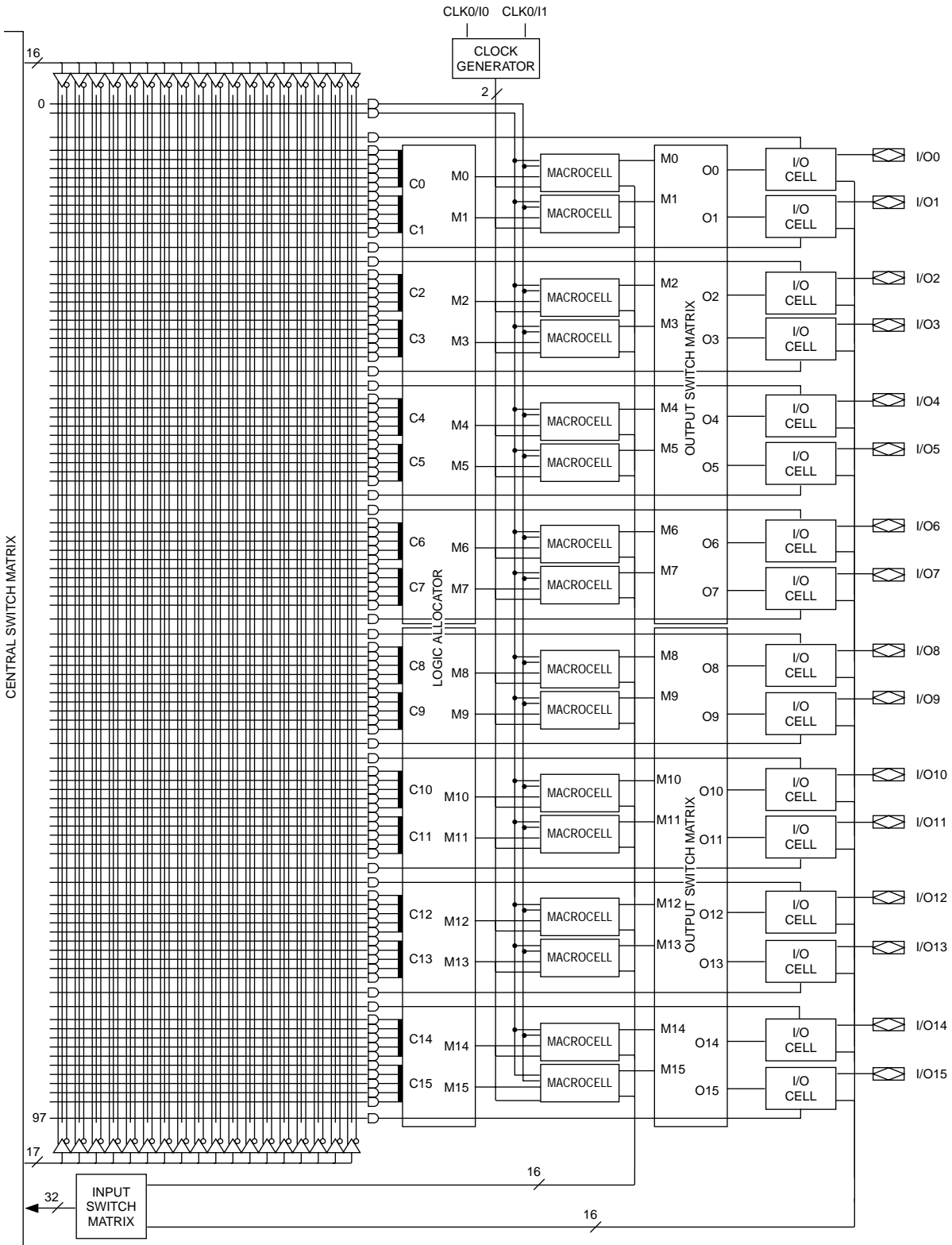
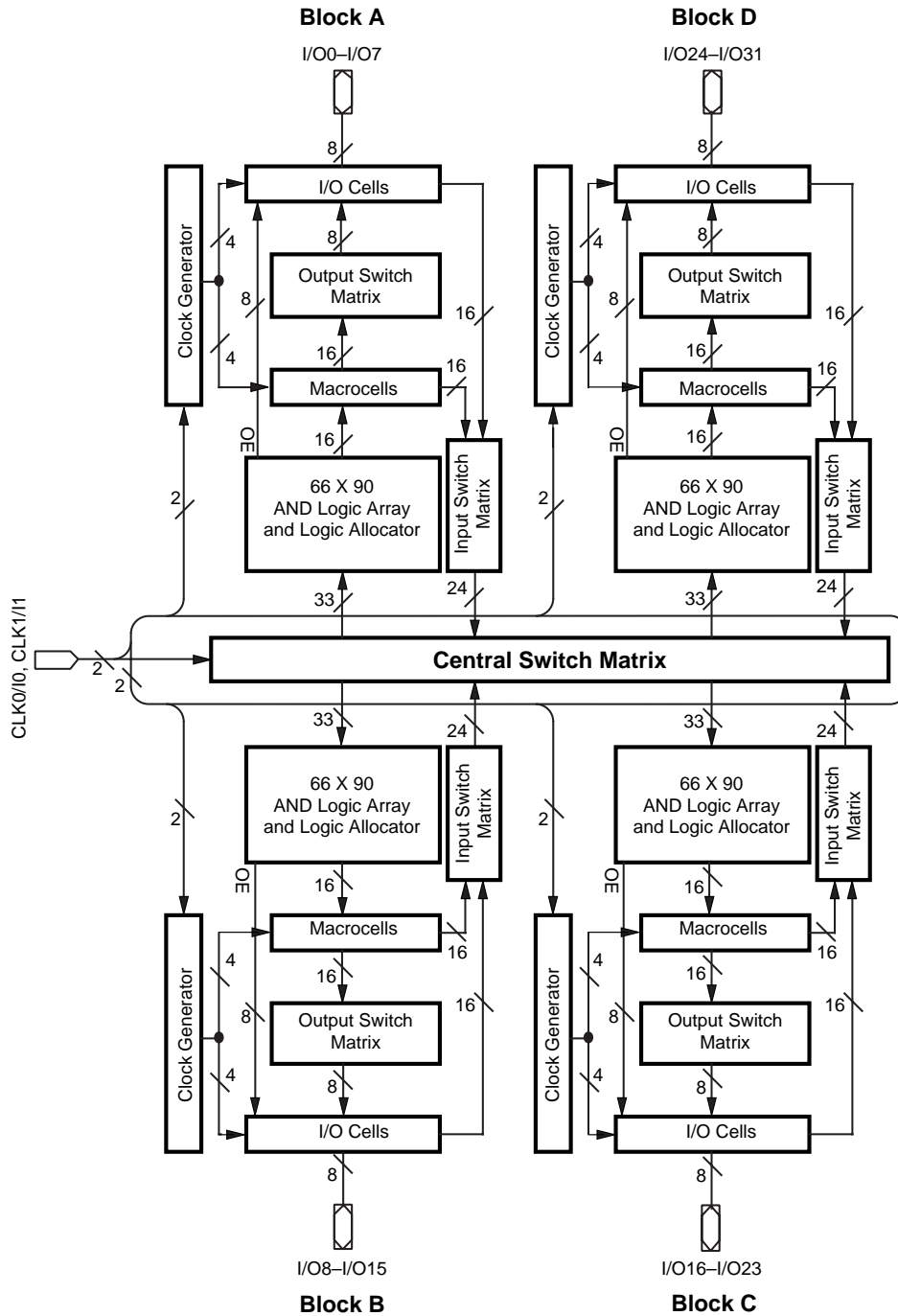


Figure 18. PAL Block for M4A (3,5)-32/32

17466H-042

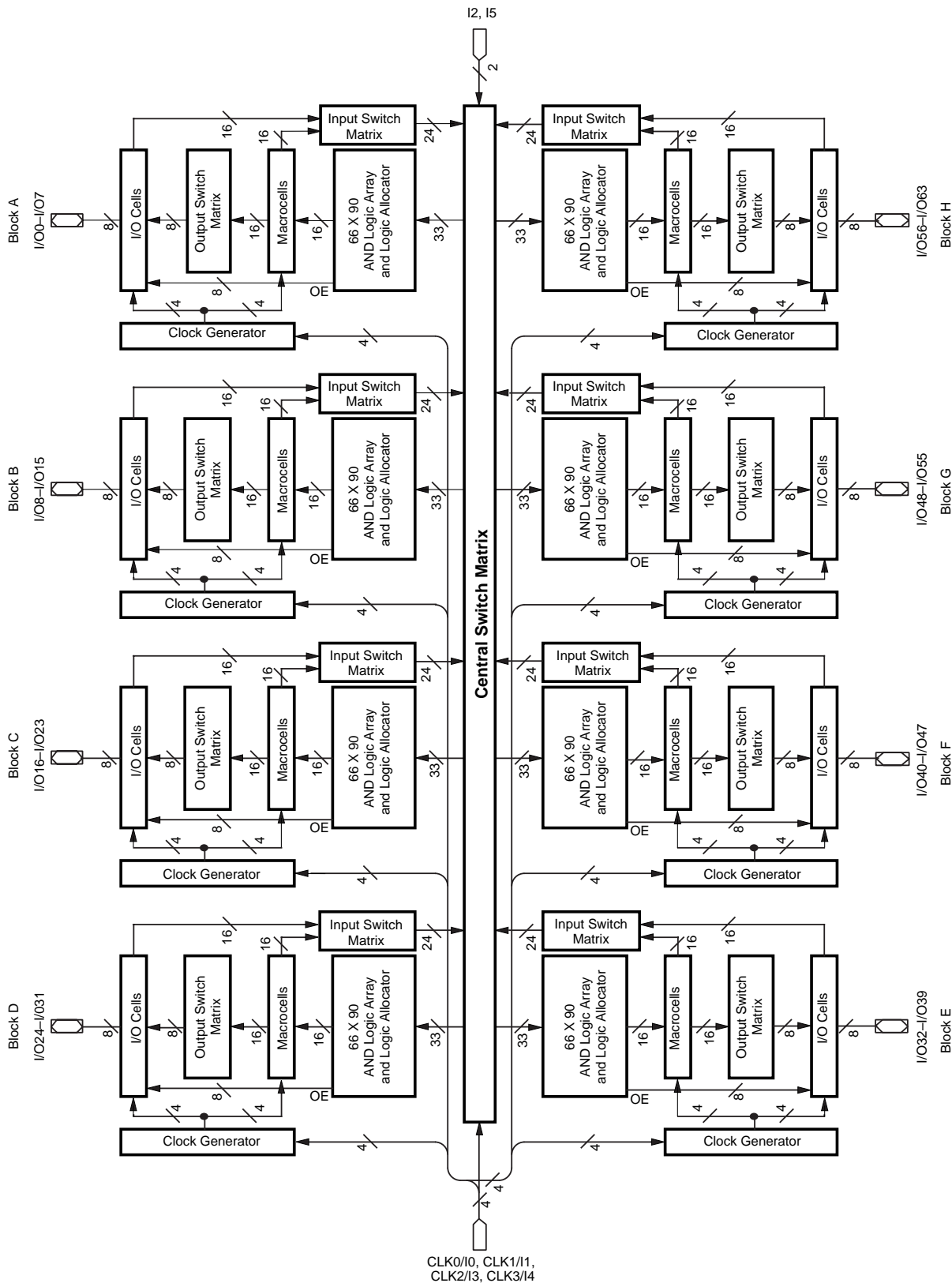
## BLOCK DIAGRAM – M4A(3,5)-64/32



17466H-020

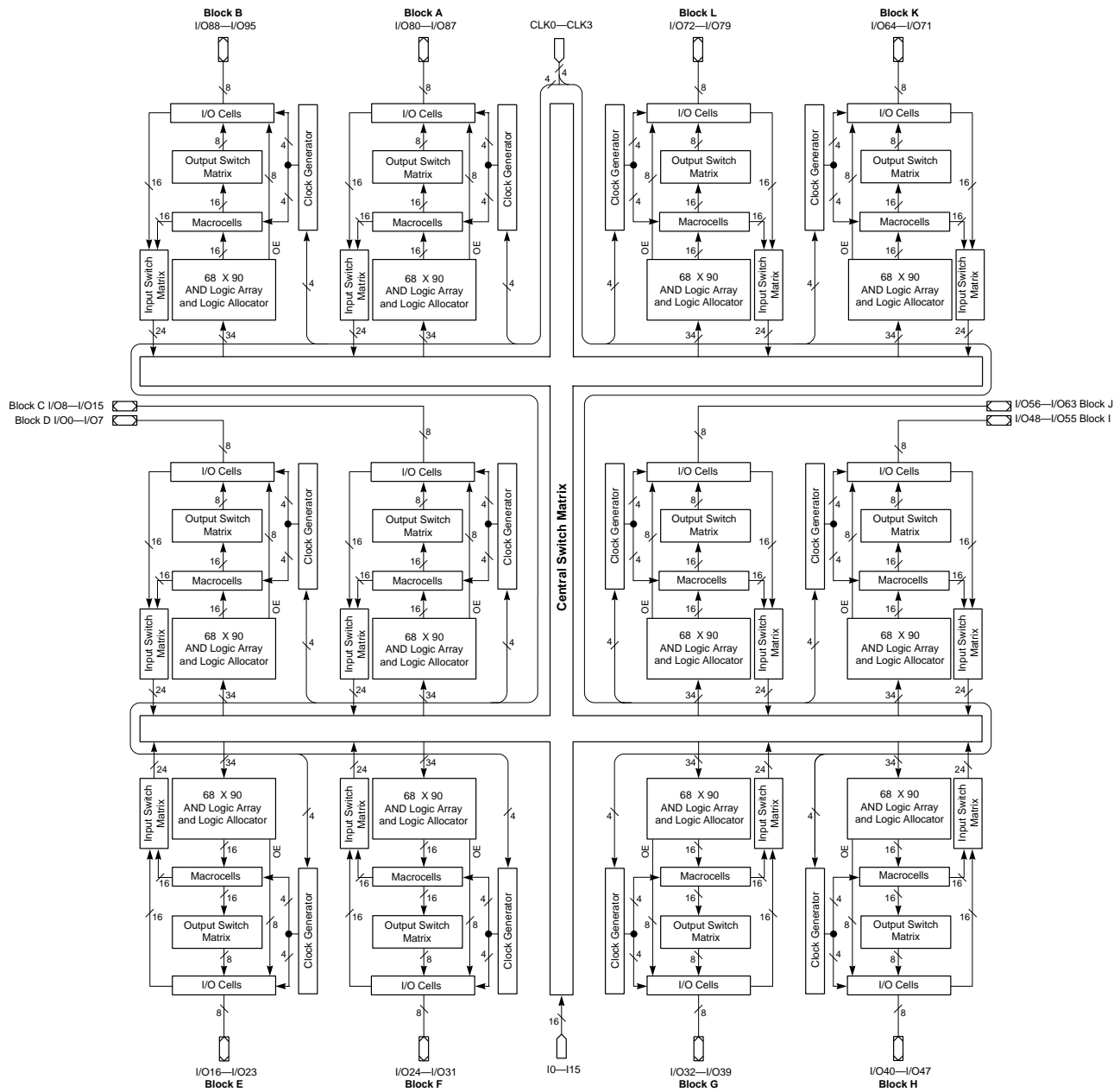


# BLOCK DIAGRAM – M4A(3,5)-128/64



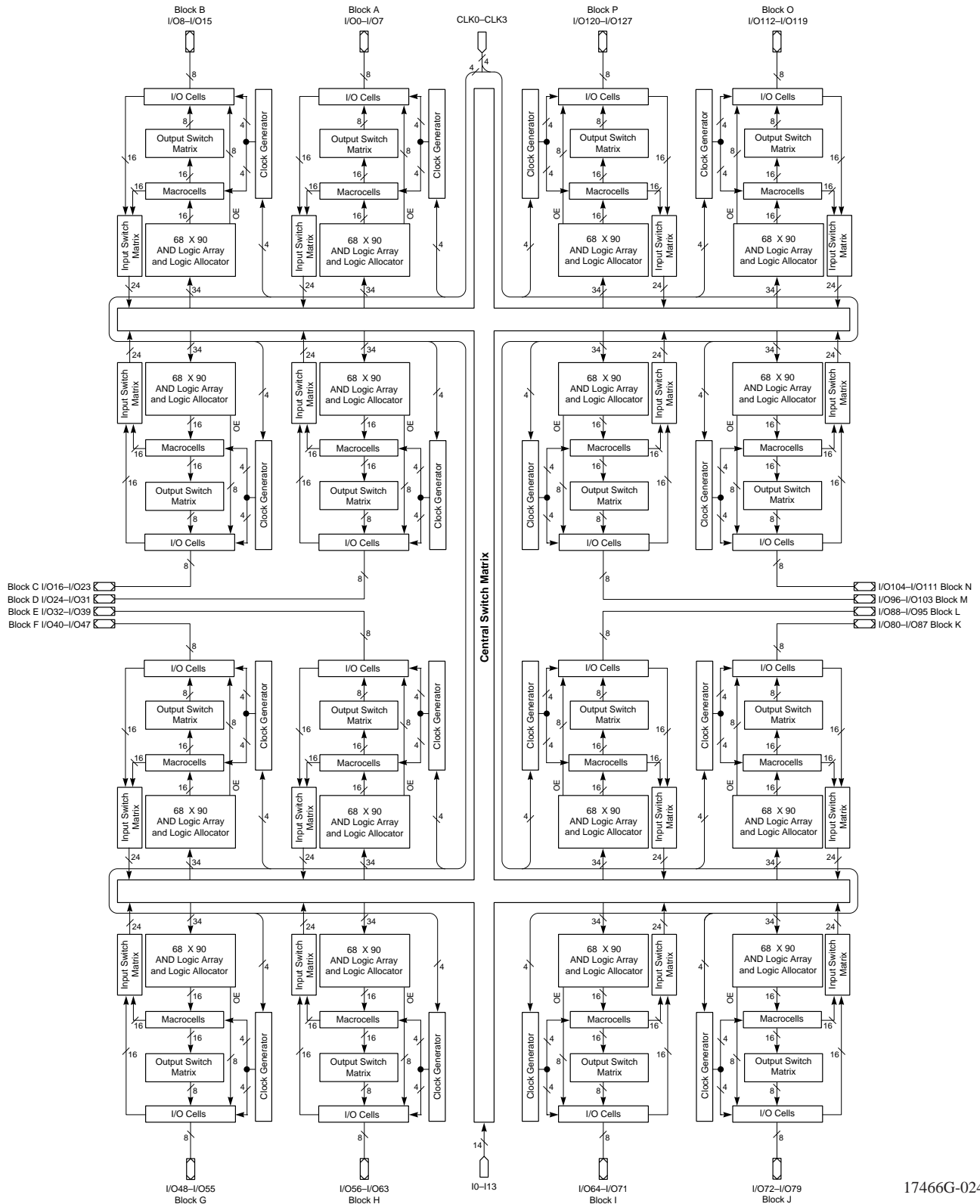
17466H-022

# BLOCK DIAGRAM – M4A(3,5)-192/96



17466G-067

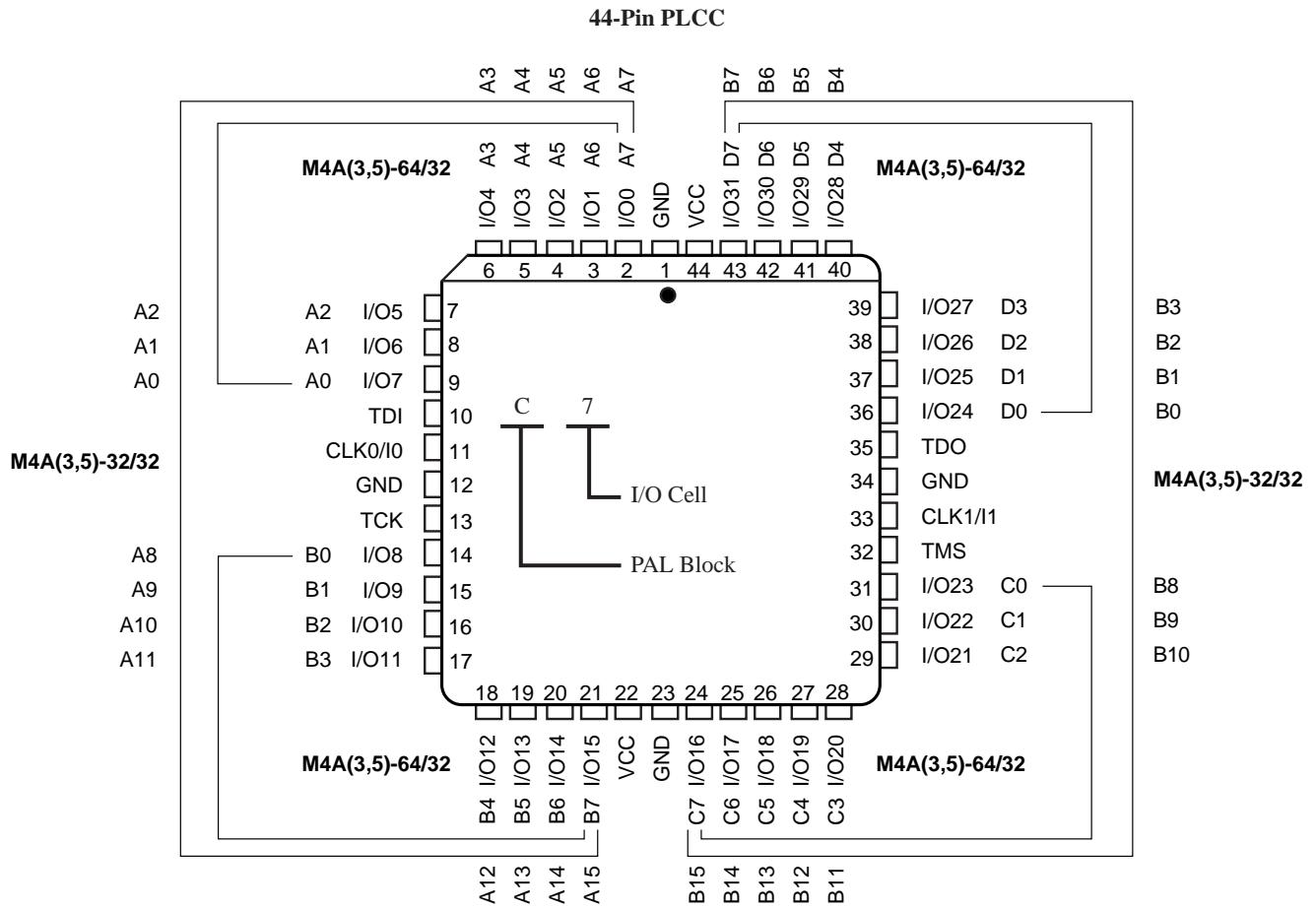
# BLOCK DIAGRAM – M4A(3,5)-256/128



17466G-024

## 44-PIN PLCC CONNECTION DIAGRAM (M4A(3,5)-32/32 AND M4A(3,5)-64/32)

### Top View



## PIN DESIGNATIONS

CLK/I = Clock or Input

GND = Ground

I/O = Input/Output

V<sub>CC</sub> = Supply Voltage

TDI = Test Data In

TCK = Test Clock

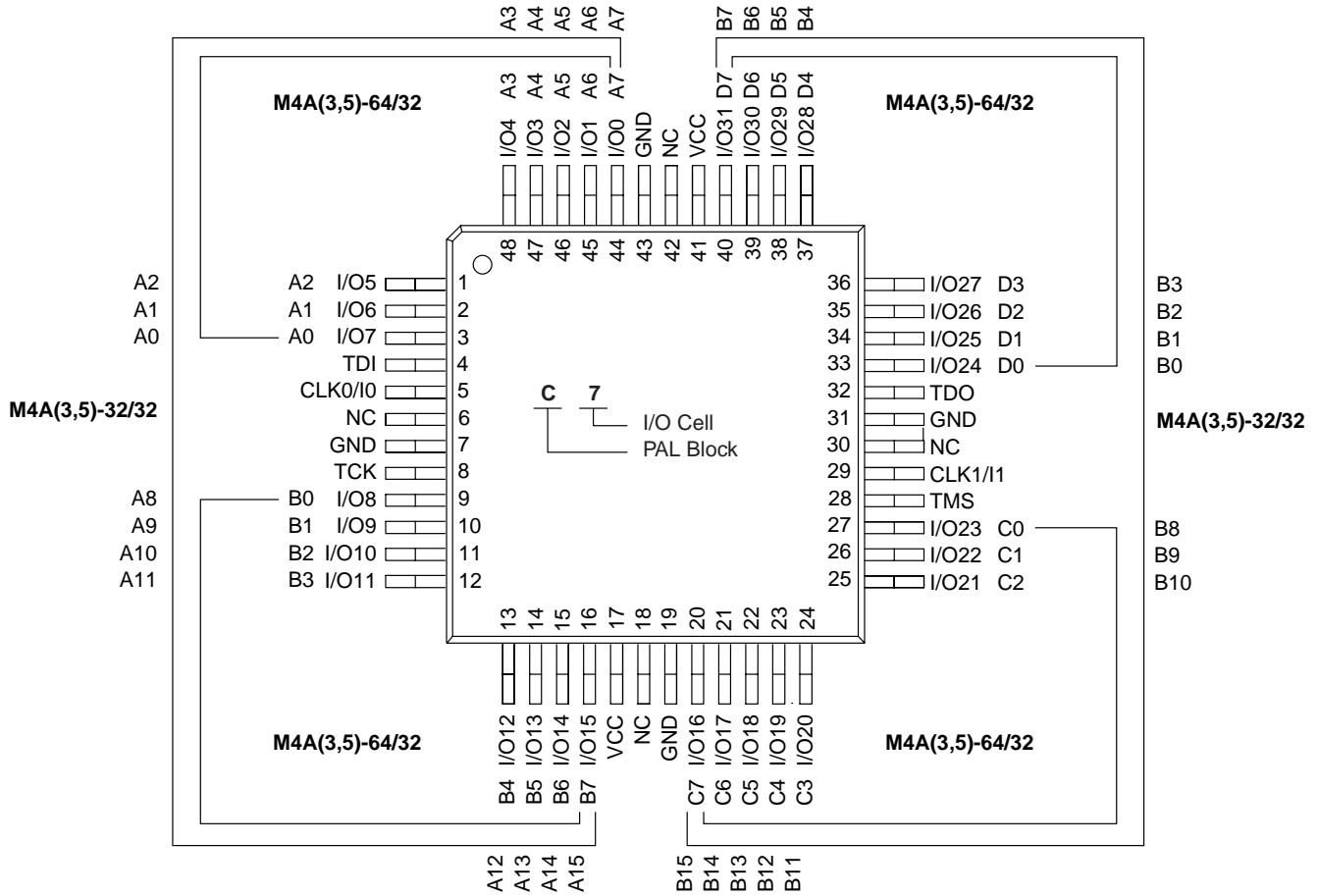
TMS = Test Mode Select

TDO = Test Data Out

# 48-PIN TQFP CONNECTION DIAGRAM (M4A(3,5)-32/32 AND M4A(3,5)-64/32)

## Top View

48-Pin TQFP (1.4mm Thickness)



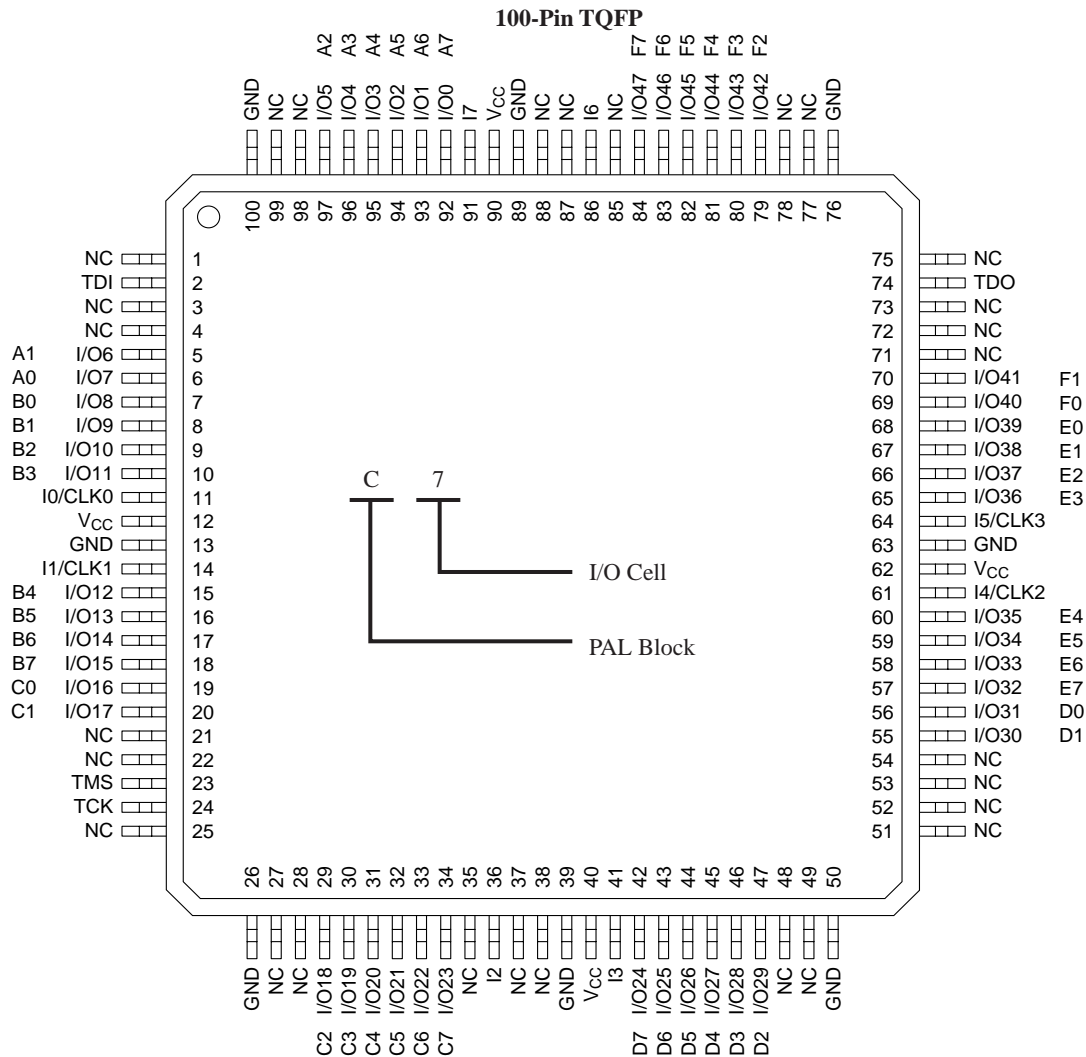
17466G-028

## PIN DESIGNATIONS

- CLK/I = Clock or Input
- GND = Ground
- I/O = Input/Output
- V<sub>CC</sub> = Supply Voltage
- NC = No Connect
- TDI = Test Data In
- TCK = Test Clock
- TMS = Test Mode Select
- TDO = Test Data Out

## 100-PIN TQFP CONNECTION DIAGRAM (M4A(3,5)-96/48)

### Top View

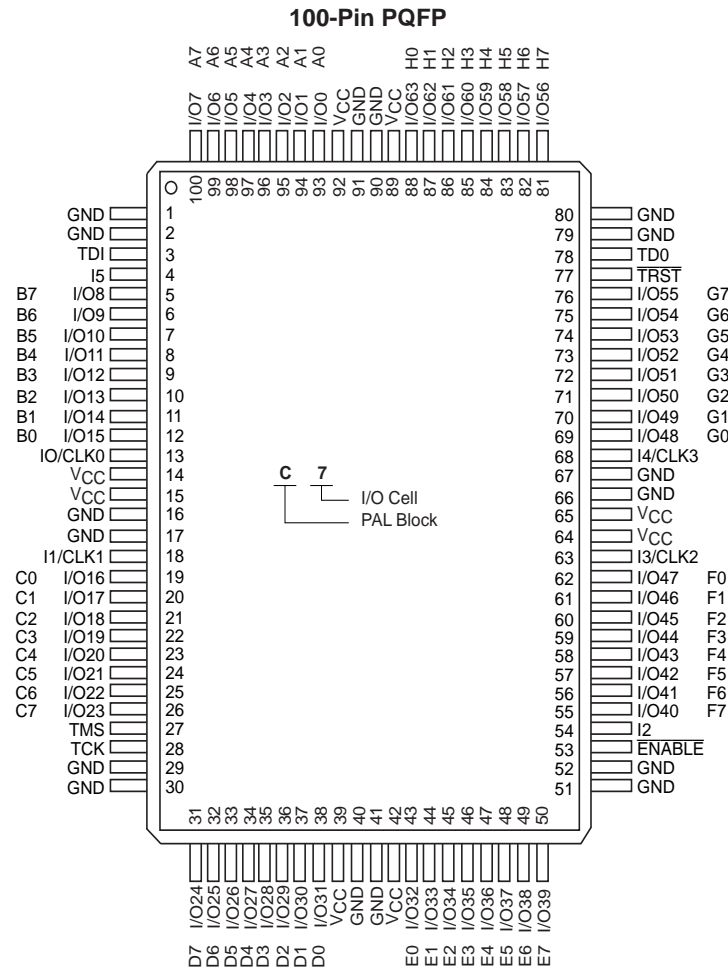


## PIN DESIGNATIONS

- CLK/I = Clock or Input
- GND = Ground
- I = Input
- I/O = Input/Output
- V<sub>CC</sub> = Supply Voltage
- NC = No Connect
- TDI = Test Data In
- TCK = Test Clock
- TMS = Test Mode Select
- TDO = Test Data Out

## 100-PIN PQFP CONNECTION DIAGRAM (M4A(3,5)-128/64)

### Top View



### PIN DESIGNATIONS

I/CLK = Input or Clock

GND = Ground

I = Input

I/O = Input/Output

V<sub>CC</sub> = Supply Voltage

TDI = Test Data In

TCK = Test Clock

TMS = Test Mode Select

TDO = Test Data Out

TRST = Test Reset

ENABLE = Program

# 144-BALL FPBGA CONNECTION DIAGRAM (M4A3-192/96)

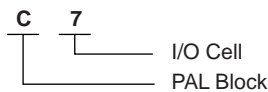
## Bottom View

144-Ball fpBGA

	12	11	10	9	8	7	6	5	4	3	2	1	
A	GND	I/O72 L7	I/O76 L3	I13	GBCLK3	I0	I/O82 A2	I/O86 A6	I/O88 B0	I/O93 B5	I/O95 B7	GND	A
B	GND	I/O73 L6	I/O77 L2	I/O79 L0	VCC	I1	I/O83 A3	I/O87 A7	I/O90 B2	I/O94 B6	I/O0 D7	TDI	B
C	GND	TD0	I/O74 L5	I14	GND	I/O80 A0	I/O84 A4	GND	I/O92 B4	I/O1 D6	I/O4 D3	I/O3 D4	C
D	I/O67 K4	I/O69 K2	I/O71 K0	I/O75 L4	GBCLK0	I/O81 A1	VCC	I/O91 B3	I/O2 D5	I2	I/O6 D1	I/O7 D0	D
E	I12	I/O64 K7	I/O66 K5	I/O70 K1	I/O78 L1	I/O85 A5	I/O89 B1	I/O5 D2	I/O8 C7	I4	GND	VCC	E
F	I10	I11	GND	I/O65 K6	I/O68 K3	I15	I3	GND	I/O12 C3	I/O11 C4	I/O10 C5	I/O9 C6	F
G	I/O60 J3	I/O61 J2	I/O62 J1	I/O63 J0	VCC	GND	I7	I/O20 E3	I/O17 E6	I/O15 C0	I/O14 C1	I/O13 C2	G
H	I/O56 J7	I/O57 J6	I/O58 J5	I/O59 J4	I/O53 I2	I/O41 H1	I/O37 G5	I/O30 F1	I/O22 E1	I/O18 E5	I/O16 E7	VCC	H
J	I/O55 I0	I/O54 I1	VCC	I/O50 I5	I/O43 H3	VCC	I/O33 G1	GBCLK2	I/O27 F4	I/O23 E0	I/O21 E2	I/O19 E4	J
K	I/O51 I4	I/O52 I3	I/O49 I6	I/O44 H4	GND	I/O36 G4	I/O32 G0	VCC	I6	I/O26 F5	TCK	TMS	K
L	GND	I/O48 I7	I/O46 H6	I/O42 H2	I/O39 G7	I/O35 G3	I9	GND	I/O31 F0	I/O29 F2	I/O25 F6	GND	L
M	GND	I/O47 H7	I/O45 H5	I/O40 H0	I/O38 G6	I/O34 G2	I8	GBCLK1	I5	I/O28 F3	I/O24 F7	GND	M
	12	11	10	9	8	7	6	5	4	3	2	1	

### PIN DESIGNATIONS

- CLK = Clock
- GND = Ground
- I = Input
- I/O = Input/Output
- N/C = No Connect
- VCC = Supply Voltage
- TDI = Test Data In
- TCK = Test Clock
- TMS = Test Mode Select
- TD0 = Test Data Out

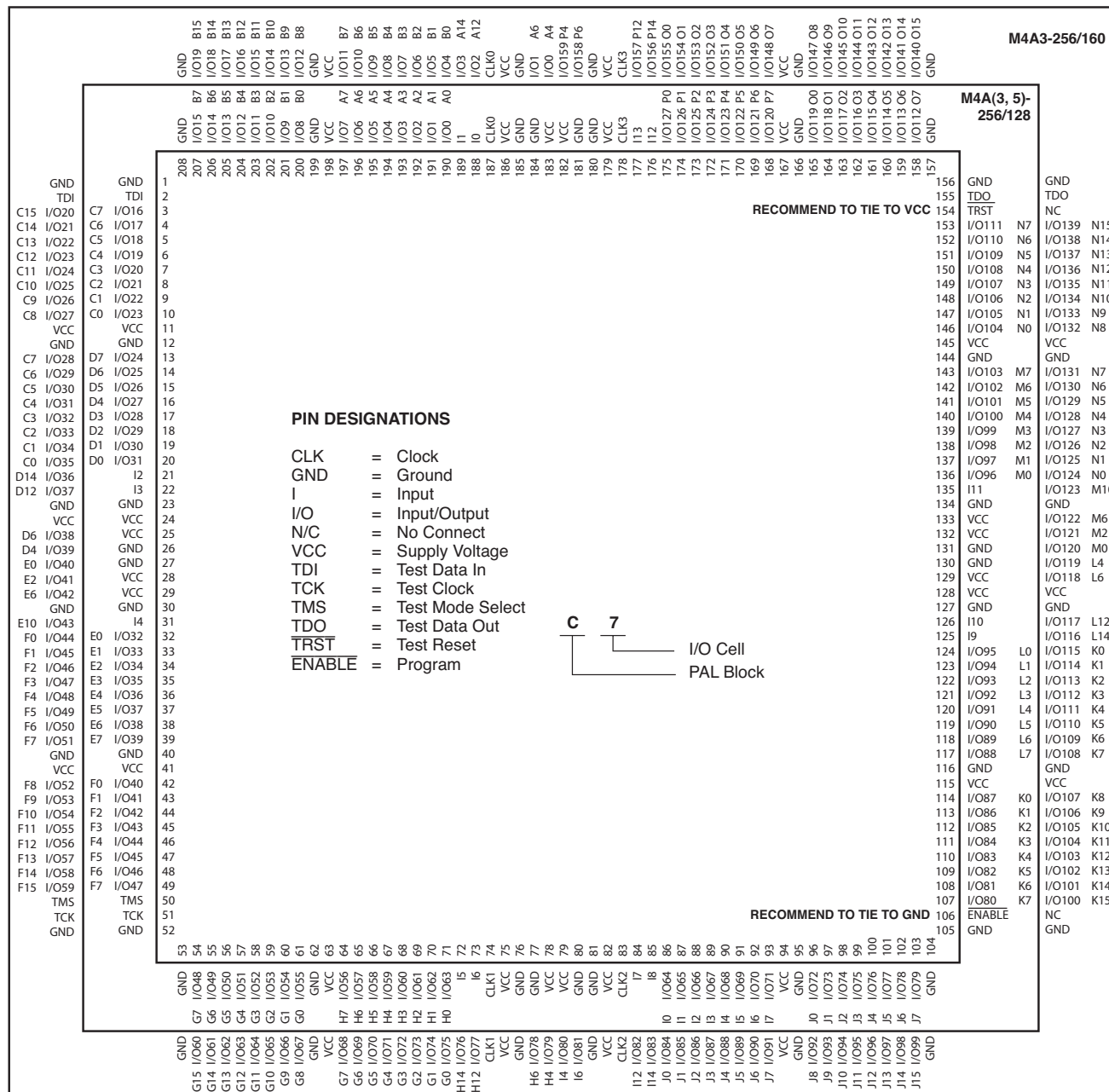




# 208-PIN PQFP CONNECTION DIAGRAM (M4A(3,5)-256/128 AND M4A3-256/160)

Top View

208-Pin PQFP



17466G-044

# 256-BALL BGA CONNECTION DIAGRAM - (M4A3-384/192)

## Bottom View

### 256-Ball BGA

	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1		
A	GND	I/O11 FX7	GND	I/O44 FX6	I/O58 CX6	GND	I/O70 CX2	I/O76 DX6	GND	GND	GND	GND	I/O108 AX5	I/O116 BX0	GND	I/O128 BX7	I/O134 O3	GND	GND	GND	A	
B	GND	I/O12 GX7	I/O28 FX5	I/O45 FX3	I/O59 CX7	I/O64 CX5	I/O71 CX3	I/O77 DX7	I/O84 DX5	I/O90 DX2	I/O96 AX0	I/O102 AX3	I/O109 AX6	I/O117 BX1	I/O122 BX4	I/O129 BX6	I/O135 O4	I/O148 O6	I/O164 O7	GND	B	
C	I/O0 GX6	I/O13 GX5	VCC	I/O46 FX4	I/O60 FX2	I/O65 FX1	I/O72 CX4	I/O78 CX0	I/O85 DX4	I/O91 DX1	I/O97 AX1	I/O103 AX4	I/O110 BX2	I/O118 BX5	I/O123 O0	I/O130 O1	I/O136 O5	VCC	I/O165 N7	I/O181 N6	C	
D	I/O1 EX7	I/O14 GX3	I/O29 GX4	VCC	VCC	I/O66 FX0	VCC	I/O79 CX1	I/O86 DX3	I/O92 DX0	I/O98 AX2	I/O104 AX7	I/O111 BX3	VCC	I/O124 O2	VCC	VCC	VCC	I/O149 N4	I/O166 N5	I/O182 P7	D
E	I/O2 EX0	I/O15 GX0	I/O30 GX1	TDI	<p style="text-align: center;"><b>PIN DESIGNATIONS</b></p> <p>           CLK = Clock            GND = Ground            I = Input            I/O = Input/Output            N/C = No Connect            VCC = Supply Voltage            TDI = Test Data In            TCK = Test Clock            TMS = Test Mode Select            TDO = Test Data Out         </p>												TDO	I/O150 N2	I/O167 N3	I/O183 P6	E	
F	GND	I/O16 EX1	I/O31 EX6	I/O47 GX2													I/O137 N1	I/O151 N0	I/O168 P5	GND	F	
G	I/O3 HX6	I/O17 EX4	I/O32 EX5	VCC													VCC	I/O152 P4	I/O169 P3	I/O184 M7	G	
H	GND	I/O18 HX5	I/O33 EX2	I/O48 EX3													I/O138 P2	I/O153 P1	I/O170 P0	GND	H	
J	I/O4 HX0	I/O19 HX1	I/O34 HX4	I/O49 HX7													I/O139 M6	I/O154 M5	I/O171 M4	I/O185 M3	J	
K	GND	CLK3	I/O35 HX2	I/O50 HX3													I/O140 M0	I/O155 M1	CLK2	I/O186 M2	K	
L	I/O5 A2	CLK0	I/O36 A0	I/O51 A1													I/O141 L3	I/O156 L4	CLK1	GND	L	
M	I/O6 A4	I/O20 A3	I/O37 A5	I/O52 A6													I/O142 L6	I/O157 L5	I/O172 L0	I/O187 L1	M	
N	GND	I/O21 A7	I/O38 D0	I/O53 D1													I/O143 I5	I/O158 I0	I/O173 L7	GND	N	
P	I/O7 D2	I/O22 D3	I/O39 D4	VCC													VCC	I/O159 I4	I/O174 I1	I/O188 L2	P	
R	GND	I/O23 D5	I/O40 D6	I/O54 D7	I/O144 K5	I/O160 K0	I/O175 I3	GND	R													
T	I/O8 B3	I/O24 B0	I/O41 B7	TCK	TMS	I/O161 K4	I/O176 K1	I/O189 I2	T													
U	I/O9 B4	I/O25 B1	I/O42 B6	VCC	VCC	I/O67 C0	VCC	I/O80 F0	I/O87 E5	I/O93 E2	I/O99 H2	I/O105 H5	I/O112 G0	VCC	I/O125 J1	VCC	VCC	I/O162 K7	I/O177 K2	I/O190 I6	U	
V	I/O10 B5	I/O26 B2	VCC	I/O55 C5	I/O61 C2	I/O68 C1	I/O73 F4	I/O81 F1	I/O88 E4	I/O94 E1	I/O100 H1	I/O106 H4	I/O113 G1	I/O119 G4	I/O126 J0	I/O131 J2	I/O145 J5	VCC	I/O178 K3	I/O191 I7	V	
W	GND	I/O27 C7	I/O43 C6	I/O56 C3	I/O62 F7	I/O69 F5	I/O74 F3	I/O82 E7	I/O89 E3	I/O95 E0	I/O101 H0	I/O107 H3	I/O114 H7	I/O120 G3	I/O127 G5	I/O132 G7	I/O146 J4	I/O163 J6	I/O179 J7	GND	W	
Y	GND	GND	GND	I/O57 C4	I/O63 F6	GND	I/O75 F2	I/O83 E6	GND	GND	GND	GND	I/O115 H6	I/O121 G2	GND	I/O133 G6	I/O147 J3	GND	I/O180 K6	GND	Y	
	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1		

17466G-046

## 256-BALL fpBGA CONNECTION DIAGRAM (M4A3-256/128)

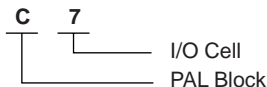
### Bottom View

#### 256-Ball fpBGA

	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	TRST	I/O117 O5	I/O116 O4	I/O113 O1	I/O126 P6	I/O124 P4	I12	NC	NC	NC	CLK0	I/O1 A1	I/O5 A5	I/O7 A7	I/O10 B2	I/O12 B4	A
B	I/O110 N6	I/O111 N7	I/O118 O6	I/O115 O3	I/O127 P7	I/O125 P5	I/O120 P0	NC	NC	NC	I1	I/O2 A2	I/O8 B0	I/O11 B3	I/O13 B5	NC	B
C	I/O108 N4	I/O109 N5	NC	I/O119 O7	I/O114 O2	I/O122 P2	I/O123 P3	NC	NC	I0	I/O4 A4	I/O6 A6	I/O15 B7	I/O14 B6	TDI	I/O23 C7	C
D	NC	I/O104 N0	TDO	GND	GND	VCC	GND	VCC	GND	GND	VCC	GND	VCC	I/O9 B1	I/O22 C6	I/O21 C5	D
E	I/O102 M6	NC	I/O107 N3	VCC	I/O105 N1	I/O106 N2	I13	CLK3	NC	NC	I/O0 A0	NC	GND	I/O20 C4	I/O19 C3	I/O31 D7	E
F	I/O98 M2	I/O103 M7	I/O101 M5	GND	I/O100 M4	I/O99 M3	I/O112 O0	I/O121 P1	NC	NC	I/O3 A3	I/O18 C2	VCC	I/O16 C0	I/O30 D6	I/O29 D5	F
G	NC	I/O96 M0	I11	VCC	NC	I/O97 M1	VCC	GND	GND	VCC	I/O17 C1	I/O28 D4	GND	I/O26 D2	I/O25 D1	I2	G
H	I/O88 L0	I10	I9	GND	I/O89 L1	I/O90 L2	GND	VCC	VCC	GND	I/O27 D3	I/O24 D0	VCC	NC	NC	NC	H
J	I/O91 L3	I/O92 L4	I/O93 L5	GND	I/O95 L7	I/O94 L6	GND	VCC	VCC	GND	I3	NC	GND	NC	NC	NC	J
K	NC	NC	NC	VCC	NC	NC	VCC	GND	GND	VCC	NC	NC	VCC	I4	NC	I/O32 E0	K
L	NC	NC	I/O80 K0	GND	I/O83 K3	NC	NC	NC	I/O59 H3	I/O61 H5	NC	NC	GND	I/O35 E3	I/O36 E4	I/O33 E1	L
M	I/O81 K1	I/O82 K2	I/O84 K4	GND	I/O67 I3	I/O65 I1	NC	NC	I/O58 H2	I/O48 G0	I/O51 G3	NC	VCC	I/O44 F4	I/O39 E7	I/O34 E2	M
N	I/O85 K5	I/O86 K6	ENABLE	VCC	GND	VCC	GND	VCC	GND	GND	VCC	GND	GND	TCK	I/O40 F0	I/O37 E5	N
P	I/O87 K7	I/O77 J5	I/O78 J6	I/O79 J7	I/O68 I4	I/O66 I2	NC	NC	NC	I6	I/O63 H7	I/O52 G4	I/O55 G7	TMS	I/O41 F1	I/O38 E6	P
R	I/O76 J4	I/O75 J3	I/O72 J0	I/O71 I7	I/O64 I0	I7	NC	NC	NC	I/O56 H0	I/O60 H4	I/O49 G1	I/O53 G5	I/O47 F7	I/O43 F3	I/O42 F2	R
T	I/O74 J2	I/O73 J1	I/O70 I6	I/O69 I5	I8	CLK2	NC	NC	CLK1	I5	I/O57 H1	I/O62 H6	I/O50 G2	I/O54 G6	I/O46 F6	I/O45 F5	T

#### PIN DESIGNATIONS

CLK = Clock  
 GND = Ground  
 I = Input  
 I/O = Input/Output  
 N/C = No Connect  
 VCC = Supply Voltage  
 TDI = Test Data In  
 TCK = Test Clock  
 TMS = Test Mode Select  
 TDO = Test Data Out  
 TRST = Test Reset  
 ENABLE = Program



m4a3.256.128\_256bga

## 256-BALL fpBGA CONNECTION DIAGRAM (M4A3-384/192)

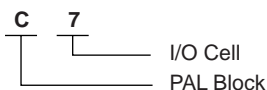
### Bottom View

#### 256-Ball fpBGA

	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	I/O175 FX7	I/O181 GX5	I/O180 GX4	I/O177 GX1	I/O166 EX6	I/O164 EX4	I/O191 HX7	I/O186 HX2	I/O1 A1	I/O3 A3	CLK0	I/O25 D1	I/O29 D5	I/O31 D7	I/O10 B2	I/O12 B4	A
B	I/O173 FX5	I/O174 FX6	I/O182 GX6	I/O179 GX3	I/O167 EX7	I/O165 EX5	I/O160 EX0	I/O187 HX3	I/O0 A0	I/O5 A5	I/O7 A7	I/O26 D2	I/O8 B0	I/O11 B3	I/O13 B5	N/C	B
C	I/O171 FX3	I/O172 FX4	N/C	I/O183 GX7	I/O178 GX2	I/O162 EX2	I/O163 EX3	I/O189 HX5	I/O184 HX0	I/O6 A6	I/O28 D4	I/O30 D6	I/O15 B7	I/O14 B6	TDI	I/O23 C7	C
D	I/O150 CX6	I/O151 CX7	TDO	GND	GND	VCC	GND	VCC	GND	GND	VCC	GND	VCC	I/O9 B1	I/O22 C6	I/O21 C5	D
E	I/O148 CX4	N/C	I/O170 FX2	VCC	I/O168 FX0	169 FX1	I/O190 HX6	CLK3	I/O188 HX4	I/O2 A2	I/O24 D0	N/C	GND	I/O20 C4	I/O19 C3	I/O47 F7	E
F	I/O144 CX0	I/O149 CX5	I/O147 CX3	GND	I/O146 CX2	I/O145 CX1	I/O176 GX0	I/O161 EX1	I/O185 HX1	I/O4 A4	I/O27 D3	I/O18 C2	VCC	I/O16 C0	I/O46 F6	I/O45 F5	F
G	I/O155 DX3	I/O158 DX6	I/O157 DX5	VCC	I/O156 DX4	I/O159 DX7	VCC	GND	GND	VCC	I/O17 C1	I/O44 F4	GND	I/O42 F2	I/O41 F1	I/O39 E7	G
H	I/O152 DX0	I/O154 DX2	I/O153 DX1	GND	I/O128 AX0	I/O129 AX1	GND	VCC	VCC	GND	I/O43 F3	I/O40 F0	VCC	I/O36 E4	I/O35 E3	I/O34 E2	H
J	I/O130 AX2	I/O131 AX3	I/O132 AX4	GND	I/O134 AX6	I/O133 AX5	GND	VCC	VCC	GND	I/O38 E6	I/O37 E5	GND	I/O57 H1	I/O56 H0	I/O58 H2	J
K	I/O135 AX7	I/O136 BX0	I/O137 BX1	VCC	I/O139 BX3	I/O138 BX2	VCC	GND	GND	VCC	I/O33 E1	I/O32 E0	VCC	I/O63 H7	I/O62 H6	I/O48 G0	K
L	I/O140 BX4	I/O141 BX5	I/O143 BX7	GND	I/O114 O2	I/O142 BX6	I/O98 M2	I/O91 L3	I/O67 I3	I/O69 I5	I/O60 H4	I/O59 H3	GND	I/O51 G3	I/O52 G4	I/O49 G1	L
M	I/O112 O0	I/O113 O1	I/O115 O3	GND	I/O123 P3	I/O121 P1	I/O100 M4	I/O90 L2	I/O66 I2	I/O80 K0	I/O83 K3	I/O61 H5	VCC	I/O76 J4	I/O55 G7	I/O50 G2	M
N	I/O116 O4	I/O117 O5	I/O119 O7	VCC	GND	VCC	GND	VCC	GND	GND	VCC	GND	GND	TCK	I/O72 J0	I/O53 G5	N
P	I/O118 O6	I/O109 N5	I/O110 N6	I/O111 N7	I/O124 P4	I/O122 P2	I/O101 M5	I/O89 L1	I/O93 L5	I/O94 L6	I/O71 I7	I/O84 K4	I/O87 K7	TMS	I/O73 J1	I/O54 G6	P
R	I/O108 N4	I/O107 N3	I/O104 N0	I/O127 P7	I/O120 P0	I/O102 M6	I/O99 M3	I/O96 M0	I/O92 L4	I/O64 I0	I/O68 I4	I/O81 K1	I/O85 K5	I/O79 J7	I/O75 J3	I/O74 J2	R
T	I/O106 N2	I/O105 N1	I/O126 P6	I/O125 P5	I/O103 M7	CLK2	I/O97 M1	I/O88 L0	CLK1	I/O95 L7	I/O65 I1	I/O70 I6	I/O82 K2	I/O86 K6	I/O78 J6	I/O77 J5	T

#### PIN DESIGNATIONS

CLK = Clock  
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 VCC = Supply Voltage  
 TDI = Test Data In  
 TCK = Test Clock  
 TMS = Test Mode Select  
 TDO = Test Data Out



5V Commercial Combinations		
M4A5-32/32	-5, -7, -10,	JC, VC, VC48
M4A5-64/32	-55, -7, -10	JC, VC, VC48
M4A5-96/48		VC
M4A5-128/64		YC, VC
M4A5-192/96	-6, -7, -10	VC
M4A5-256/128	-65, -7, -10	YC

5V Industrial Combinations		
M4A5-32/32	-7, -10, -12	JJ, VI, VI48
M4A5-64/32	-7, -10, -12	JJ, VI, VI48
M4A5-96/48		VI
M4A5-128/64		YI, VI
M4A5-192/96	-7, -10, -12	VI
M4A5-256/128	-10, -12	YI

## Lead-free Packaging

3.3V Commercial Combinations		
M4A3-32/32	-5, -7, -10	VNC, VNC48, JNC
M4A3-64/32	-55, -7, -10	VNC, VNC48, JNC
M4A3-64/64		VNC
M4A3-128/64		VNC
M4A3-192/96	-6, -7, -10	VNC
M4A3-256/128	-55, -7, -10	FANC, YNC
M4A3-256/160	-7, -10	YNC
M4A3-256/192		FANC
M4A3-384/192	-65, -10, -12	FANC
M4A3-512/192	-7, -10, -12	FANC

3.3V Industrial Combinations		
M4A3-32/32	-7, -10, -12	VNI, VNI48, JNI
M4A3-64/32		VNI, VNI48, JNI
M4A3-64/64		VNI
M4A3-128/64		VNI
M4A3-192/96	-10, -12	VNI
M4A3-256/128		FANI, YNI
M4A3-256/160		YNI
M4A3-256/192	-10, -12, -14	FANI
M4A3-384/192		FANI
M4A3-512/192		FANI

5V Commercial Combinations		
M4A5-32/32	-5, -7, -10	VNC, VNC48, JNC
M4A5-64/32	-55, -7, -10	VNC, VNC48, JNC
M4A5-96/48		VNC
M4A5-128/64		VNC, YNC
M4A5-192/96	-6, -7, -10	VNC
M4A5-256/128	-65, -7, -10	YNC

5V Industrial Combinations		
M4A5-32/32	-7, -10, -12	VNI, VNI48, JNI
M4A5-64/32		VNI, VNI48, JNI
M4A5-96/48		VNI
M4A5-128/64		VNI, YNI
M4A5-192/96		VNI
M4A5-256/128		YNI

Most ispMACH devices are dual-marked with both Commercial and Industrial grades. The Industrial speed grade is slower, i.e., M4A3-256/128-7YC-10YI

### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local Lattice sales office to confirm availability of specific valid combinations and to check on newly released combinations.