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## Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

## Applications of Embedded - CPLDs

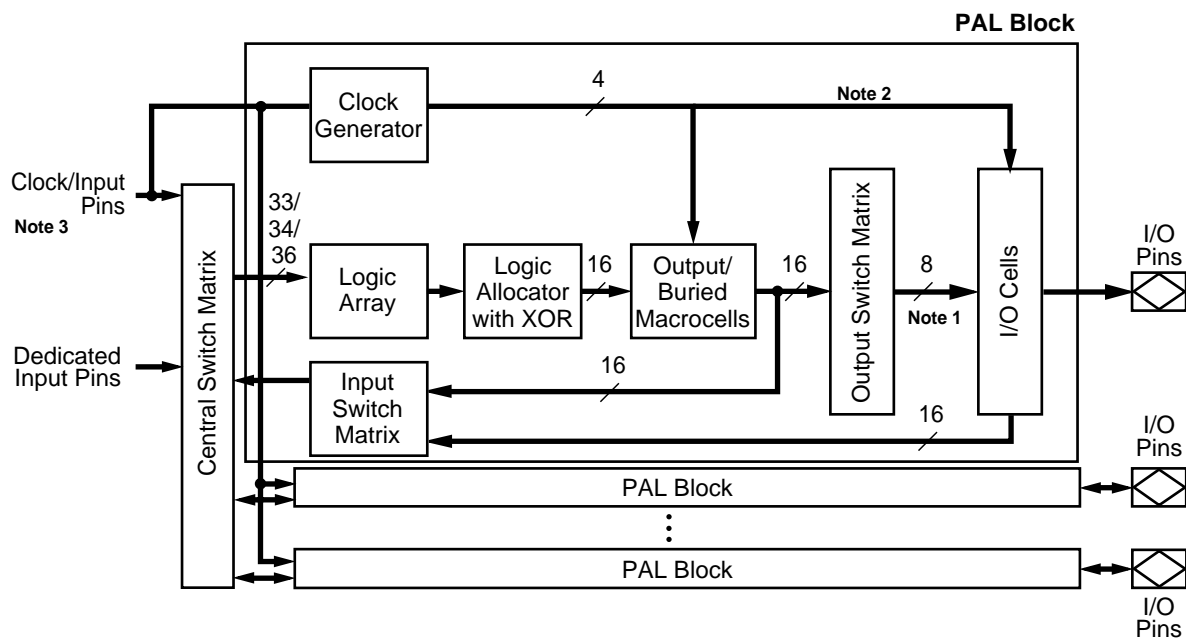
### Details

Product Status	Not For New Designs
Programmable Type	In System Programmable
Delay Time tpd(1) Max	10 ns
Voltage Supply - Internal	4.5V ~ 5.5V
Number of Logic Elements/Blocks	-
Number of Macrocells	64
Number of Gates	-
Number of I/O	32
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/lattice-semiconductor/m4a5-64-32-10vni">https://www.e-xfl.com/product-detail/lattice-semiconductor/m4a5-64-32-10vni</a>

## FUNCTIONAL DESCRIPTION

The fundamental architecture of ispMACH 4A devices (Figure 1) consists of multiple, optimized PAL<sup>®</sup> blocks interconnected by a central switch matrix. The central switch matrix allows communication between PAL blocks and routes inputs to the PAL blocks. Together, the PAL blocks and central switch matrix allow the logic designer to create large designs in a single device instead of having to use multiple devices.

The key to being able to make effective use of these devices lies in the interconnect schemes. In the ispMACH 4A architecture, the macrocells are flexibly coupled to the product terms through the logic allocator, and the I/O pins are flexibly coupled to the macrocells due to the output switch matrix. In addition, more input routing options are provided by the input switch matrix. These resources provide the flexibility needed to fit designs efficiently.



17466G-001

Figure 1. ispMACH 4A Block Diagram and PAL Block Structure

### Notes:

1. 16 for ispMACH 4A devices with 1:1 macrocell-I/O cell ratio (see next page).
2. Block clocks do not go to I/O cells in M4A(3,5)-32/32.
3. M4A(3,5)-192, M4A(3,5)-256, M4A3-384, and M4A3-512 have dedicated clock pins which cannot be used as inputs and do not connect to the central switch matrix.

**Table 4. Architectural Summary of ispMACH 4A devices**

	ispMACH 4A Devices	
		M4A3-64/32, M4A5-64/32 M4A3-96/48, M4A5-96/48 M4A3-128/64, M4A5-128/64 M4A3-192/96, M4A5-192/96 M4A3-256/128, M4A5-256/128 M4A3-384 M4A3-512
Macrocell-I/O Cell Ratio	2:1	1:1
Input Switch Matrix	Yes	Yes <sup>1</sup>
Input Registers	Yes	No
Central Switch Matrix	Yes	Yes
Output Switch Matrix	Yes	Yes

The Macrocell-I/O cell ratio is defined as the number of macrocells versus the number of I/O cells internally in a PAL block (Table 4).

The central switch matrix takes all dedicated inputs and signals from the input switch matrices and routes them as needed to the PAL blocks. Feedback signals that return to the same PAL block still must go through the central switch matrix. This mechanism ensures that PAL blocks in ispMACH 4A devices communicate with each other with consistent, predictable delays.

The central switch matrix makes a ispMACH 4A device more advanced than simply several PAL devices on a single chip. It allows the designer to think of the device not as a collection of blocks, but as a single programmable device; the software partitions the design into PAL blocks through the central switch matrix so that the designer does not have to be concerned with the internal architecture of the device.

Each PAL block consists of:

- ◆ Product-term array
- ◆ Logic allocator
- ◆ Macrocells
- ◆ Output switch matrix
- ◆ I/O cells
- ◆ Input switch matrix
- ◆ Clock generator

**Notes:**

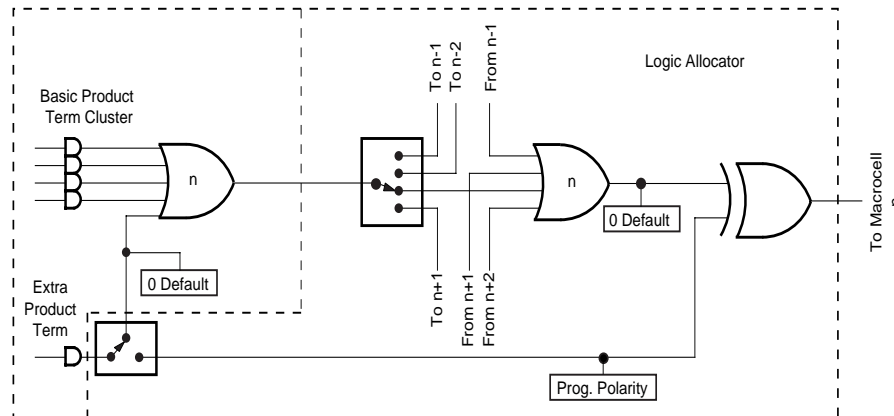
1. M4A3-64/64 internal switch matrix functionality embedded in central switch matrix.

**Table 6. Logic Allocator for All ispMACH 4A Devices (except M4A(3,5)-32/32)**

Output Macrocell	Available Clusters	Output Macrocell	Available Clusters
M <sub>0</sub>	C <sub>0</sub> , C <sub>1</sub> , C <sub>2</sub>	M <sub>8</sub>	C <sub>7</sub> , C <sub>8</sub> , C <sub>9</sub> , C <sub>10</sub>
M <sub>1</sub>	C <sub>0</sub> , C <sub>1</sub> , C <sub>2</sub> , C <sub>3</sub>	M <sub>9</sub>	C <sub>8</sub> , C <sub>9</sub> , C <sub>10</sub> , C <sub>11</sub>
M <sub>2</sub>	C <sub>1</sub> , C <sub>2</sub> , C <sub>3</sub> , C <sub>4</sub>	M <sub>10</sub>	C <sub>9</sub> , C <sub>10</sub> , C <sub>11</sub> , C <sub>12</sub>
M <sub>3</sub>	C <sub>2</sub> , C <sub>3</sub> , C <sub>4</sub> , C <sub>5</sub>	M <sub>11</sub>	C <sub>10</sub> , C <sub>11</sub> , C <sub>12</sub> , C <sub>13</sub>
M <sub>4</sub>	C <sub>3</sub> , C <sub>4</sub> , C <sub>5</sub> , C <sub>6</sub>	M <sub>12</sub>	C <sub>11</sub> , C <sub>12</sub> , C <sub>13</sub> , C <sub>14</sub>
M <sub>5</sub>	C <sub>4</sub> , C <sub>5</sub> , C <sub>6</sub> , C <sub>7</sub>	M <sub>13</sub>	C <sub>12</sub> , C <sub>13</sub> , C <sub>14</sub> , C <sub>15</sub>
M <sub>6</sub>	C <sub>5</sub> , C <sub>6</sub> , C <sub>7</sub> , C <sub>8</sub>	M <sub>14</sub>	C <sub>13</sub> , C <sub>14</sub> , C <sub>15</sub>
M <sub>7</sub>	C <sub>6</sub> , C <sub>7</sub> , C <sub>8</sub> , C <sub>9</sub>	M <sub>15</sub>	C <sub>14</sub> , C <sub>15</sub>

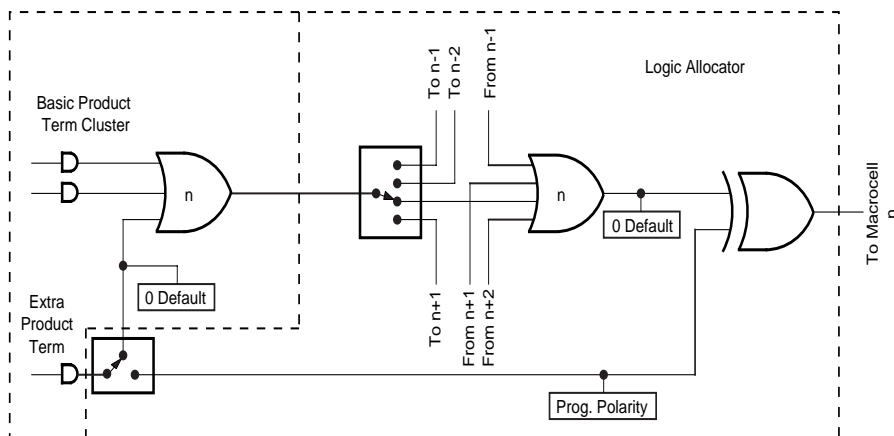
**Table 7. Logic Allocator for M4A(3,5)-32/32**

Output Macrocell	Available Clusters	Output Macrocell	Available Clusters
M <sub>0</sub>	C <sub>0</sub> , C <sub>1</sub> , C <sub>2</sub>	M <sub>8</sub>	C <sub>8</sub> , C <sub>9</sub> , C <sub>10</sub>
M <sub>1</sub>	C <sub>0</sub> , C <sub>1</sub> , C <sub>2</sub> , C <sub>3</sub>	M <sub>9</sub>	C <sub>8</sub> , C <sub>9</sub> , C <sub>10</sub> , C <sub>11</sub>
M <sub>2</sub>	C <sub>1</sub> , C <sub>2</sub> , C <sub>3</sub> , C <sub>4</sub>	M <sub>10</sub>	C <sub>9</sub> , C <sub>10</sub> , C <sub>11</sub> , C <sub>12</sub>
M <sub>3</sub>	C <sub>2</sub> , C <sub>3</sub> , C <sub>4</sub> , C <sub>5</sub>	M <sub>11</sub>	C <sub>10</sub> , C <sub>11</sub> , C <sub>12</sub> , C <sub>13</sub>
M <sub>4</sub>	C <sub>3</sub> , C <sub>4</sub> , C <sub>5</sub> , C <sub>6</sub>	M <sub>12</sub>	C <sub>11</sub> , C <sub>12</sub> , C <sub>13</sub> , C <sub>14</sub>
M <sub>5</sub>	C <sub>4</sub> , C <sub>5</sub> , C <sub>6</sub> , C <sub>7</sub>	M <sub>13</sub>	C <sub>12</sub> , C <sub>13</sub> , C <sub>14</sub> , C <sub>15</sub>
M <sub>6</sub>	C <sub>5</sub> , C <sub>6</sub> , C <sub>7</sub>	M <sub>14</sub>	C <sub>13</sub> , C <sub>14</sub> , C <sub>15</sub>
M <sub>7</sub>	C <sub>6</sub> , C <sub>7</sub>	M <sub>15</sub>	C <sub>14</sub> , C <sub>15</sub>



**a. Synchronous Mode**

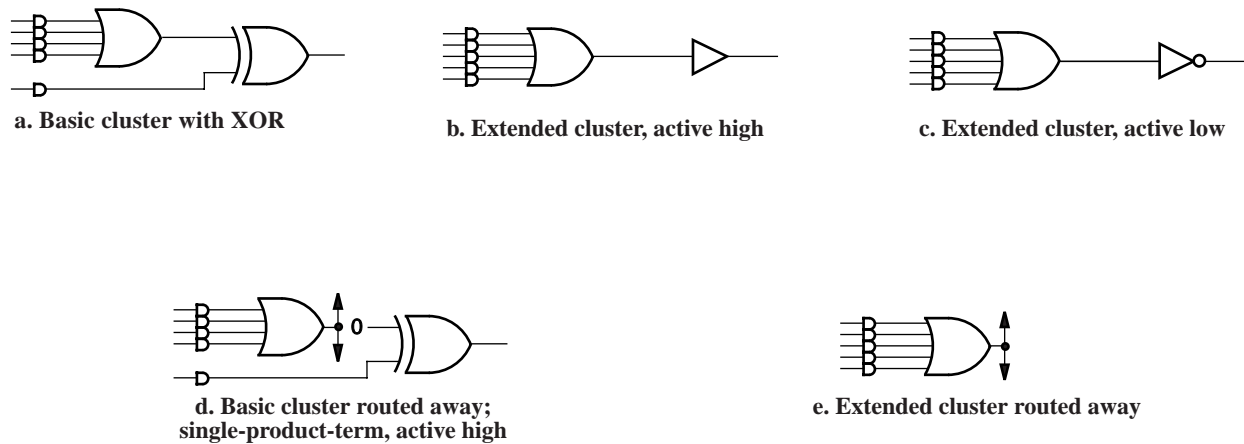
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**b. Asynchronous Mode**

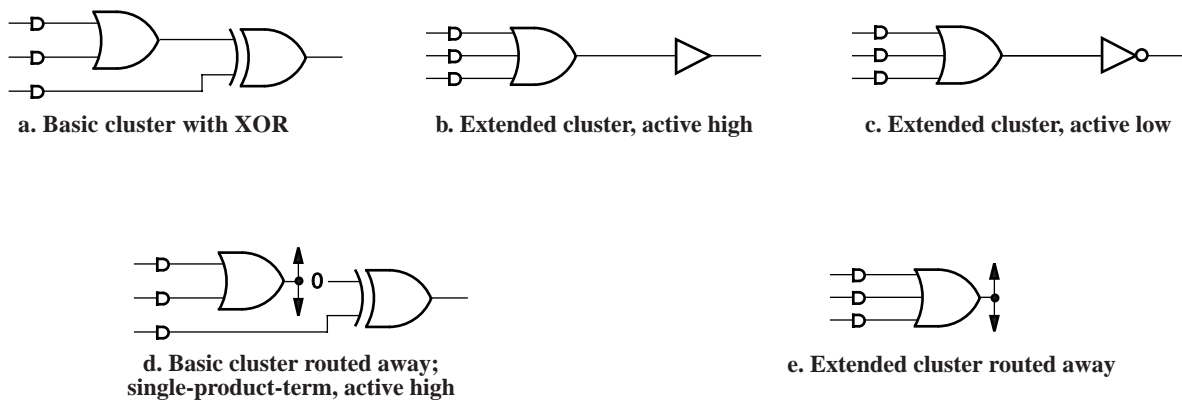
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**Figure 2. Logic Allocator: Configuration of Cluster “n” Set by Mode of Macrocell “n”**



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**Figure 3. Logic Allocator Configurations: Synchronous Mode**



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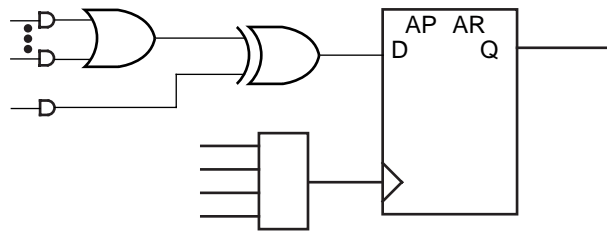
**Figure 4. Logic Allocator Configurations: Asynchronous Mode**

Note that the configuration of the logic allocator has absolutely no impact on the speed of the signal. All configurations have the same delay. This means that designers do not have to decide between optimizing resources or speed; both can be optimized.

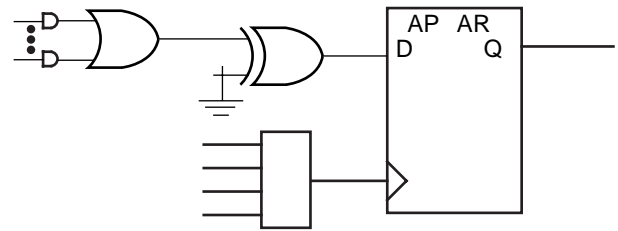
If not used in the cluster, the extra product term can act in conjunction with the basic cluster to provide XOR logic for such functions as data comparison, or it can work with the D-,T-type flip-flop to provide for J-K, and S-R register operation. In addition, if the basic cluster is routed to another macrocell, the extra product term is still available for logic. In this case, the first XOR input will be a logic 0. This circuit has the flexibility to route product terms elsewhere without giving up the use of the macrocell.

Product term clusters do not “wrap” around a PAL block. This means that the macrocells at the ends of the block have fewer product terms available.

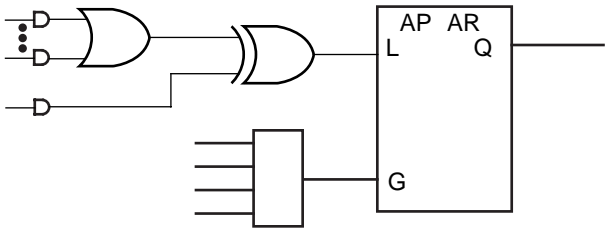
The flip-flop can be configured as a D-type or T-type latch. J-K or S-R registers can be synthesized. The primary flip-flop configurations are shown in Figure 6, although others are possible. Flip-flop functionality is defined in Table 8. Note that a J-K latch is inadvisable as it will cause oscillation if both J and K inputs are HIGH.



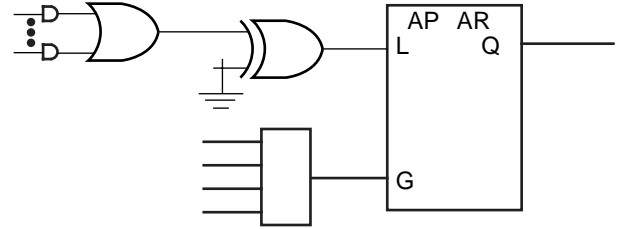
a. D-type with XOR



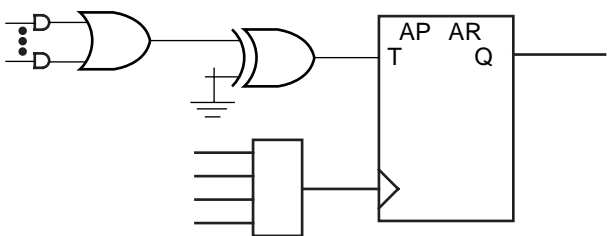
b. D-type with programmable D polarity



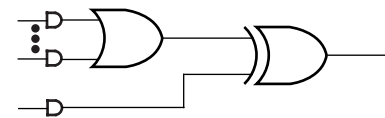
c. Latch with XOR



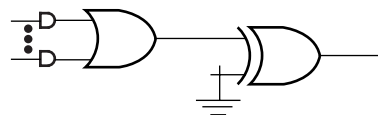
d. Latch with programmable D polarity



e. T-type with programmable T polarity



f. Combinatorial with XOR



g. Combinatorial with programmable polarity

Figure 6. Primary Macrocell Configurations

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**Table 8. Register/Latch Operation**

Configuration	Input(s)	CLK/LE <sup>1</sup>	Q+
D-type Register	D=X	0, 1, ↓ (↑)	Q
	D=0	↑ (↓)	0
	D=1	↑ (↓)	1
T-type Register	T=X	0, 1, ↓ (↑)	Q
	T=0	↑ (↓)	Q
	T=1	↑ (↓)	$\bar{Q}$
D-type Latch	D=X	1 (0)	Q
	D=0	0 (1)	0
	D=1	0 (1)	1

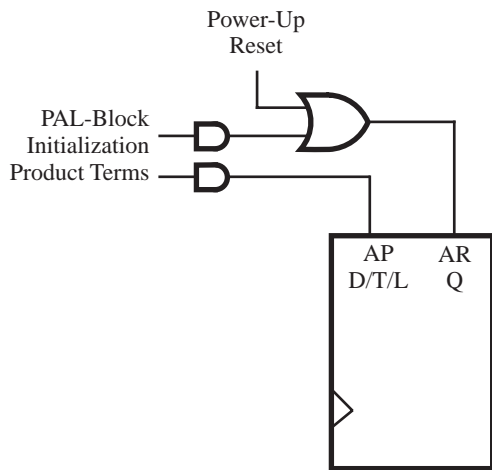
**Note:**

1. Polarity of CLK/LE can be programmed

Although the macrocell shows only one input to the register, the XOR gate in the logic allocator allows the D-, T-type register to emulate J-K, and S-R behavior. In this case, the available product terms are divided between J and K (or S and R). When configured as J-K, S-R, or T-type, the extra product term must be used on the XOR gate input for flip-flop emulation. In any register type, the polarity of the inputs can be programmed.

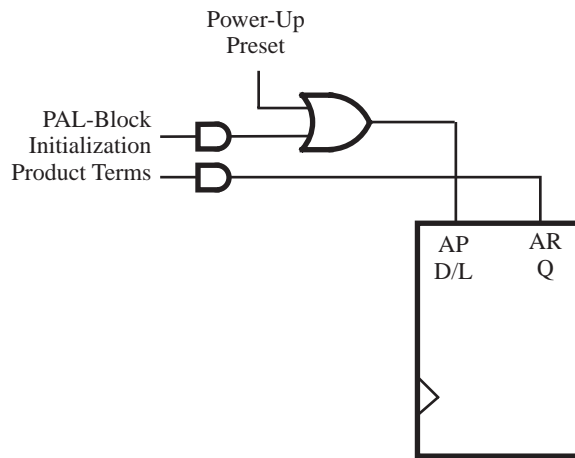
The clock input to the flip-flop can select any of the four PAL block clocks in synchronous mode, with the additional choice of either polarity of an individual product term clock in the asynchronous mode.

The initialization circuit depends on the mode. In synchronous mode (Figure 7), asynchronous reset and preset are provided, each driven by a product term common to the entire PAL block.



a. Power-up reset

17466G-012



b. Power-up preset

17466G-013

**Figure 7. Synchronous Mode Initialization Configurations**

**Table 10. Output Switch Matrix Combinations for ispMACH 4A Devices with 2:1 Macrocell-I/O Cell Ratio**

Macrocell	Routable to I/O Cells
M12, M13	I/03, I/04, I/05, I/06
M14, M15	I/04, I/05, I/06, I/07

I/O Cell	Available Macrocells
I/00	M0, M1, M2, M3, M4, M5, M6, M7
I/01	M2, M3, M4, M5, M6, M7, M8, M9
I/02	M4, M5, M6, M7, M8, M9, M10, M11
I/03	M6, M7, M8, M9, M10, M11, M12, M13
I/04	M8, M9, M10, M11, M12, M13, M14, M15
I/05	M0, M1, M10, M11, M12, M13, M14, M15
I/06	M0, M1, M2, M3, M12, M13, M14, M15
I/07	M0, M1, M2, M3, M4, M5, M14, M15

**Table 11. Output Switch Matrix Combinations for M4A3-256/160 and M4A3-256/192**

Macrocell	Routable to I/O Cells							
M0	I/00	I/01	I/02	I/03	I/04	I/05	I/06	I/07
M1	I/00	I/01	I/02	I/03	I/04	I/05	I/06	I/07
M2	I/00	I/01	I/02	I/03	I/04	I/05	I/06	I/07
M3	I/00	I/01	I/02	I/03	I/04	I/05	I/06	I/07
M4	I/00	I/01	I/02	I/03	I/04	I/05	I/06	I/07
M5	I/00	I/01	I/02	I/03	I/04	I/05	I/06	I/07
M6	I/00	I/01	I/02	I/03	I/04	I/05	I/06	I/07
M7	I/00	I/01	I/02	I/03	I/04	I/05	I/06	I/07
M8	I/08	I/09	I/010	I/011	I/012	I/013	I/014	I/015
M9	I/08	I/09	I/010	I/011	I/012	I/013	I/014	I/015
M10	I/08	I/09	I/010	I/011	I/012	I/013	I/014	I/015
M11	I/08	I/09	I/010	I/011	I/012	I/013	I/014	I/015
M12	I/08	I/09	I/010	I/011	I/012	I/013	I/014	I/015
M13	I/08	I/09	I/010	I/011	I/012	I/013	I/014	I/015
M14	I/08	I/09	I/010	I/011	I/012	I/013	I/014	I/015
M15	I/08	I/09	I/010	I/011	I/012	I/013	I/014	I/015

I/O Cell	Available Macrocells							
I/00	M0	M1	M2	M3	M4	M5	M6	M7
I/01	M0	M1	M2	M3	M4	M5	M6	M7
I/02	M0	M1	M2	M3	M4	M5	M6	M7
I/03	M0	M1	M2	M3	M4	M5	M6	M7
I/04	M0	M1	M2	M3	M4	M5	M6	M7
I/05	M0	M1	M2	M3	M4	M5	M6	M7
I/06	M0	M1	M2	M3	M4	M5	M6	M7
I/07	M0	M1	M2	M3	M4	M5	M6	M7



## I/O Cell

The I/O cell (Figures 10 and 11) simply consists of a programmable output enable, a feedback path, and flip-flop (except ispMACH 4A devices with 1:1 macrocell-I/O cell ratio). An individual output enable product term is provided for each I/O cell. The feedback signal drives the input switch matrix.



17466G-017

**Figure 10. I/O Cell for ispMACH 4A Devices with 2:1 Macrocell-I/O Cell Ratio**



17466G-018

**Figure 11. I/O Cell for ispMACH 4A Devices with 1:1 Macrocell-I/O Cell Ratio**

The I/O cell (Figure 10) contains a flip-flop, which provides the capability for storing the input in a D-type register or latch. The clock can be any of the PAL block clocks. Both the direct and registered versions of the input are sent to the input switch matrix. This allows for such functions as “time-domain-multiplexed” data comparison, where the first data value is stored, and then the second data value is put on the I/O pin and compared with the previous stored value.

Note that the flip-flop used in the ispMACH 4A I/O cell is independent of the flip-flops in the macrocells. It powers up to a logic low.

### **Zero-Hold-Time Input Register**

The ispMACH 4A devices have a zero-hold-time (ZHT) fuse which controls the time delay associated with loading data into all I/O cell registers and latches. When programmed, the ZHT fuse increases the data path setup delays to input storage elements, matching equivalent delays in the clock path. When the fuse is erased, the setup time to the input storage element is minimized. This feature facilitates doing worst-case designs for which data is loaded from sources which have low (or zero) minimum output propagation delays from clock edges.

## Input Switch Matrix

The input switch matrix (Figures 12 and 13) optimizes routing of inputs to the central switch matrix. Without the input switch matrix, each input and feedback signal has only one way to enter the central switch matrix. The input switch matrix provides additional ways for these signals to enter the central switch matrix.



17466G-002

Figure 12. ispMACH 4A with 2:1 Macrocell-I/O Cell Ratio - Input Switch Matrix



17466G-003

Figure 13. ispMACH 4A with 1:1 Macrocell-I/O Cell Ratio - Input Switch Matrix

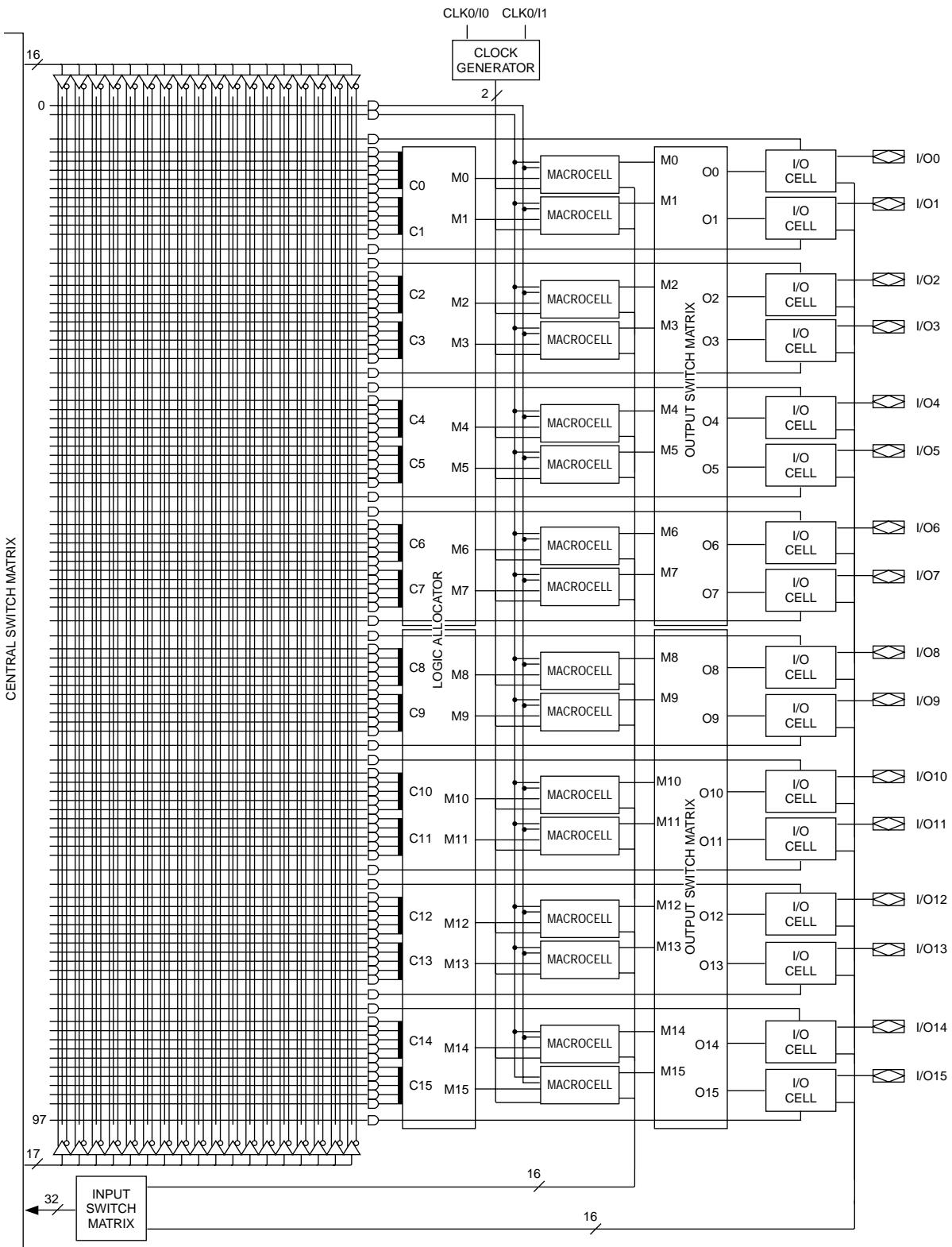
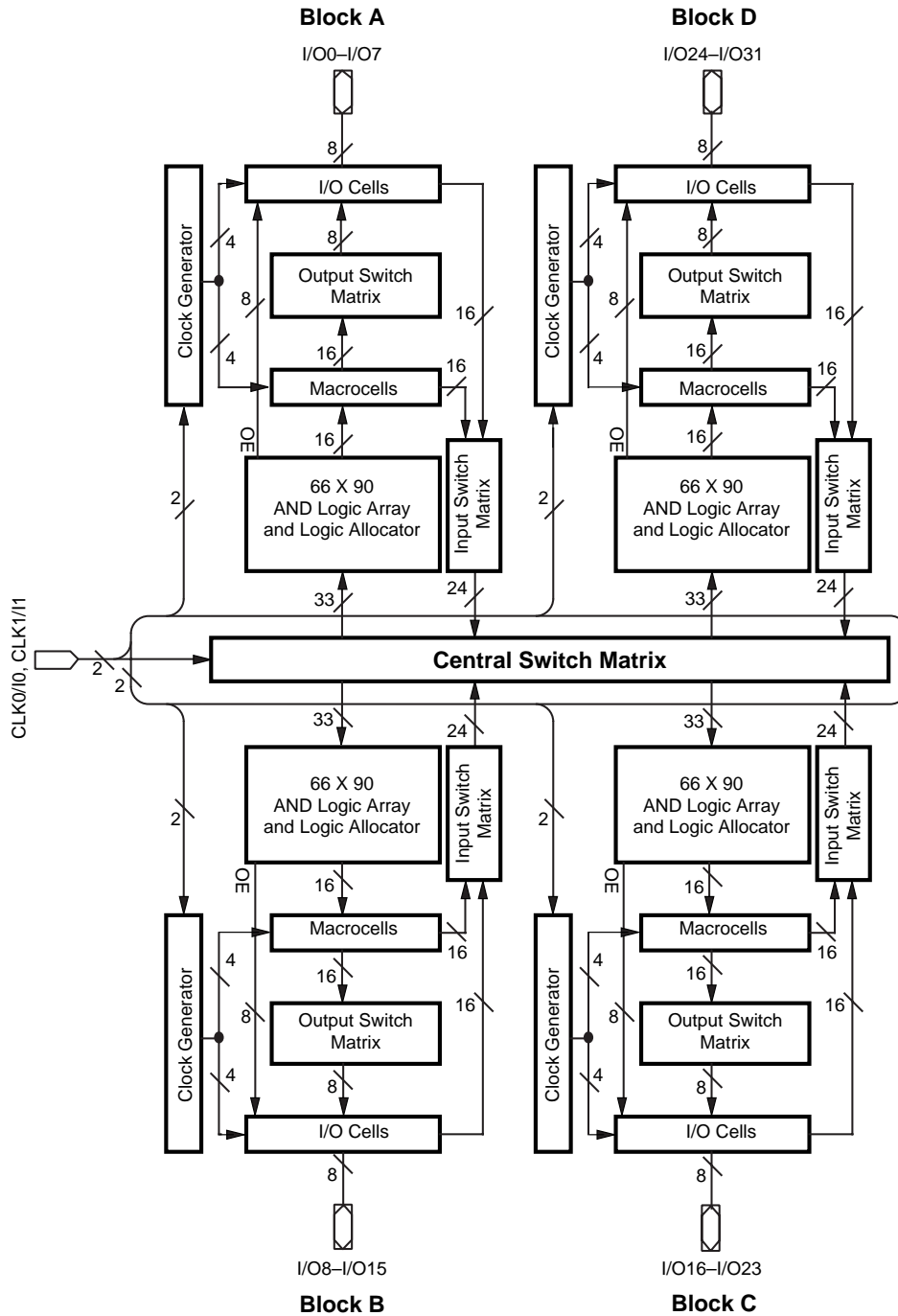


Figure 18. PAL Block for M4A (3,5)-32/32

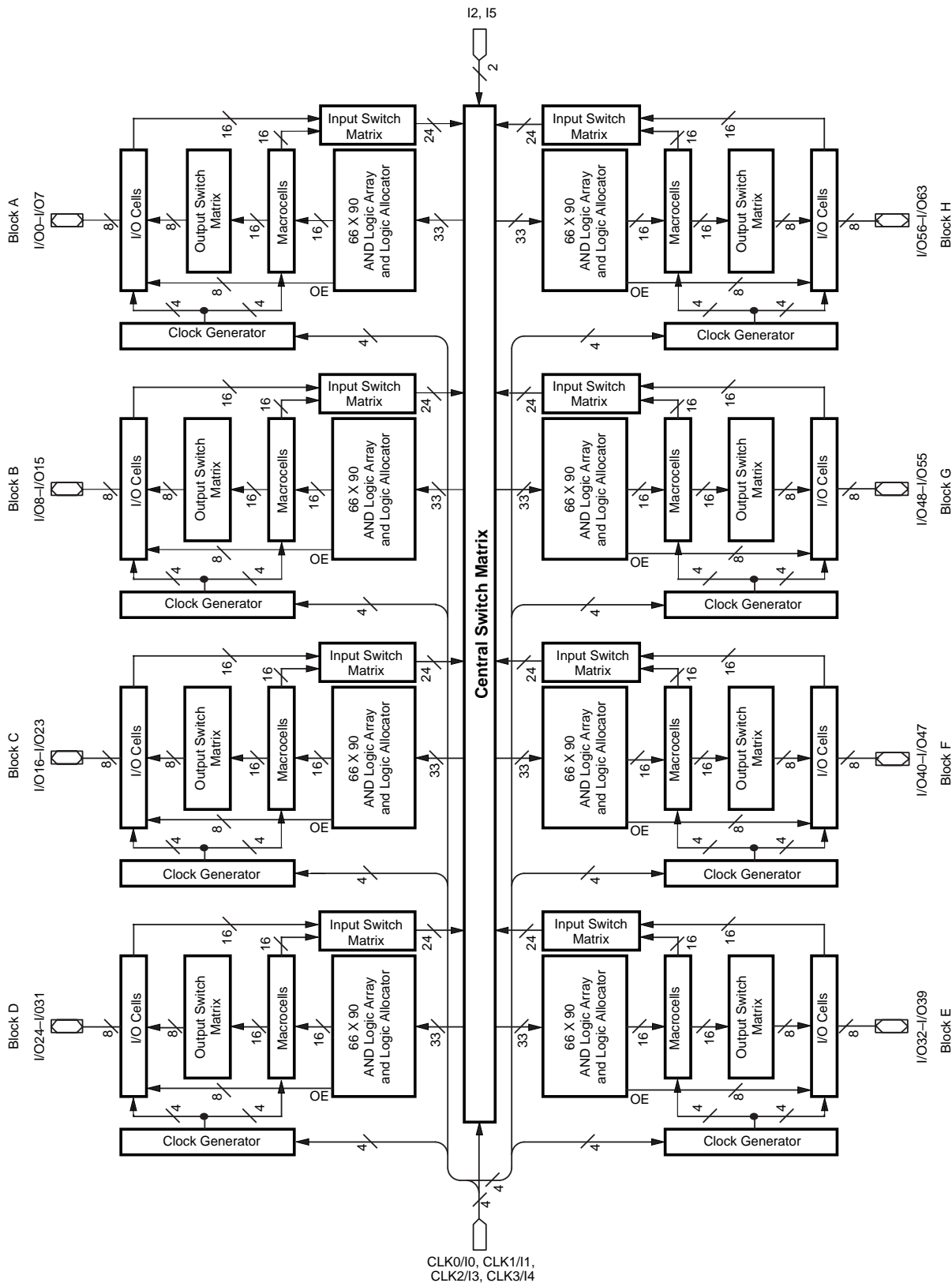
17466H-042

## BLOCK DIAGRAM – M4A(3,5)-64/32



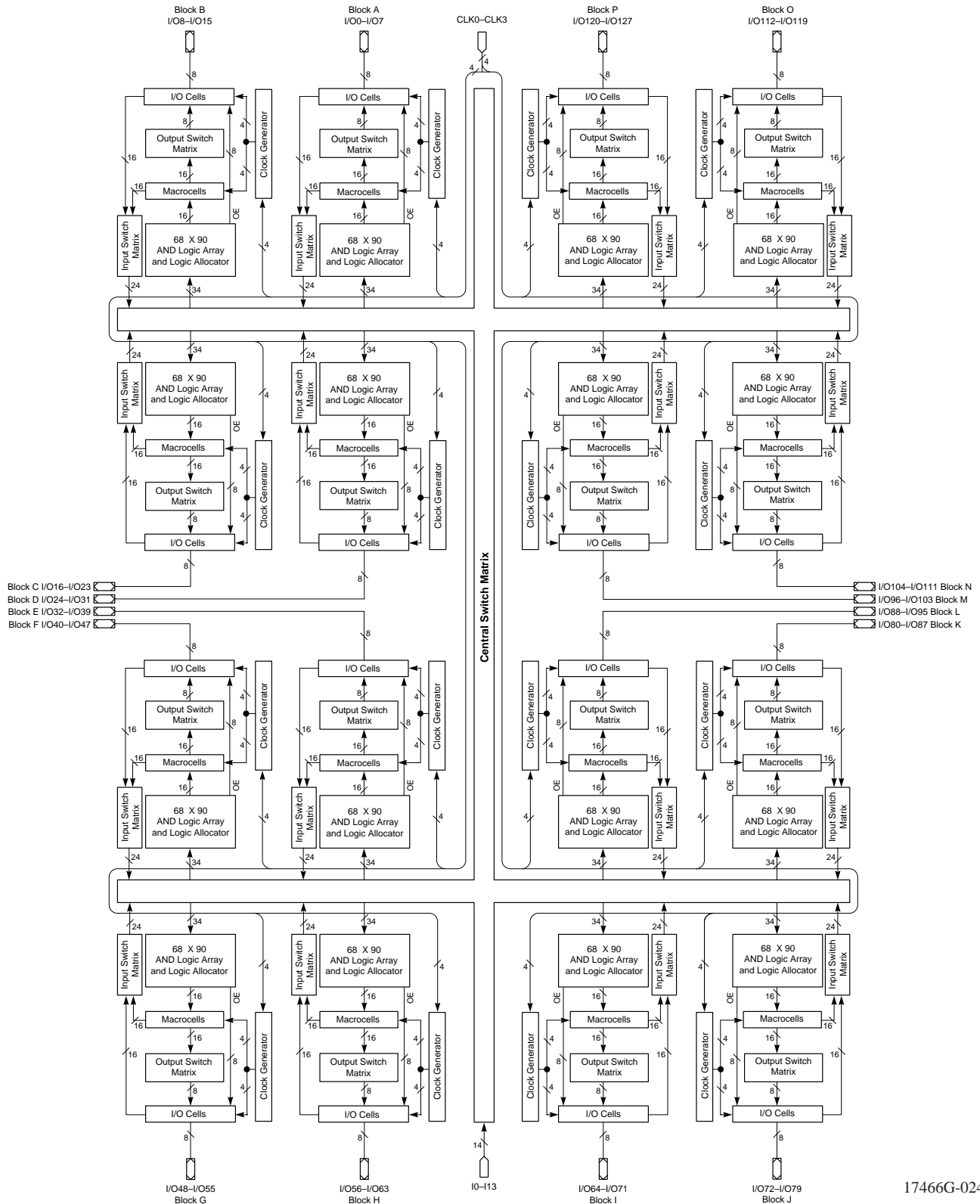
17466H-020

# BLOCK DIAGRAM – M4A(3,5)-128/64



17466H-022

# BLOCK DIAGRAM – M4A(3,5)-256/128



17466G-024

## ispMACH 4A TIMING PARAMETERS OVER OPERATING RANGES<sup>1</sup>

		-5		-55		-6		-65		-7		-10		-12		-14		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
<b>Input Register Delays with ZHT Option:</b>																		
$t_{SIRZ}$	Input register setup time - ZHT	6.0		6.0		6.0		6.0		6.0		6.0		6.0		6.0		ns
$t_{HIRZ}$	Input register hold time - ZHT	0.0		0.0		0.0		0.0		0.0		0.0		0.0		0.0		ns
<b>Input Latch Delays with ZHT Option:</b>																		
$t_{SILZ}$	Input latch setup time - ZHT	6.0		6.0		6.0		6.0		6.0		6.0		6.0		6.0		ns
$t_{HILZ}$	Input latch hold time - ZHT	0.0		0.0		0.0		0.0		0.0		0.0		0.0		0.0		ns
$t_{PDIL}$ $Z_i$	Transparent input latch to internal feedback - ZHT		6.0		6.0		6.0		6.0		6.0		6.0		6.0		6.0	ns
<b>Output Delays:</b>																		
$t_{BUF}$	Output buffer delay		1.5		1.5		1.8		2.0		2.5		3.0		3.0		3.0	ns
$t_{SIW}$	Slow slew rate delay adder		2.5		2.5		2.5		2.5		2.5		2.5		2.5		2.5	ns
$t_{EA}$	Output enable time		7.5		7.5		8.5		8.5		9.5		10.0		12.0		15.0	ns
$t_{ER}$	Output disable time		7.5		7.5		8.5		8.5		9.5		10.0		12.0		15.0	ns
<b>Power Delay:</b>																		
$t_{PL}$	Power-down mode delay adder		2.5		2.5		2.5		2.5		2.5		2.5		2.5		2.5	ns
<b>Reset and Preset Delays:</b>																		
$t_{SRi}$	Asynchronous reset or preset to internal register output		7.5		7.7		8.0		8.0		9.5		11.0		13.0		16.0	ns
$t_{SR}$	Asynchronous reset or preset to register output		9.0		9.2		10.0		10.0		12.0		14.0		16.0		19.0	ns
$t_{SRR}$	Asynchronous reset and preset register recovery time	7.0		7.0		7.5		7.5		8.0		8.0		10.0		15.0		ns
$t_{SRW}$	Asynchronous reset or preset width	7.0		7.0		8.0		8.0		10.0		10.0		12.0		15.0		ns
<b>Clock/LE Width:</b>																		
$t_{WLS}$	Global clock width low	2.0		2.0		2.5		2.5		3.0		4.0		5.0		6.0		ns
$t_{WHS}$	Global clock width high	2.0		2.0		2.5		2.5		3.0		4.0		5.0		6.0		ns
$t_{WLA}$	Product term clock width low	3.0		3.0		3.5		3.5		4.0		5.0		8.0		9.0		ns
$t_{WHA}$	Product term clock width high	3.0		3.0		3.5		3.5		4.0		5.0		8.0		9.0		ns
$t_{CWS}$	Global gate width low (for low transparent) or high (for high transparent)	4.0		4.0		4.5		4.5		5.0		5.0		6.0		6.0		ns
$t_{CWA}$	Product term gate width low (for low transparent) or high (for high transparent)	4.0		4.0		4.5		4.5		5.0		5.0		6.0		9.0		ns
$t_{WIRL}$	Input register clock width low	3.0		3.0		3.5		3.5		4.0		5.0		6.0		6.0		ns
$t_{WIRH}$	Input register clock width high	3.0		3.0		3.5		3.5		4.0		5.0		6.0		6.0		ns
$t_{WIL}$	Input latch gate width	4.0		4.0		4.5		4.5		5.0		5.0		6.0		6.0		ns

## I<sub>CC</sub> vs. FREQUENCY

These curves represent the typical power consumption for a particular device at system frequency. The selected “typical” pattern is a 16-bit up-down counter. This pattern fills the device and exercises every macrocell. Maximum frequency shown uses internal feedback and a D-type register. Power/Speed are optimized to obtain the highest counter frequency and the lowest power. The highest frequency (LSBs) is placed in common PAL blocks, which are set to high power. The lowest frequency signals (MSBs) are placed in a common PAL block and set to lowest power.

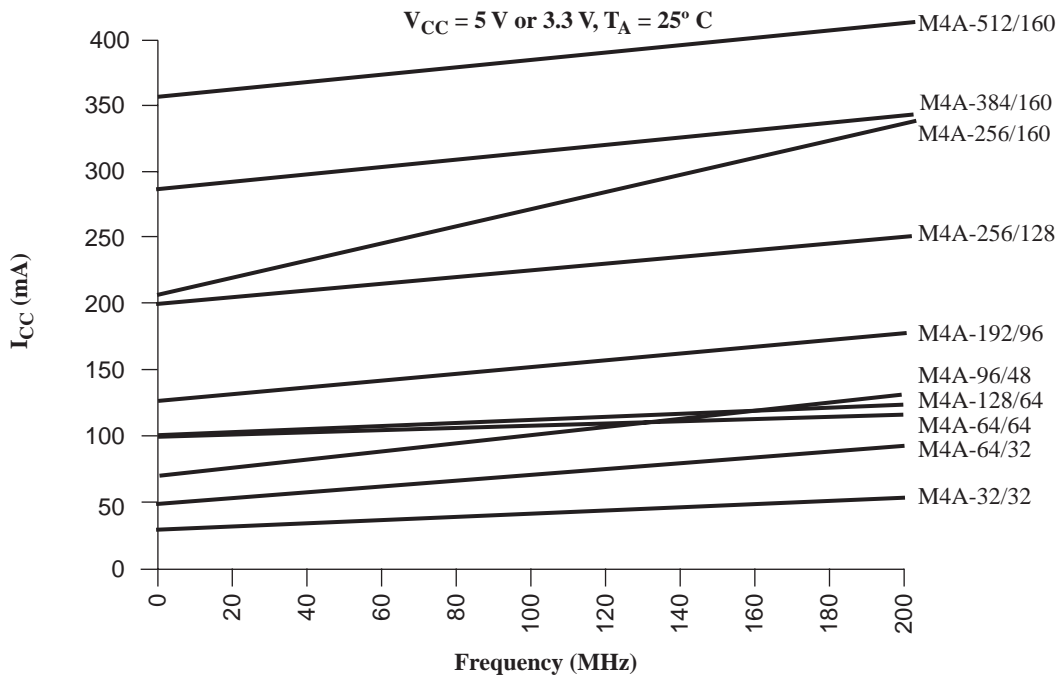


Figure 19. ispMACH 4A I<sub>CC</sub> Curves at High Speed Mode

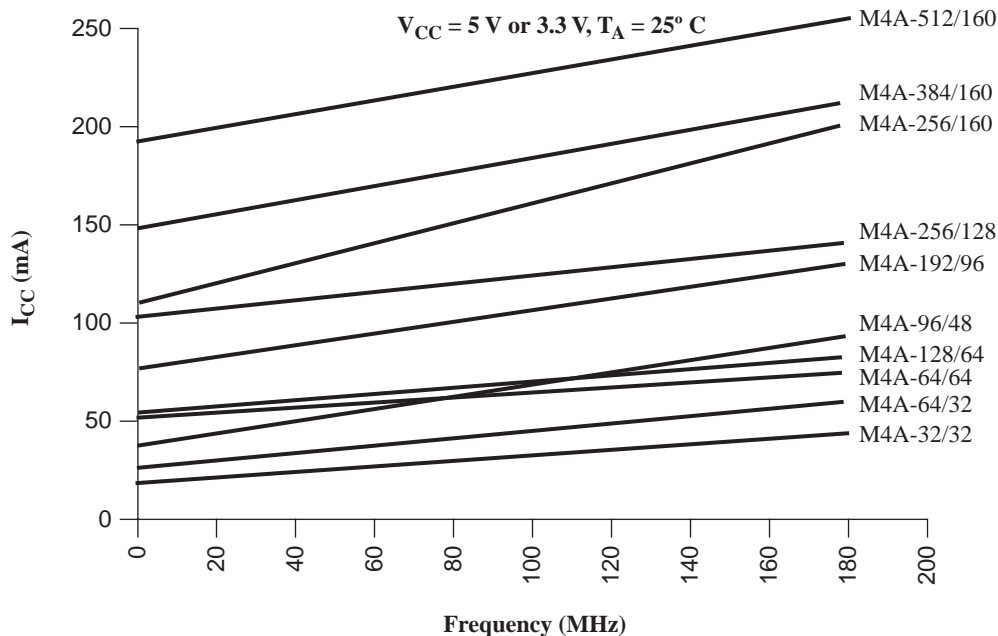
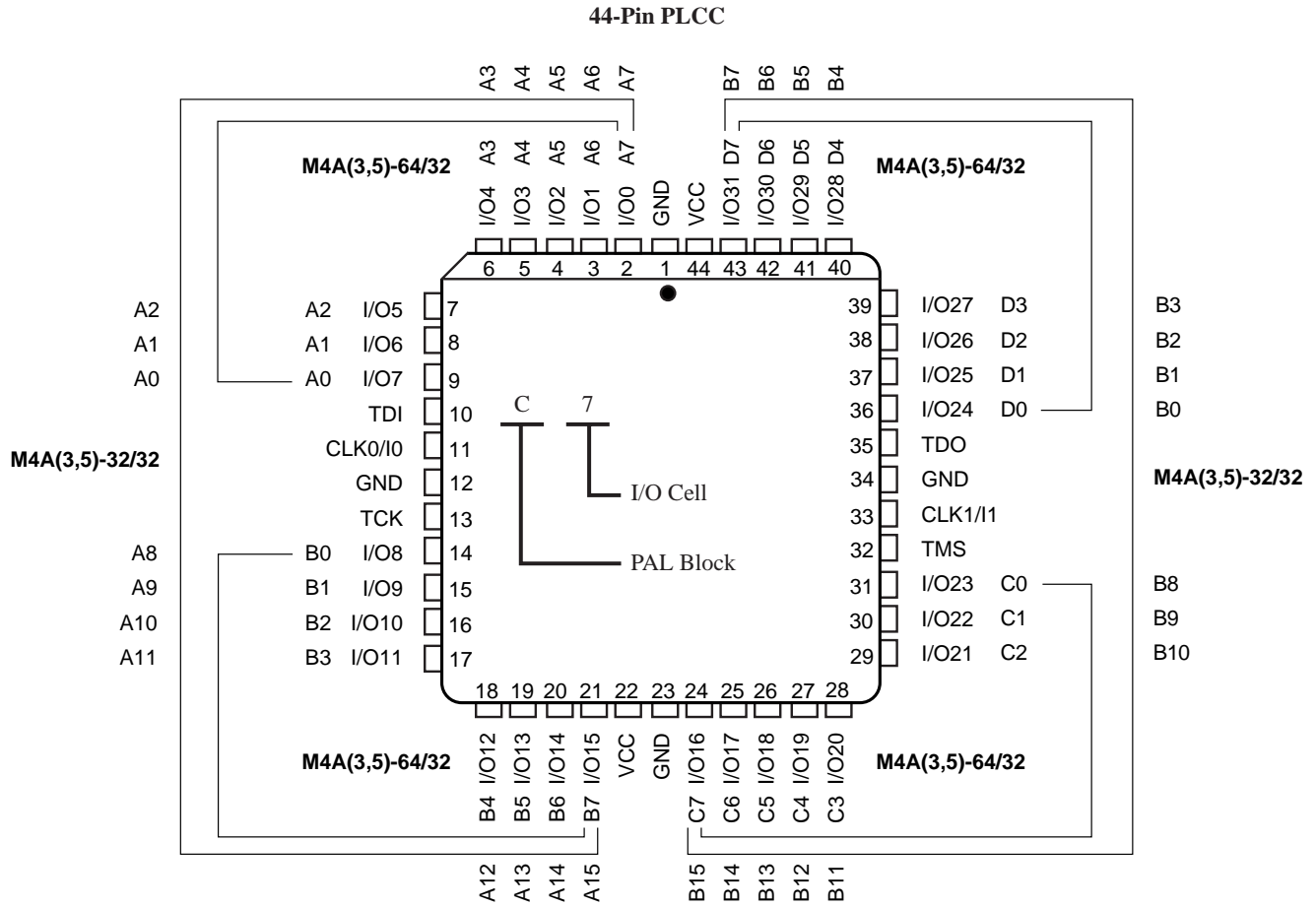


Figure 20. ispMACH 4A I<sub>CC</sub> Curves at Low Power Mode



## 44-PIN PLCC CONNECTION DIAGRAM (M4A(3,5)-32/32 AND M4A(3,5)-64/32)

### Top View



17466G-026

## PIN DESIGNATIONS

CLK/I = Clock or Input

GND = Ground

I/O = Input/Output

V<sub>CC</sub> = Supply Voltage

TDI = Test Data In

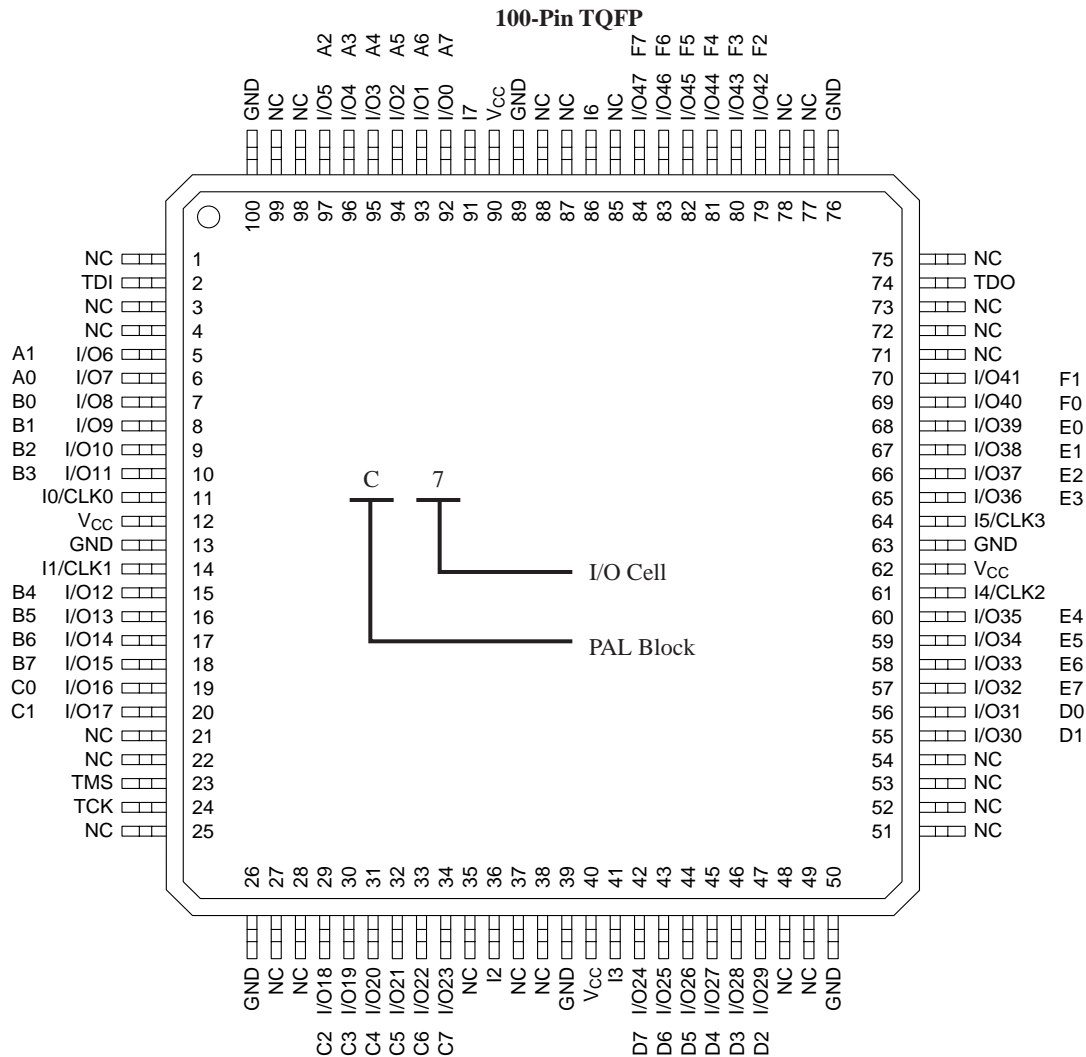
TCK = Test Clock

TMS = Test Mode Select

TDO = Test Data Out

## 100-PIN TQFP CONNECTION DIAGRAM (M4A(3,5)-96/48)

### Top View



17466G-029

## PIN DESIGNATIONS

- CLK/I = Clock or Input
- GND = Ground
- I = Input
- I/O = Input/Output
- V<sub>CC</sub> = Supply Voltage
- NC = No Connect
- TDI = Test Data In
- TCK = Test Clock
- TMS = Test Mode Select
- TDO = Test Data Out

# 100-BALL caBGA CONNECTION DIAGRAM (M4A3-128/64)

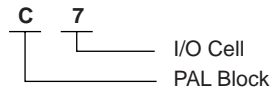
## Bottom View

### 100-Ball caBGA

	10	9	8	7	6	5	4	3	2	1	
A	GND	I/O63 H7	I/O60 H4	I/O57 H1	GND	GND	I/O1 A1	I/O4 A4	I/O7 A7	GND	A
B	$\overline{\text{TRST}}$	GND	I/O61 H5	I5	VCC	I/O0 A0	I/O6 A6	GND	TDI	I/O15 B7	B
C	I/O53 G5	TDO	I/O62 H6	I/O58 H2	I/O56 H0	I/O2 A2	GND	I/O14 B6	I/O13 B5	I/O12 B4	C
D	I/O50 G2	I/O55 G7	GND	I/O59 H3	I/O3 A3	I/O5 A5	I/O11 B3	I/O10 B2	CLK0/I0	I/O9 B1	D
E	CLK3/I4	I/O49 G1	I/O51 G3	I/O54 G6	VCC	I/O16 C0	I/O20 C4	I/O8 B0	VCC	GND	E
F	GND	VCC	I/O40 F0	I/O52 G4	I/O48 G0	VCC	I/O22 C6	I/O19 C3	I/O17 C1	CLK1/I1	F
G	I/O41 F1	CLK2/I3	I/O42 F2	I/O43 F3	I/O37 E5	I/O35 E3	I/O27 D3	GND	I/O23 C7	I/O18 C2	G
H	I/O44 F4	I/O45 F5	I/O46 F6	GND	I/O34 E2	I/O24 D0	I/O26 D2	I/O30 D6	TCK	I/O21 C5	H
J	I/O47 F7	$\overline{\text{ENABLE}}$	GND	I/O38 E6	I/O32 E0	VCC	I2	I/O29 D5	GND	TMS	J
K	GND	I/O39 E7	I/O36 E4	I/O33 E1	GND	GND	I/O25 D1	I/O28 D4	I/O31 D7	GND	K

#### PIN DESIGNATIONS

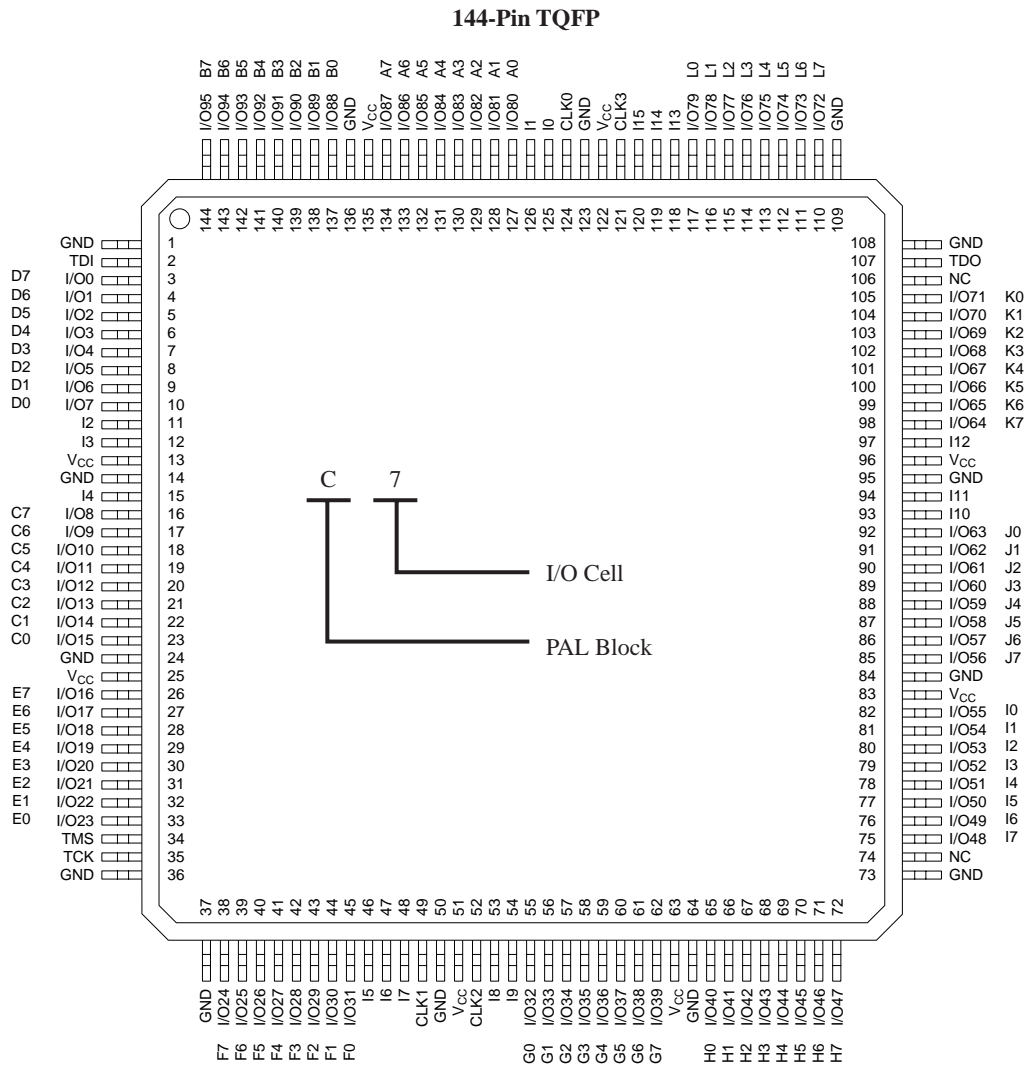
CLK = Clock  
 GND = Ground  
 I = Input  
 I/O = Input/Output  
 N/C = No Connect  
 VCC = Supply Voltage  
 TDI = Test Data In  
 TCK = Test Clock  
 TMS = Test Mode Select  
 TDO = Test Data Out  
 $\overline{\text{TRST}}$  = Test Reset  
 ENABLE = Program



17466G-100cabga

# 144-PIN TQFP CONNECTION DIAGRAM (M4A(3,5)-192/96)

## Top View



17466G-033

## PIN DESIGNATIONS

- CLK = Clock
- GND = Ground
- I = Input
- I/O = Input/Output
- V<sub>CC</sub> = Supply Voltage
- TDI = Test Data In
- TCK = Test Clock
- TMS = Test Mode Select
- TDO = Test Data Out

# 256-BALL BGA CONNECTION DIAGRAM (M4A3-256/128)

## Bottom View

### 256-Ball BGA

	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	GND	N/C	GND	I/O108 N4	I/O105 N1	GND	I/O100 M4	I/O96 M0	GND	GND	GND	GND	I/O95 L0	I/O91 L4	GND	I/O87 K0	N/C	GND	GND	GND	A
B	GND	I/O113 O6	N/C	I/O109 N5	I/O106 N2	I/O103 M7	I/O102 M6	I/O98 M2	N/C	I11	N/C	N/C	I/O93 L2	I/O89 L6	I/O88 L7	I/O85 K2	I/O83 K4	I/O82 K5	N/C	GND	B
C	I/O116 O3	N/C	VCC	TRST	I/O111 N7	I/O107 N3	I/O104 N0	I/O101 M5	I/O97 M1	N/C	I10	I/O94 L1	I/O90 L5	I/O86 K1	I/O84 K3	I/O80 K7	ENABLE	VCC	I/O78 J6	I/O74 J2	C
D	I/O120 P7	I/O117 O2	I/O112 O7	VCC	VCC	I/O110 N6	VCC	N/C	I/O99 M3	N/C	I9	I/O92 L3	N/C	VCC	I/O81 K6	VCC	VCC	I/O79 J7	I/O75 J3	I/O71 I7	D
E	I/O123 P4	I/O119 O0	I/O114 O5	TDI	<p style="text-align: center;"><b>PIN DESIGNATIONS</b></p> <p>           CLK = Clock            GND = Ground            I = Input            I/O = Input/Output            N/C = No Connect            VCC = Supply Voltage            TDI = Test Data In            TCK = Test Clock            TMS = Test Mode Select            TDO = Test Data Out            TRST = Test Reset            ENABLE = Program         </p>												TDO	I/O77 J5	I/O72 J0	I/O68 I4	E
F	GND	I/O122 P5	I/O118 O1	I/O115 O4													I/O76 J4	I/O73 J1	I/O69 I5	GND	F
G	I12	I/O125 P2	I/O121 P6	VCC													VCC	I/O70 I6	I/O65 I1	I8	G
H	GND	I/O127 P0	I/O126 P1	I/O124 P3													I/O67 I3	I/O66 I2	I/O64 I0	GND	H
J	N/C	N/C	N/C	I13													I7	N/C	N/C	N/C	J
K	GND	CLK3	N/C	N/C													N/C	N/C	CLK2	N/C	K
L	N/C	CLK0	N/C	N/C													N/C	N/C	CLK1	GND	L
M	N/C	N/C	N/C	I0													I6	N/C	I/O63 H0	I/O62 H1	M
N	GND	I/O0 A0	I/O2 A2	I/O3 A3													I/O60 H3	I/O61 H2	I/O59 H4	GND	N
P	I1	I/O1 A1	I/O6 A6	VCC													VCC	I/O57 H6	I/O58 H5	I5	P
R	GND	I/O5 A5	I/O9 B1	N/C	I/O51 G4	I/O54 G1	I/O56 H7	GND	R												
T	I/O4 A4	I/O8 B0	I/O12 B4	TCK	TMS	I/O50 G5	I/O55 G0	N/C	T												
U	I/O7 A7	I/O11 B3	I/O15 B7	VCC	VCC	I/O18 C5	VCC	I/O24 D7	I/O29 D2	I2	N/C	I/O35 E3	N/C	VCC	N/C	VCC	VCC	I/O48 G7	I/O53 G2	N/C	U
V	I/O10 B2	I/O13 B5	VCC	I/O16 C7	I/O17 C6	I/O21 C2	I/O23 C0	I/O27 D4	I/O31 D0	I3	N/C	I/O33 E1	I/O37 E5	I/O41 F1	I/O43 F3	I/O46 F6	I/O47 F7	VCC	I/O52 G3	N/C	V
W	GND	I/O14 B6	N/C	N/C	I/O19 C4	I/O22 C1	I/O25 D6	I/O28 D3	N/C	N/C	I4	N/C	I/O34 E2	I/O38 E6	I/O39 E7	I/O42 F2	I/O45 F5	N/C	I/O49 G6	GND	W
Y	GND	GND	GND	N/C	I/O20 C3	GND	I/O26 D5	I/O30 D1	GND	GND	GND	GND	I/O32 E0	I/O36 E4	GND	I/O40 F0	I/O44 F4	GND	N/C	GND	Y

17466G-045