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## Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

## Applications of Embedded - CPLDs

### Details

Product Status	Not For New Designs
Programmable Type	In System Programmable
Delay Time tpd(1) Max	12 ns
Voltage Supply - Internal	4.5V ~ 5.5V
Number of Logic Elements/Blocks	-
Number of Macrocells	64
Number of Gates	-
Number of I/O	32
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-TQFP (7x7)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/lattice-semiconductor/m4a5-64-32-12vni48">https://www.e-xfl.com/product-detail/lattice-semiconductor/m4a5-64-32-12vni48</a>

## FUNCTIONAL DESCRIPTION

The fundamental architecture of ispMACH 4A devices (Figure 1) consists of multiple, optimized PAL<sup>®</sup> blocks interconnected by a central switch matrix. The central switch matrix allows communication between PAL blocks and routes inputs to the PAL blocks. Together, the PAL blocks and central switch matrix allow the logic designer to create large designs in a single device instead of having to use multiple devices.

The key to being able to make effective use of these devices lies in the interconnect schemes. In the ispMACH 4A architecture, the macrocells are flexibly coupled to the product terms through the logic allocator, and the I/O pins are flexibly coupled to the macrocells due to the output switch matrix. In addition, more input routing options are provided by the input switch matrix. These resources provide the flexibility needed to fit designs efficiently.

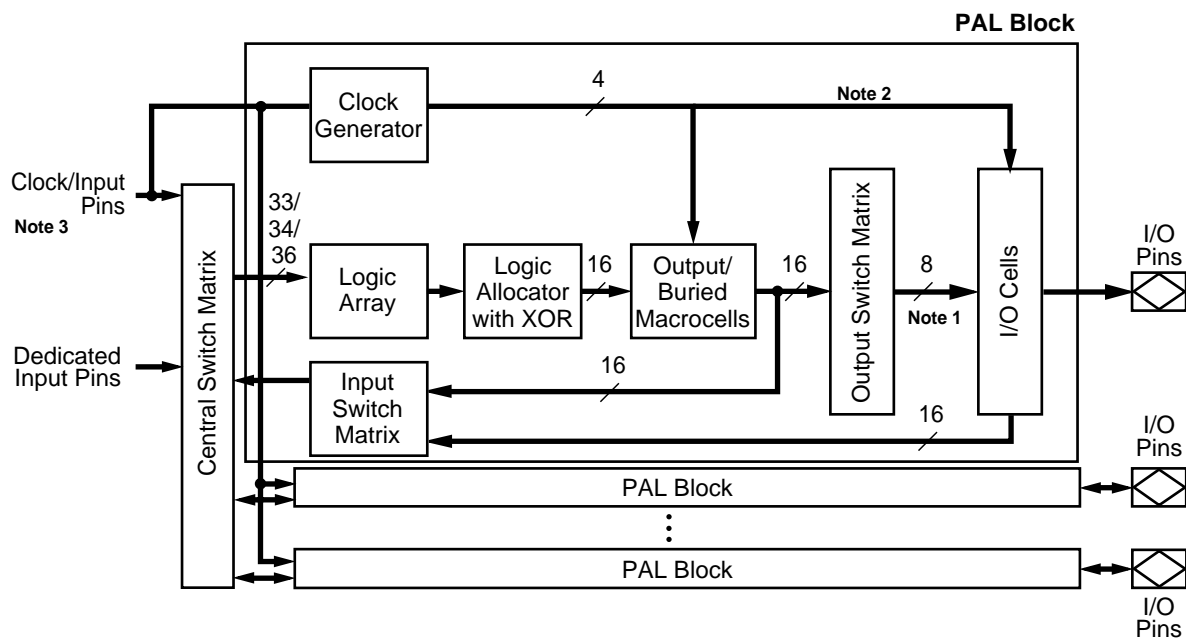


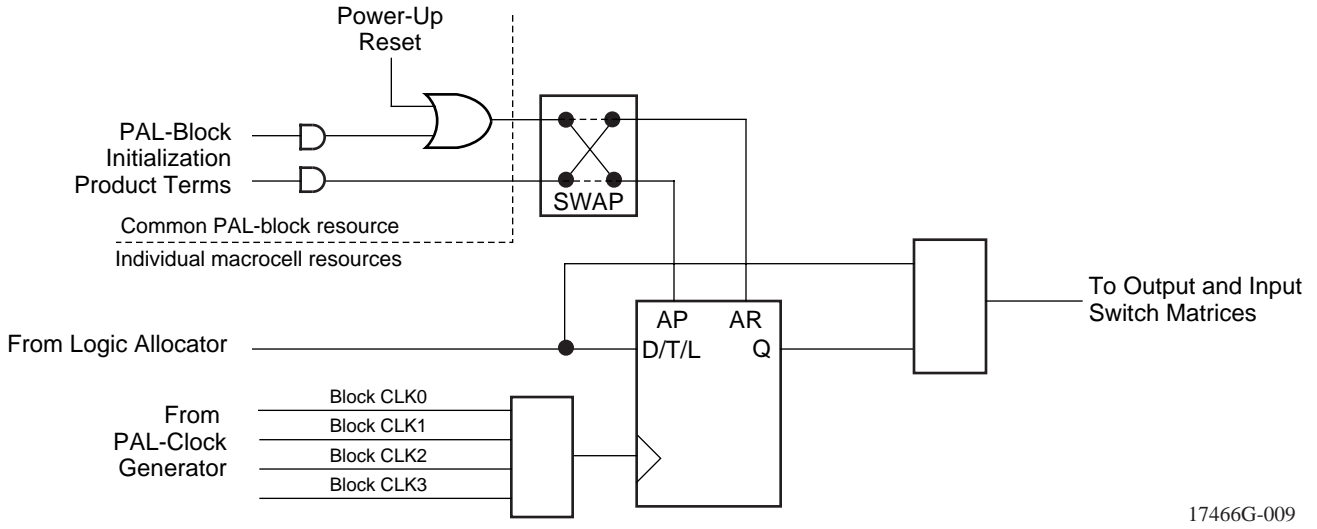
Figure 1. ispMACH 4A Block Diagram and PAL Block Structure

### Notes:

1. 16 for ispMACH 4A devices with 1:1 macrocell-I/O cell ratio (see next page).
2. Block clocks do not go to I/O cells in M4A(3,5)-32/32.
3. M4A(3,5)-192, M4A(3,5)-256, M4A3-384, and M4A3-512 have dedicated clock pins which cannot be used as inputs and do not connect to the central switch matrix.

## Macrocell

The macrocell consists of a storage element, routing resources, a clock multiplexer, and initialization control. The macrocell has two fundamental modes: synchronous and asynchronous (Figure 5). The mode chosen only affects clocking and initialization in the macrocell.



a. Synchronous mode

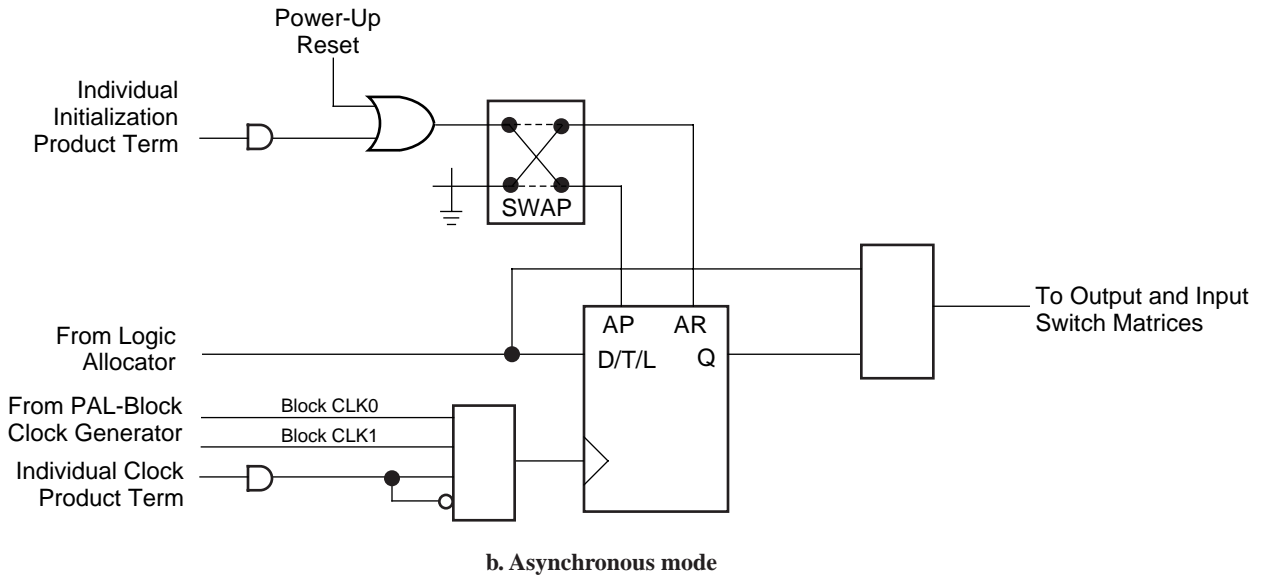
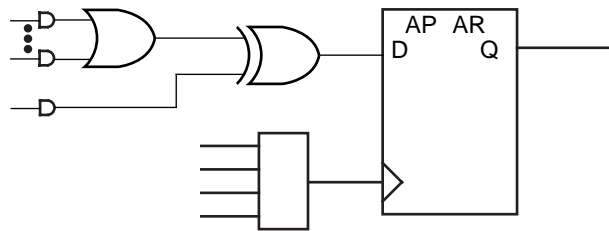


Figure 5. Macrocell

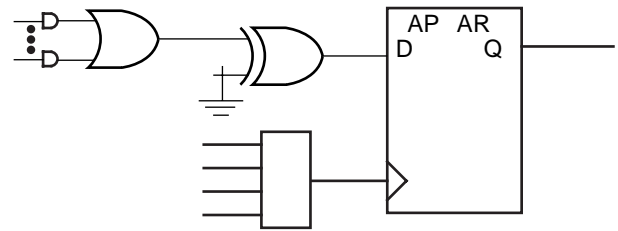
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In either mode, a combinatorial path can be used. For combinatorial logic, the synchronous mode will generally be used, since it provides more product terms in the allocator.

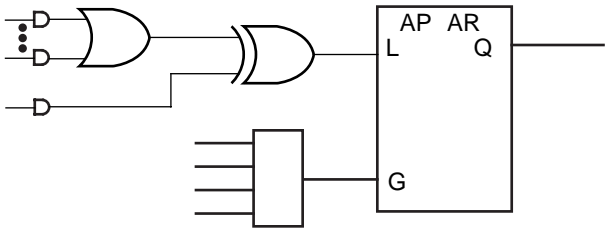
The flip-flop can be configured as a D-type or T-type latch. J-K or S-R registers can be synthesized. The primary flip-flop configurations are shown in Figure 6, although others are possible. Flip-flop functionality is defined in Table 8. Note that a J-K latch is inadvisable as it will cause oscillation if both J and K inputs are HIGH.



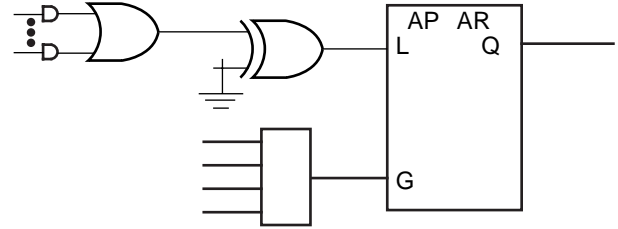
a. D-type with XOR



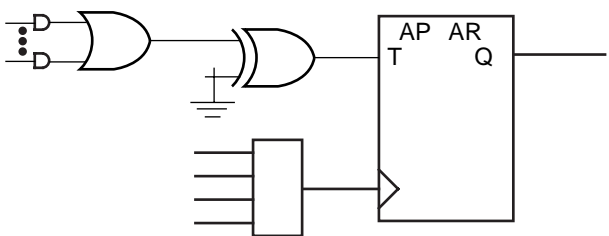
b. D-type with programmable D polarity



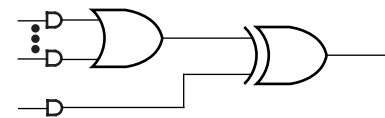
c. Latch with XOR



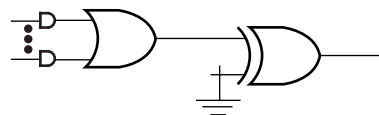
d. Latch with programmable D polarity



e. T-type with programmable T polarity



f. Combinatorial with XOR



g. Combinatorial with programmable polarity

Figure 6. Primary Macrocell Configurations

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**Table 10. Output Switch Matrix Combinations for ispMACH 4A Devices with 2:1 Macrocell-I/O Cell Ratio**

Macrocell	Routable to I/O Cells
M12, M13	I/03, I/04, I/05, I/06
M14, M15	I/04, I/05, I/06, I/07

I/O Cell	Available Macrocells
I/00	M0, M1, M2, M3, M4, M5, M6, M7
I/01	M2, M3, M4, M5, M6, M7, M8, M9
I/02	M4, M5, M6, M7, M8, M9, M10, M11
I/03	M6, M7, M8, M9, M10, M11, M12, M13
I/04	M8, M9, M10, M11, M12, M13, M14, M15
I/05	M0, M1, M10, M11, M12, M13, M14, M15
I/06	M0, M1, M2, M3, M12, M13, M14, M15
I/07	M0, M1, M2, M3, M4, M5, M14, M15

**Table 11. Output Switch Matrix Combinations for M4A3-256/160 and M4A3-256/192**

Macrocell	Routable to I/O Cells							
M0	I/00	I/01	I/02	I/03	I/04	I/05	I/06	I/07
M1	I/00	I/01	I/02	I/03	I/04	I/05	I/06	I/07
M2	I/00	I/01	I/02	I/03	I/04	I/05	I/06	I/07
M3	I/00	I/01	I/02	I/03	I/04	I/05	I/06	I/07
M4	I/00	I/01	I/02	I/03	I/04	I/05	I/06	I/07
M5	I/00	I/01	I/02	I/03	I/04	I/05	I/06	I/07
M6	I/00	I/01	I/02	I/03	I/04	I/05	I/06	I/07
M7	I/00	I/01	I/02	I/03	I/04	I/05	I/06	I/07
M8	I/08	I/09	I/010	I/011	I/012	I/013	I/014	I/015
M9	I/08	I/09	I/010	I/011	I/012	I/013	I/014	I/015
M10	I/08	I/09	I/010	I/011	I/012	I/013	I/014	I/015
M11	I/08	I/09	I/010	I/011	I/012	I/013	I/014	I/015
M12	I/08	I/09	I/010	I/011	I/012	I/013	I/014	I/015
M13	I/08	I/09	I/010	I/011	I/012	I/013	I/014	I/015
M14	I/08	I/09	I/010	I/011	I/012	I/013	I/014	I/015
M15	I/08	I/09	I/010	I/011	I/012	I/013	I/014	I/015

I/O Cell	Available Macrocells							
I/00	M0	M1	M2	M3	M4	M5	M6	M7
I/01	M0	M1	M2	M3	M4	M5	M6	M7
I/02	M0	M1	M2	M3	M4	M5	M6	M7
I/03	M0	M1	M2	M3	M4	M5	M6	M7
I/04	M0	M1	M2	M3	M4	M5	M6	M7
I/05	M0	M1	M2	M3	M4	M5	M6	M7
I/06	M0	M1	M2	M3	M4	M5	M6	M7
I/07	M0	M1	M2	M3	M4	M5	M6	M7

**Table 11. Output Switch Matrix Combinations for M4A3-256/160 and M4A3-256/192**

Macrocell	Routable to I/O Cells							
I/O8	M8	M9	M10	M11	M12	M13	M14	M15
I/O9	M8	M9	M10	M11	M12	M13	M14	M15
I/O10	M8	M9	M10	M11	M12	M13	M14	M15
I/O11	M8	M9	M10	M11	M12	M13	M14	M15
I/O12	M8	M9	M10	M11	M12	M13	M14	M15
I/O13	M8	M9	M10	M11	M12	M13	M14	M15
I/O14	M8	M9	M10	M11	M12	M13	M14	M15
I/O15	M8	M9	M10	M11	M12	M13	M14	M15

**Table 12. Output Switch Matrix Combinations for M4A(3,5)-32/32**

Macrocell	Routable to I/O Cells
M0, M1, M2, M3, M4, M5, M6, M7	I/O0, I/O1, I/O2, I/O3, I/O4, I/O5, I/O6, I/O7
M8, M9, M10, M11, M12, M13, M14, M15	I/O8, I/O9, I/O10, I/O11, I/O12, I/O13, I/O14, I/O15

I/O Cell	Available Macrocells
I/O0, I/O1, I/O2, I/O3, I/O4, I/O5, I/O6, I/O7	M0, M1, M2, M3, M4, M5, M6, M7
I/O8, I/O9, I/O10, I/O11, I/O12, I/O13, I/O14, I/O15	M8, M9, M10, M11, M12, M13, M14, M15

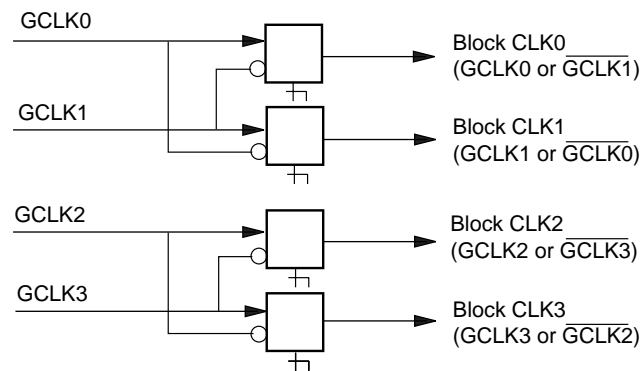
**Table 13. Output Switch Matrix Combinations for M4A3-64/64**

Macrocell	Routable to I/O Cells
M0, M1	I/O0, I/O1, I/O10, I/O11, I/O12, I/O13, I/O14, I/O15
M2, M3	I/O0, I/O1, I/O2, I/O3, I/O12, I/O13, I/O14, I/O15
M4, M5	I/O0, I/O1, I/O2, I/O3, I/O4, I/O5, I/O14, I/O15
M6, M7	I/O0, I/O1, I/O2, I/O3, I/O4, I/O5, I/O6, I/O7
M8, M9	I/O2, I/O3, I/O4, I/O5, I/O6, I/O7, I/O8, I/O9
M10, M11	I/O4, I/O5, I/O6, I/O7, I/O8, I/O9, I/O10, I/O11
M12, M13	I/O6, I/O7, I/O8, I/O9, I/O10, I/O11, I/O12, I/O13
M14, M15	I/O8, I/O9, I/O10, I/O11, I/O12, I/O13, I/O14, I/O15

I/O Cell	Available Macrocells
I/O0, I/O1	M0, M1, M2, M3, M4, M5, M6, M7
I/O2, I/O3	M2, M3, M4, M5, M6, M7, M8, M9
I/O4, I/O5	M4, M5, M6, M7, M8, M9, M10, M11
I/O6, I/O7	M6, M7, M8, M9, M10, M11, M12, M13
I/O8, I/O9	M8, M9, M10, M11, M12, M13, M14, M15
I/O10, I/O11	M0, M1, M10, M11, M12, M13, M14, M15
I/O12, I/O13	M0, M1, M2, M3, M12, M13, M14, M15
I/O14, I/O15	M0, M1, M2, M3, M4, M5, M14, M15

## PAL Block Clock Generation

Each ispMACH 4A device has four clock pins that can also be used as inputs. These pins drive a clock generator in each PAL block (Figure 14). The clock generator provides four clock signals that can be used anywhere in the PAL block. These four PAL block clock signals can consist of a large number of combinations of the true and complement edges of the global clock signals. Table 14 lists the possible combinations.



17466G-004

**Figure 14. PAL Block Clock Generator<sup>1</sup>**

1. *M4A(3,5)-32/32 and M4A(3,5)-64/32 have only two clock pins, GCLK0 and GCLK1. GCLK2 is tied to GCLK0, and GCLK3 is tied to GCLK1.*

**Table 14. PAL Block Clock Combinations<sup>1</sup>**

Block CLK0	Block CLK1	Block CLK2	Block CLK3
GCLK0	GCLK1	X	X
$\overline{GCLK1}$	GCLK1	X	X
GCLK0	$\overline{GCLK0}$	X	X
$\overline{GCLK1}$	$\overline{GCLK0}$	X	X
X	X	GCLK2 (GCLK0)	GCLK3 (GCLK1)
X	X	$\overline{GCLK3}$ ( $\overline{GCLK1}$ )	GCLK3 (GCLK1)
X	X	GCLK2 (GCLK0)	$\overline{GCLK2}$ ( $\overline{GCLK0}$ )
X	X	$\overline{GCLK3}$ ( $\overline{GCLK1}$ )	$\overline{GCLK2}$ ( $\overline{GCLK0}$ )

**Note:**

1. *Values in parentheses are for the M4A(3,5)-32/32 and M4A(3,5)-64/32.*

This feature provides high flexibility for partitioning state machines and dual-phase clocks. It also allows latches to be driven with either polarity of latch enable, and in a master-slave configuration.

weakly pulled up. For the circuit diagram, please refer to the document entitled *MACH Endurance Characteristics* on the Lattice Data Book CD-ROM or Lattice web site.

## **POWER MANAGEMENT**

Each individual PAL block in ispMACH 4A devices features a programmable low-power mode, which results in power savings of up to 50%. The signal speed paths in the low-power PAL block will be slower than those in the non-low-power PAL block. This feature allows speed critical paths to run at maximum frequency while the rest of the signal paths operate in the low-power mode.

## **PROGRAMMABLE SLEW RATE**

Each ispMACH 4A device I/O has an individually programmable output slew rate control bit. Each output can be individually configured for the higher speed transition (3 V/ns) or for the lower noise transition (1 V/ns). For high-speed designs with long, unterminated traces, the slow-slew rate will introduce fewer reflections, less noise, and keep ground bounce to a minimum. For designs with short traces or well terminated lines, the fast slew rate can be used to achieve the highest speed. The slew rate is adjusted independent of power.

## **POWER-UP RESET/SET**

All flip-flops power up to a known state for predictable system initialization. If a macrocell is configured to SET on a signal from the control generator, then that macrocell will be SET during device power-up. If a macrocell is configured to RESET on a signal from the control generator or is not configured for set/reset, then that macrocell will RESET on power-up. To guarantee initialization values, the  $V_{CC}$  rise must be monotonic, and the clock must be inactive until the reset delay time has elapsed.

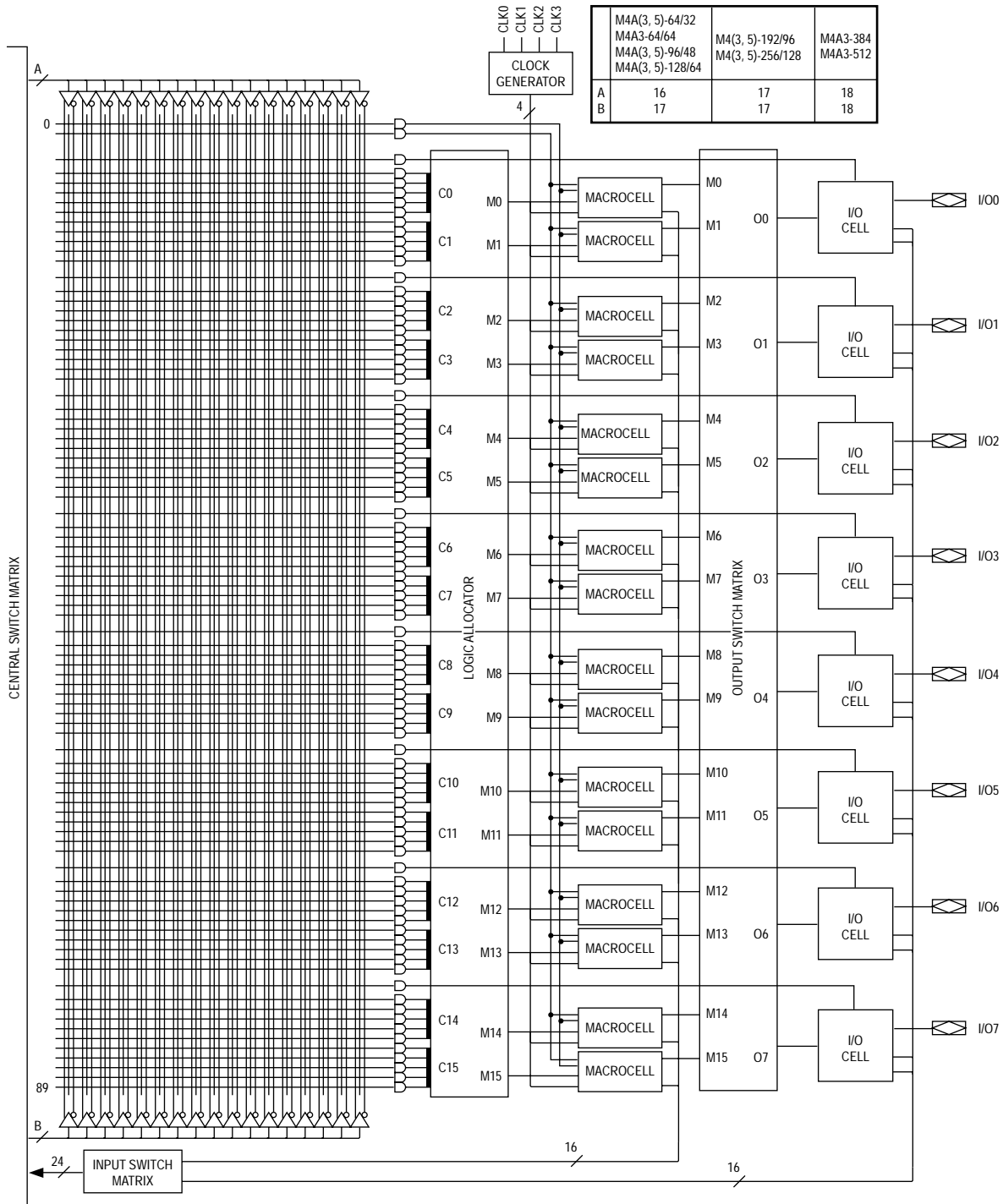
## **SECURITY BIT**

A programmable security bit is provided on the ispMACH 4A devices as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, this bit defeats readback of the programmed pattern by a device programmer, securing proprietary designs from competitors. Programming and verification are also defeated by the security bit. The bit can only be reset by erasing the entire device.

## **HOT SOCKETING**

ispMACH 4A devices are well-suited for those applications that require hot socketing capability. Hot socketing a device requires that the device, when powered down, can tolerate active signals on the I/Os and inputs without being damaged. Additionally, it requires that the effects of the powered-down MACH devices be minimal on active signals.





**Figure 16. PAL Block for ispMACH 4A with 2:1 Macrocell - I/O Cell Ratio**

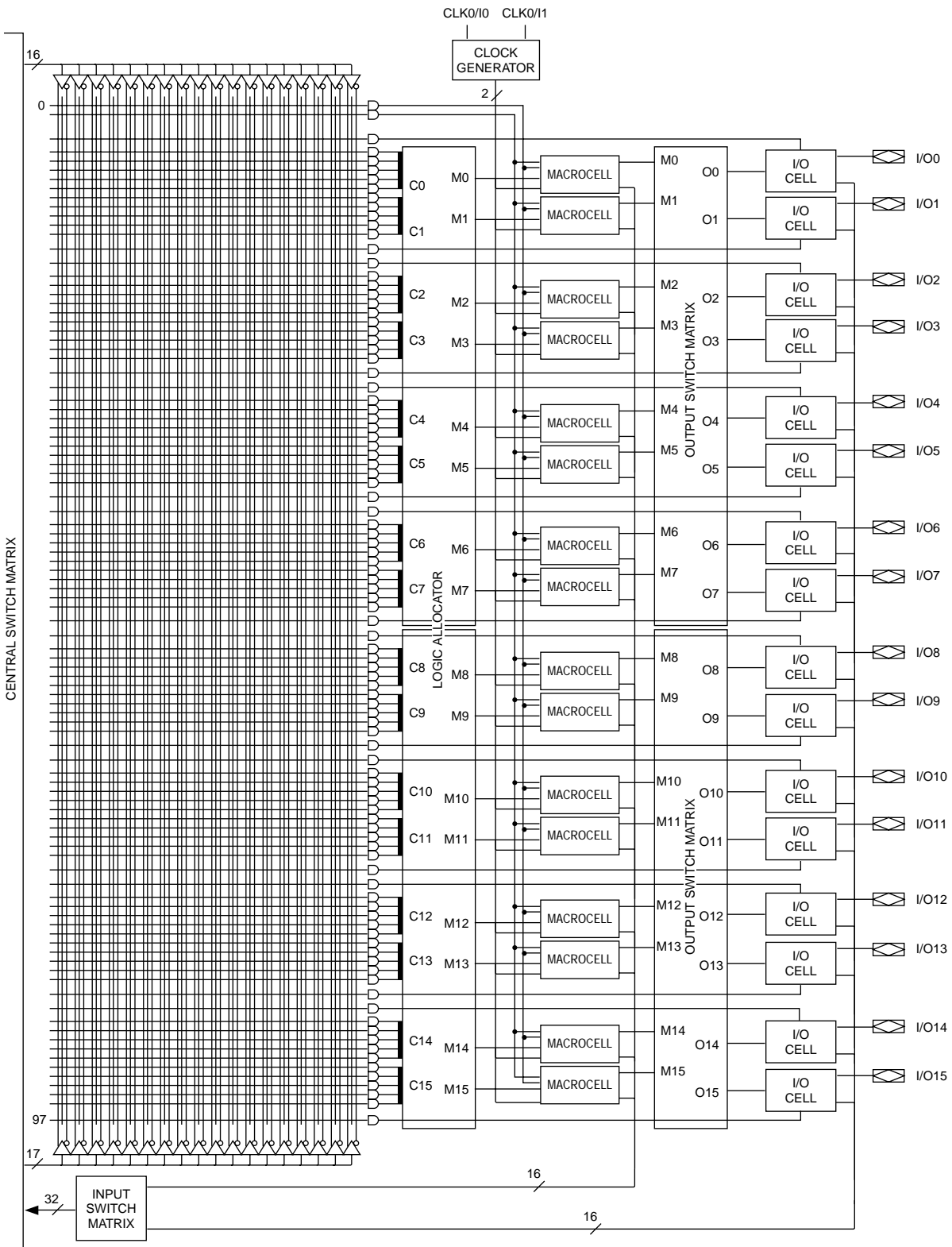
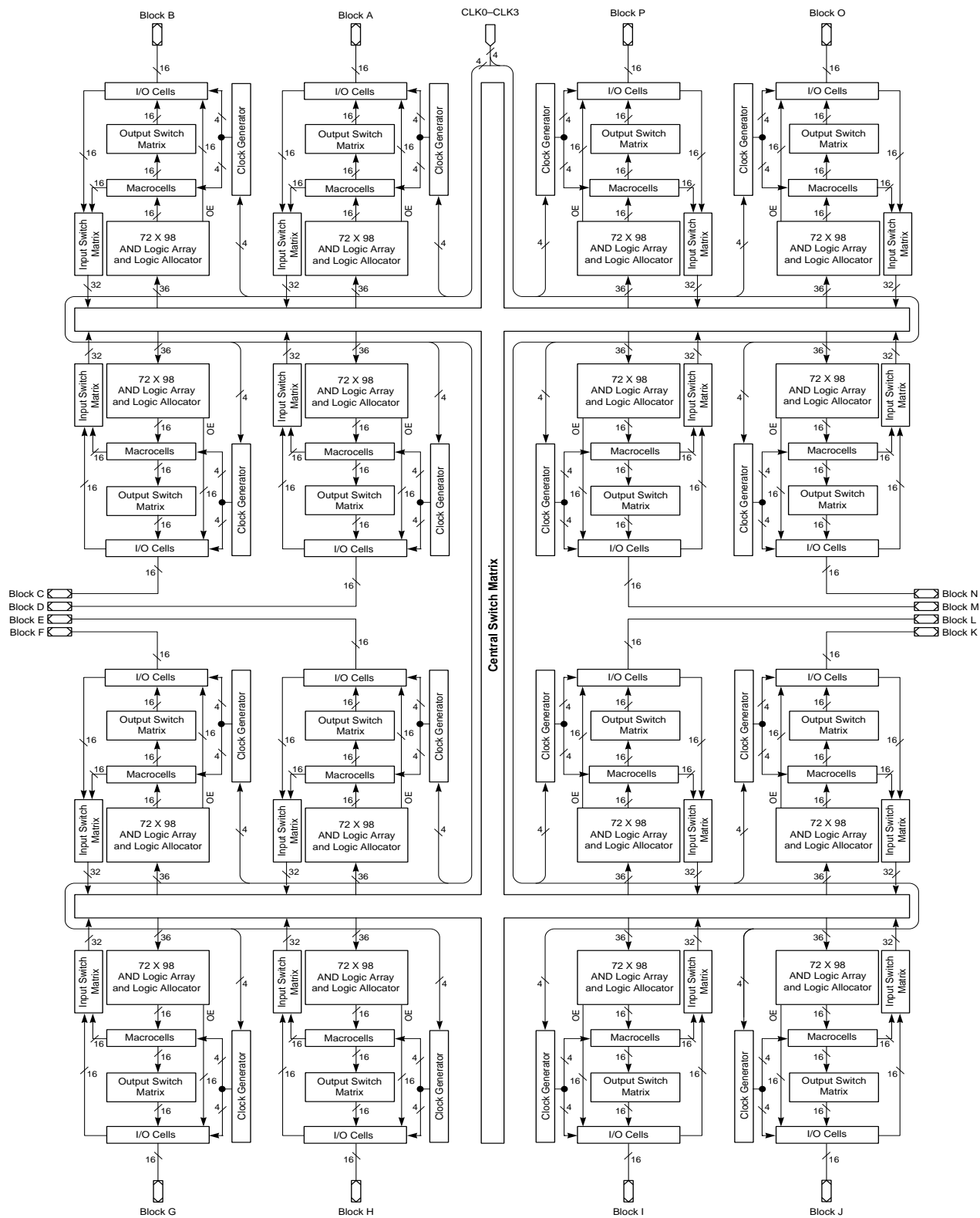


Figure 18. PAL Block for M4A (3,5)-32/32

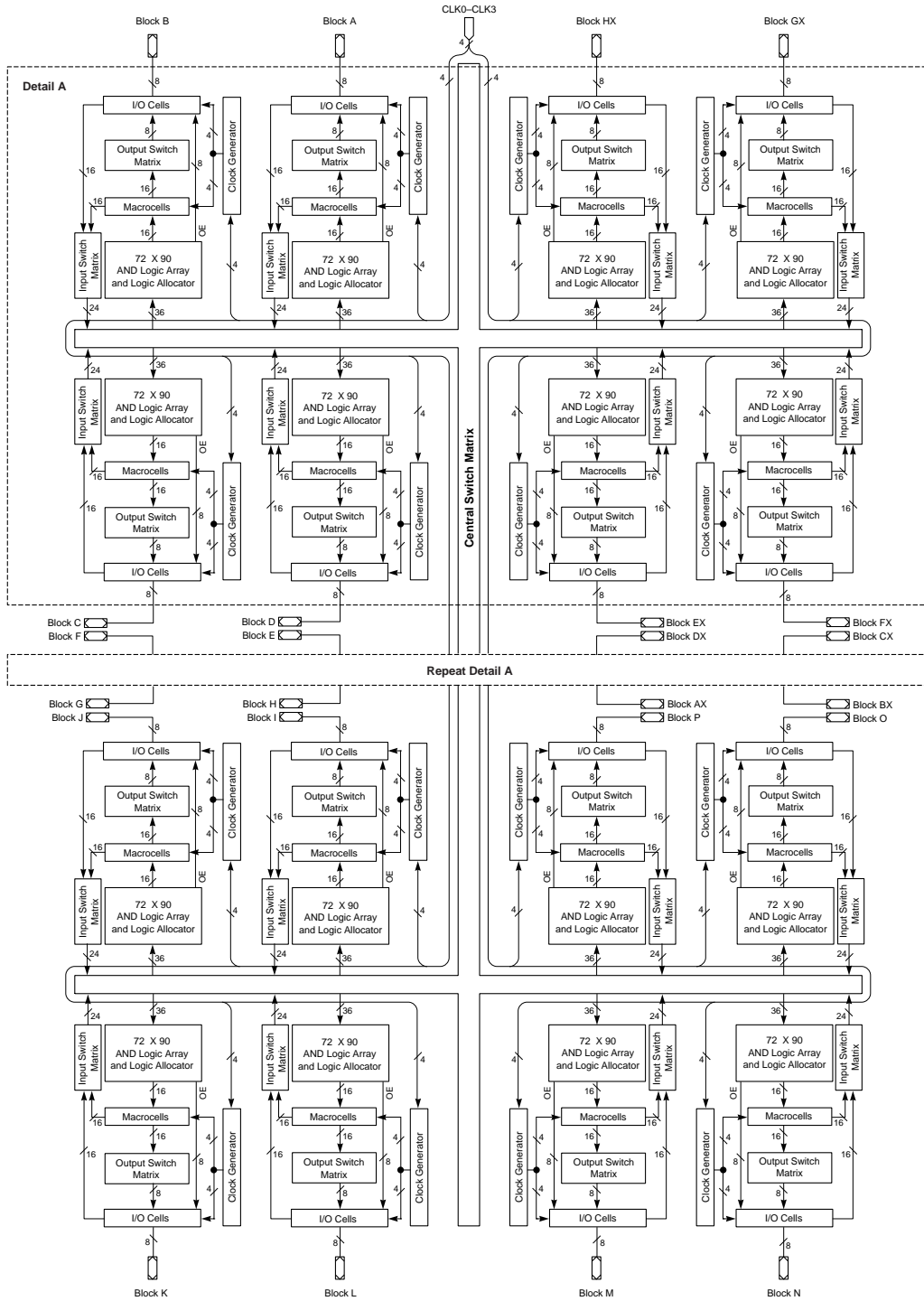
17466H-042

# BLOCK DIAGRAM – M4A3-256/160, M4A3-256/192



17466G-050

# BLOCK DIAGRAM – M4A3-384/160, M4A3-384/192



## ABSOLUTE MAXIMUM RATINGS

### M4A3

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-55°C to +100°C
Device Junction Temperature	+130°C
Supply Voltage with Respect to Ground	-0.5 V to +4.5 V
DC Input Voltage	-0.5 V to 6.0 V
Static Discharge Voltage	2000 V
Latchup Current ( $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ )	200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

## OPERATING RANGES

### Commercial (C) Devices

Ambient Temperature ( $T_A$ )	Operating in Free Air	0°C to +70°C
Supply Voltage ( $V_{CC}$ )	with Respect to Ground	+3.0 V to +3.6 V

### Industrial (I) Devices

Ambient Temperature ( $T_A$ )	Operating in Free Air	-40°C to +85°C
Supply Voltage ( $V_{CC}$ )	with Respect to Ground	+3.0 V to +3.6 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

## 3.3-V DC CHARACTERISTICS OVER OPERATING RANGES

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
$V_{OH}$	Output HIGH Voltage	$V_{CC} = \text{Min}$ $V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -100 \mu\text{A}$	$V_{CC} - 0.2$		V
			$I_{OH} = -3.2 \text{ mA}$	2.4		V
$V_{OL}$	Output LOW Voltage	$V_{CC} = \text{Min}$ $V_{IN} = V_{IH}$ or $V_{IL}$ (Note 1)	$I_{OL} = 100 \mu\text{A}$		0.2	V
			$I_{OL} = 24 \text{ mA}$		0.5	V
$V_{IH}$	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs	2.0		5.5	V
$V_{IL}$	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs	-0.3		0.8	V
$I_{IH}$	Input HIGH Leakage Current	$V_{IN} = 3.6 \text{ V}$ , $V_{CC} = \text{Max}$ (Note 2)			5	$\mu\text{A}$
$I_{IL}$	Input LOW Leakage Current	$V_{IN} = 0 \text{ V}$ , $V_{CC} = \text{Max}$ (Note 2)			-5	$\mu\text{A}$
$I_{OZH}$	Off-State Output Leakage Current HIGH	$V_{OUT} = 3.6 \text{ V}$ , $V_{CC} = \text{Max}$ $V_{IN} = V_{IH}$ or $V_{IL}$ (Note 2)			5	$\mu\text{A}$
$I_{OZL}$	Off-State Output Leakage Current LOW	$V_{OUT} = 0 \text{ V}$ , $V_{CC} = \text{Max}$ $V_{IN} = V_{IH}$ or $V_{IL}$ (Note 2)			-5	$\mu\text{A}$
$I_{SC}$	Output Short-Circuit Current	$V_{OUT} = 0.5 \text{ V}$ , $V_{CC} = \text{Max}$ (Note 3)	-15		-160	mA

#### Notes:

- Total  $I_{OL}$  for one PAL block should not exceed 64 mA.
- I/O pin leakage is the worst case of  $I_{IL}$  and  $I_{OZL}$  (or  $I_{IH}$  and  $I_{OZH}$ ).
- Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

#### Notes:

- See "MACH Switching Test Circuit" document on the Literature Download page of the Lattice web site.
- This parameter does not apply to flip-flops in the emulated mode since the feedback path is required for emulation.

## ispMACH 4A TIMING PARAMETERS OVER OPERATING RANGES<sup>1</sup>

		-5		-55		-6		-65		-7		-10		-12		-14		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
<b>Combinatorial Delay:</b>																		
$t_{PDi}$	Internal combinatorial propagation delay		3.5		4.0		4.3		4.5		5.0		7.0		9.0		11.0	ns
$t_{PD}$	Combinatorial propagation delay		5.0		5.5		6.0		6.5		7.5		10.0		12.0		14.0	ns
<b>Registered Delays:</b>																		
$t_{SS}$	Synchronous clock setup time, D-type register	3.0		3.5		3.5		3.5		5.0		5.5		7.0		10.0		ns
$t_{SST}$	Synchronous clock setup time, T-type register	4.0		4.0		4.0		4.0		6.0		6.5		8.0		11.0		ns
$t_{SA}$	Asynchronous clock setup time, D-type register	2.5		2.5		2.5		3.0		3.5		4.0		5.0		8.0		ns
$t_{SAT}$	Asynchronous clock setup time, T-type register	3.0		3.0		3.0		3.5		4.5		5.0		6.0		9.0		ns
$t_{HS}$	Synchronous clock hold time	0.0		0.0		0.0		0.0		0.0		0.0		0.0		0.0		ns
$t_{HA}$	Asynchronous clock hold time	2.5		2.5		2.5		3.0		3.5		4.0		5.0		8.0		ns
$t_{COSi}$	Synchronous clock to internal output		2.5		2.5		2.8		3.0		3.0		3.0		3.5		3.5	ns
$t_{COS}$	Synchronous clock to output		4.0		4.0		4.5		5.0		5.5		6.0		6.5		6.5	ns
$t_{COAi}$	Asynchronous clock to internal output		5.0		5.0		5.0		5.0		6.0		8.0		10.0		12.0	ns
$t_{COA}$	Asynchronous clock to output		6.5		6.5		6.8		7.0		8.5		11.0		13.0		15.0	ns
<b>Latched Delays:</b>																		
$t_{SSL}$	Synchronous latch setup time	4.0		4.0		4.0		4.5		6.0		7.0		8.0		10.0		ns
$t_{SAL}$	Asynchronous latch setup time	3.0		3.0		3.5		3.5		4.0		4.0		5.0		8.0		ns
$t_{HSL}$	Synchronous latch hold time	0.0		0.0		0.0		0.0		0.0		0.0		0.0		0.0		ns
$t_{HAL}$	Asynchronous latch hold time	3.0		3.0		3.5		3.5		4.0		4.0		5.0		8.0		ns
$t_{PDLi}$	Transparent latch to internal output		5.5		5.5		5.8		6.0		7.5		9.0		11.0		12.0	ns
$t_{PDL}$	Propagation delay through transparent latch to output		7.0		7.0		7.5		8.0		10.0		12.0		14.0		15.0	ns
$t_{GOSi}$	Synchronous gate to internal output		3.0		3.0		3.0		3.0		3.5		4.5		7.0		8.0	ns
$t_{GOS}$	Synchronous gate to output		4.5		4.5		4.8		5.0		6.0		7.5		10.0		11.0	ns
$t_{GOAi}$	Asynchronous gate to internal output		6.0		6.0		6.0		6.0		8.5		10.0		13.0		15.0	ns
$t_{GOA}$	Asynchronous gate to output		7.5		7.5		7.8		8.0		11.0		13.0		16.0		18.0	ns
<b>Input Register Delays:</b>																		
$t_{SIRS}$	Input register setup time	1.5		1.5		2.0		2.0		2.0		2.0		2.0		2.0		ns
$t_{HIRS}$	Input register hold time	2.5		2.5		3.0		3.0		3.0		3.0		3.0		4.0		ns
$t_{ICOSi}$	Input register clock to internal feedback		3.0		3.0		3.0		3.0		3.5		4.5		6.0		6.0	ns
<b>Input Latch Delays:</b>																		
$t_{SIL}$	Input latch setup time	1.5		1.5		1.5		2.0		2.0		2.0		2.0		2.0		ns
$t_{HIL}$	Input latch hold time	2.5		2.5		2.5		3.0		3.0		3.0		3.0		4.0		ns
$t_{IGOSi}$	Input latch gate to internal feedback		3.5		3.5		3.8		4.0		4.0		4.0		4.0		5.0	ns
$t_{PDILi}$	Transparent input latch to internal feedback		1.5		1.5		1.5		1.5		2.0		2.0		2.0		2.0	ns

# 100-PIN TQFP CONNECTION DIAGRAM (M4A3-64/64 AND M4A(3,5)-128/64)

## Top View



## PIN DESIGNATIONS

CLK/I = Clock or Input

GND = Ground

I = Input

I/O = Input/Output

V<sub>CC</sub> = Supply Voltage

TDI = Test Data In

TCK = Test Clock

TMS = Test Mode Select

TDO = Test Data Out

TRST = Test Reset

ENABLE = Program

# 100-BALL caBGA CONNECTION DIAGRAM (M4A3-128/64)

## Bottom View

### 100-Ball caBGA

	10	9	8	7	6	5	4	3	2	1	
A	GND	I/O63 H7	I/O60 H4	I/O57 H1	GND	GND	I/O1 A1	I/O4 A4	I/O7 A7	GND	A
B	$\overline{\text{TRST}}$	GND	I/O61 H5	I5	VCC	I/O0 A0	I/O6 A6	GND	TDI	I/O15 B7	B
C	I/O53 G5	TDO	I/O62 H6	I/O58 H2	I/O56 H0	I/O2 A2	GND	I/O14 B6	I/O13 B5	I/O12 B4	C
D	I/O50 G2	I/O55 G7	GND	I/O59 H3	I/O3 A3	I/O5 A5	I/O11 B3	I/O10 B2	CLK0/I0	I/O9 B1	D
E	CLK3/I4	I/O49 G1	I/O51 G3	I/O54 G6	VCC	I/O16 C0	I/O20 C4	I/O8 B0	VCC	GND	E
F	GND	VCC	I/O40 F0	I/O52 G4	I/O48 G0	VCC	I/O22 C6	I/O19 C3	I/O17 C1	CLK1/I1	F
G	I/O41 F1	CLK2/I3	I/O42 F2	I/O43 F3	I/O37 E5	I/O35 E3	I/O27 D3	GND	I/O23 C7	I/O18 C2	G
H	I/O44 F4	I/O45 F5	I/O46 F6	GND	I/O34 E2	I/O24 D0	I/O26 D2	I/O30 D6	TCK	I/O21 C5	H
J	I/O47 F7	$\overline{\text{ENABLE}}$	GND	I/O38 E6	I/O32 E0	VCC	I2	I/O29 D5	GND	TMS	J
K	GND	I/O39 E7	I/O36 E4	I/O33 E1	GND	GND	I/O25 D1	I/O28 D4	I/O31 D7	GND	K

#### PIN DESIGNATIONS

CLK = Clock  
 GND = Ground  
 I = Input  
 I/O = Input/Output  
 N/C = No Connect  
 VCC = Supply Voltage  
 TDI = Test Data In  
 TCK = Test Clock  
 TMS = Test Mode Select  
 TDO = Test Data Out  
 $\overline{\text{TRST}}$  = Test Reset  
 ENABLE = Program



17466G-100cabga



# 144-PIN TQFP CONNECTION DIAGRAM (M4A(3,5)-192/96)

## Top View



17466G-033

## PIN DESIGNATIONS

- CLK = Clock
- GND = Ground
- I = Input
- I/O = Input/Output
- V<sub>CC</sub> = Supply Voltage
- TDI = Test Data In
- TCK = Test Clock
- TMS = Test Mode Select
- TDO = Test Data Out

# 144-BALL FPBGA CONNECTION DIAGRAM (M4A3-192/96)

## Bottom View

144-Ball fpBGA

	12	11	10	9	8	7	6	5	4	3	2	1	
<b>A</b>	GND	I/O72 L7	I/O76 L3	I13	GBCLK3	I0	I/O82 A2	I/O86 A6	I/O88 B0	I/O93 B5	I/O95 B7	GND	<b>A</b>
<b>B</b>	GND	I/O73 L6	I/O77 L2	I/O79 L0	VCC	I1	I/O83 A3	I/O87 A7	I/O90 B2	I/O94 B6	I/O0 D7	TDI	<b>B</b>
<b>C</b>	GND	TD0	I/O74 L5	I14	GND	I/O80 A0	I/O84 A4	GND	I/O92 B4	I/O1 D6	I/O4 D3	I/O3 D4	<b>C</b>
<b>D</b>	I/O67 K4	I/O69 K2	I/O71 K0	I/O75 L4	GBCLK0	I/O81 A1	VCC	I/O91 B3	I/O2 D5	I2	I/O6 D1	I/O7 D0	<b>D</b>
<b>E</b>	I12	I/O64 K7	I/O66 K5	I/O70 K1	I/O78 L1	I/O85 A5	I/O89 B1	I/O5 D2	I/O8 C7	I4	GND	VCC	<b>E</b>
<b>F</b>	I10	I11	GND	I/O65 K6	I/O68 K3	I15	I3	GND	I/O12 C3	I/O11 C4	I/O10 C5	I/O9 C6	<b>F</b>
<b>G</b>	I/O60 J3	I/O61 J2	I/O62 J1	I/O63 J0	VCC	GND	I7	I/O20 E3	I/O17 E6	I/O15 C0	I/O14 C1	I/O13 C2	<b>G</b>
<b>H</b>	I/O56 J7	I/O57 J6	I/O58 J5	I/O59 J4	I/O53 I2	I/O41 H1	I/O37 G5	I/O30 F1	I/O22 E1	I/O18 E5	I/O16 E7	VCC	<b>H</b>
<b>J</b>	I/O55 I0	I/O54 I1	VCC	I/O50 I5	I/O43 H3	VCC	I/O33 G1	GBCLK2	I/O27 F4	I/O23 E0	I/O21 E2	I/O19 E4	<b>J</b>
<b>K</b>	I/O51 I4	I/O52 I3	I/O49 I6	I/O44 H4	GND	I/O36 G4	I/O32 G0	VCC	I6	I/O26 F5	TCK	TMS	<b>K</b>
<b>L</b>	GND	I/O48 I7	I/O46 H6	I/O42 H2	I/O39 G7	I/O35 G3	I9	GND	I/O31 F0	I/O29 F2	I/O25 F6	GND	<b>L</b>
<b>M</b>	GND	I/O47 H7	I/O45 H5	I/O40 H0	I/O38 G6	I/O34 G2	I8	GBCLK1	I5	I/O28 F3	I/O24 F7	GND	<b>M</b>
	12	11	10	9	8	7	6	5	4	3	2	1	

### PIN DESIGNATIONS

- CLK = Clock
- GND = Ground
- I = Input
- I/O = Input/Output
- N/C = No Connect
- VCC = Supply Voltage
- TDI = Test Data In
- TCK = Test Clock
- TMS = Test Mode Select
- TD0 = Test Data Out



# 208-PIN PQFP CONNECTION DIAGRAM (M4A(3,5)-256/128 AND M4A3-256/160)

Top View

208-Pin PQFP



17466G-044

## 256-BALL fpBGA CONNECTION DIAGRAM (M4A3-256/192)

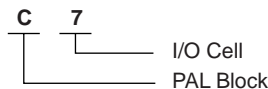
### Bottom View

#### 256-Ball fpBGA

	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	I/O167 N15	I/O181 O13	I/O180 O12	I/O177 O9	I/O174 O6	I/O172 O4	I/O191 P14	I/O186 P4	I/O1 A2	I/O3 A6	GCLK0	I/O9 B1	I/O13 B5	I/O15 B7	I/O18 B10	I/O20 B12	A
B	I/O165 N13	I/O166 N14	I/O182 O14	I/O179 O11	I/O175 O7	I/O173 O5	I/O168 O0	I/O187 P6	I/O0 A0	I/O5 A10	I/O7 A14	I/O10 B2	I/O16 B8	I/O19 B11	I/O21 B13	NC	B
C	I/O163 N11	I/O164 N12	NC	I/O183 O15	I/O178 O10	I/O170 O2	I/O171 O3	I/O189 P10	I/O184 P0	I/O6 A12	I/O12 B4	I/O14 B6	I/O23 B15	I/O22 B14	TDI	I/O39 C15	C
D	I/O158 N6	I/O159 N7	TDO	GND	GND	VCC	GND	VCC	GND	GND	VCC	GND	VCC	I/O17 B9	I/O38 C14	I/O37 C13	D
E	I/O156 N4	NC	I/O162 N10	VCC	I/O160 N8	I/O161 N9	I/O190 P12	GCLK3	I/O188 P8	I/O2 A4	I/O8 B0	NC	GND	I/O36 C12	I/O35 C11	I/O31 C7	E
F	I/O152 N0	I/O157 N5	I/O155 N3	GND	I/O154 N2	I/O153 N1	I/O176 O8	I/O169 O1	I/O185 P2	I/O4 A8	I/O11 B3	I/O34 C10	VCC	I/O32 C8	I/O30 C6	I/O29 C5	F
G	I/O147 M6	I/O150 M12	I/O149 M10	VCC	I/O148 M8	I/O151 M14	VCC	GND	GND	VCC	I/O33 C9	I/O28 C4	GND	I/O26 C2	I/O25 C1	I/O47 D14	G
H	I/O144 M0	I/O146 M4	I/O145 OM2	GND	I/O136 L0	I/O137 L2	GND	VCC	VCC	GND	I/O27 C3	I/O24 C0	VCC	I/O44 D8	I/O43 D6	I/O42 D4	H
J	I/O138 L4	I/O139 L6	I/O140 L8	GND	I/O142 L12	I/O141 L10	GND	VCC	VCC	GND	I/O46 D12	I/O45 D10	GND	I/O49 E2	I/O48 E0	I/O50 E4	J
K	I/O143 L14	I/O120 K0	I/O121 K1	VCC	I/O123 K3	I/O122 K2	VCC	GND	GND	VCC	I/O41 D2	I/O40 D0	VCC	I/O55 E14	I/O54 E12	I/O56 F0	K
L	I/O124 K4	I/O125 K5	I/O127 K7	GND	I/O130 K10	I/O126 K6	I/O98 I4	I/O91 H6	I/O75 G3	I/O77 G5	I/O52 E8	I/O51 E6	GND	I/O59 F3	I/O60 F4	I/O57 F1	L
M	I/O128 K8	I/O129 K9	I/O131 K11	GND	I/O107 J3	I/O105 J1	I/O100 I8	I/O90 H4	I/O74 G2	I/O80 G8	I/O83 G11	I/O53 E10	VCC	I/O68 F12	I/O63 F7	I/O58 F2	M
N	I/O132 K12	I/O133 K13	I/O135 K15	VCC	GND	VCC	GND	VCC	GND	GND	VCC	GND	GND	TCK	I/O64 F8	I/O61 F5	N
P	I/O134 K14	I/O117 J13	I/O118 J14	I/O119 J15	I/O108 J4	I/O106 J2	I/O101 I10	I/O89 H2	I/O93 H10	I/O94 H12	I/O79 G7	I/O84 G12	I/O87 G15	TMS	I/O65 F9	I/O62 F6	P
R	I/O116 J12	I/O115 J11	I/O112 J8	I/O111 J7	I/O104 J0	I/O102 I12	I/O99 I6	I/O96 I0	I/O92 H8	I/O72 G0	I/O76 G4	I/O81 G9	I/O85 G13	I/O71 F15	I/O67 F11	I/O66 F10	R
T	I/O114 J10	I/O113 J9	I/O110 J6	I/O109 J5	I/O103 I14	GCLK2	I/O97 I2	I/O88 H0	GCLK1	I/O95 H14	I/O73 G1	I/O78 G6	I/O82 G10	I/O86 G14	I/O70 F14	I/O69 F13	T

#### PIN DESIGNATIONS

CLK = Clock  
 GND = Ground  
 I = Input  
 I/O = Input/Output  
 N/C = No Connect  
 VCC = Supply Voltage  
 TDI = Test Data In  
 TCK = Test Clock  
 TMS = Test Mode Select  
 TDO = Test Data Out



17466G-047

# 256-BALL fpBGA CONNECTION DIAGRAM (M4A3-512/192)

## Bottom View

### 256-Ball fpBGA

	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	I/O159 KX7	I/O181 OX5	I/O180 OX4	I/O177 OX1	I/O174 NX6	I/O172 NX4	I/O191 PX7	I/O186 PX2	I/O1 A1	I/O3 A3	CLK0	I/O17 C1	I/O21 C5	I/O23 C7	I/O10 B2	I/O12 B4	A
B	I/O157 KX5	I/O158 KX6	I/O182 OX6	I/O179 OX3	I/O175 NX7	I/O173 NX5	I/O168 NX0	I/O187 PX3	I/O0 A0	I/O5 A5	I/O7 A7	I/O18 C2	I/O8 B0	I/O11 B3	I/O13 B5	N/C	B
C	I/O155 KX3	I/O156 KX4	N/C	I/O183 OX7	I/O178 OX2	I/O170 NX2	I/O171 NX3	I/O189 PX5	I/O184 PX0	I/O6 A6	I/O20 C4	I/O22 C6	I/O15 B7	I/O14 B6	TDI	I/O39 F7	C
D	I/O150 JX6	I/O151 JX7	TDO	GND	GND	VCC	GND	VCC	GND	GND	VCC	GND	VCC	I/O9 B1	I/O38 F6	I/O37 F5	D
E	I/O148 JX4	N/C	I/O154 KX2	VCC	I/O152 KX0	I/O153 KX1	I/O190 PX6	CLK3	I/O188 PX4	I/O2 A2	I/O16 C0	N/C	GND	I/O36 F4	I/O35 F3	I/O47 G7	E
F	I/O144 JX0	I/O149 JX5	I/O147 JX3	GND	I/O146 JX2	I/O145 JX1	I/O176 OX0	I/O169 NX1	I/O185 PX1	I/O4 A4	I/O19 C3	I/O34 F2	VCC	I/O32 F0	I/O46 G6	I/O45 G5	F
G	I/O163 LX3	I/O166 LX6	I/O165 LX5	VCC	I/O164 LX4	I/O167 LX7	VCC	GND	GND	VCC	I/O33 F1	I/O44 G4	GND	I/O42 G2	I/O41 G1	I/O31 E7	G
H	I/O160 LX0	I/O162 LX2	I/O161 LX1	GND	I/O120 EX0	I/O121 EX1	GND	VCC	VCC	GND	I/O43 G3	I/O40 G0	VCC	I/O28 E4	I/O27 E3	I/O26 E2	H
J	I/O122 EX2	I/O123 EX3	I/O124 EX4	GND	I/O126 EX6	I/O125 EX5	GND	VCC	VCC	GND	I/O30 E6	I/O29 E5	GND	I/O65 L1	I/O64 L0	I/O66 L2	J
K	I/O127 EX7	I/O136 GX0	I/O137 GX1	VCC	I/O139 GX3	I/O138 GX2	VCC	GND	GND	VCC	I/O25 E1	I/O24 E0	VCC	I/O71 L7	I/O70 L6	I/O48 J0	K
L	I/O140 GX4	I/O141 GX5	I/O143 GX7	GND	I/O130 FX2	I/O142 GX6	I/O98 AX2	I/O91 P3	I/O75 N3	I/O77 N5	I/O68 L4	I/O67 L3	GND	I/O51 J3	I/O52 J4	I/O49 J1	L
M	I/O128 FX0	I/O129 FX1	I/O131 FX3	GND	I/O115 CX3	I/O113 CX1	I/O100 AX4	I/O90 P2	I/O74 N2	I/O80 O0	I/O83 O3	I/O69 L5	VCC	I/O60 K4	I/O55 J7	I/O50 J2	M
N	I/O132 FX4	I/O133 FX5	I/O135 FX7	VCC	GND	VCC	GND	VCC	GND	GND	VCC	GND	GND	TCK	I/O56 K0	I/O53 J5	N
P	I/O134 FX6	I/O109 BX5	I/O110 BX6	I/O111 BX7	I/O116 CX4	I/O114 CX2	I/O101 AX5	I/O89 P1	I/O93 P5	I/O94 P6	I/O79 N7	I/O84 O4	I/O87 O7	TMS	I/O57 K1	I/O54 J6	P
R	I/O108 BX4	I/O107 BX3	I/O104 BX0	I/O119 CX7	I/O112 CX0	I/O102 AX6	I/O99 AX3	I/O96 AX0	I/O92 P4	I/O72 N0	I/O76 N4	I/O81 O1	I/O85 O5	I/O63 K7	I/O59 K3	I/O58 K2	R
T	I/O106 BX2	I/O105 BX1	I/O118 CX6	I/O117 CX5	I/O103 AX7	CLK2	I/O97 AX1	I/O88 P0	CLK1	I/O95 P7	I/O73 N1	I/O78 N6	I/O82 O2	I/O86 O6	I/O62 K6	I/O61 K5	T

#### PIN DESIGNATIONS

- CLK = Clock
- GND = Ground
- I = Input
- I/O = Input/Output
- N/C = No Connect
- VCC = Supply Voltage
- TDI = Test Data In
- TCK = Test Clock
- TMS = Test Mode Select
- TDO = Test Data Out

