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## Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

## Applications of Embedded - CPLDs

### Details

Product Status	Not For New Designs
Programmable Type	In System Programmable
Delay Time tpd(1) Max	5.5 ns
Voltage Supply - Internal	4.75V ~ 5.25V
Number of Logic Elements/Blocks	-
Number of Macrocells	64
Number of Gates	-
Number of I/O	32
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-TQFP (7x7)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/lattice-semiconductor/m4a5-64-32-55vnc48">https://www.e-xfl.com/product-detail/lattice-semiconductor/m4a5-64-32-55vnc48</a>

**Table 1. ispMACH 4A Device Features**

<b>3.3 V Devices</b>								
<b>Feature</b>	<b>M4A3-32</b>	<b>M4A3-64</b>	<b>M4A3-96</b>	<b>M4A3-128</b>	<b>M4A3-192</b>	<b>M4A3-256</b>	<b>M4A3-384</b>	<b>M4A3-512</b>
Macrocells	32	64	96	128	192	256	384	512
User I/O options	32	32/64	48	64	96	128/160/192	160/192	160/192/256
$t_{PD}$ (ns)	5.0	5.5	5.5	5.5	6.0	5.5	6.5	7.5
$f_{CNT}$ (MHz)	182	167	167	167	160	167	154	125
$t_{COS}$ (ns)	4.0	4.0	4.0	4.0	4.5	4.0	4.5	5.5
$t_{SS}$ (ns)	3.0	3.5	3.5	3.5	3.5	3.5	3.5	5.0
Static Power (mA)	20	25/52	40	55	85	110/150	149/155	179
JTAG Compliant	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
PCI Compliant	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes

<b>5 V Devices</b>						
<b>Feature</b>	<b>M4A5-32</b>	<b>M4A5-64</b>	<b>M4A5-96</b>	<b>M4A5-128</b>	<b>M4A5-192</b>	<b>M4A5-256</b>
Macrocells	32	64	96	128	192	256
User I/O options	32	32	48	64	96	128
$t_{PD}$ (ns)	5.0	5.5	5.5	5.5	6.0	6.5
$f_{CNT}$ (MHz)	182	167	167	167	160	154
$t_{COS}$ (ns)	4.0	4.0	4.0	4.0	4.5	5.0
$t_{SS}$ (ns)	3.0	3.5	3.5	3.5	3.5	3.5
Static Power (mA)	20	25	40	55	74	110
JTAG Compliant	Yes	Yes	Yes	Yes	Yes	Yes
PCI Compliant	Yes	Yes	Yes	Yes	Yes	Yes

## Product-Term Array

The product-term array consists of a number of product terms that form the basis of the logic being implemented. The inputs to the AND gates come from the central switch matrix (Table 5), and are provided in both true and complement forms for efficient logic implementation.

**Table 5. PAL Block Inputs**

Device	Number of Inputs to PAL Block
M4A3-32/32 and M4A5-32/32	33
M4A3-64/32 and M4A5-64/32	33
M4A3-64/64	33
M4A3-96/48 and M4A5-96/48	33
M4A3-128/64 and M4A5-128/64	33
M4A3-192/96 and M4A5-192/96	34
M4A3-256/128 and M4A5-256/128	34
M4A3-256/160 and M4A3-256/192	36
M4A3-384	36
M4A3-512	36

## Logic Allocator

Within the logic allocator, product terms are allocated to macrocells in “product term clusters.” The availability and distribution of product term clusters are automatically considered by the software as it fits functions within a PAL block. The size of a product term cluster has been optimized to provide high utilization of product terms, making complex functions using many product terms possible. Yet when few product terms are used, there will be a minimal number of unused—or wasted—product terms left over. The product term clusters available to each macrocell within a PAL block are shown in Tables 6 and 7.

Each product term cluster is associated with a macrocell. The size of a cluster depends on the configuration of the associated macrocell. When the macrocell is used in synchronous mode (Figure 2a), the basic cluster has 4 product terms. When the associated macrocell is used in asynchronous mode (Figure 2b), the cluster has 2 product terms. Note that if the product term cluster is routed to a different macrocell, the allocator configuration is not determined by the mode of the macrocell actually being driven. The configuration is always set by the mode of the macrocell that the cluster will drive if not routed away, regardless of the actual routing.

In addition, there is an extra product term that can either join the basic cluster to give an extended cluster, or drive the second input of an exclusive-OR gate in the signal path. If included with the basic cluster, this provides for up to 20 product terms on a synchronous function that uses four extended 5-product-term clusters. A similar asynchronous function can have up to 18 product terms.

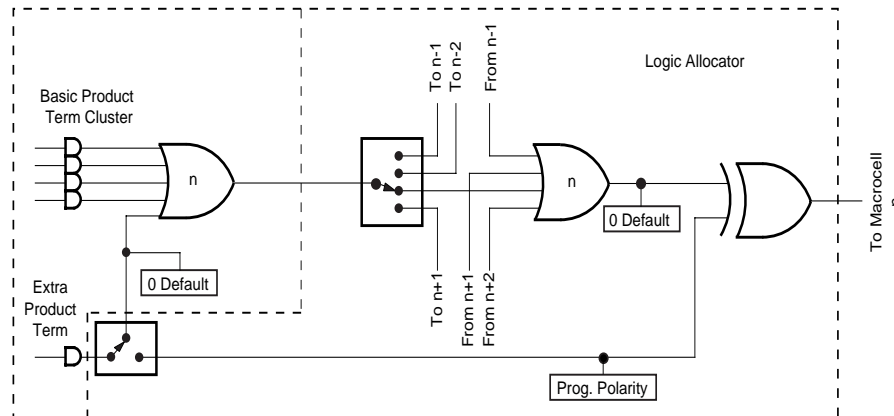
When the extra product term is used to extend the cluster, the value of the second XOR input can be programmed as a 0 or a 1, giving polarity control. The possible configurations of the logic allocator are shown in Figures 3 and 4.

**Table 6. Logic Allocator for All ispMACH 4A Devices (except M4A(3,5)-32/32)**

Output Macrocell	Available Clusters	Output Macrocell	Available Clusters
M <sub>0</sub>	C <sub>0</sub> , C <sub>1</sub> , C <sub>2</sub>	M <sub>8</sub>	C <sub>7</sub> , C <sub>8</sub> , C <sub>9</sub> , C <sub>10</sub>
M <sub>1</sub>	C <sub>0</sub> , C <sub>1</sub> , C <sub>2</sub> , C <sub>3</sub>	M <sub>9</sub>	C <sub>8</sub> , C <sub>9</sub> , C <sub>10</sub> , C <sub>11</sub>
M <sub>2</sub>	C <sub>1</sub> , C <sub>2</sub> , C <sub>3</sub> , C <sub>4</sub>	M <sub>10</sub>	C <sub>9</sub> , C <sub>10</sub> , C <sub>11</sub> , C <sub>12</sub>
M <sub>3</sub>	C <sub>2</sub> , C <sub>3</sub> , C <sub>4</sub> , C <sub>5</sub>	M <sub>11</sub>	C <sub>10</sub> , C <sub>11</sub> , C <sub>12</sub> , C <sub>13</sub>
M <sub>4</sub>	C <sub>3</sub> , C <sub>4</sub> , C <sub>5</sub> , C <sub>6</sub>	M <sub>12</sub>	C <sub>11</sub> , C <sub>12</sub> , C <sub>13</sub> , C <sub>14</sub>
M <sub>5</sub>	C <sub>4</sub> , C <sub>5</sub> , C <sub>6</sub> , C <sub>7</sub>	M <sub>13</sub>	C <sub>12</sub> , C <sub>13</sub> , C <sub>14</sub> , C <sub>15</sub>
M <sub>6</sub>	C <sub>5</sub> , C <sub>6</sub> , C <sub>7</sub> , C <sub>8</sub>	M <sub>14</sub>	C <sub>13</sub> , C <sub>14</sub> , C <sub>15</sub>
M <sub>7</sub>	C <sub>6</sub> , C <sub>7</sub> , C <sub>8</sub> , C <sub>9</sub>	M <sub>15</sub>	C <sub>14</sub> , C <sub>15</sub>

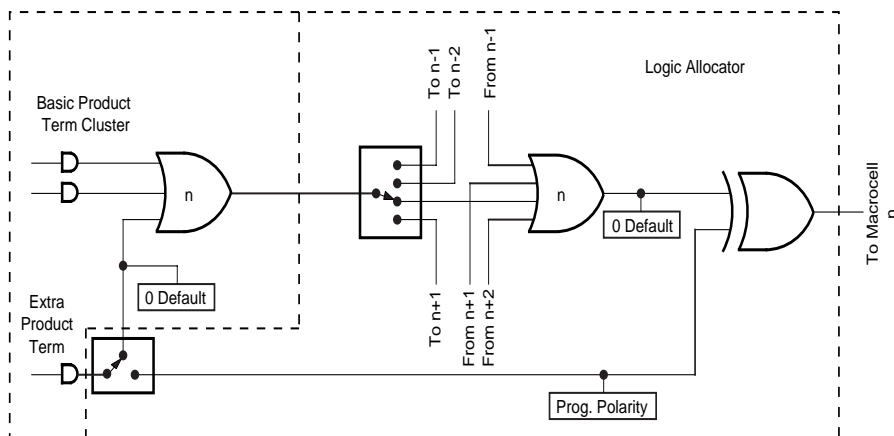
**Table 7. Logic Allocator for M4A(3,5)-32/32**

Output Macrocell	Available Clusters	Output Macrocell	Available Clusters
M <sub>0</sub>	C <sub>0</sub> , C <sub>1</sub> , C <sub>2</sub>	M <sub>8</sub>	C <sub>8</sub> , C <sub>9</sub> , C <sub>10</sub>
M <sub>1</sub>	C <sub>0</sub> , C <sub>1</sub> , C <sub>2</sub> , C <sub>3</sub>	M <sub>9</sub>	C <sub>8</sub> , C <sub>9</sub> , C <sub>10</sub> , C <sub>11</sub>
M <sub>2</sub>	C <sub>1</sub> , C <sub>2</sub> , C <sub>3</sub> , C <sub>4</sub>	M <sub>10</sub>	C <sub>9</sub> , C <sub>10</sub> , C <sub>11</sub> , C <sub>12</sub>
M <sub>3</sub>	C <sub>2</sub> , C <sub>3</sub> , C <sub>4</sub> , C <sub>5</sub>	M <sub>11</sub>	C <sub>10</sub> , C <sub>11</sub> , C <sub>12</sub> , C <sub>13</sub>
M <sub>4</sub>	C <sub>3</sub> , C <sub>4</sub> , C <sub>5</sub> , C <sub>6</sub>	M <sub>12</sub>	C <sub>11</sub> , C <sub>12</sub> , C <sub>13</sub> , C <sub>14</sub>
M <sub>5</sub>	C <sub>4</sub> , C <sub>5</sub> , C <sub>6</sub> , C <sub>7</sub>	M <sub>13</sub>	C <sub>12</sub> , C <sub>13</sub> , C <sub>14</sub> , C <sub>15</sub>
M <sub>6</sub>	C <sub>5</sub> , C <sub>6</sub> , C <sub>7</sub>	M <sub>14</sub>	C <sub>13</sub> , C <sub>14</sub> , C <sub>15</sub>
M <sub>7</sub>	C <sub>6</sub> , C <sub>7</sub>	M <sub>15</sub>	C <sub>14</sub> , C <sub>15</sub>



**a. Synchronous Mode**

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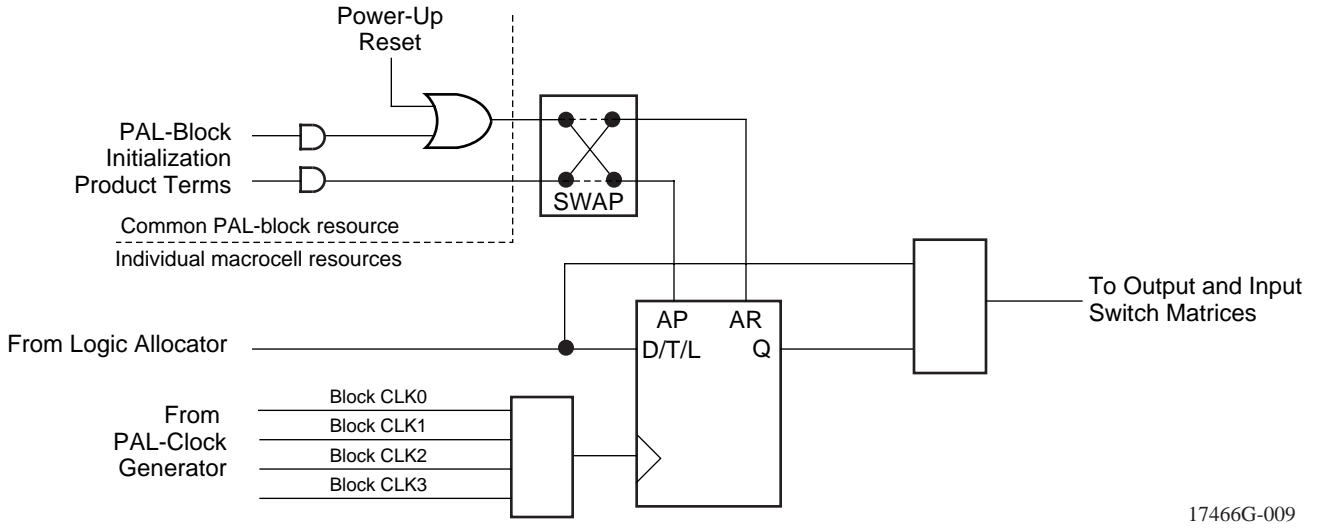
**b. Asynchronous Mode**

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**Figure 2. Logic Allocator: Configuration of Cluster “n” Set by Mode of Macrocell “n”**

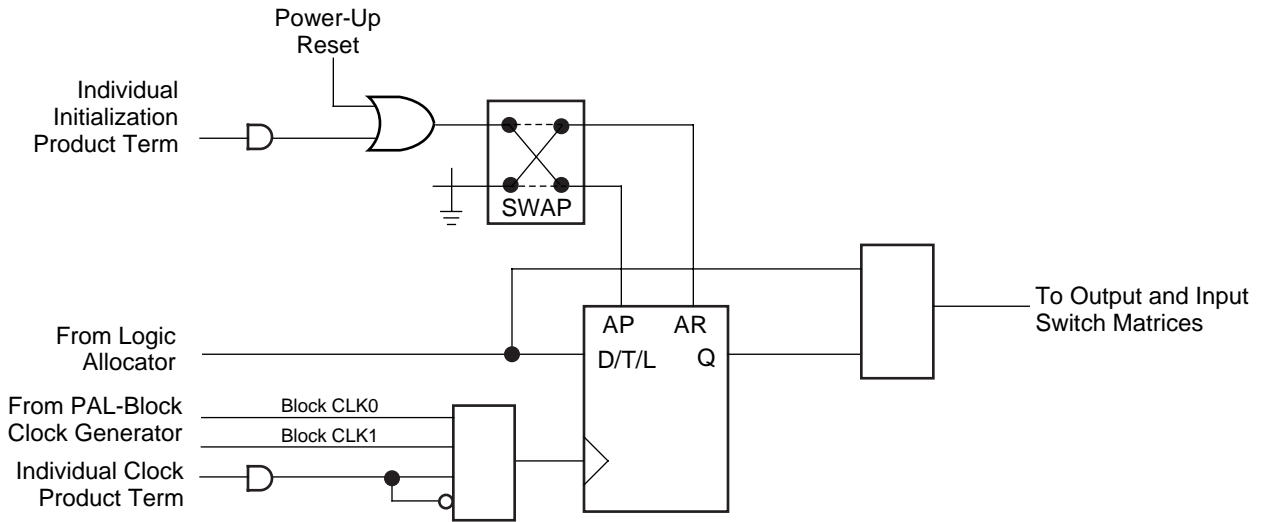
## Macrocell

The macrocell consists of a storage element, routing resources, a clock multiplexer, and initialization control. The macrocell has two fundamental modes: synchronous and asynchronous (Figure 5). The mode chosen only affects clocking and initialization in the macrocell.



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**a. Synchronous mode**



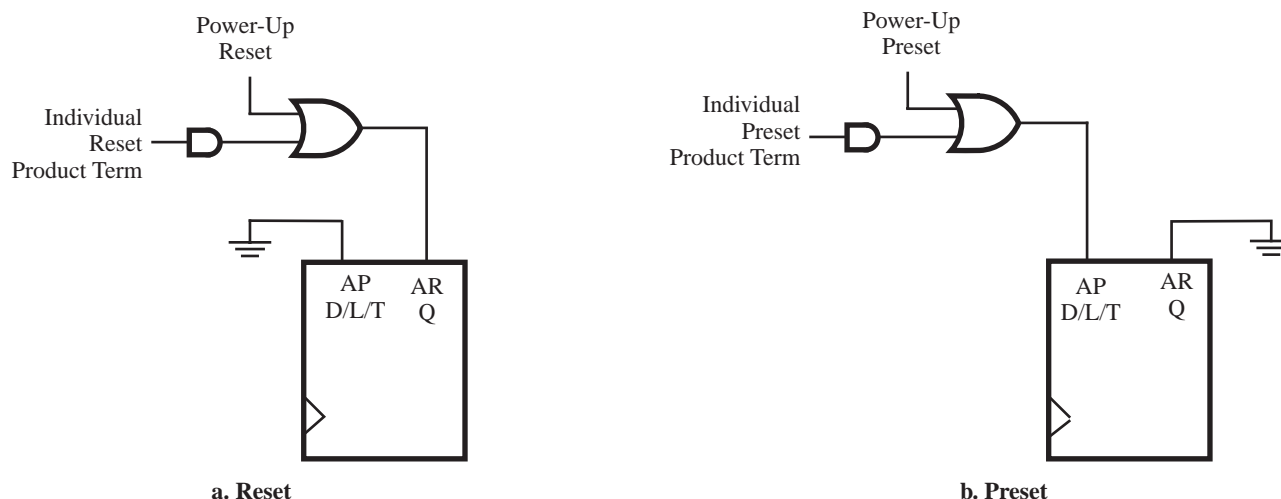
**b. Asynchronous mode**

17466G-010

**Figure 5. Macrocell**

In either mode, a combinatorial path can be used. For combinatorial logic, the synchronous mode will generally be used, since it provides more product terms in the allocator.

A reset/preset swapping feature in each macrocell allows for reset and preset to be exchanged, providing flexibility. In asynchronous mode (Figure 8), a single individual product term is provided for initialization. It can be selected to control reset or preset.



17466G-014

17466G-015

**Figure 8. Asynchronous Mode Initialization Configurations**

Note that the reset/preset swapping selection feature effects power-up reset as well. The initialization functionality of the flip-flops is illustrated in Table 9. The macrocell sends its data to the output switch matrix and the input switch matrix. The output switch matrix can route this data to an output if so desired. The input switch matrix can send the signal back to the central switch matrix as feedback.

**Table 9. Asynchronous Reset/Preset Operation**

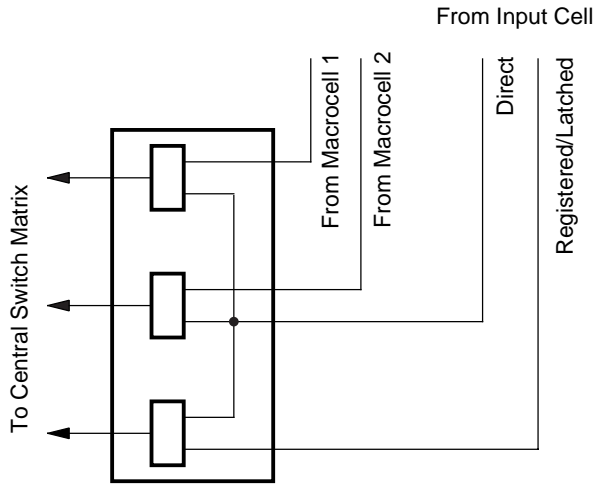
AR	AP	CLK/LE <sup>1</sup>	Q+
0	0	X	See Table 8
0	1	X	1
1	0	X	0
1	1	X	0

**Note:**

- Transparent latch is unaffected by AR, AP

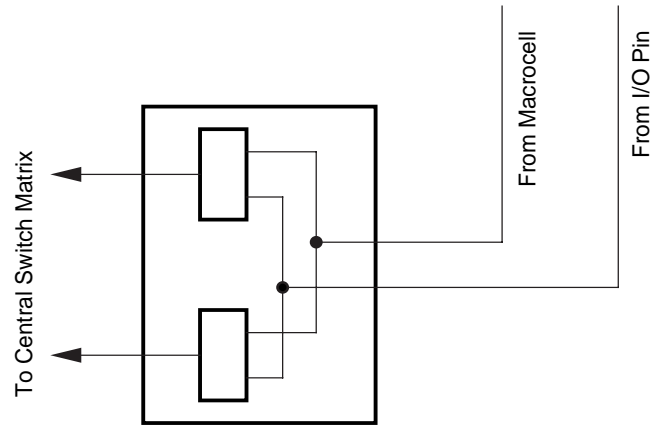
## Input Switch Matrix

The input switch matrix (Figures 12 and 13) optimizes routing of inputs to the central switch matrix. Without the input switch matrix, each input and feedback signal has only one way to enter the central switch matrix. The input switch matrix provides additional ways for these signals to enter the central switch matrix.



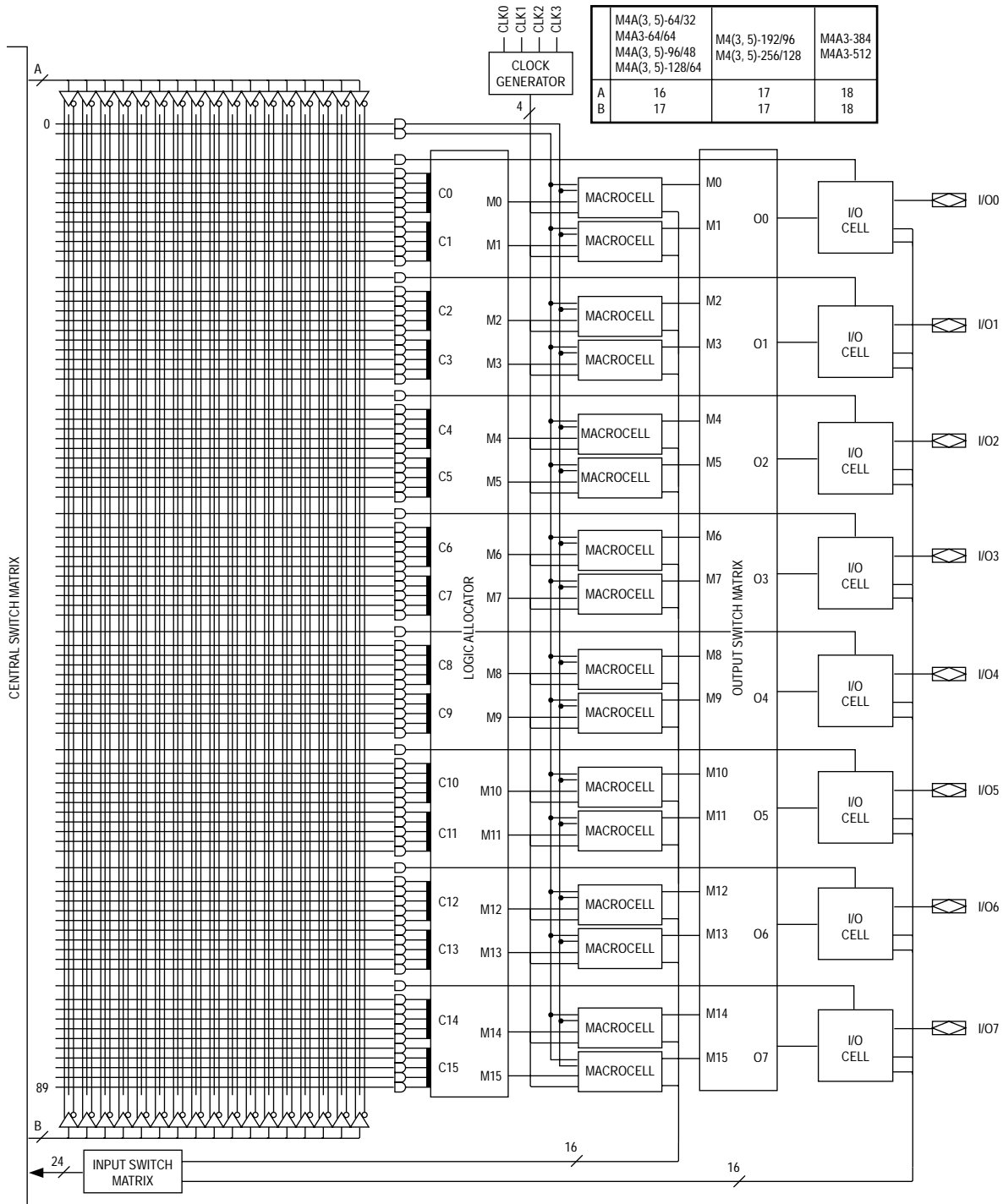
17466G-002

Figure 12. ispMACH 4A with 2:1 Macrocell-I/O Cell Ratio - Input Switch Matrix



17466G-003

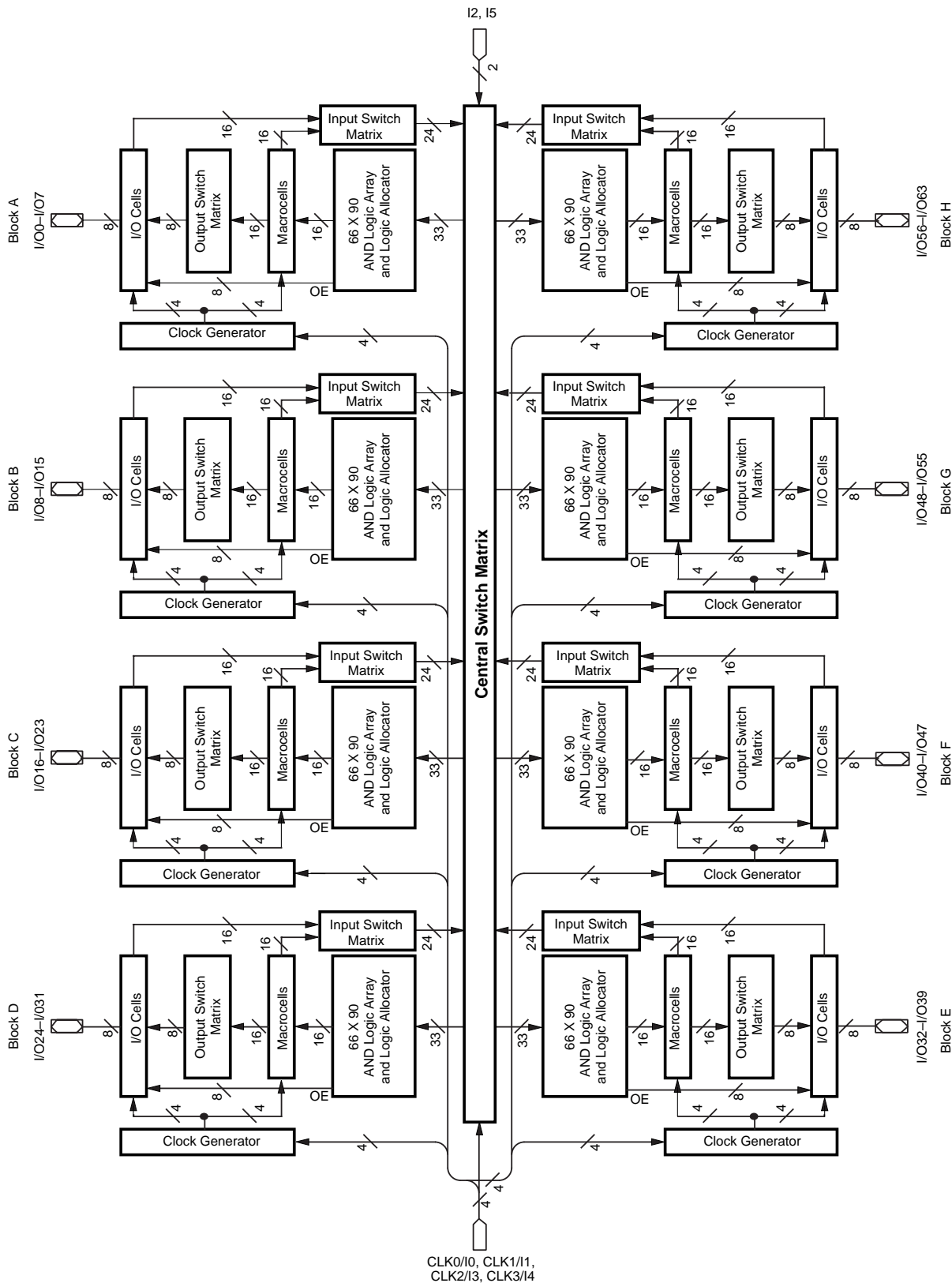
Figure 13. ispMACH 4A with 1:1 Macrocell-I/O Cell Ratio - Input Switch Matrix



**Figure 16. PAL Block for ispMACH 4A with 2:1 Macrocell - I/O Cell Ratio**

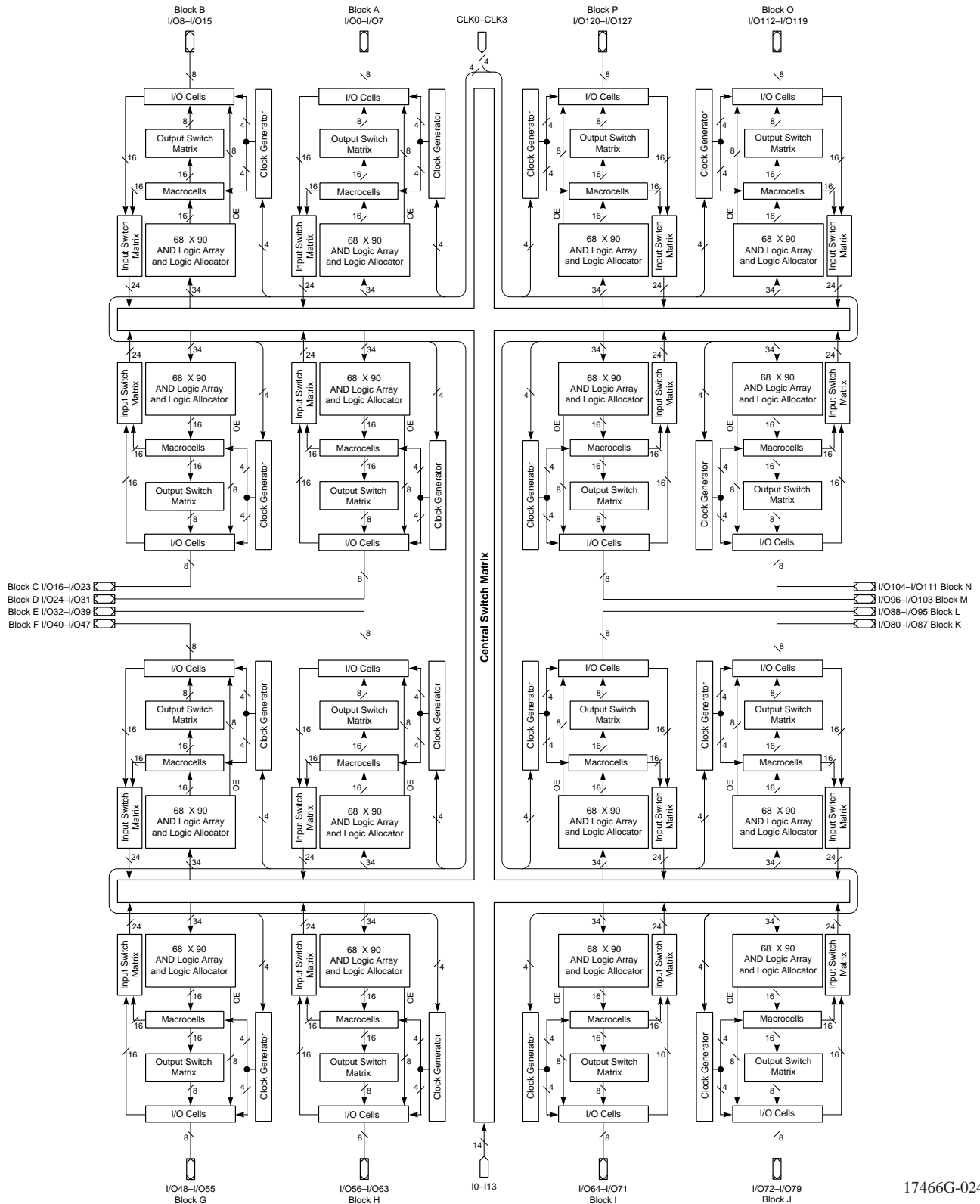


# BLOCK DIAGRAM – M4A(3,5)-128/64



17466H-022

# BLOCK DIAGRAM – M4A(3,5)-256/128



17466G-024

# BLOCK DIAGRAM - M4A3-512/160, M4A3-512/192, M4A3-512/256



17466G-068

## ispMACH 4A TIMING PARAMETERS OVER OPERATING RANGES<sup>1</sup>

		-5		-55		-6		-65		-7		-10		-12		-14		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
<b>Combinatorial Delay:</b>																		
$t_{PDi}$	Internal combinatorial propagation delay		3.5		4.0		4.3		4.5		5.0		7.0		9.0		11.0	ns
$t_{PD}$	Combinatorial propagation delay		5.0		5.5		6.0		6.5		7.5		10.0		12.0		14.0	ns
<b>Registered Delays:</b>																		
$t_{SS}$	Synchronous clock setup time, D-type register	3.0		3.5		3.5		3.5		5.0		5.5		7.0		10.0		ns
$t_{SST}$	Synchronous clock setup time, T-type register	4.0		4.0		4.0		4.0		6.0		6.5		8.0		11.0		ns
$t_{SA}$	Asynchronous clock setup time, D-type register	2.5		2.5		2.5		3.0		3.5		4.0		5.0		8.0		ns
$t_{SAT}$	Asynchronous clock setup time, T-type register	3.0		3.0		3.0		3.5		4.5		5.0		6.0		9.0		ns
$t_{HS}$	Synchronous clock hold time	0.0		0.0		0.0		0.0		0.0		0.0		0.0		0.0		ns
$t_{HA}$	Asynchronous clock hold time	2.5		2.5		2.5		3.0		3.5		4.0		5.0		8.0		ns
$t_{COSi}$	Synchronous clock to internal output		2.5		2.5		2.8		3.0		3.0		3.0		3.5		3.5	ns
$t_{COS}$	Synchronous clock to output		4.0		4.0		4.5		5.0		5.5		6.0		6.5		6.5	ns
$t_{COAi}$	Asynchronous clock to internal output		5.0		5.0		5.0		5.0		6.0		8.0		10.0		12.0	ns
$t_{COA}$	Asynchronous clock to output		6.5		6.5		6.8		7.0		8.5		11.0		13.0		15.0	ns
<b>Latched Delays:</b>																		
$t_{SSL}$	Synchronous latch setup time	4.0		4.0		4.0		4.5		6.0		7.0		8.0		10.0		ns
$t_{SAL}$	Asynchronous latch setup time	3.0		3.0		3.5		3.5		4.0		4.0		5.0		8.0		ns
$t_{HSL}$	Synchronous latch hold time	0.0		0.0		0.0		0.0		0.0		0.0		0.0		0.0		ns
$t_{HAL}$	Asynchronous latch hold time	3.0		3.0		3.5		3.5		4.0		4.0		5.0		8.0		ns
$t_{PDLi}$	Transparent latch to internal output		5.5		5.5		5.8		6.0		7.5		9.0		11.0		12.0	ns
$t_{PDL}$	Propagation delay through transparent latch to output		7.0		7.0		7.5		8.0		10.0		12.0		14.0		15.0	ns
$t_{GOSi}$	Synchronous gate to internal output		3.0		3.0		3.0		3.0		3.5		4.5		7.0		8.0	ns
$t_{GOS}$	Synchronous gate to output		4.5		4.5		4.8		5.0		6.0		7.5		10.0		11.0	ns
$t_{GOAi}$	Asynchronous gate to internal output		6.0		6.0		6.0		6.0		8.5		10.0		13.0		15.0	ns
$t_{GOA}$	Asynchronous gate to output		7.5		7.5		7.8		8.0		11.0		13.0		16.0		18.0	ns
<b>Input Register Delays:</b>																		
$t_{SIRS}$	Input register setup time	1.5		1.5		2.0		2.0		2.0		2.0		2.0		2.0		ns
$t_{HIRS}$	Input register hold time	2.5		2.5		3.0		3.0		3.0		3.0		3.0		4.0		ns
$t_{ICOSi}$	Input register clock to internal feedback		3.0		3.0		3.0		3.0		3.5		4.5		6.0		6.0	ns
<b>Input Latch Delays:</b>																		
$t_{SIL}$	Input latch setup time	1.5		1.5		1.5		2.0		2.0		2.0		2.0		2.0		ns
$t_{HIL}$	Input latch hold time	2.5		2.5		2.5		3.0		3.0		3.0		3.0		4.0		ns
$t_{IGOSi}$	Input latch gate to internal feedback		3.5		3.5		3.8		4.0		4.0		4.0		4.0		5.0	ns
$t_{PDILi}$	Transparent input latch to internal feedback		1.5		1.5		1.5		1.5		2.0		2.0		2.0		2.0	ns

## ispMACH 4A TIMING PARAMETERS OVER OPERATING RANGES<sup>1</sup>

		-5		-55		-6		-65		-7		-10		-12		-14		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
<b>Frequency:</b>																		
$f_{MAXS}$	External feedback, D-type, Min of $1/(t_{WIS} + t_{WHS})$ or $1/(t_{SS} + t_{COS})$	143		133		125		118		95.2		87.0		74.1		60.6		MHz
	External feedback, T-type, Min of $1/(t_{WIS} + t_{WHS})$ or $1/(t_{SST} + t_{COS})$	125		125		118		111		87.0		80.0		69.0		57.1		MHz
	Internal feedback ( $f_{CNT}$ ), D-type, Min of $1/(t_{WIS} + t_{WHS})$ or $1/(t_{SS} + t_{COSi})$	182		167		160		154		125		118		95.0		74.1		MHz
	Internal feedback ( $f_{CNT}$ ), T-type, Min of $1/(t_{WIS} + t_{WHS})$ or $1/(t_{SST} + t_{COSi})$	154		154		148		143		111		105		87.0		69.0		MHz
	No feedback <sup>2</sup> , Min of $1/(t_{WIS} + t_{WHS})$ , $1/(t_{SS} + t_{HS})$ or $1/(t_{SST} + t_{HS})$	250		250		200		200		154		125		100		83.3		MHz
$f_{MAXA}$	External feedback, D-type, Min of $1/(t_{WLA} + t_{WHA})$ or $1/(t_{SA} + t_{COA})$	111		111		108		100		83.3		66.7		55.6		43.5		MHz
	External feedback, T-type, Min of $1/(t_{WLA} + t_{WHA})$ or $1/(t_{SAT} + t_{COA})$	105		105		102		95.2		76.9		62.5		52.6		41.7		MHz
	Internal feedback ( $f_{CNTA}$ ), D-type, Min of $1/(t_{WLA} + t_{WHA})$ or $1/(t_{SA} + t_{COAi})$	133		133		125		125		105		83.3		66.7		50.0		MHz
	Internal feedback ( $f_{CNTA}$ ), T-type, Min of $1/(t_{WLA} + t_{WHA})$ or $1/(t_{SAT} + t_{COAi})$	125		125		125		118		95.2		76.9		62.5		47.6		MHz
	No feedback <sup>2</sup> , Min of $1/(t_{WLA} + t_{WHA})$ , $1/(t_{SA} + t_{HA})$ or $1/(t_{SAT} + t_{HA})$	167		167		143		143		125		100		62.5		55.6		MHz
$f_{MAXI}$	Maximum input register frequency, Min of $1/(t_{WIRH} + t_{WIRL})$ or $1/(t_{SIRS} + t_{HIRS})$	167		167		143		143		125		100		83.3		83.3		MHz

### Notes:

1. See "Switching Test Circuit" document on the Literature Download page of the Lattice web site.
2. This parameter does not apply to flip-flops in the emulated mode since the feedback path is required for emulation.

## CAPACITANCE<sup>1</sup>

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
$C_{IN}$	Input capacitance	$V_{IN}=2.0\text{ V}$	3.3 V or 5 V, 25°C, 1 MHz	6	pF
$C_{I/O}$	Output capacitance	$V_{OUT}=2.0\text{ V}$	3.3 V or 5 V, 25°C, 1 MHz	8	pF

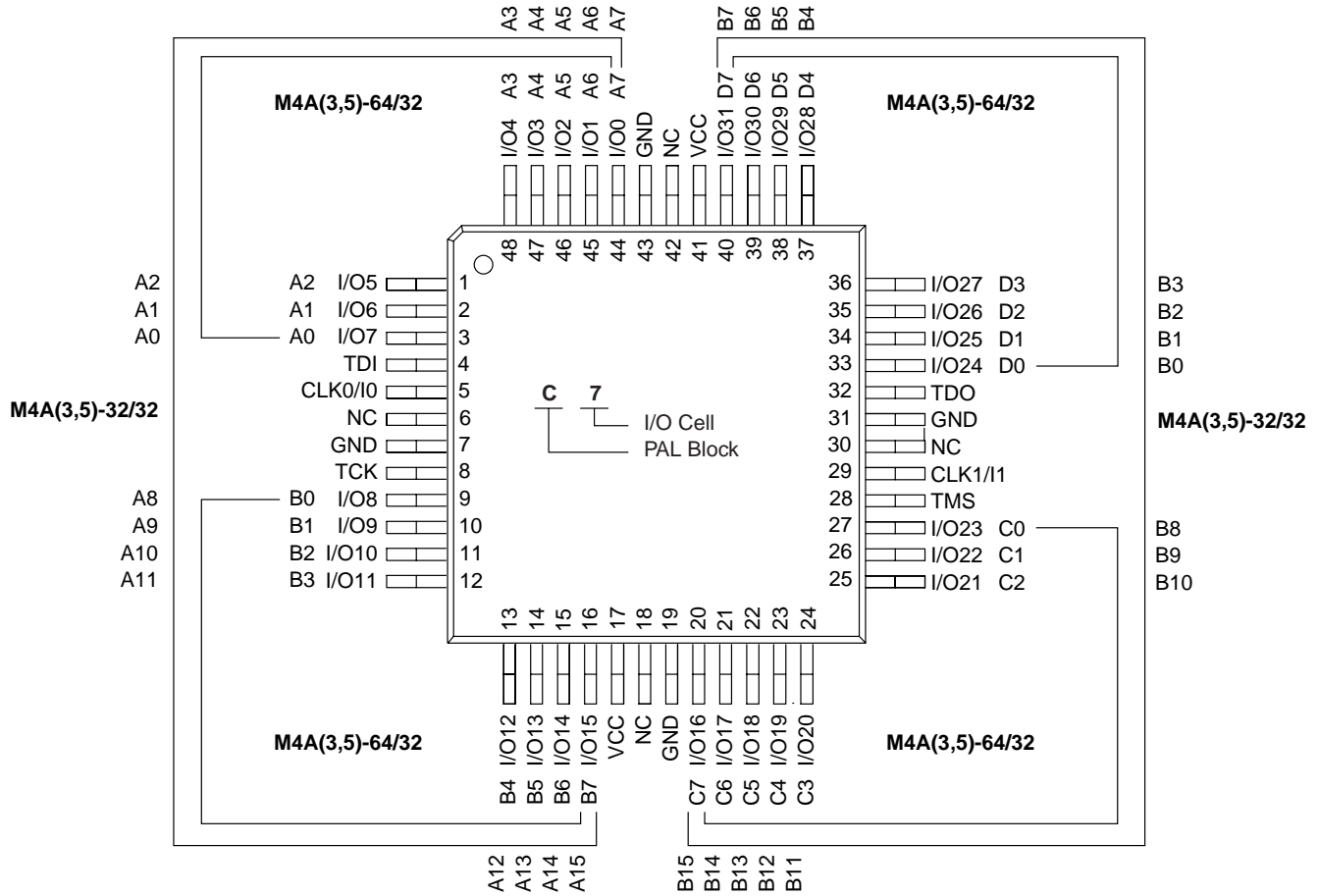
### Note:

1. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where this parameter may be affected.

# 48-PIN TQFP CONNECTION DIAGRAM (M4A(3,5)-32/32 AND M4A(3,5)-64/32)

## Top View

48-Pin TQFP (1.4mm Thickness)



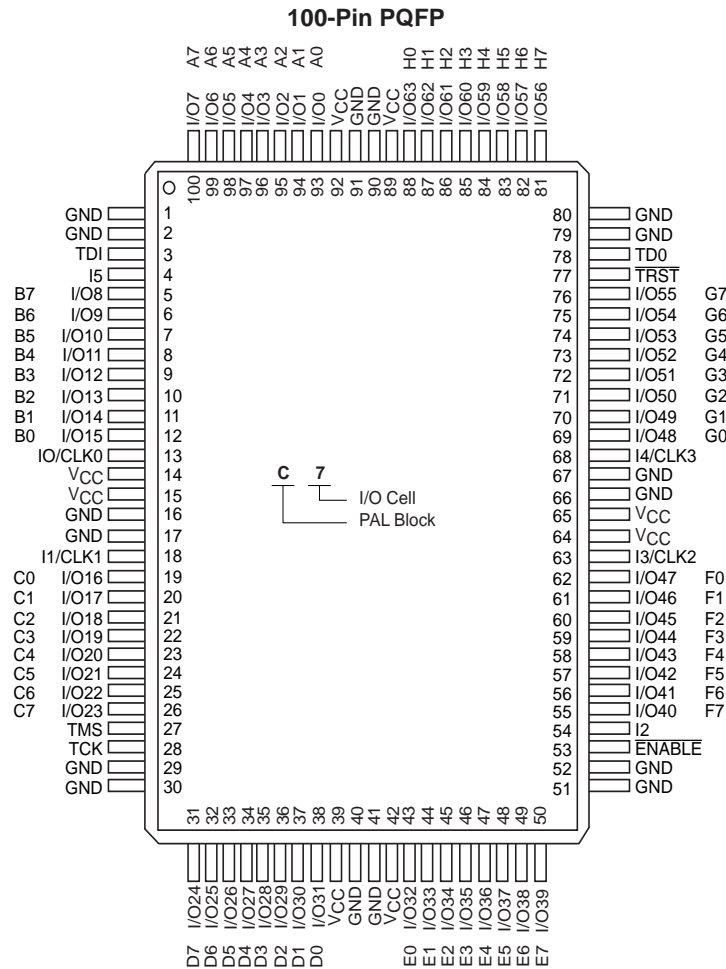
17466G-028

## PIN DESIGNATIONS

- CLK/I = Clock or Input
- GND = Ground
- I/O = Input/Output
- V<sub>CC</sub> = Supply Voltage
- NC = No Connect
- TDI = Test Data In
- TCK = Test Clock
- TMS = Test Mode Select
- TDO = Test Data Out

## 100-PIN PQFP CONNECTION DIAGRAM (M4A(3,5)-128/64)

### Top View



17466G-031

## PIN DESIGNATIONS

I/CLK = Input or Clock

GND = Ground

I = Input

I/O = Input/Output

V<sub>CC</sub> = Supply Voltage

TDI = Test Data In

TCK = Test Clock

TMS = Test Mode Select

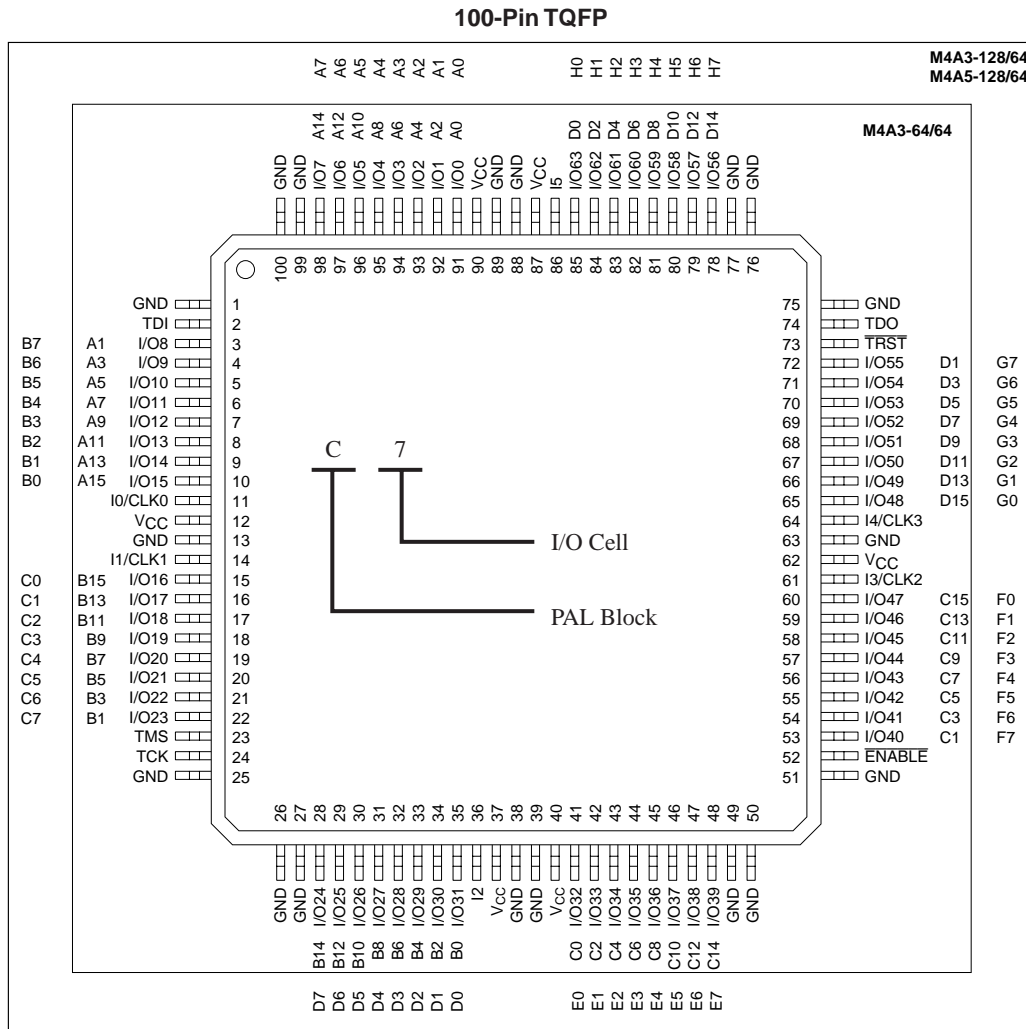
TDO = Test Data Out

TRST = Test Reset

ENABLE = Program

# 100-PIN TQFP CONNECTION DIAGRAM (M4A3-64/64 AND M4A(3,5)-128/64)

## Top View



## PIN DESIGNATIONS

CLK/I = Clock or Input

GND = Ground

I = Input

I/O = Input/Output

V<sub>CC</sub> = Supply Voltage

TDI = Test Data In

TCK = Test Clock

TMS = Test Mode Select

TDO = Test Data Out

TRST = Test Reset

ENABLE = Program



# 144-PIN TQFP CONNECTION DIAGRAM (M4A(3,5)-192/96)

## Top View



17466G-033

## PIN DESIGNATIONS

- CLK = Clock
- GND = Ground
- I = Input
- I/O = Input/Output
- V<sub>CC</sub> = Supply Voltage
- TDI = Test Data In
- TCK = Test Clock
- TMS = Test Mode Select
- TDO = Test Data Out

# 256-BALL BGA CONNECTION DIAGRAM (M4A3-256/128)

## Bottom View

### 256-Ball BGA

	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	GND	N/C	GND	I/O108 N4	I/O105 N1	GND	I/O100 M4	I/O96 M0	GND	GND	GND	GND	I/O95 L0	I/O91 L4	GND	I/O87 K0	N/C	GND	GND	GND	A
B	GND	I/O113 O6	N/C	I/O109 N5	I/O106 N2	I/O103 M7	I/O102 M6	I/O98 M2	N/C	I11	N/C	N/C	I/O93 L2	I/O89 L6	I/O88 L7	I/O85 K2	I/O83 K4	I/O82 K5	N/C	GND	B
C	I/O116 O3	N/C	VCC	TRST	I/O111 N7	I/O107 N3	I/O104 N0	I/O101 M5	I/O97 M1	N/C	I10	I/O94 L1	I/O90 L5	I/O86 K1	I/O84 K3	I/O80 K7	ENABLE	VCC	I/O78 J6	I/O74 J2	C
D	I/O120 P7	I/O117 O2	I/O112 O7	VCC	VCC	I/O110 N6	VCC	N/C	I/O99 M3	N/C	I9	I/O92 L3	N/C	VCC	I/O81 K6	VCC	VCC	I/O79 J7	I/O75 J3	I/O71 I7	D
E	I/O123 P4	I/O119 O0	I/O114 O5	TDI	<p style="text-align: center;"><b>PIN DESIGNATIONS</b></p> <p>           CLK = Clock            GND = Ground            I = Input            I/O = Input/Output            N/C = No Connect            VCC = Supply Voltage            TDI = Test Data In            TCK = Test Clock            TMS = Test Mode Select            TDO = Test Data Out            TRST = Test Reset            ENABLE = Program         </p>												TDO	I/O77 J5	I/O72 J0	I/O68 I4	E
F	GND	I/O122 P5	I/O118 O1	I/O115 O4													I/O76 J4	I/O73 J1	I/O69 I5	GND	F
G	I12	I/O125 P2	I/O121 P6	VCC													VCC	I/O70 I6	I/O65 I1	I8	G
H	GND	I/O127 P0	I/O126 P1	I/O124 P3													I/O67 I3	I/O66 I2	I/O64 I0	GND	H
J	N/C	N/C	N/C	I13													I7	N/C	N/C	N/C	J
K	GND	CLK3	N/C	N/C													N/C	N/C	CLK2	N/C	K
L	N/C	CLK0	N/C	N/C													N/C	N/C	CLK1	GND	L
M	N/C	N/C	N/C	I0													I6	N/C	I/O63 H0	I/O62 H1	M
N	GND	I/O0 A0	I/O2 A2	I/O3 A3													I/O60 H3	I/O61 H2	I/O59 H4	GND	N
P	I1	I/O1 A1	I/O6 A6	VCC													VCC	I/O57 H6	I/O58 H5	I5	P
R	GND	I/O5 A5	I/O9 B1	N/C	I/O51 G4	I/O54 G1	I/O56 H7	GND	R												
T	I/O4 A4	I/O8 B0	I/O12 B4	TCK	TMS	I/O50 G5	I/O55 G0	N/C	T												
U	I/O7 A7	I/O11 B3	I/O15 B7	VCC	VCC	I/O18 C5	VCC	I/O24 D7	I/O29 D2	I2	N/C	I/O35 E3	N/C	VCC	N/C	VCC	VCC	I/O48 G7	I/O53 G2	N/C	U
V	I/O10 B2	I/O13 B5	VCC	I/O16 C7	I/O17 C6	I/O21 C2	I/O23 C0	I/O27 D4	I/O31 D0	I3	N/C	I/O33 E1	I/O37 E5	I/O41 F1	I/O43 F3	I/O46 F6	I/O47 F7	VCC	I/O52 G3	N/C	V
W	GND	I/O14 B6	N/C	N/C	I/O19 C4	I/O22 C1	I/O25 D6	I/O28 D3	N/C	N/C	I4	N/C	I/O34 E2	I/O38 E6	I/O39 E7	I/O42 F2	I/O45 F5	N/C	I/O49 G6	GND	W
Y	GND	GND	GND	N/C	I/O20 C3	GND	I/O26 D5	I/O30 D1	GND	GND	GND	GND	I/O32 E0	I/O36 E4	GND	I/O40 F0	I/O44 F4	GND	N/C	GND	Y

17466G-045

# 256-BALL BGA CONNECTION DIAGRAM - (M4A3-384/192)

## Bottom View

### 256-Ball BGA

	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1													
A	GND	I/O11 FX7	GND	I/O44 FX6	I/O58 CX6	GND	I/O70 CX2	I/O76 DX6	GND	GND	GND	GND	I/O108 AX5	I/O116 BX0	GND	I/O128 BX7	I/O134 O3	GND	GND	GND	A												
B	GND	I/O12 GX7	I/O28 FX5	I/O45 FX3	I/O59 CX7	I/O64 CX5	I/O71 CX3	I/O77 DX7	I/O84 DX5	I/O90 DX2	I/O96 AX0	I/O102 AX3	I/O109 AX6	I/O117 BX1	I/O122 BX4	I/O129 BX6	I/O135 O4	I/O148 O6	I/O164 O7	GND	B												
C	I/O0 GX6	I/O13 GX5	VCC	I/O46 FX4	I/O60 FX2	I/O65 FX1	I/O72 CX4	I/O78 CX0	I/O85 DX4	I/O91 DX1	I/O97 AX1	I/O103 AX4	I/O110 BX2	I/O118 BX5	I/O123 O0	I/O130 O1	I/O136 O5	VCC	I/O165 N7	I/O181 N6	C												
D	I/O1 EX7	I/O14 GX3	I/O29 GX4	VCC	VCC	I/O66 FX0	VCC	I/O79 CX1	I/O86 DX3	I/O92 DX0	I/O98 AX2	I/O104 AX7	I/O111 BX3	VCC	I/O124 O2	VCC	VCC	VCC	I/O149 N4	I/O166 N5	I/O182 P7	D											
E	I/O2 EX0	I/O15 GX0	I/O30 GX1	TDI	<p style="text-align: center;"><b>PIN DESIGNATIONS</b></p> <p>                     CLK = Clock                      GND = Ground                      I = Input                      I/O = Input/Output                      N/C = No Connect                      VCC = Supply Voltage                      TDI = Test Data In                      TCK = Test Clock                      TMS = Test Mode Select                      TDO = Test Data Out                 </p>												TDO	I/O150 N2	I/O167 N3	I/O183 P6	E												
F	GND	I/O16 EX1	I/O31 EX6	I/O47 GX2																									I/O137 N1	I/O151 N0	I/O168 P5	GND	F
G	I/O3 HX6	I/O17 EX4	I/O32 EX5	VCC																									VCC	I/O152 P4	I/O169 P3	I/O184 M7	G
H	GND	I/O18 HX5	I/O33 EX2	I/O48 EX3																									I/O138 P2	I/O153 P1	I/O170 P0	GND	H
J	I/O4 HX0	I/O19 HX1	I/O34 HX4	I/O49 HX7																									I/O139 M6	I/O154 M5	I/O171 M4	I/O185 M3	J
K	GND	CLK3	I/O35 HX2	I/O50 HX3																									I/O140 M0	I/O155 M1	CLK2	I/O186 M2	K
L	I/O5 A2	CLK0	I/O36 A0	I/O51 A1																									I/O141 L3	I/O156 L4	CLK1	GND	L
M	I/O6 A4	I/O20 A3	I/O37 A5	I/O52 A6																									I/O142 L6	I/O157 L5	I/O172 L0	I/O187 L1	M
N	GND	I/O21 A7	I/O38 D0	I/O53 D1																									I/O143 I5	I/O158 I0	I/O173 L7	GND	N
P	I/O7 D2	I/O22 D3	I/O39 D4	VCC																									VCC	I/O159 I4	I/O174 I1	I/O188 L2	P
R	GND	I/O23 D5	I/O40 D6	I/O54 D7													I/O144 K5	I/O160 K0	I/O175 I3	GND	R												
T	I/O8 B3	I/O24 B0	I/O41 B7	TCK													TMS	I/O161 K4	I/O176 K1	I/O189 I2	T												
U	I/O9 B4	I/O25 B1	I/O42 B6	VCC	VCC	I/O67 C0	VCC	I/O80 F0	I/O87 E5	I/O93 E2	I/O99 H2	I/O105 H5	I/O112 G0	VCC	I/O125 J1	VCC	VCC	I/O162 K7	I/O177 K2	I/O190 I6	U												
V	I/O10 B5	I/O26 B2	VCC	I/O55 C5	I/O61 C2	I/O68 C1	I/O73 F4	I/O81 F1	I/O88 E4	I/O94 E1	I/O100 H1	I/O106 H4	I/O113 G1	I/O119 G4	I/O126 J0	I/O131 J2	I/O145 J5	VCC	I/O178 K3	I/O191 I7	V												
W	GND	I/O27 C7	I/O43 C6	I/O56 C3	I/O62 F7	I/O69 F5	I/O74 F3	I/O82 E7	I/O89 E3	I/O95 E0	I/O101 H0	I/O107 H3	I/O114 H7	I/O120 G3	I/O127 G5	I/O132 G7	I/O146 J4	I/O163 J6	I/O179 J7	GND	W												
Y	GND	GND	GND	I/O57 C4	I/O63 F6	GND	I/O75 F2	I/O83 E6	GND	GND	GND	GND	I/O115 H6	I/O121 G2	GND	I/O133 G6	I/O147 J3	GND	I/O180 K6	GND	Y												
	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1													

17466G-046

# 388-BALL fpBGA CONNECTION DIAGRAM (M4A3-512/256)

## Bottom View

### 388-Ball fpBGA

	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	GND	I/O243 OX3	I/O240 OX0	I/O241 OX1	I/O236 NX4	I/O231 MX7	I/O228 MX4	I/O226 MX2	I/O255 PX7	I/O251 PX3	I/O248 PX0	I/O0 A0	I/O5 A5	I/O6 A6	I/O27 D3	I/O30 D6	I/O17 C1	I/O22 C6	I/O8 B0	I/O10 B2	N/C	GND	A
B	N/C	GND	I/O245 OX5	I/O242 OX2	I/O238 NX6	I/O234 NX2	I/O232 NX0	I/O229 MX5	I/O224 MX0	I/O253 PX5	I/O249 PX1	I/O2 A2	CLK0	I/O26 D2	I/O29 D5	I/O31 D7	I/O20 C4	I/O9 B1	I/O12 B4	I/O13 B5	GND	TDI	B
C	I/O213 KX5	TDO	GND	I/O247 OX7	I/O244 OX4	I/O239 NX7	I/O235 NX3	I/O230 MX6	I/O227 MX3	CLK3	I/O250 PX2	I/O1 A1	I/O7 A7	I/O25 D1	I/O16 C0	I/O18 C2	I/O23 C7	I/O11 B3	I/O15 B7	GND	I/O47 F7	I/O44 F4	C
D	I/O210 KX2	I/O212 KX4	I/O215 KX7	GND	I/O246 OX6	VCC	I/O237 NX5	I/O233 NX1	VCC	I/O254 PX6	VCC	I/O3 A3	I/O24 D0	VCC	I/O19 C3	I/O21 C5	VCC	I/O14 B6	GND	I/O46 F6	I/O43 F3	I/O41 F1	D
E	I/O207 JX7	I/O209 KX1	I/O211 KX3	I/O214 KX6															I/O45 F5	I/O42 F2	I/O40 F0	I/O54 G6	E
F	I/O203 JX3	I/O205 JX5	I/O208 KX0	VCC															VCC	I/O55 G7	I/O52 G4	I/O50 G2	F
G	I/O200 JX0	I/O202 JX2	I/O204 JX4	I/O206 JX6			VCC	VCC	N/C	I/O225 MX1	I/O252 PX4	I/O4 A4	I/O28 D4	N/C	VCC	VCC			I/O53 G5	I/O51 G3	I/O49 G1	I/O39 E7	G
H	I/O221 LX5	I/O222 LX6	I/O223 LX7	I/O201 JX1			VCC	N/C	GND	GND	GND	GND	GND	GND	N/C	VCC			I/O48 G0	I/O38 E6	I/O37 E5	I/O36 E4	H
J	I/O218 LX2	I/O219 LX3	I/O220 LX4	VCC			N/C	GND	GND	GND	GND	GND	GND	GND	GND	N/C			VCC	I/O35 E3	I/O34 E2	I/O32 E0	J
K	I/O197 IX5	I/O198 IX6	I/O199 IX7	I/O216 LX0			I/O217 LX1	GND	GND	GND	GND	GND	GND	GND	GND	I/O33 E1			I/O63 H7	I/O62 H6	I/O61 H5	I/O60 H4	K
L	I/O192 IX0	I/O194 IX2	I/O195 IX3	I/O196 IX4			I/O193 IX1	GND	GND	GND	GND	GND	GND	GND	GND	I/O58 H2			VCC	I/O59 H3	I/O57 H1	I/O56 H0	L
M	I/O184 HX0	I/O185 HX1	I/O187 HX3	VCC			I/O186 HX2	GND	GND	GND	GND	GND	GND	GND	GND	I/O69 I5			I/O67 I3	I/O65 I1	I/O66 I2	I/O64 I0	M
N	I/O188 HX4	I/O189 HX5	I/O191 HX7	I/O190 HX6			I/O182 EX2	GND	GND	GND	GND	GND	GND	GND	GND	I/O89 L1			I/O88 L0	I/O71 I7	I/O70 I6	I/O68 I4	N
P	I/O160 EX0	I/O161 EX1	I/O163 EX3	VCC			N/C	GND	GND	GND	GND	GND	GND	GND	GND	N/C			VCC	I/O92 L4	I/O91 L3	I/O90 L2	P
R	I/O164 EX4	I/O165 EX5	I/O166 EX6	I/O177 GX1			VCC	N/C	GND	GND	GND	GND	GND	GND	N/C	VCC			I/O74 J2	I/O95 L7	I/O94 L6	I/O93 L5	R
T	I/O167 EX7	I/O176 GX0	I/O179 GX3	I/O181 GX5			VCC	VCC	N/C	I/O152 DX0	I/O131 AX3	I/O122 P2	I/O98 M2	N/C	VCC	VCC			I/O78 J6	I/O76 J4	I/O73 J1	I/O72 J0	T
U	I/O178 GX2	I/O180 GX4	I/O183 GX7	VCC															VCC	I/O80 K0	I/O77 J5	I/O75 J3	U
V	I/O182 GX6	N/C	I/O169 FX1	I/O172 FX4															I/O86 K6	I/O83 K3	I/O81 K1	I/O79 J7	V
W	I/O168 FX0	I/O170 FX2	I/O173 FX5	GND	I/O143 BX7	VCC	I/O150 CX6	I/O145 CX1	VCC	I/O153 DX1	I/O123 P3	VCC	I/O96 M0	VCC	I/O104 N0	I/O111 N7	VCC	I/O119 O7	GND	I/O87 K7	I/O84 K4	I/O82 K2	W
Y	I/O171 FX3	I/O174 FX6	GND	I/O141 BX5	I/O138 BX2	I/O136 BX0	I/O147 CX3	I/O158 DX6	I/O156 DX4	CLK2	I/O132 AX4	I/O121 P1	I/O125 P5	I/O99 M3	I/O101 M5	I/O106 N2	I/O110 N6	I/O115 O3	I/O118 O6	GND	TMS	I/O85 K5	Y
AA	I/O175 FX7	GND	I/O142 BX6	I/O140 BX4	I/O151 CX7	I/O149 CX5	I/O144 CX0	I/O157 DX5	I/O154 DX2	I/O134 AX6	I/O130 AX2	I/O128 AX0	CLK1	I/O127 P7	I/O100 M4	I/O103 M7	I/O108 N4	I/O109 N5	I/O113 O1	I/O116 O4	GND	TCK	AA
AB	GND	N/C	I/O139 BX3	I/O137 BX1	I/O148 CX4	I/O146 CX2	I/O159 DX7	I/O155 DX3	I/O135 AX7	I/O133 AX5	I/O129 AX1	I/O120 P0	I/O124 P4	I/O126 P6	I/O97 M1	I/O102 M6	I/O105 N1	I/O107 N3	I/O112 O0	I/O114 O2	I/O117 O5	GND	AB

#### PIN DESIGNATIONS

- CLK = Clock
- GND = Ground
- I = Input
- I/O = Input/Output
- N/C = No Connect
- VCC = Supply Voltage
- TDI = Test Data In
- TCK = Test Clock
- TMS = Test Mode Select
- TDO = Test Data Out



m4a3.512.256\_388bga

# ispMACH 4A PRODUCT ORDERING INFORMATION

## ispMACH 4A Devices Commercial and Industrial - 3.3V and 5V

Lattice programmable logic products are available with several ordering options. The order number (Valid Combination) is formed by a combination of:

<p><b>FAMILY TYPE</b></p> <p>M4A3- = ispMACH 4A Family Low Voltage Advanced Feature (3.3-V <math>V_{CC}</math>)</p> <p>M4A5- = ispMACH 4A Family Advanced Feature (5-V <math>V_{CC}</math>)</p> <p><b>MACROCELL DENSITY</b></p> <table border="0"> <tr> <td>32 = 32 Macrocells</td> <td>192 = 192 Macrocells</td> </tr> <tr> <td>64 = 64 Macrocells</td> <td>256 = 256 Macrocells</td> </tr> <tr> <td>96 = 96 Macrocells</td> <td>384 = 384 Macrocells</td> </tr> <tr> <td>128 = 128 Macrocells</td> <td>512 = 512 Macrocells</td> </tr> </table> <p><b>I/Os</b></p> <p>/32 = 32 I/Os in 44-pin PLCC, 44-pin TQFP or 48-pin TQFP</p> <p>/48 = 48 I/Os in 100-pin TQFP</p> <p>/64 = 64 I/Os in 100-pin TQFP, 100-pin PQFP, or 100-ball caBGA</p> <p>/96 = 96 I/Os in 144-pin TQFP or 144-ball fpBGA</p> <p>/128 = 128 I/Os in 208-pin PQFP, 256-ball BGA or 256-ball fpBGA</p> <p>/160 = 160 I/Os in 208-pin PQFP</p> <p>/192 = 192 I/Os in 256-ball BGA or 256-ball fpBGA</p> <p>/256 = 256 I/Os in 388-ball fpBGA</p>	32 = 32 Macrocells	192 = 192 Macrocells	64 = 64 Macrocells	256 = 256 Macrocells	96 = 96 Macrocells	384 = 384 Macrocells	128 = 128 Macrocells	512 = 512 Macrocells	<p><b>M4A3-</b>    <b>256 / 128</b>    <b>-7</b>    <b>Y</b>    <b>C</b></p>	<p><b>OPERATING CONDITIONS</b></p> <p>C = Commercial (0°C to +70°C)</p> <p>I = Industrial (-40°C to +85°C)</p> <p><b>PACKAGE TYPE</b></p> <p>SA = Ball Grid Array (BGA)</p> <p>J = Plastic Leaded Chip Carrier (PLCC)</p> <p>JN = Lead-free Plastic Leaded Chip Carrier (PLCC)</p> <p>V = Thin Quad Flat Pack (TQFP)</p> <p>VN = Lead-free Thin Quad Flat Pack (TQFP)</p> <p>Y = Plastic Quad Flat Pack (PQFP)</p> <p>YN = Lead-free Plastic Quad Flat Pack (PQFP)</p> <p>FA = Fine-pitch Ball Grid Array (fpBGA)</p> <p>FAN = Lead-free Fine-pitch Ball Grid Array (fpBGA)</p> <p>CA = Chip-array Ball Grid Array (caBGA)</p> <p><b>SPEED</b></p> <p>-5 = 5.0 ns <math>t_{PD}</math></p> <p>-55 = 5.5 ns <math>t_{PD}</math></p> <p>-6 = 6.0 ns <math>t_{PD}</math></p> <p>-65 = 6.5 ns <math>t_{PD}</math></p> <p>-7 = 7.5 ns <math>t_{PD}</math></p> <p>-10 = 10 ns <math>t_{PD}</math></p> <p>-12 = 12 ns <math>t_{PD}</math></p> <p>-14 = 14 ns <math>t_{PD}</math></p>
32 = 32 Macrocells	192 = 192 Macrocells									
64 = 64 Macrocells	256 = 256 Macrocells									
96 = 96 Macrocells	384 = 384 Macrocells									
128 = 128 Macrocells	512 = 512 Macrocells									

\*Package obsolete, contact factory.

### Conventional Packaging

3.3V Commercial Combinations		
M4A3-32/32	-5, -7, -10	JC, VC, VC48
M4A3-64/32		JC, VC, VC48
M4A3-64/64	-55, -7, -10	VC
M4A3-96/48		VC
M4A3-128/64		YC, VC, CAC
M4A3-192/96	-6, -7, -10	VC, FAC
M4A3-256/128	-55, -65 <sup>1</sup> , -7, -10	YC, FAC, SAC
M4A3-256/160	-7, -10	YC
M4A3-256/192		FAC
M4A3-384/160	-65, -10, -12	YC
M4A3-384/192		SAC, FAC
M4A3-512/160	-7, -10, -12	YC
M4A3-512/192		FAC
M4A3-512/256		FAC

3.3V Industrial Combinations		
M4A3-32/32	-7, -10, -12	JI, VI, VI48
M4A3-64/32		JI, VI, VI48
M4A3-64/64		VI
M4A3-96/48		VI
M4A3-128/64		YI, VI, CAI
M4A3-192/96		VI, FAI
M4A3-256/128	-10, -12	YI, FAI, SAI
M4A3-256/160		YI
M4A3-256/192		FAI
M4A3-384/160	-10, -12, -14	YI
M4A3-384/192		FAI
M4A3-512/160		YI
M4A3-512/192		FAI
M4A3-512/256		FAI

1. Use 5.5ns for new designs.