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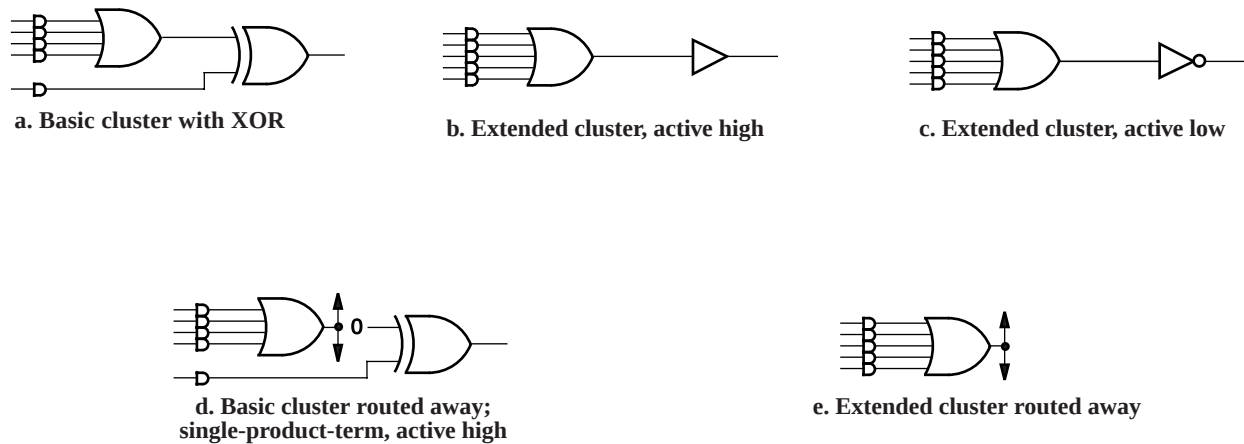
## Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

## Applications of Embedded - CPLDs

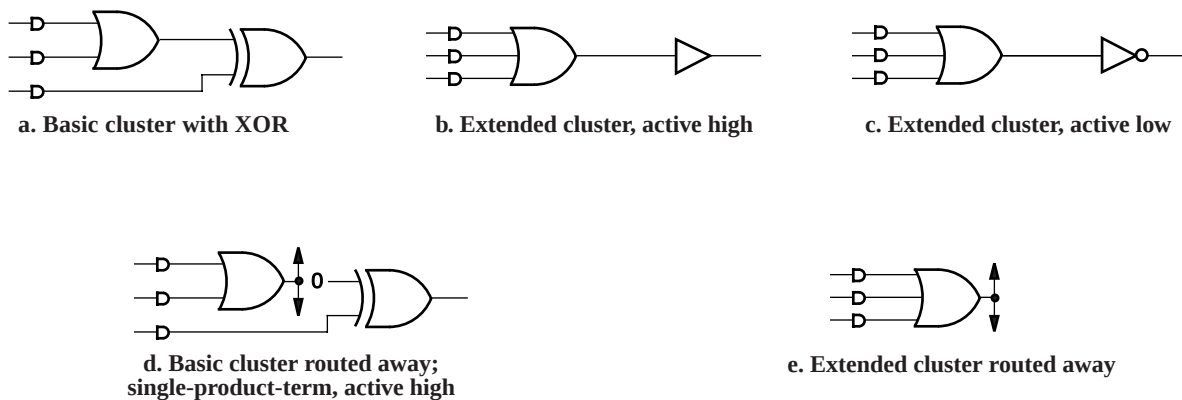
### Details

|                                 |                                                                                                                                                                     |
|---------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Product Status                  | Not For New Designs                                                                                                                                                 |
| Programmable Type               | In System Programmable                                                                                                                                              |
| Delay Time tpd(1) Max           | 7.5 ns                                                                                                                                                              |
| Voltage Supply - Internal       | 4.75V ~ 5.25V                                                                                                                                                       |
| Number of Logic Elements/Blocks | -                                                                                                                                                                   |
| Number of Macrocells            | 96                                                                                                                                                                  |
| Number of Gates                 | -                                                                                                                                                                   |
| Number of I/O                   | 48                                                                                                                                                                  |
| Operating Temperature           | 0°C ~ 70°C (TA)                                                                                                                                                     |
| Mounting Type                   | Surface Mount                                                                                                                                                       |
| Package / Case                  | 100-LQFP                                                                                                                                                            |
| Supplier Device Package         | 100-TQFP (14x14)                                                                                                                                                    |
| Purchase URL                    | <a href="https://www.e-xfl.com/product-detail/lattice-semiconductor/m4a5-96-48-7vnc">https://www.e-xfl.com/product-detail/lattice-semiconductor/m4a5-96-48-7vnc</a> |



17466G-007

**Figure 3. Logic Allocator Configurations: Synchronous Mode**



17466G-008

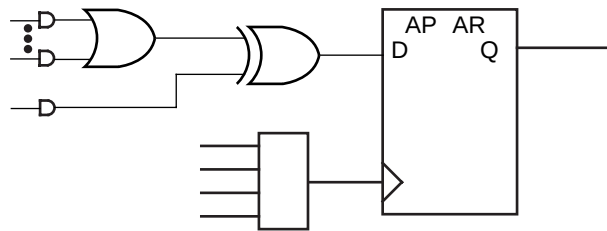
**Figure 4. Logic Allocator Configurations: Asynchronous Mode**

Note that the configuration of the logic allocator has absolutely no impact on the speed of the signal. All configurations have the same delay. This means that designers do not have to decide between optimizing resources or speed; both can be optimized.

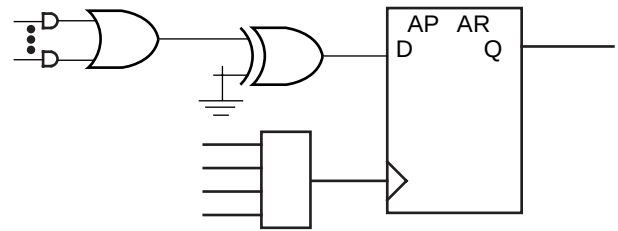
If not used in the cluster, the extra product term can act in conjunction with the basic cluster to provide XOR logic for such functions as data comparison, or it can work with the D-,T-type flip-flop to provide for J-K, and S-R register operation. In addition, if the basic cluster is routed to another macrocell, the extra product term is still available for logic. In this case, the first XOR input will be a logic 0. This circuit has the flexibility to route product terms elsewhere without giving up the use of the macrocell.

Product term clusters do not “wrap” around a PAL block. This means that the macrocells at the ends of the block have fewer product terms available.

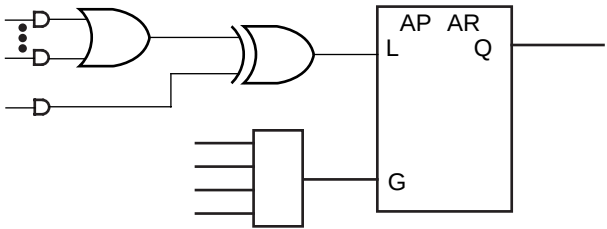
The flip-flop can be configured as a D-type or T-type latch. J-K or S-R registers can be synthesized. The primary flip-flop configurations are shown in Figure 6, although others are possible. Flip-flop functionality is defined in Table 8. Note that a J-K latch is inadvisable as it will cause oscillation if both J and K inputs are HIGH.



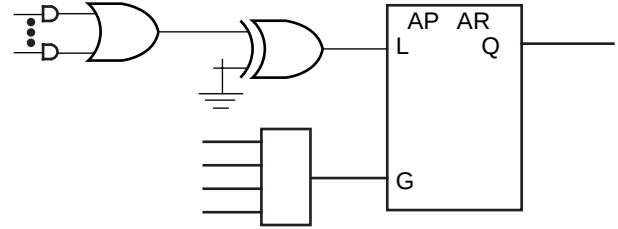
a. D-type with XOR



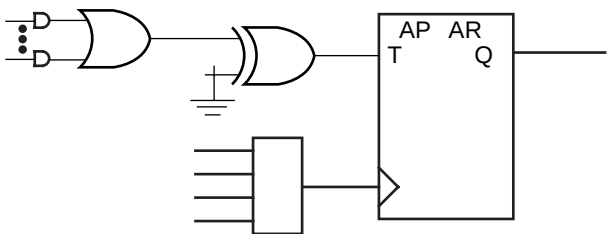
b. D-type with programmable D polarity



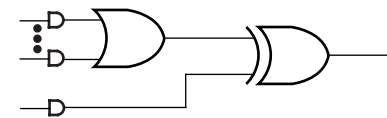
c. Latch with XOR



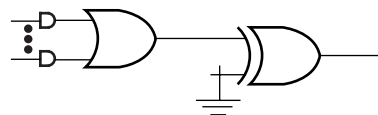
d. Latch with programmable D polarity



e. T-type with programmable T polarity



f. Combinatorial with XOR

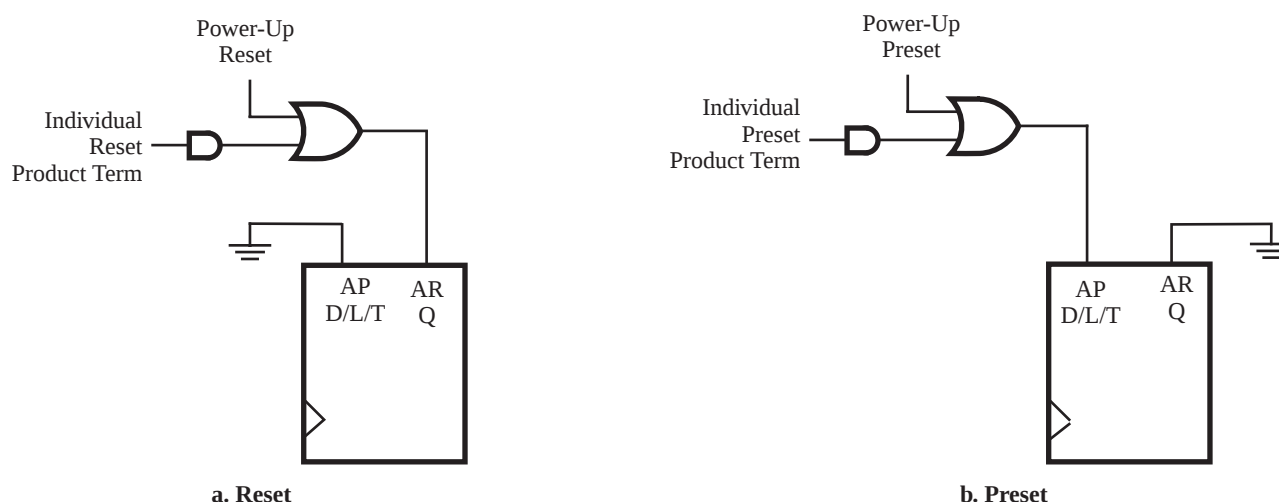


g. Combinatorial with programmable polarity

Figure 6. Primary Macrocell Configurations

17466G-011

A reset/preset swapping feature in each macrocell allows for reset and preset to be exchanged, providing flexibility. In asynchronous mode (Figure 8), a single individual product term is provided for initialization. It can be selected to control reset or preset.



17466G-014

17466G-015

**Figure 8. Asynchronous Mode Initialization Configurations**

Note that the reset/preset swapping selection feature effects power-up reset as well. The initialization functionality of the flip-flops is illustrated in Table 9. The macrocell sends its data to the output switch matrix and the input switch matrix. The output switch matrix can route this data to an output if so desired. The input switch matrix can send the signal back to the central switch matrix as feedback.

**Table 9. Asynchronous Reset/Preset Operation**

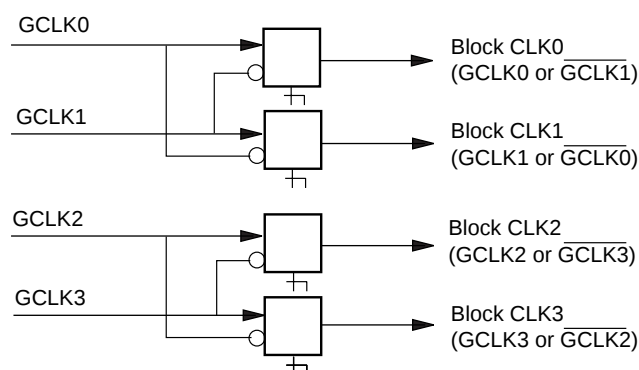
| AR | AP | CLK/LE <sup>1</sup> | Q+          |
|----|----|---------------------|-------------|
| 0  | 0  | X                   | See Table 8 |
| 0  | 1  | X                   | 1           |
| 1  | 0  | X                   | 0           |
| 1  | 1  | X                   | 0           |

**Note:**

- Transparent latch is unaffected by AR, AP

## PAL Block Clock Generation

Each ispMACH 4A device has four clock pins that can also be used as inputs. These pins drive a clock generator in each PAL block (Figure 14). The clock generator provides four clock signals that can be used anywhere in the PAL block. These four PAL block clock signals can consist of a large number of combinations of the true and complement edges of the global clock signals. Table 14 lists the possible combinations.



17466G-004

**Figure 14. PAL Block Clock Generator**<sup>1</sup>

1. M4A(3,5)-32/32 and M4A(3,5)-64/32 have only two clock pins, GCLK0 and GCLK1. GCLK2 is tied to GCLK0, and GCLK3 is tied to GCLK1.

**Table 14. PAL Block Clock Combinations**<sup>1</sup>

| Block CLK0                | Block CLK1                | Block CLK2                                              | Block CLK3                                              |
|---------------------------|---------------------------|---------------------------------------------------------|---------------------------------------------------------|
| GCLK0                     | GCLK1                     | X                                                       | X                                                       |
| $\overline{\text{GCLK1}}$ | GCLK1                     | X                                                       | X                                                       |
| GCLK0                     | $\overline{\text{GCLK0}}$ | X                                                       | X                                                       |
| $\overline{\text{GCLK1}}$ | $\overline{\text{GCLK0}}$ | X                                                       | X                                                       |
| X                         | X                         | GCLK2 (GCLK0)                                           | GCLK3 (GCLK1)                                           |
| X                         | X                         | $\overline{\text{GCLK3}}$ ( $\overline{\text{GCLK1}}$ ) | GCLK3 (GCLK1)                                           |
| X                         | X                         | GCLK2 (GCLK0)                                           | $\overline{\text{GCLK2}}$ ( $\overline{\text{GCLK0}}$ ) |
| X                         | X                         | $\overline{\text{GCLK3}}$ (GCLK1)                       | $\overline{\text{GCLK2}}$ ( $\overline{\text{GCLK0}}$ ) |

**Note:**

1. Values in parentheses are for the M4A(3,5)-32/32 and M4A(3,5)-64/32.

This feature provides high flexibility for partitioning state machines and dual-phase clocks. It also allows latches to be driven with either polarity of latch enable, and in a master-slave configuration.

weakly pulled up. For the circuit diagram, please refer to the document entitled *MACH Endurance Characteristics* on the Lattice Data Book CD-ROM or Lattice web site.

## **POWER MANAGEMENT**

Each individual PAL block in ispMACH 4A devices features a programmable low-power mode, which results in power savings of up to 50%. The signal speed paths in the low-power PAL block will be slower than those in the non-low-power PAL block. This feature allows speed critical paths to run at maximum frequency while the rest of the signal paths operate in the low-power mode.

## **PROGRAMMABLE SLEW RATE**

Each ispMACH 4A device I/O has an individually programmable output slew rate control bit. Each output can be individually configured for the higher speed transition (3 V/ns) or for the lower noise transition (1 V/ns). For high-speed designs with long, unterminated traces, the slow-slew rate will introduce fewer reflections, less noise, and keep ground bounce to a minimum. For designs with short traces or well terminated lines, the fast slew rate can be used to achieve the highest speed. The slew rate is adjusted independent of power.

## **POWER-UP RESET/SET**

All flip-flops power up to a known state for predictable system initialization. If a macrocell is configured to SET on a signal from the control generator, then that macrocell will be SET during device power-up. If a macrocell is configured to RESET on a signal from the control generator or is not configured for set/reset, then that macrocell will RESET on power-up. To guarantee initialization values, the  $V_{CC}$  rise must be monotonic, and the clock must be inactive until the reset delay time has elapsed.

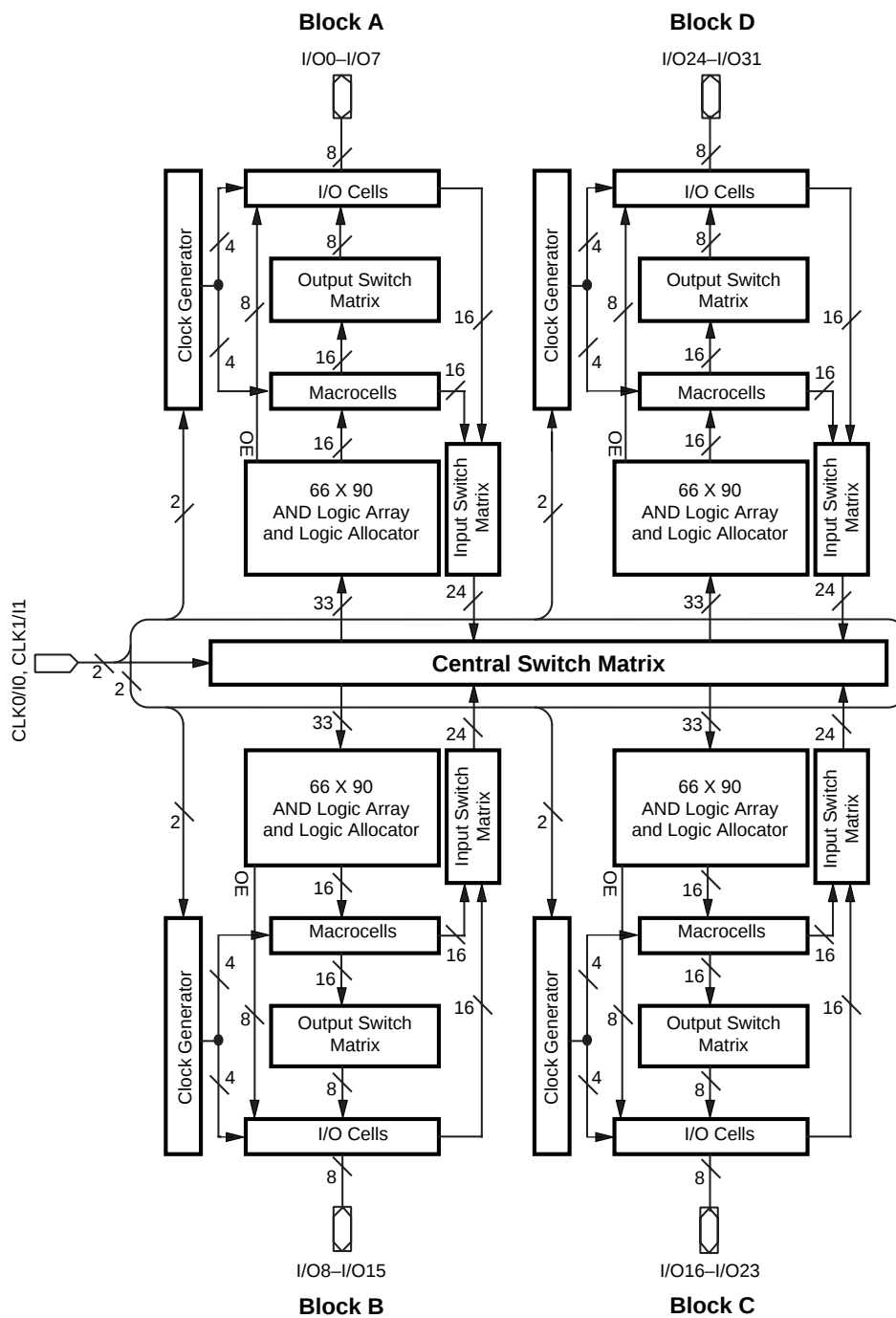
## **SECURITY BIT**

A programmable security bit is provided on the ispMACH 4A devices as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, this bit defeats readback of the programmed pattern by a device programmer, securing proprietary designs from competitors. Programming and verification are also defeated by the security bit. The bit can only be reset by erasing the entire device.

## **HOT SOCKETING**

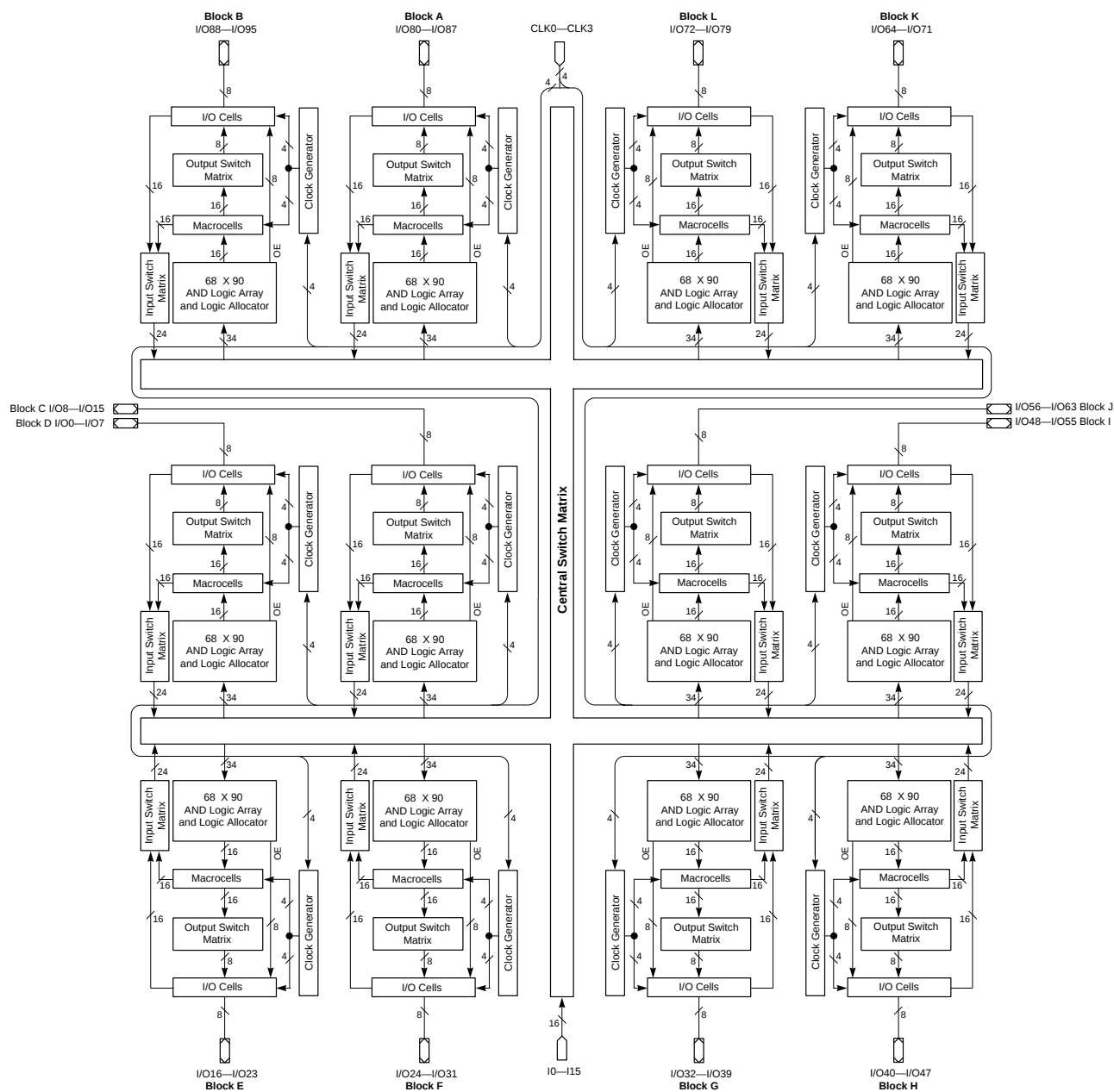
ispMACH 4A devices are well-suited for those applications that require hot socketing capability. Hot socketing a device requires that the device, when powered down, can tolerate active signals on the I/Os and inputs without being damaged. Additionally, it requires that the effects of the powered-down MACH devices be minimal on active signals.

## BLOCK DIAGRAM – M4A(3,5)-64/32



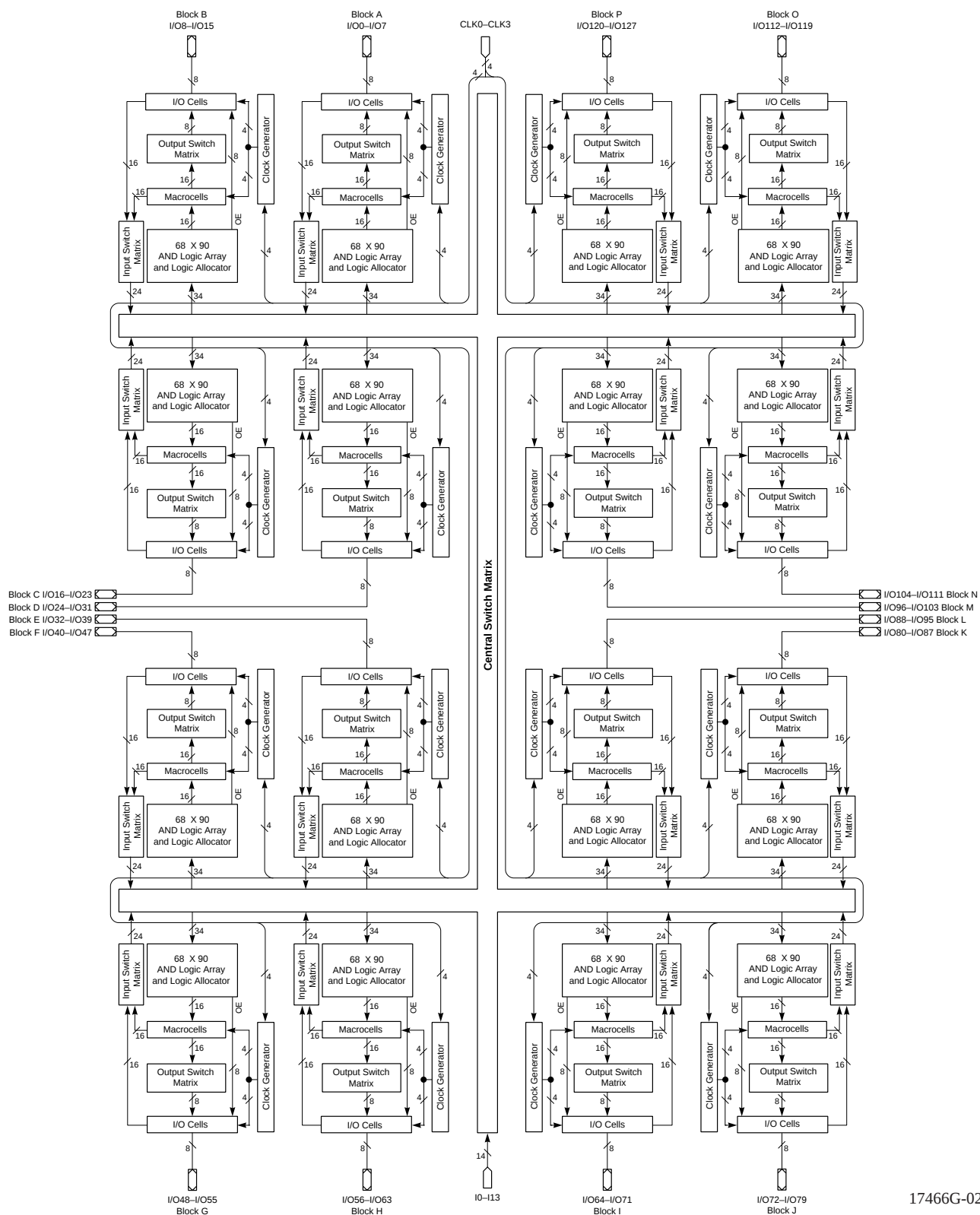
17466H-020

## BLOCK DIAGRAM – M4A(3,5)-192/96



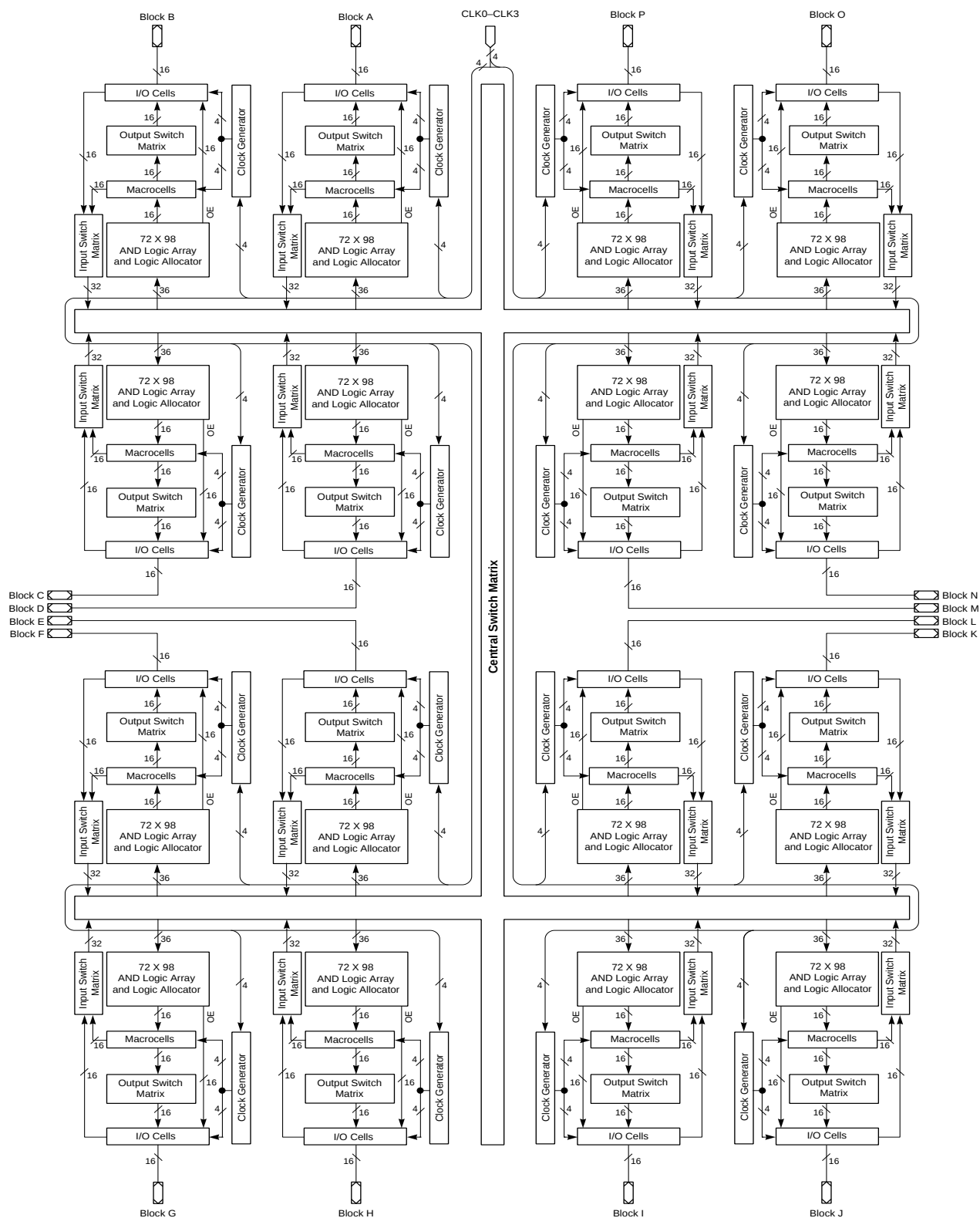
17466G-067

## BLOCK DIAGRAM – M4A(3,5)-256/128



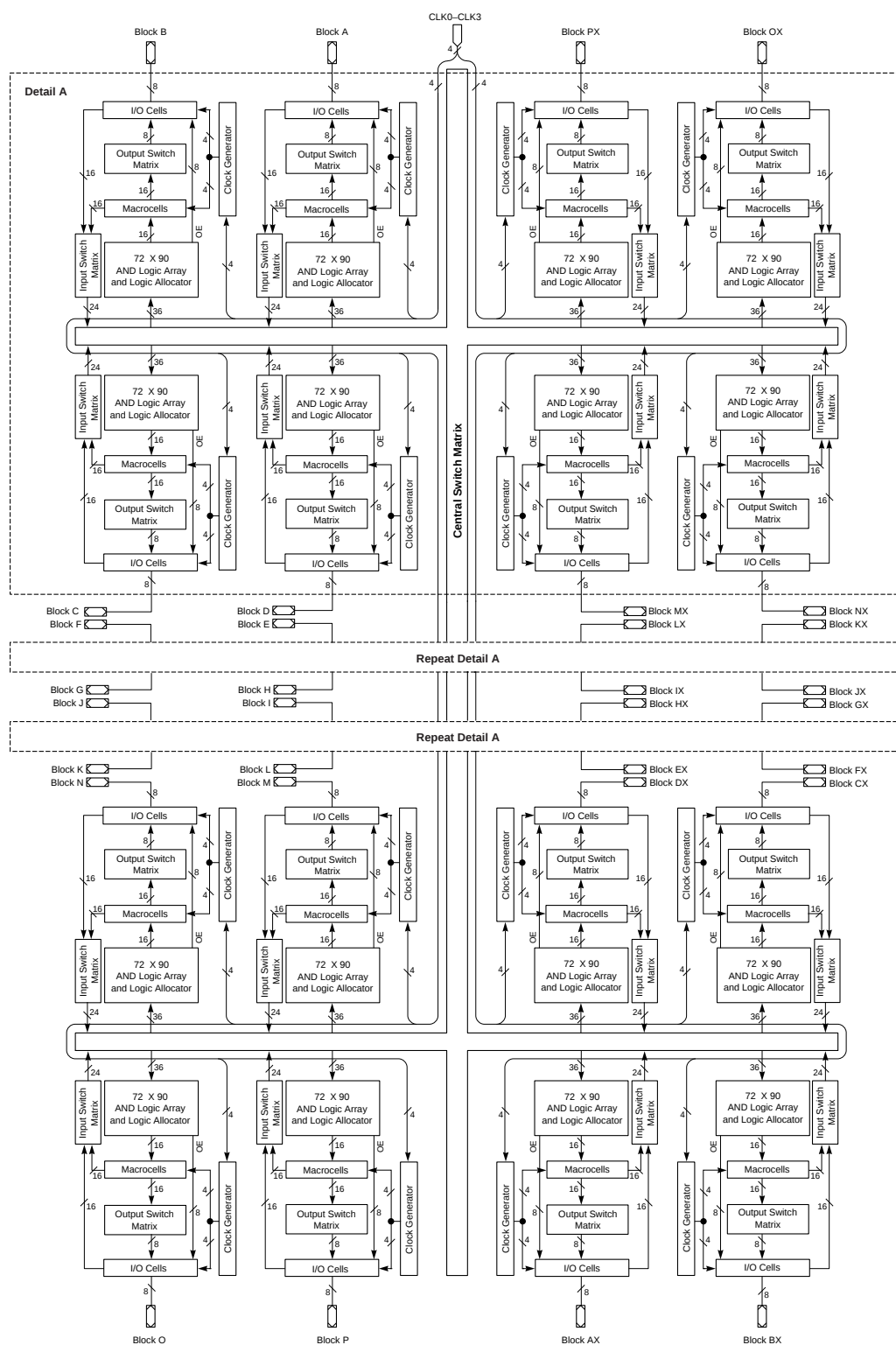
17466G-024

## BLOCK DIAGRAM – M4A3-256/160, M4A3-256/192



17466G-050

# BLOCK DIAGRAM - M4A3-512/160, M4A3-512/192, M4A3-512/256



17466G-068

## ABSOLUTE MAXIMUM RATINGS

### M4A5

Storage Temperature. . . . . -65°C to +150°C  
 Ambient Temperature  
 with Power Applied. . . . . -55°C to +100°C  
 Device Junction Temperature. . . . . +130°C  
 Supply Voltage  
 with Respect to Ground . . . . . -0.5 V to +7.0 V  
 DC Input Voltage . . . . . -0.5 V to  $V_{CC} + 0.5$  V  
 Static Discharge Voltage . . . . . 2000 V  
 Latchup Current ( $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ) . . . . . 200 mA

*Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.*

## OPERATING RANGES

### Commercial (C) Devices

Ambient Temperature ( $T_A$ )  
 Operating in Free Air. . . . .  $0^\circ\text{C}$  to  $+70^\circ\text{C}$   
 Supply Voltage ( $V_{CC}$ )  
 with Respect to Ground. . . . . +4.75 V to +5.25 V

### Industrial (I) Devices

Ambient Temperature ( $T_A$ )  
 Operating in Free Air. . . . .  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$   
 Supply Voltage ( $V_{CC}$ )  
 with Respect to Ground. . . . . +4.50 V to +5.5 V  
*Operating ranges define those limits between which the functionality of the device is guaranteed.*

## 5-V DC CHARACTERISTICS OVER OPERATING RANGES

| Parameter Symbol | Parameter Description                 | Test Conditions                                                                       | Min | Typ | Max  | Unit          |
|------------------|---------------------------------------|---------------------------------------------------------------------------------------|-----|-----|------|---------------|
| $V_{OH}$         | Output HIGH Voltage                   | $I_{OH} = -3.2$ mA, $V_{CC} = \text{Min}$ , $V_{IN} = V_{IH}$ or $V_{IL}$             | 2.4 |     |      | V             |
|                  |                                       | $I_{OH} = -100$ $\mu\text{A}$ , $V_{CC} = \text{Max}$ , $V_{IN} = V_{IH}$ or $V_{IL}$ |     | 3.3 | 3.6  | V             |
| $V_{OL}$         | Output LOW Voltage                    | $I_{OL} = 24$ mA, $V_{CC} = \text{Min}$ , $V_{IN} = V_{IH}$ or $V_{IL}$ (Note 1)      |     |     | 0.5  | V             |
| $V_{IH}$         | Input HIGH Voltage                    | Guaranteed Input Logical HIGH Voltage for all Inputs (Note 2)                         | 2.0 |     |      | V             |
| $V_{IL}$         | Input LOW Voltage                     | Guaranteed Input Logical LOW Voltage for all Inputs (Note 2)                          |     |     | 0.8  | V             |
| $I_{IH}$         | Input HIGH Leakage Current            | $V_{IN} = 5.25$ V, $V_{CC} = \text{Max}$ (Note 3)                                     |     |     | 10   | $\mu\text{A}$ |
| $I_{IL}$         | Input LOW Leakage Current             | $V_{IN} = 0$ V, $V_{CC} = \text{Max}$ (Note 3)                                        |     |     | -10  | $\mu\text{A}$ |
| $I_{OZH}$        | Off-State Output Leakage Current HIGH | $V_{OUT} = 5.25$ V, $V_{CC} = \text{Max}$ , $V_{IN} = V_{IH}$ or $V_{IL}$ (Note 3)    |     |     | 10   | $\mu\text{A}$ |
| $I_{OZL}$        | Off-State Output Leakage Current LOW  | $V_{OUT} = 0$ V, $V_{CC} = \text{Max}$ , $V_{IN} = V_{IH}$ or $V_{IL}$ (Note 3)       |     |     | -10  | $\mu\text{A}$ |
| $I_{SC}$         | Output Short-Circuit Current          | $V_{OUT} = 0.5$ V, $V_{CC} = \text{Max}$ (Note 4)                                     | -30 |     | -160 | mA            |

### Notes:

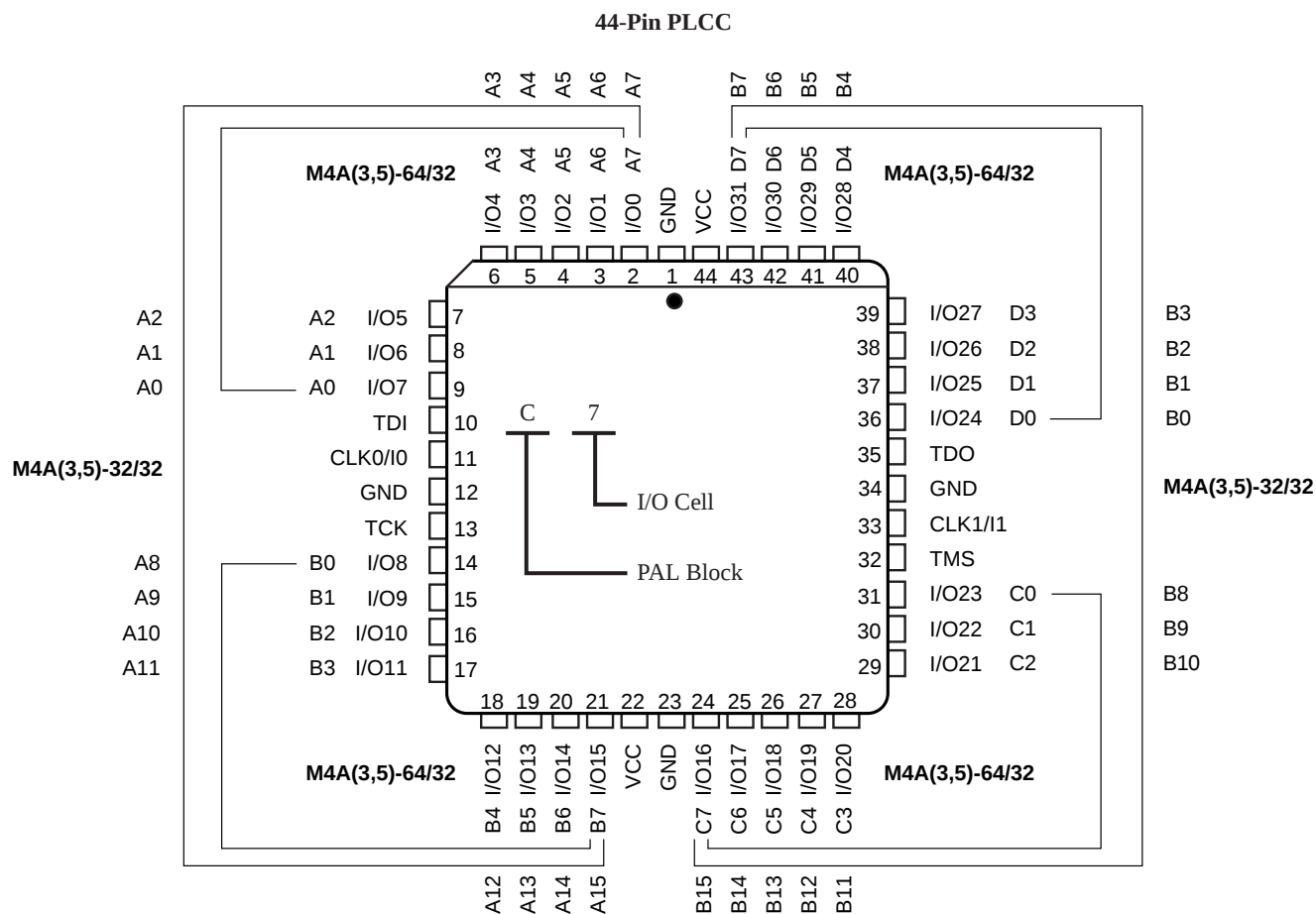
1. Total  $I_{OL}$  for one PAL block should not exceed 64 mA.
2. These are absolute values with respect to device ground, and all overshoots due to system or tester noise are included.
3. I/O pin leakage is the worst case of  $I_{IL}$  and  $I_{OZL}$  (or  $I_{IH}$  and  $I_{OZH}$ ).
4. Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.  
 $V_{OUT} = 0.5$  V has been chosen to avoid test problems caused by tester ground degradation.

## ispMACH 4A TIMING PARAMETERS OVER OPERATING RANGES<sup>1</sup>

|                        |                                                       | -5  |     | -55 |     | -6  |     | -65 |     | -7  |      | -10 |      | -12 |      | -14  |      | Unit |
|------------------------|-------------------------------------------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|------|-----|------|-----|------|------|------|------|
|                        |                                                       | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max  | Min | Max  | Min | Max  | Min  | Max  |      |
| Combinatorial Delay:   |                                                       |     |     |     |     |     |     |     |     |     |      |     |      |     |      |      |      |      |
| t <sub>PDi</sub>       | Internal combinatorial propagation delay              |     | 3.5 |     | 4.0 |     | 4.3 |     | 4.5 |     | 5.0  |     | 7.0  |     | 9.0  |      | 11.0 | ns   |
| t <sub>PD</sub>        | Combinatorial propagation delay                       |     | 5.0 |     | 5.5 |     | 6.0 |     | 6.5 |     | 7.5  |     | 10.0 |     | 12.0 |      | 14.0 | ns   |
| Registered Delays:     |                                                       |     |     |     |     |     |     |     |     |     |      |     |      |     |      |      |      |      |
| t <sub>SS</sub>        | Synchronous clock setup time, D-type register         | 3.0 |     | 3.5 |     | 3.5 |     | 3.5 |     | 5.0 |      | 5.5 |      | 7.0 |      | 10.0 |      | ns   |
| t <sub>SST</sub>       | Synchronous clock setup time, T-type register         | 4.0 |     | 4.0 |     | 4.0 |     | 4.0 |     | 6.0 |      | 6.5 |      | 8.0 |      | 11.0 |      | ns   |
| t <sub>SA</sub>        | Asynchronous clock setup time, D-type register        | 2.5 |     | 2.5 |     | 2.5 |     | 3.0 |     | 3.5 |      | 4.0 |      | 5.0 |      | 8.0  |      | ns   |
| t <sub>SAT</sub>       | Asynchronous clock setup time, T-type register        | 3.0 |     | 3.0 |     | 3.0 |     | 3.5 |     | 4.5 |      | 5.0 |      | 6.0 |      | 9.0  |      | ns   |
| t <sub>HS</sub>        | Synchronous clock hold time                           | 0.0 |     | 0.0 |     | 0.0 |     | 0.0 |     | 0.0 |      | 0.0 |      | 0.0 |      | 0.0  |      | ns   |
| t <sub>HA</sub>        | Asynchronous clock hold time                          | 2.5 |     | 2.5 |     | 2.5 |     | 3.0 |     | 3.5 |      | 4.0 |      | 5.0 |      | 8.0  |      | ns   |
| t <sub>COsi</sub>      | Synchronous clock to internal output                  |     | 2.5 |     | 2.5 |     | 2.8 |     | 3.0 |     | 3.0  |     | 3.0  |     | 3.5  |      | 3.5  | ns   |
| t <sub>COS</sub>       | Synchronous clock to output                           |     | 4.0 |     | 4.0 |     | 4.5 |     | 5.0 |     | 5.5  |     | 6.0  |     | 6.5  |      | 6.5  | ns   |
| t <sub>COAi</sub>      | Asynchronous clock to internal output                 |     | 5.0 |     | 5.0 |     | 5.0 |     | 5.0 |     | 6.0  |     | 8.0  |     | 10.0 |      | 12.0 | ns   |
| t <sub>COA</sub>       | Asynchronous clock to output                          |     | 6.5 |     | 6.5 |     | 6.8 |     | 7.0 |     | 8.5  |     | 11.0 |     | 13.0 |      | 15.0 | ns   |
| Latched Delays:        |                                                       |     |     |     |     |     |     |     |     |     |      |     |      |     |      |      |      |      |
| t <sub>SSL</sub>       | Synchronous latch setup time                          | 4.0 |     | 4.0 |     | 4.0 |     | 4.5 |     | 6.0 |      | 7.0 |      | 8.0 |      | 10.0 |      | ns   |
| t <sub>SAL</sub>       | Asynchronous latch setup time                         | 3.0 |     | 3.0 |     | 3.5 |     | 3.5 |     | 4.0 |      | 4.0 |      | 5.0 |      | 8.0  |      | ns   |
| t <sub>HSL</sub>       | Synchronous latch hold time                           | 0.0 |     | 0.0 |     | 0.0 |     | 0.0 |     | 0.0 |      | 0.0 |      | 0.0 |      | 0.0  |      | ns   |
| t <sub>HAL</sub>       | Asynchronous latch hold time                          | 3.0 |     | 3.0 |     | 3.5 |     | 3.5 |     | 4.0 |      | 4.0 |      | 5.0 |      | 8.0  |      | ns   |
| t <sub>PDLi</sub>      | Transparent latch to internal output                  |     | 5.5 |     | 5.5 |     | 5.8 |     | 6.0 |     | 7.5  |     | 9.0  |     | 11.0 |      | 12.0 | ns   |
| t <sub>PDL</sub>       | Propagation delay through transparent latch to output |     | 7.0 |     | 7.0 |     | 7.5 |     | 8.0 |     | 10.0 |     | 12.0 |     | 14.0 |      | 15.0 | ns   |
| t <sub>GOSi</sub>      | Synchronous gate to internal output                   |     | 3.0 |     | 3.0 |     | 3.0 |     | 3.0 |     | 3.5  |     | 4.5  |     | 7.0  |      | 8.0  | ns   |
| t <sub>GOS</sub>       | Synchronous gate to output                            |     | 4.5 |     | 4.5 |     | 4.8 |     | 5.0 |     | 6.0  |     | 7.5  |     | 10.0 |      | 11.0 | ns   |
| t <sub>GOAi</sub>      | Asynchronous gate to internal output                  |     | 6.0 |     | 6.0 |     | 6.0 |     | 6.0 |     | 8.5  |     | 10.0 |     | 13.0 |      | 15.0 | ns   |
| t <sub>GOA</sub>       | Asynchronous gate to output                           |     | 7.5 |     | 7.5 |     | 7.8 |     | 8.0 |     | 11.0 |     | 13.0 |     | 16.0 |      | 18.0 | ns   |
| Input Register Delays: |                                                       |     |     |     |     |     |     |     |     |     |      |     |      |     |      |      |      |      |
| t <sub>SIRS</sub>      | Input register setup time                             | 1.5 |     | 1.5 |     | 2.0 |     | 2.0 |     | 2.0 |      | 2.0 |      | 2.0 |      | 2.0  |      | ns   |
| t <sub>HIRS</sub>      | Input register hold time                              | 2.5 |     | 2.5 |     | 3.0 |     | 3.0 |     | 3.0 |      | 3.0 |      | 3.0 |      | 4.0  |      | ns   |
| t <sub>ICOSi</sub>     | Input register clock to internal feedback             |     | 3.0 |     | 3.0 |     | 3.0 |     | 3.0 |     | 3.5  |     | 4.5  |     | 6.0  |      | 6.0  | ns   |
| Input Latch Delays:    |                                                       |     |     |     |     |     |     |     |     |     |      |     |      |     |      |      |      |      |
| t <sub>SIL</sub>       | Input latch setup time                                | 1.5 |     | 1.5 |     | 1.5 |     | 2.0 |     | 2.0 |      | 2.0 |      | 2.0 |      | 2.0  |      | ns   |
| t <sub>HIL</sub>       | Input latch hold time                                 | 2.5 |     | 2.5 |     | 2.5 |     | 3.0 |     | 3.0 |      | 3.0 |      | 3.0 |      | 4.0  |      | ns   |
| t <sub>IGOSi</sub>     | Input latch gate to internal feedback                 |     | 3.5 |     | 3.5 |     | 3.8 |     | 4.0 |     | 4.0  |     | 4.0  |     | 4.0  |      | 5.0  | ns   |
| t <sub>PDILi</sub>     | Transparent input latch to internal feedback          |     | 1.5 |     | 1.5 |     | 1.5 |     | 1.5 |     | 2.0  |     | 2.0  |     | 2.0  |      | 2.0  | ns   |

## 44-PIN PLCC CONNECTION DIAGRAM (M4A(3,5)-32/32 AND M4A(3,5)-64/32)

### Top View



17466G-026

## PIN DESIGNATIONS

CLK/I = Clock or Input

GND = Ground

I/O = Input/Output

V<sub>CC</sub> = Supply Voltage

TDI = Test Data In

TCK = Test Clock

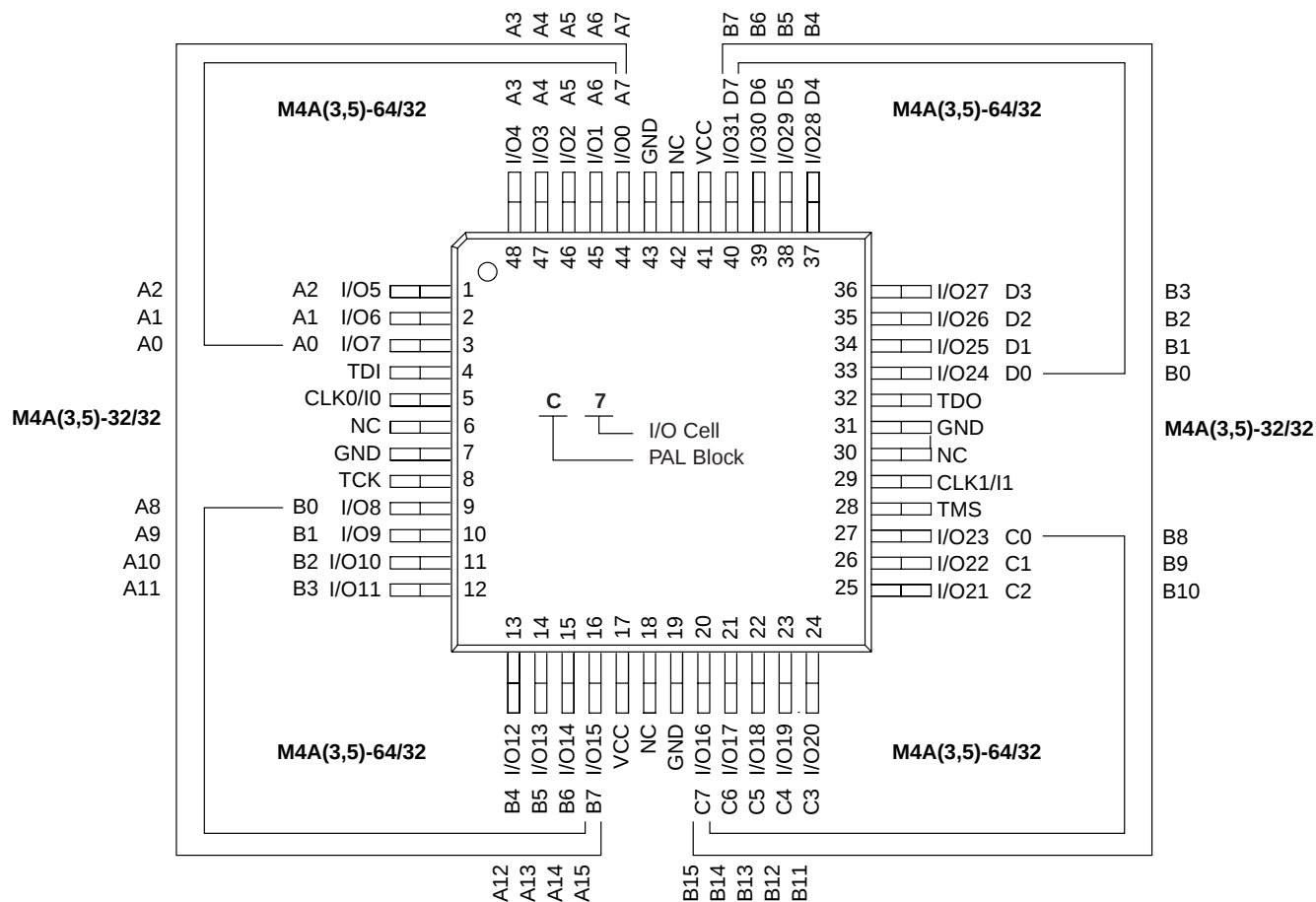
TMS = Test Mode Select

TDO = Test Data Out

## 48-PIN TQFP CONNECTION DIAGRAM (M4A(3,5)-32/32 AND M4A(3,5)-64/32)

### Top View

48-Pin TQFP (1.4mm Thickness)



17466G-028

## PIN DESIGNATIONS

CLK/I = Clock or Input

GND = Ground

I/O = Input/Output

V<sub>CC</sub> = Supply Voltage

NC = No Connect

TDI = Test Data In

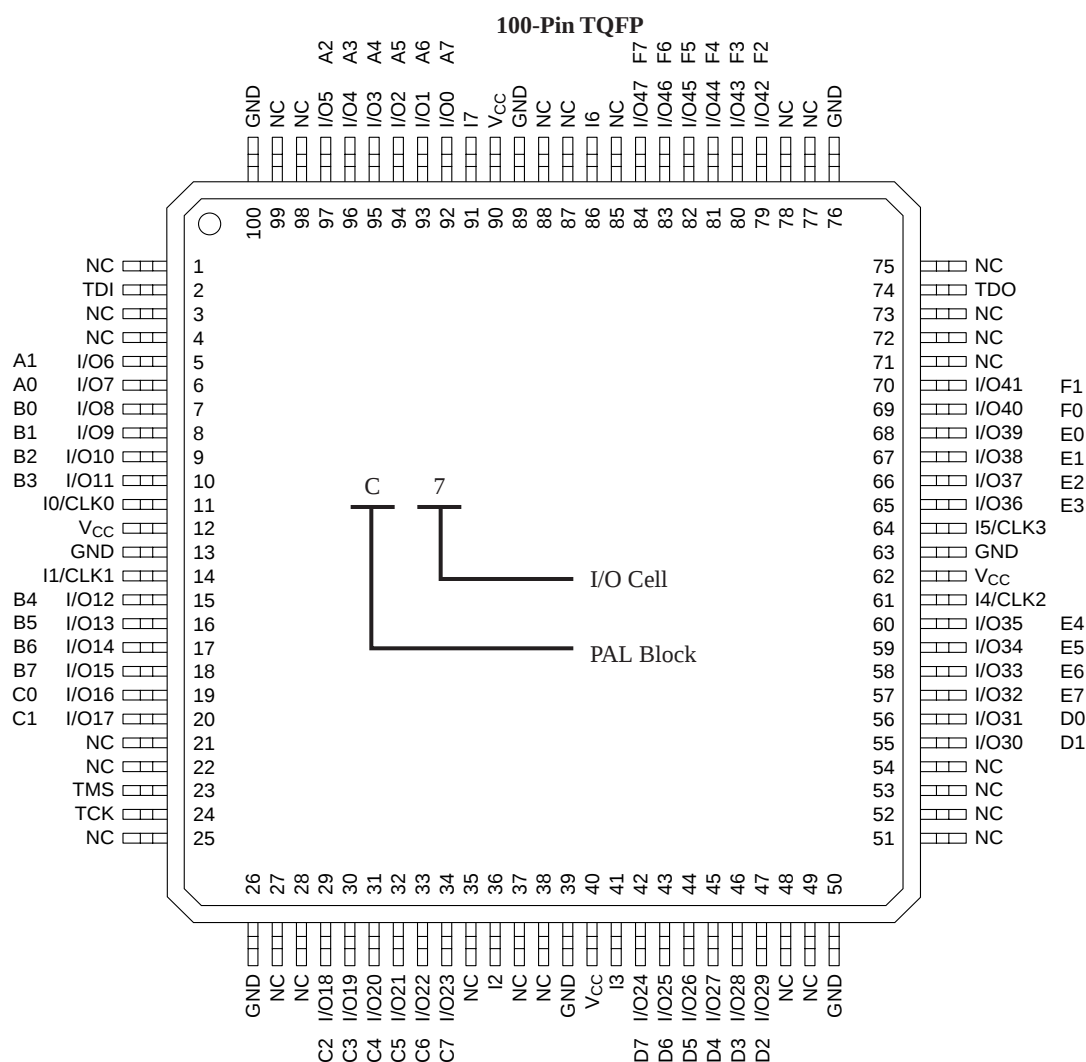
TCK = Test Clock

TMS = Test Mode Select

TDO = Test Data Out

## 100-PIN TQFP CONNECTION DIAGRAM (M4A(3,5)-96/48)

### Top View



17466G-029

## PIN DESIGNATIONS

CLK/I = Clock or Input

GND = Ground

I = Input

I/O = Input/Output

V<sub>CC</sub> = Supply Voltage

NC = No Connect

TDI = Test Data In

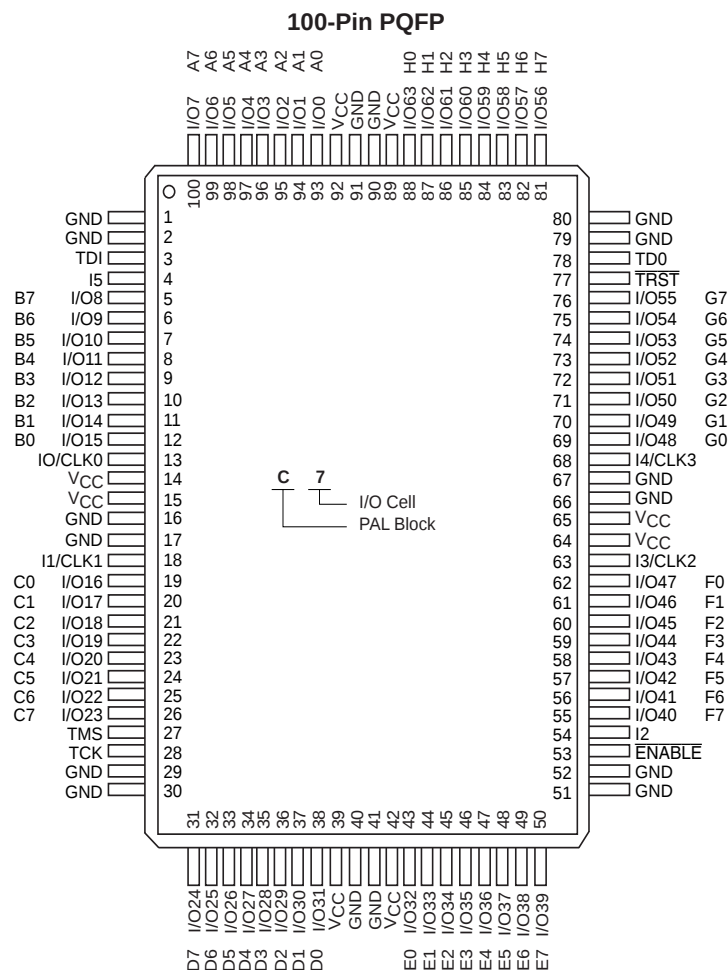
TCK = Test Clock

TMS = Test Mode Select

TDO = Test Data Out

## 100-PIN PQFP CONNECTION DIAGRAM (M4A(3,5)-128/64)

### Top View



17466G-031

## PIN DESIGNATIONS

I/CLK = Input or Clock

GND = Ground

I = Input

I/O = Input/Output

V<sub>CC</sub> = Supply Voltage

TDI = Test Data In

TCK = Test Clock

TMS = Test Mode Select

TDO = Test Data Out

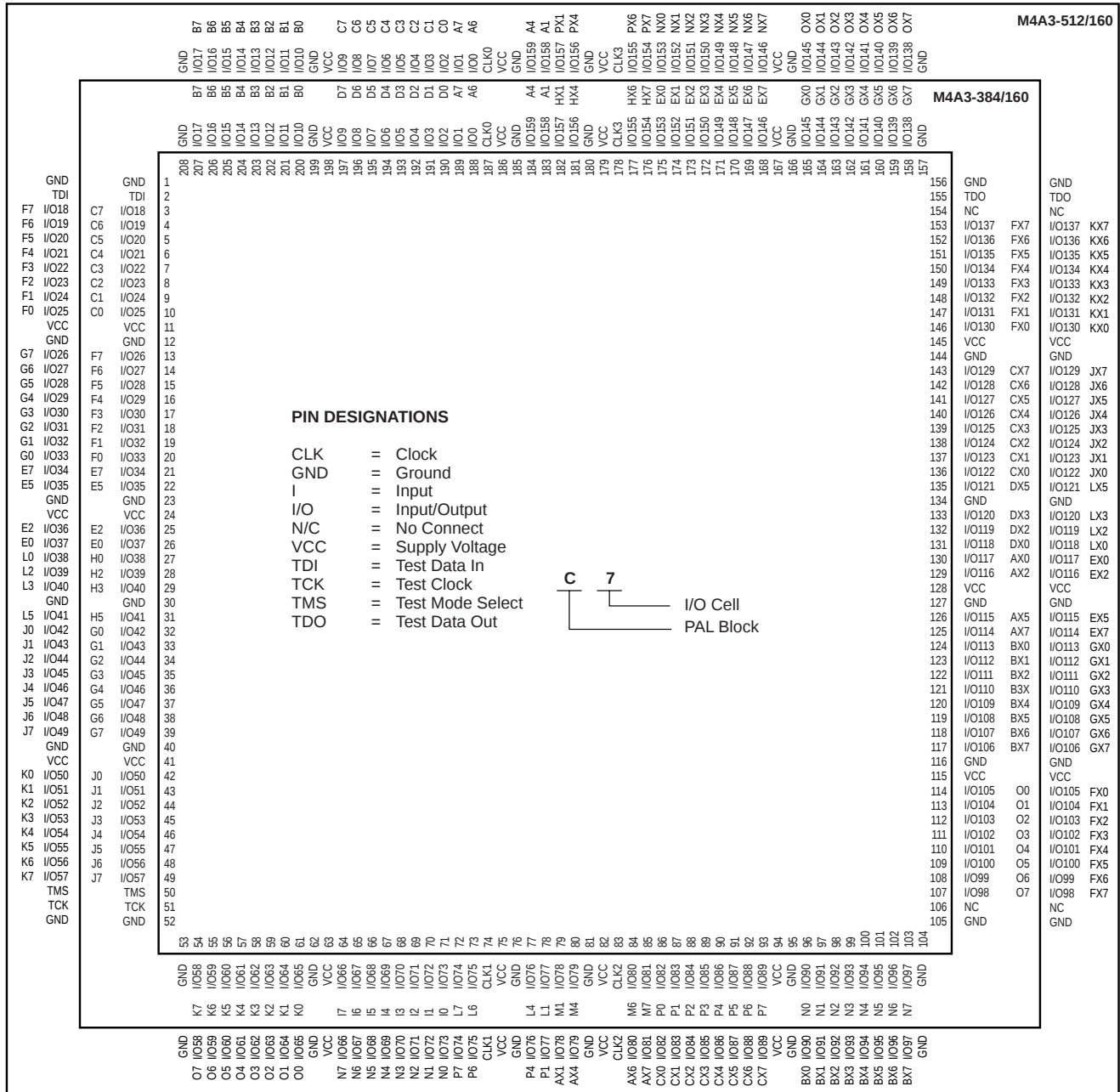
TRST = Test Reset

ENABLE = Program

## 208-PIN PQFP CONNECTION DIAGRAM (M4A3-384/160 AND M4A3-512/160)

### Top View

#### 208-Pin PQFP



17466Ga-044

## 256-BALL fpBGA CONNECTION DIAGRAM (M4A3-256/128)

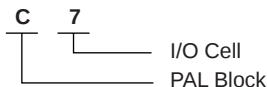
### Bottom View

#### 256-Ball fpBGA

|   | 16           | 15           | 14           | 13           | 12           | 11           | 10           | 9            | 8           | 7           | 6           | 5           | 4           | 3           | 2           | 1           |   |
|---|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|---|
| A | TRST         | I/O117<br>O5 | I/O116<br>O4 | I/O113<br>O1 | I/O126<br>P6 | I/O124<br>P4 | I12          | NC           | NC          | NC          | CLK0        | I/O1<br>A1  | I/O5<br>A5  | I/O7<br>A7  | I/O10<br>B2 | I/O12<br>B4 | A |
| B | I/O110<br>N6 | I/O111<br>N7 | I/O118<br>O6 | I/O115<br>O3 | I/O127<br>P7 | I/O125<br>P5 | I/O120<br>P0 | NC           | NC          | NC          | I1          | I/O2<br>A2  | I/O8<br>B0  | I/O11<br>B3 | I/O13<br>B5 | NC          | B |
| C | I/O108<br>N4 | I/O109<br>N5 | NC           | I/O119<br>O7 | I/O114<br>O2 | I/O122<br>P2 | I/O123<br>P3 | NC           | NC          | I0          | I/O4<br>A4  | I/O6<br>A6  | I/O15<br>B7 | I/O14<br>B6 | TDI         | I/O23<br>C7 | C |
| D | NC           | I/O104<br>N0 | TDO          | GND          | GND          | VCC          | GND          | VCC          | GND         | GND         | VCC         | GND         | VCC         | I/O9<br>B1  | I/O22<br>C6 | I/O21<br>C5 | D |
| E | I/O102<br>M6 | NC           | I/O107<br>N3 | VCC          | I/O105<br>N1 | I/O106<br>N2 | I13          | CLK3         | NC          | NC          | I/O0<br>A0  | NC          | GND         | I/O20<br>C4 | I/O19<br>C3 | I/O31<br>D7 | E |
| F | I/O98<br>M2  | I/O103<br>M7 | I/O101<br>M5 | GND          | I/O100<br>M4 | I/O99<br>M3  | I/O112<br>O0 | I/O121<br>P1 | NC          | NC          | I/O3<br>A3  | I/O18<br>C2 | VCC         | I/O16<br>C0 | I/O30<br>D6 | I/O29<br>D5 | F |
| G | NC           | I/O96<br>M0  | I11          | VCC          | NC           | I/O97<br>M1  | VCC          | GND          | GND         | VCC         | I/O17<br>C1 | I/O28<br>D4 | GND         | I/O26<br>D2 | I/O25<br>D1 | I2          | G |
| H | I/O88<br>L0  | I10          | I9           | GND          | I/O89<br>L1  | I/O90<br>L2  | GND          | VCC          | VCC         | GND         | I/O27<br>D3 | I/O24<br>D0 | VCC         | NC          | NC          | NC          | H |
| J | I/O91<br>L3  | I/O92<br>L4  | I/O93<br>L5  | GND          | I/O95<br>L7  | I/O94<br>L6  | GND          | VCC          | VCC         | GND         | I3          | NC          | GND         | NC          | NC          | NC          | J |
| K | NC           | NC           | NC           | VCC          | NC           | NC           | VCC          | GND          | GND         | VCC         | NC          | NC          | VCC         | I4          | NC          | I/O32<br>E0 | K |
| L | NC           | NC           | I/O80<br>K0  | GND          | I/O83<br>K3  | NC           | NC           | NC           | I/O59<br>H3 | I/O61<br>H5 | NC          | NC          | GND         | I/O35<br>E3 | I/O36<br>E4 | I/O33<br>E1 | L |
| M | I/O81<br>K1  | I/O82<br>K2  | I/O84<br>K4  | GND          | I/O67<br>I3  | I/O65<br>I1  | NC           | NC           | I/O58<br>H2 | I/O48<br>G0 | I/O51<br>G3 | NC          | VCC         | I/O44<br>F4 | I/O39<br>E7 | I/O34<br>E2 | M |
| N | I/O85<br>K5  | I/O86<br>K6  | ENABLE       | VCC          | GND          | VCC          | GND          | VCC          | GND         | GND         | VCC         | GND         | GND         | TCK         | I/O40<br>F0 | I/O37<br>E5 | N |
| P | I/O87<br>K7  | I/O77<br>J5  | I/O78<br>J6  | I/O79<br>J7  | I/O68<br>I4  | I/O66<br>I2  | NC           | NC           | NC          | I6          | I/O63<br>H7 | I/O52<br>G4 | I/O55<br>G7 | TMS         | I/O41<br>F1 | I/O38<br>E6 | P |
| R | I/O76<br>J4  | I/O75<br>J3  | I/O72<br>J0  | I/O71<br>I7  | I/O64<br>I0  | I7           | NC           | NC           | NC          | I/O56<br>H0 | I/O60<br>H4 | I/O49<br>G1 | I/O53<br>G5 | I/O47<br>F7 | I/O43<br>F3 | I/O42<br>F2 | R |
| T | I/O74<br>J2  | I/O73<br>J1  | I/O70<br>I6  | I/O69<br>I5  | I8           | CLK2         | NC           | NC           | CLK1        | I5          | I/O57<br>H1 | I/O62<br>H6 | I/O50<br>G2 | I/O54<br>G6 | I/O46<br>F6 | I/O45<br>F5 | T |
|   | 16           | 15           | 14           | 13           | 12           | 11           | 10           | 9            | 8           | 7           | 6           | 5           | 4           | 3           | 2           | 1           |   |

#### PIN DESIGNATIONS

CLK = Clock  
 GND = Ground  
 I = Input  
 I/O = Input/Output  
 N/C = No Connect  
 VCC = Supply Voltage  
 TDI = Test Data In  
 TCK = Test Clock  
 TMS = Test Mode Select  
 TDO = Test Data Out  
 TRST = Test Reset  
 ENABLE = Program



m4a3.256.128\_256bga

# 388-BALL fpBGA CONNECTION DIAGRAM (M4A3-512/256)

## Bottom View

### 388-Ball fpBGA

|    | 22         | 21         | 20         | 19         | 18         | 17         | 16         | 15         | 14         | 13         | 12         | 11         | 10        | 9         | 8         | 7         | 6         | 5         | 4         | 3         | 2         | 1        |    |
|----|------------|------------|------------|------------|------------|------------|------------|------------|------------|------------|------------|------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|----------|----|
| A  | GND        | I/O243 OX3 | I/O240 OX0 | I/O241 OX1 | I/O236 NX4 | I/O231 MX7 | I/O228 MX4 | I/O226 MX2 | I/O255 PX7 | I/O251 PX3 | I/O248 PX0 | I/O0 A0    | I/O5 A5   | I/O6 A6   | I/O27 D3  | I/O30 D6  | I/O17 C1  | I/O22 C6  | I/O8 B0   | I/O10 B2  | N/C       | GND      | A  |
| B  | N/C        | GND        | I/O245 OX5 | I/O242 OX2 | I/O238 NX6 | I/O234 NX2 | I/O232 NX0 | I/O229 MX5 | I/O224 MX0 | I/O253 PX5 | I/O249 PX1 | I/O2 A2    | CLK0      | I/O26 D2  | I/O29 D5  | I/O31 D7  | I/O20 C4  | I/O9 B1   | I/O12 B4  | I/O13 B5  | GND       | TDI      | B  |
| C  | I/O213 KX5 | TDO        | GND        | I/O247 OX7 | I/O244 OX4 | I/O239 NX7 | I/O235 NX3 | I/O230 MX6 | I/O227 MX3 | CLK3       | I/O250 PX2 | I/O1 A1    | I/O7 A7   | I/O25 D1  | I/O16 C0  | I/O18 C2  | I/O23 C7  | I/O11 B3  | I/O15 B7  | GND       | I/O47 F7  | I/O44 F4 | C  |
| D  | I/O210 KX2 | I/O212 KX4 | I/O215 KX7 | GND        | I/O246 OX6 | VCC        | I/O237 NX5 | I/O233 NX1 | VCC        | I/O254 PX6 | VCC        | I/O3 A3    | I/O24 D0  | VCC       | I/O19 C3  | I/O21 C5  | VCC       | I/O14 B6  | GND       | I/O46 F6  | I/O43 F3  | I/O41 F1 | D  |
| E  | I/O207 JX7 | I/O209 KX1 | I/O211 KX3 | I/O214 KX6 |            |            |            |            |            |            |            |            |           |           |           |           |           |           | I/O45 F5  | I/O42 F2  | I/O40 F0  | I/O54 G6 | E  |
| F  | I/O203 JX3 | I/O205 JX5 | I/O208 KX0 | VCC        |            |            |            |            |            |            |            |            |           |           |           |           |           |           | VCC       | I/O55 G7  | I/O52 G4  | I/O50 G2 | F  |
| G  | I/O200 JX0 | I/O202 JX2 | I/O204 JX4 | I/O206 JX6 |            |            | VCC        | VCC        | N/C        | I/O225 MX1 | I/O252 PX4 | I/O4 A4    | I/O28 D4  | N/C       | VCC       | VCC       |           |           | I/O53 G5  | I/O51 G3  | I/O49 G1  | I/O39 E7 | G  |
| H  | I/O221 LX5 | I/O222 LX6 | I/O223 LX7 | I/O201 JX1 |            |            | VCC        | N/C        | GND        | GND        | GND        | GND        | GND       | GND       | N/C       | VCC       |           |           | I/O48 G0  | I/O38 E6  | I/O37 E5  | I/O36 E4 | H  |
| J  | I/O218 LX2 | I/O219 LX3 | I/O220 LX4 | VCC        |            |            | N/C        | GND        | GND        | GND        | GND        | GND        | GND       | GND       | GND       | N/C       |           |           | VCC       | I/O35 E3  | I/O34 E2  | I/O32 E0 | J  |
| K  | I/O197 IX5 | I/O198 IX6 | I/O199 IX7 | I/O216 LX0 |            |            | I/O217 LX1 | GND        | GND        | GND        | GND        | GND        | GND       | GND       | GND       | I/O33 E1  |           |           | I/O63 H7  | I/O62 H6  | I/O61 H5  | I/O60 H4 | K  |
| L  | I/O192 IX0 | I/O194 IX2 | I/O195 IX3 | I/O196 IX4 |            |            | I/O193 IX1 | GND        | GND        | GND        | GND        | GND        | GND       | GND       | GND       | I/O58 H2  |           |           | VCC       | I/O59 H3  | I/O57 H1  | I/O56 H0 | L  |
| M  | I/O184 HX0 | I/O185 HX1 | I/O187 HX3 | VCC        |            |            | I/O186 HX2 | GND        | GND        | GND        | GND        | GND        | GND       | GND       | GND       | I/O69 I5  |           |           | I/O67 I3  | I/O65 I1  | I/O66 I2  | I/O64 I0 | M  |
| N  | I/O188 HX4 | I/O189 HX5 | I/O191 HX7 | I/O190 HX6 |            |            | I/O162 EX2 | GND        | GND        | GND        | GND        | GND        | GND       | GND       | GND       | I/O89 L1  |           |           | I/O88 L0  | I/O71 I7  | I/O70 I6  | I/O68 I4 | N  |
| P  | I/O160 EX0 | I/O161 EX1 | I/O163 EX3 | VCC        |            |            | N/C        | GND        | GND        | GND        | GND        | GND        | GND       | GND       | GND       | N/C       |           |           | VCC       | I/O92 L4  | I/O91 L3  | I/O90 L2 | P  |
| R  | I/O164 EX4 | I/O165 EX5 | I/O166 EX6 | I/O177 GX1 |            |            | VCC        | N/C        | GND        | GND        | GND        | GND        | GND       | GND       | N/C       | VCC       |           |           | I/O74 J2  | I/O95 L7  | I/O94 L6  | I/O93 L5 | R  |
| T  | I/O167 EX7 | I/O176 GX0 | I/O179 GX3 | I/O181 GX5 |            |            | VCC        | VCC        | N/C        | I/O152 DX0 | I/O131 AX3 | I/O122 P2  | I/O98 M2  | N/C       | VCC       | VCC       |           |           | I/O78 J6  | I/O76 J4  | I/O73 J1  | I/O72 J0 | T  |
| U  | I/O178 GX2 | I/O180 GX4 | I/O183 GX7 | VCC        |            |            |            |            |            |            |            |            |           |           |           |           |           |           | VCC       | I/O80 K0  | I/O77 J5  | I/O75 J3 | U  |
| V  | I/O182 GX6 | N/C        | I/O169 FX1 | I/O172 FX4 |            |            |            |            |            |            |            |            |           |           |           |           |           |           | I/O86 K6  | I/O83 K3  | I/O81 K1  | I/O79 J7 | V  |
| W  | I/O168 FX0 | I/O170 FX2 | I/O173 FX5 | GND        | I/O143 BX7 | VCC        | I/O150 CX6 | I/O145 CX1 | VCC        | I/O153 DX1 | I/O123 P3  | VCC        | I/O96 M0  | VCC       | I/O104 N0 | I/O111 N7 | VCC       | I/O119 O7 | GND       | I/O87 K7  | I/O84 K4  | I/O82 K2 | W  |
| Y  | I/O171 FX3 | I/O174 FX6 | GND        | I/O141 BX5 | I/O138 BX2 | I/O136 BX0 | I/O147 CX3 | I/O158 DX6 | I/O156 DX4 | CLK2       | I/O132 AX4 | I/O121 P1  | I/O125 P5 | I/O99 M3  | I/O101 M5 | I/O106 N2 | I/O110 N6 | I/O115 O3 | I/O118 O6 | GND       | TMS       | I/O85 K5 | Y  |
| AA | I/O175 FX7 | GND        | I/O142 BX6 | I/O140 BX4 | I/O151 CX7 | I/O149 CX5 | I/O144 CX0 | I/O157 DX5 | I/O154 DX2 | I/O134 AX6 | I/O130 AX2 | I/O128 AX0 | CLK1      | I/O127 P7 | I/O100 M4 | I/O103 M7 | I/O108 N4 | I/O109 N5 | I/O113 O1 | I/O116 O4 | GND       | TCK      | AA |
| AB | GND        | N/C        | I/O139 BX3 | I/O137 BX1 | I/O148 CX4 | I/O146 CX2 | I/O159 DX7 | I/O155 DX3 | I/O135 AX7 | I/O133 AX5 | I/O129 AX1 | I/O120 P0  | I/O124 P4 | I/O126 P6 | I/O97 M1  | I/O102 M6 | I/O105 N1 | I/O107 N3 | I/O112 O0 | I/O114 O2 | I/O117 O5 | GND      | AB |

### PIN DESIGNATIONS

CLK = Clock  
 GND = Ground  
 I = Input  
 I/O = Input/Output  
 N/C = No Connect  
 VCC = Supply Voltage  
 TDI = Test Data In  
 TCK = Test Clock  
 TMS = Test Mode Select  
 TDO = Test Data Out



m4a3.512.256\_388bga

## ispMACH 4A PRODUCT ORDERING INFORMATION

### ispMACH 4A Devices Commercial and Industrial - 3.3V and 5V

Lattice programmable logic products are available with several ordering options. The order number (Valid Combination) is formed by a combination of:

| M4A3- 256 / 128 -7 Y C                                                   |  | L48                                                                       |  |
|--------------------------------------------------------------------------|--|---------------------------------------------------------------------------|--|
| <b>FAMILY TYPE</b>                                                       |  | = 48-pin TQFP for<br>M4A3-32/32 or M4A3-64/32<br>M4A5-32/32 or M4A5-64/32 |  |
| M4A3- = ispMACH 4A Family Low Voltage Advanced Feature (3.3-V $V_{CC}$ ) |  | <b>OPERATING CONDITIONS</b>                                               |  |
| M4A5- = ispMACH 4A Family Advanced Feature (5-V $V_{CC}$ )               |  | C = Commercial (0°C to +70°C)                                             |  |
| <b>MACROCELL DENSITY</b>                                                 |  | I = Industrial (-40°C to +85°C)                                           |  |
| 32 = 32 Macrocells      192 = 192 Macrocells                             |  | <b>PACKAGE TYPE</b>                                                       |  |
| 64 = 64 Macrocells      256 = 256 Macrocells                             |  | SA = Ball Grid Array (BGA)                                                |  |
| 96 = 96 Macrocells      384 = 384 Macrocells                             |  | J = Plastic Leaded Chip Carrier (PLCC)                                    |  |
| 128 = 128 Macrocells      512 = 512 Macrocells                           |  | JN = Lead-free Plastic Leaded Chip Carrier (PLCC)                         |  |
| <b>I/Os</b>                                                              |  | V = Thin Quad Flat Pack (TQFP)                                            |  |
| /32 = 32 I/Os in 44-pin PLCC, 44-pin TQFP or 48-pin TQFP                 |  | VN = Lead-free Thin Quad Flat Pack (TQFP)                                 |  |
| /48 = 48 I/Os in 100-pin TQFP                                            |  | Y = Plastic Quad Flat Pack (PQFP)                                         |  |
| /64 = 64 I/Os in 100-pin TQFP, 100-pin PQFP, or 100-ball caBGA           |  | YN = Lead-free Plastic Quad Flat Pack (PQFP)                              |  |
| /96 = 96 I/Os in 144-pin TQFP or 144-ball fpBGA                          |  | FA = Fine-pitch Ball Grid Array (fpBGA)                                   |  |
| /128 = 128 I/Os in 208-pin PQFP, 256-ball BGA or 256-ball fpBGA          |  | FAN = Lead-free Fine-pitch Ball Grid Array (fpBGA)                        |  |
| /160 = 160 I/Os in 208-pin PQFP                                          |  | CA = Chip-array Ball Grid Array (caBGA)                                   |  |
| /192 = 192 I/Os in 256-ball BGA or 256-ball fpBGA                        |  | <b>SPEED</b>                                                              |  |
| /256 = 256 I/Os in 388-ball fpBGA                                        |  | -5 = 5.0 ns $t_{PD}$                                                      |  |
|                                                                          |  | -55 = 5.5 ns $t_{PD}$                                                     |  |
|                                                                          |  | -6 = 6.0 ns $t_{PD}$                                                      |  |
|                                                                          |  | -65 = 6.5 ns $t_{PD}$                                                     |  |
|                                                                          |  | -7 = 7.5 ns $t_{PD}$                                                      |  |
|                                                                          |  | -10 = 10 ns $t_{PD}$                                                      |  |
|                                                                          |  | -12 = 12 ns $t_{PD}$                                                      |  |
|                                                                          |  | -14 = 14 ns $t_{PD}$                                                      |  |

\*Package obsolete, contact factory.

### Conventional Packaging

| 3.3V Commercial Combinations |                                 |              | 3.3V Industrial Combinations |               |              |
|------------------------------|---------------------------------|--------------|------------------------------|---------------|--------------|
| M4A3-32/32                   | -5, -7, -10                     | JC, VC, VC48 | M4A3-32/32                   | -7, -10, -12  | JI, VI, VI48 |
| M4A3-64/32                   | -55, -7, -10                    | JC, VC, VC48 | M4A3-64/32                   |               | JI, VI, VI48 |
| M4A3-64/64                   |                                 | VC           | M4A3-64/64                   |               | VI           |
| M4A3-96/48                   |                                 | VC           | M4A3-96/48                   |               | VI           |
| M4A3-128/64                  |                                 | YC, VC, CAC  | M4A3-128/64                  |               | YI, VI, CAI  |
| M4A3-192/96                  | -6, -7, -10                     | VC, FAC      | M4A3-192/96                  |               | VI, FAI      |
| M4A3-256/128                 | -55, -65 <sup>1</sup> , -7, -10 | YC, FAC, SAC | M4A3-256/128                 | -10, -12      | YI, FAI, SAI |
| M4A3-256/160                 | -7, -10                         | YC           | M4A3-256/160                 |               | YI           |
| M4A3-256/192                 |                                 | FAC          | M4A3-256/192                 | -10, -12, -14 | FAI          |
| M4A3-384/160                 | -65, -10, -12                   | YC           | M4A3-384/160                 |               | YI           |
| M4A3-384/192                 |                                 | SAC, FAC     | M4A3-384/192                 |               | FAI          |
| M4A3-512/160                 | -7, -10, -12                    | YC           | M4A3-512/160                 |               | YI           |
| M4A3-512/192                 |                                 | FAC          | M4A3-512/192                 |               | FAI          |
| M4A3-512/256                 |                                 | FAC          | M4A3-512/256                 |               | FAI          |

1. Use 5.5ns for new designs.