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#### Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

#### Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

#### Details

Product Status	Obsolete
Core Processor	PowerPC e300
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	266MHz
Co-Processors/DSP	-
RAM Controllers	DDR
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	620-BBGA Exposed Pad
Supplier Device Package	620-HBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8347zqagdb

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Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

- Enhanced host controller interface (EHCI) compatible
- Complies with USB Specification Rev. 2.0
- High-speed (480 Mbps), full-speed (12 Mbps), and low-speed (1.5 Mbps) operations
- Direct connection to a high-speed device without an external hub
- External PHY with serial and low-pin count (ULPI) interfaces
- Local bus controller (LBC)
  - Multiplexed 32-bit address and data operating at up to 133 MHz
  - Four chip selects support four external slaves
  - Up to eight-beat burst transfers
  - 32-, 16-, and 8-bit port sizes controlled by an on-chip memory controller
  - Three protocol engines on a per chip select basis:
    - General-purpose chip select machine (GPCM)
    - Three user-programmable machines (UPMs)
    - Dedicated single data rate SDRAM controller
  - Parity support
  - Default boot ROM chip select with configurable bus width (8-, 16-, or 32-bit)
- Programmable interrupt controller (PIC)
  - Functional and programming compatibility with the MPC8260 interrupt controller
  - Support for 8 external and 35 internal discrete interrupt sources
  - Support for 1 external (optional) and 7 internal machine checkstop interrupt sources
  - Programmable highest priority request
  - Four groups of interrupts with programmable priority
  - External and internal interrupts directed to host processor
  - Redirects interrupts to external INTA pin in core disable mode.
  - Unique vector number for each interrupt source
- Dual industry-standard I<sup>2</sup>C interfaces
  - Two-wire interface
  - Multiple master support
  - Master or slave  $I^2C$  mode support
  - On-chip digital filtering rejects spikes on the bus
  - System initialization data optionally loaded from I<sup>2</sup>C-1 EPROM by boot sequencer embedded hardware
- DMA controller
  - Four independent virtual channels
  - Concurrent execution across multiple channels with programmable bandwidth control
  - All channels accessible to local core and remote PCI masters
  - Misaligned transfer capability

Parameter/Condition	Min	Мах	Unit	Notes
Input hold time for POR configuration signals with respect to negation of HRESET	0	_	ns	
Time for the MPC8347E to turn off POR configuration signals with respect to the assertion of $\overline{\text{HRESET}}$	—	4	ns	3
Time for the MPC8347E to turn on POR configuration signals with respect to the negation of HRESET	1	_	<sup>t</sup> PCI_SYNC_IN	1, 3

#### Table 9. RESET Initialization Timing Specifications (continued)

#### Notes:

1. t<sub>PCI\_SYNC\_IN</sub> is the clock period of the input clock applied to PCI\_SYNC\_IN. In PCI host mode, the primary clock is applied to the CLKIN input, and PCI\_SYNC\_IN period depends on the value of CFG\_CLKIN\_DIV. See the *MPC8349E PowerQUICC™ II Pro Integrated Host Processor Family Reference Manual*.

- 2. t<sub>CLKIN</sub> is the clock period of the input clock applied to CLKIN. It is valid only in PCI host mode. See the MPC8349E PowerQUICC™ II Pro Integrated Host Processor Family Reference Manual.
- 3. POR configuration signals consist of CFG\_RESET\_SOURCE[0:2] and CFG\_CLKIN\_DIV.

#### Table 10 lists the PLL and DLL lock times.

#### Table 10. PLL and DLL Lock Times

Parameter/Condition	Min	Мах	Unit	Notes
PLL lock times	—	100	μs	
DLL lock times	7680	122,880	csb_clk cycles	1, 2

#### Notes:

1. DLL lock times are a function of the ratio between the output clock and the coherency system bus clock (csb\_clk). A 2:1 ratio results in the minimum and an 8:1 ratio results in the maximum.

2. The csb\_clk is determined by the CLKIN and system PLL ratio. See Section 19, "Clocking."

## 6.2 DDR SDRAM AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR SDRAM interface.

## 6.2.1 DDR SDRAM Input AC Timing Specifications

Table 13 provides the input AC timing specifications for the DDR SDRAM interface.

#### Table 13. DDR SDRAM Input AC Timing Specifications

At recommended operating conditions with GV\_{DD} of 2.5 V  $\pm$  5%.

Parameter	Symbol	Min	Max	Unit	Notes
AC input low voltage	V <sub>IL</sub>	—	MV <sub>REF</sub> – 0.31	V	
AC input high voltage	V <sub>IH</sub>	MV <sub>REF</sub> + 0.31	GV <sub>DD</sub> + 0.3	V	
MDQS—MDQ/MECC input skew per byte 333 MHz 266 MHz	t <sub>DISKEW</sub>	_	750 1125	ps	1

Note:

1. Maximum possible skew between a data strobe (MDQS[n]) and any corresponding bit of data (MDQ[8n + {0...7}] if 0 <= n <= 7) or ECC (MECC[{0...7}] if n = 8).

Figure 4 illustrates the DDR input timing diagram showing the t<sub>DISKEW</sub> timing parameter.



Figure 4. DDR Input Timing Diagram

### 6.2.2 DDR SDRAM Output AC Timing Specifications

Table 14 and Table 15 provide the output AC timing specifications and measurement conditions for the DDR SDRAM interface.

#### Table 14. DDR SDRAM Output AC Timing Specifications for Source Synchronous Mode

At recommended operating conditions with  $GV_{DD}$  of 2.5 V ± 5%.

Parameter	Symbol <sup>1</sup>	Min	Мах	Unit	Notes
MCK[n] cycle time, (MCK[n]/MCK[n] crossing)	t <sub>MCK</sub>	6	10	ns	2
Skew between any MCK to ADDR/CMD 333 MHz 266 MHz 200 MHz	t <sub>AOSKEW</sub>	1000 1100 1200	200 300 400	ps	3
ADDR/CMD output setup with respect to MCK 333 MHz 266 MHz 200 MHz	t <sub>DDKHAS</sub>	2.8 3.45 4.6	_	ns	4
ADDR/CMD output hold with respect to MCK 333 MHz 266 MHz 200 MHz	<sup>t</sup> DDKHAX	2.0 2.65 3.8	_	ns	4
MCS(n) output setup with respect to MCK 333 MHz 266 MHz 200 MHz	<sup>t</sup> DDKHCS	2.8 3.45 4.6	_	ns	4
MCS(n) output hold with respect to MCK 333 MHz 266 MHz 200 MHz	<sup>t</sup> DDKHCX	2.0 2.65 3.8	_	ns	4
MCK to MDQS 333 MHz 266 MHz 200 MHz	<sup>t</sup> DDKHMH	-0.9 -1.1 -1.2	0.3 0.5 0.6	ns	5
MDQ/MECC/MDM output setup with respect to MDQS 333 MHz 266 MHz 200 MHz	<sup>t</sup> DDKHDS, <sup>t</sup> DDKLDS	900 900 1200	_	ps	6
MDQ/MECC/MDM output hold with respect to MDQS 333 MHz 266 MHz 200 MHz	<sup>t</sup> ddkhdx, <sup>t</sup> ddkldx	900 900 1200	_	ps	6
MDQS preamble start	t <sub>DDKHMP</sub>	$-0.25\times t_{MCK}-0.9$	$-0.25 \times t_{\text{MCK}} + 0.3$	ns	7

## 8 Ethernet: Three-Speed Ethernet, MII Management

This section provides the AC and DC electrical characteristics for three-speeds (10/100/1000 Mbps) and MII management.

## 8.1 Three-Speed Ethernet Controller (TSEC)— GMII/MII/TBI/RGMII/RTBI Electrical Characteristics

The electrical characteristics specified here apply to the gigabit media independent interface (GMII), the media independent interface (MII), ten-bit interface (TBI), reduced gigabit media independent interface (RGMII), and reduced ten-bit interface (RTBI) signals except management data input/output (MDIO) and management data clock (MDC). The MII, GMII, and TBI interfaces are defined for 3.3 V, and the RGMII and RTBI interfaces are defined for 2.5 V. The RGMII and RTBI interfaces follow the Hewlett-Packard *Reduced Pin-Count Interface for Gigabit Ethernet Physical Layer Device Specification*, Version 1.2a (9/22/2000). The electrical characteristics for MDIO and MDC are specified in Section 8.3, "Ethernet Management Interface Electrical Characteristics."

## 8.1.1 **TSEC DC Electrical Characteristics**

GMII, MII, TBI, RGMII, and RTBI drivers and receivers comply with the DC parametric attributes specified in Table 19 and Table 20. The RGMII and RTBI signals in Table 20 are based on a 2.5-V CMOS interface voltage as defined by JEDEC EIA/JESD8-5.

Parameter	Symbol	Conditions		Min	Мах	Unit
Supply voltage 3.3 V	$LV_{DD}^2$	—		2.97	3.63	V
Output high voltage	V <sub>OH</sub>	I <sub>OH</sub> = -4.0 mA	$LV_{DD} = Min$	2.40	LV <sub>DD</sub> + 0.3	V
Output low voltage	V <sub>OL</sub>	$I_{OL} = 4.0 \text{ mA}$ $LV_{DD} = Min$		GND	0.50	V
Input high voltage	V <sub>IH</sub>	—			LV <sub>DD</sub> + 0.3	V
Input low voltage	V <sub>IL</sub>	—	—	-0.3	0.90	V
Input high current	IIH	$V_{IN}^{1} = LV_{DD}$		-	40	μA
Input low current	IIL	V <sub>IN</sub> <sup>1</sup> =	GND	-600	—	μA

Table 19. GMII/TBI and MII DC Electrical Characteristics

#### Notes:

1. The symbol V<sub>IN</sub>, in this case, represents the LV<sub>IN</sub> symbol referenced in Table 1 and Table 2.

2. GMII/MII pins not needed for RGMII or RTBI operation are powered by the  $\ensuremath{\mathsf{OV}_{\mathsf{DD}}}$  supply.

#### Ethernet: Three-Speed Ethernet, MII Management

Figure 8 shows the GMII transmit AC timing diagram.



Figure 8. GMII Transmit AC Timing Diagram

### 8.2.1.2 GMII Receive AC Timing Specifications

Table 22 provides the GMII receive AC timing specifications.

#### Table 22. GMII Receive AC Timing Specifications

At recommended operating conditions with  $LV_{DD}/OV_{DD}$  of 3.3 V ± 10%.

Parameter/Condition	Symbol <sup>1</sup>	Min	Тур	Мах	Unit
RX_CLK clock period	t <sub>GRX</sub>	_	8.0	—	ns
RX_CLK duty cycle	t <sub>GRXH</sub> /t <sub>GRX</sub>	40	—	60	%
RXD[7:0], RX_DV, RX_ER setup time to RX_CLK	t <sub>GRDVKH</sub>	2.0	—	—	ns
RXD[7:0], RX_DV, RX_ER hold time to RX_CLK	t <sub>GRDXKH</sub>	0.5	—	—	ns
RX_CLK clock rise, V <sub>IL</sub> (min) to V <sub>IH</sub> (max)	t <sub>GRXR</sub>		—	1.0	ns
RX_CLK clock fall time, $V_{IH}(max)$ to $V_{IL}(min)$	t <sub>GRXF</sub>			1.0	ns

#### Note:

1. The symbols for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t<sub>(first two letters of functional block)</sub>(reference)(state)(signal)(state) for outputs. For example, t<sub>GRDVKH</sub> symbolizes GMII receive timing (GR) with respect to the time data input signals (D) reaching the valid state (V) relative to the t<sub>RX</sub> clock reference (K) going to the high state (H) or setup time. Also, t<sub>GRDXKL</sub> symbolizes GMII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t<sub>GRX</sub> clock reference (K) going to the low (L) state or hold time. In general, the clock reference symbol is based on three letters representing the clock of a particular function. For example, the subscript of t<sub>GRX</sub> represents the GMII (G) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).</sub>

Figure 9 shows the GMII receive AC timing diagram.



Figure 9. GMII Receive AC Timing Diagram

### 8.2.2 MII AC Timing Specifications

This section describes the MII transmit and receive AC timing specifications.

### 8.2.2.1 MII Transmit AC Timing Specifications

Table 23 provides the MII transmit AC timing specifications.

#### Table 23. MII Transmit AC Timing Specifications

At recommended operating conditions with  $LV_{DD}/OV_{DD}$  of 3.3 V ± 10%.

Parameter/Condition	Symbol <sup>1</sup>	Min	Тур	Max	Unit
TX_CLK clock period 10 Mbps	t <sub>MTX</sub>	—	400	_	ns
TX_CLK clock period 100 Mbps	t <sub>MTX</sub>	_	40	_	ns
TX_CLK duty cycle	t <sub>MTXH</sub> /t <sub>MTX</sub>	35	—	65	%
TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay	t <sub>MTKHDX</sub>	1	5	15	ns
TX_CLK data clock rise V <sub>IL</sub> (min) to V <sub>IH</sub> (max)	t <sub>MTXR</sub>	1.0	—	4.0	ns
TX_CLK data clock fall $V_{IH}(max)$ to $V_{IL}(min)$	t <sub>MTXF</sub>	1.0	_	4.0	ns

Note:

The symbols for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t<sub>(first two letters of functional block)(reference)(state)(signal)(state)</sub> for outputs. For example, t<sub>MTKHDX</sub> symbolizes MII transmit timing (MT) for the time t<sub>MTX</sub> clock reference (K) going high (H) until data outputs (D) are invalid (X). In general, the clock reference symbol is based on two to three letters representing the clock of a particular function. For example, the subscript of t<sub>MTX</sub> represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
</sub>

Figure 12 shows the MII receive AC timing diagram.



Figure 12. MII Receive AC Timing Diagram

### 8.2.3 TBI AC Timing Specifications

This section describes the TBI transmit and receive AC timing specifications.

### 8.2.3.1 TBI Transmit AC Timing Specifications

Table 25 provides the TBI transmit AC timing specifications.

#### Table 25. TBI Transmit AC Timing Specifications

At recommended operating conditions with  $\text{LV}_{\text{DD}}/\text{OV}_{\text{DD}}$  of 3.3 V ± 10%.

Parameter/Condition	Symbol <sup>1</sup>	Min	Тур	Мах	Unit
GTX_CLK clock period	t <sub>TTX</sub>	_	8.0	—	ns
GTX_CLK duty cycle	t <sub>TTXH</sub> /t <sub>TTX</sub>	40	—	60	%
GTX_CLK to TBI data TXD[7:0], TX_ER, TX_EN delay	t <sub>TTKHDX</sub>	1.0	—	5.0	ns
GTX_CLK clock rise, V <sub>IL</sub> (min) to V <sub>IH</sub> (max)	t <sub>TTXR</sub>	_	—	1.0	ns
GTX_CLK clock fall time, V <sub>IH</sub> (max) to V <sub>IL</sub> (min)	t <sub>TTXF</sub>	_	—	1.0	ns
GTX_CLK125 reference clock period	t <sub>G125</sub> 2	_	8.0	—	ns
GTX_CLK125 reference clock duty cycle	t <sub>G125H</sub> /t <sub>G125</sub>	45	—	55	ns

Notes:

1. The symbols for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t<sub>(first two letters of functional block)(reference)(state)(signal)(state)</sub> for outputs. For example, t<sub>TTKHDV</sub> symbolizes the TBI transmit timing (TT) with respect to the time from t<sub>TTX</sub> (K) going high (H) until the referenced data signals (D) reach the valid state (V) or setup time. Also, t<sub>TTKHDX</sub> symbolizes the TBI transmit timing (TT) with respect to the time from t<sub>TTX</sub> (K) going high (H) until the referenced data signals (D) reach the valid state (V) or setup time. Also, t<sub>TTKHDX</sub> symbolizes the TBI transmit timing (TT) with respect to the time from t<sub>TTX</sub> (K) going high (H) until the referenced data signals (D) reach the invalid state (X) or hold time. In general, the clock reference symbol is based on three letters representing the clock of a particular function. For example, the subscript of t<sub>TTX</sub> represents the TBI (T) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).</sub>

2. This symbol represents the external GTX\_CLK125 and does not follow the original symbol naming convention

Figure 14 shows the TBI receive AC timing diagram.



Figure 14. TBI Receive AC Timing Diagram

## 8.2.4 RGMII and RTBI AC Timing Specifications

#### Table 27 presents the RGMII and RTBI AC timing specifications.

#### Table 27. RGMII and RTBI AC Timing Specifications

At recommended operating conditions with LV<sub>DD</sub> of 2.5 V  $\pm$  5%.

Parameter/Condition	Symbol <sup>1</sup>	Min	Тур	Мах	Unit
Data to clock output skew (at transmitter)	t <sub>SKRGT</sub>	-0.5	—	0.5	ns
Data to clock input skew (at receiver) <sup>2</sup>	t <sub>SKRGT</sub>	1.0	—	2.8	ns
Clock cycle duration <sup>3</sup>	t <sub>RGT</sub>	7.2	8.0	8.8	ns
Duty cycle for 1000Base-T <sup>4, 5</sup>	t <sub>RGTH</sub> /t <sub>RGT</sub>	45	50	55	%
Duty cycle for 10BASE-T and 100BASE-TX <sup>3, 5</sup>	t <sub>RGTH</sub> /t <sub>RGT</sub>	40	50	60	%
Rise time (20%–80%)	t <sub>RGTR</sub>	—	—	0.75	ns
Fall time (20%–80%)	t <sub>RGTF</sub>	—	—	0.75	ns
GTX_CLK125 reference clock period	t <sub>G12</sub> 6	—	8.0	—	ns
GTX_CLK125 reference clock duty cycle	t <sub>G125H</sub> /t <sub>G125</sub>	47	—	53	%

Notes:

 In general, the clock reference symbol for this section is based on the symbols RGT to represent RGMII and RTBI timing. For example, the subscript of t<sub>RGT</sub> represents the TBI (T) receive (RX) clock. Also, the notation for rise (R) and fall (F) times follows the clock symbol. For symbols representing skews, the subscript is SK followed by the clock being skewed (RGT).

2. This implies that PC board design requires clocks to be routed so that an additional trace delay of greater than 1.5 ns is added to the associated clock signal.

3. For 10 and 100 Mbps,  $t_{RGT}$  scales to 400 ns  $\pm$  40 ns and 40 ns  $\pm$  4 ns, respectively.

- 4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t<sub>RGT</sub> of the lowest speed transitioned.
- 5. Duty cycle reference is  $LV_{DD}/2$ .

6. This symbol represents the external GTX\_CLK125 and does not follow the original symbol naming convention.

9 USB

This section provides the AC and DC electrical specifications for the USB interface of the MPC8347E.

## 9.1 USB DC Electrical Characteristics

Table 31 provides the DC electrical characteristics for the USB interface.

Parameter	Symbol	Min	Мах	Unit
High-level input voltage	V <sub>IH</sub>	2	OV <sub>DD</sub> + 0.3	V
Low-level input voltage	V <sub>IL</sub>	-0.3	0.8	V
Input current	I <sub>IN</sub>	—	±5	μA
High-level output voltage, $I_{OH} = -100 \ \mu A$	V <sub>OH</sub>	OV <sub>DD</sub> – 0.2	-	V
Low-level output voltage, $I_{OL} = 100 \ \mu A$	V <sub>OL</sub>	—	0.2	V

#### Table 31. USB DC Electrical Characteristics

## 9.2 USB AC Electrical Specifications

Table 32 describes the general timing parameters of the USB interface of the MPC8347E.

Table 32.	USB C	General	Timing	Parameters	(ULPI	Mode	Only)
					<b>\-</b>		

Parameter	Symbol <sup>1</sup>	Min	Мах	Unit	Notes
USB clock cycle time	t <sub>USCK</sub>	15	-	ns	2–5
Input setup to USB clock—all inputs	t <sub>USIVKH</sub>	4	-	ns	2–5
Input hold to USB clock—all inputs	t <sub>USIXKH</sub>	1	-	ns	2–5
USB clock to output valid—all outputs	t <sub>USKHOV</sub>	—	7	ns	2–5
Output hold from USB clock—all outputs	t <sub>USKHOX</sub>	2		ns	2–5

Notes:

 The symbols for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t<sub>(first two letters of functional block)</sub>(reference)(state)(signal)(state) for outputs. For example, t<sub>USIXKH</sub> symbolizes USB timing (US) for the input (I) to go invalid (X) with respect to the time the USB clock reference (K) goes high (H). Also, t<sub>USKHOX</sub> symbolizes USB timing (US) for the USB clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
</sub>

2. All timings are in reference to USB clock.

- 3. All signals are measured from  $OV_{DD}/2$  of the rising edge of the USB clock to  $0.4 \times OV_{DD}$  of the signal in question for 3.3 V signaling levels.
- 4. Input timings are measured at the pin.
- 5. For active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to that of the leakage current specification.



Figure 25. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4 (DLL Enabled)

Parameter	Symbol <sup>1</sup>	Min	Мах	Unit
Fall time of both SDA and SCL signals <sup>5</sup>	t <sub>I2CF</sub>	—	300	ns
Setup time for STOP condition	t <sub>I2PVKH</sub>	0.6	—	μs
Bus free time between a STOP and START condition	t <sub>I2KHDX</sub>	1.3	—	μs
Noise margin at the LOW level for each connected device (including hysteresis)	V <sub>NL</sub>	$0.1 \times OV_{DD}$	—	V
Noise margin at the HIGH level for each connected device (including hysteresis)	V <sub>NH</sub>	$0.2 \times \text{OV}_{\text{DD}}$	_	V

#### Table 39. I<sup>2</sup>C AC Electrical Specifications (continued)

Notes:

- 1. The symbols for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t<sub>(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t<sub>12DVKH</sub> symbolizes I<sup>2</sup>C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the t<sub>12C</sub> clock reference (K) going to the high (H) state or setup time. Also, t<sub>12SXKL</sub> symbolizes I<sup>2</sup>C timing (I2) for the time that the data with respect to the start condition (S) goes invalid (X) relative to the t<sub>12C</sub> clock reference (K) going to the time that the data with respect to the start condition (S) invalid (I2) for the time that the data with respect to the stop condition (P) reaches the valid state (V) relative to the t<sub>12C</sub> clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).</sub></sub>
- MPC8347E provides a hold time of at least 300 ns for the SDA signal (referred to the V<sub>IH</sub>(min) of the SCL signal) to bridge the undefined region of the falling edge of SCL.
- 3. The maximum t<sub>I2DVKH</sub> must be met only if the device does not stretch the LOW period (t<sub>I2CL</sub>) of the SCL signal.
- 4.  $C_B$  = capacitance of one bus line in pF.
- 5.) The MPC8347E does not follow the "I2C-BUS Specifications" version 2.1 regarding the tI2CF AC parameter.

Figure 31 provides the AC test load for the  $I^2C$ .



Figure 31. I<sup>2</sup>C AC Test Load

Figure 32 shows the AC timing diagram for the  $I^2C$  bus.



Figure 32. I<sup>2</sup>C Bus AC Timing Diagram

#### Table 41. PCI AC Timing Specifications at 66 MHz<sup>1</sup> (continued)

Parameter	Symbol <sup>2</sup>	Min	Max	Unit	Notes
Input hold from clock	t <sub>PCIXKH</sub>	0	—	ns	3, 5

Notes:

- 1. PCI timing depends on M66EN and the ratio between PCI1/PCI2. Refer to the PCI chapter of the reference manual for a description of M66EN.
- 2. The symbols for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t<sub>(first two letters of functional block)</sub>(reference)(state)(signal)(state) for outputs. For example, t<sub>PCIVKH</sub> symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the PCI\_SYNC\_IN clock, t<sub>SYS</sub>, reference (K) going to the high (H) state or setup time. Also, t<sub>PCRHFV</sub> symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.</sub>
- 3. See the timing measurement conditions in the PCI 2.2 Local Bus Specifications.
- 4. For active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
- 5. Input timings are measured at the pin.

#### Table 42 provides the PCI AC timing specifications at 33 MHz.

Table 42. PCI AC	Ciming	<b>Specifications</b>	at 33 MHz
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Parameter	Symbol <sup>1</sup>	Min	Max	Unit	Notes
Clock to output valid	<sup>t</sup> PCKHOV	—	11	ns	2
Output hold from clock	t <sub>PCKHOX</sub>	2	_	ns	2
Clock to output high impedance	t <sub>PCKHOZ</sub>	—	14	ns	2, 3
Input setup to clock	t <sub>PCIVKH</sub>	3.0	-	ns	2, 4
Input hold from clock	t <sub>PCIXKH</sub>	0		ns	2, 4

#### Notes:

- The symbols for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t<sub>(first two letters of functional block)</sub>(reference)(state)(signal)(state) for outputs. For example, t<sub>PCIVKH</sub> symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the PCI\_SYNC\_IN clock, t<sub>SYS</sub>, reference (K) going to the high (H) state or setup time. Also, t<sub>PCRHFV</sub> symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
  </sub>
- 2. See the timing measurement conditions in the PCI 2.2 Local Bus Specifications.
- 3. For active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
- 4. Input timings are measured at the pin.

#### Figure 33 provides the AC test load for PCI.



Figure 33. PCI AC Test Load

Timers

## 14 Timers

This section describes the DC and AC electrical specifications for the timers.

## 14.1 Timer DC Electrical Characteristics

Table 43 provides the DC electrical characteristics for the MPC8347E timer pins, including TIN,  $\overline{\text{TOUT}}$ ,  $\overline{\text{TGATE}}$ , and RTC\_CLK.

Characteristic	Symbol	Condition	Min	Мах	Unit
Input high voltage	V <sub>IH</sub>		2.0	OV <sub>DD</sub> + 0.3	V
Input low voltage	V <sub>IL</sub>		-0.3	0.8	V
Input current	I <sub>IN</sub>			±5	μA
Output high voltage	V <sub>OH</sub>	I <sub>OH</sub> = -8.0 mA	2.4	—	V
Output low voltage	V <sub>OL</sub>	I <sub>OL</sub> = 8.0 mA	—	0.5	V
Output low voltage	V <sub>OL</sub>	I <sub>OL</sub> = 3.2 mA	—	0.4	V

Table 43. Timer DC Electrical Characteristics

## 14.2 Timer AC Timing Specifications

Table 44 provides the timer input and output AC timing specifications.

#### Table 44. Timers Input AC Timing Specifications<sup>1</sup>

Characteristic	Symbol <sup>2</sup>	Min	Unit
Timers inputs—minimum pulse width	t <sub>TIWID</sub>	20	ns

#### Notes:

1. Input specifications are measured from the 50 percent level of the signal to the 50 percent level of the rising edge of CLKIN. Timings are measured at the pin.

2. Timer inputs and outputs are asynchronous to any visible clock. Timer outputs should be synchronized before use by external synchronous logic. Timer inputs are required to be valid for at least t<sub>TIWID</sub> ns to ensure proper operation.

Package and Pin Listings

## 18.2 Mechanical Dimensions for the MPC8347E TBGA

Figure 39 shows the mechanical dimensions and bottom surface nomenclature for the MPC8347E, 672-TBGA package.



#### Notes:

1.All dimensions are in millimeters.

2.Dimensions and tolerances per ASME Y14.5M-1994.

3.Maximum solder ball diameter measured parallel to datum A.

4.Datum A, the seating plane, is determined by the spherical crowns of the solder balls.

5.Parallelism measurement must exclude any effect of mark on top surface of package.

Figure 39. Mechanical Dimensions and Bottom Surface Nomenclature for the MPC8347E TBGA

Table 51	. MPC8347E	(TBGA)	Pinout	Listing	(continued)
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Signal	Package Pin Number	Pin Type	Power Supply	Notes
	DUART			
UART_SOUT[1:2]/MSRCID[0:1]/LSRCID[0:1]	AK27, AN29	0	OV <sub>DD</sub>	
UART_SIN[1:2]/MSRCID[2:3]/LSRCID[2:3]	AL28, AM29	I/O	OV <sub>DD</sub>	
UART_CTS[1]/MSRCID4/LSRCID4	AP30	I/O	OV <sub>DD</sub>	
UART_CTS[2]/MDVAL/ LDVAL	AN30	I/O	OV <sub>DD</sub>	
UART_RTS[1:2]	AP31, AM30	0	OV <sub>DD</sub>	
	I <sup>2</sup> C interface			
IIC1_SDA	AK29	I/O	OV <sub>DD</sub>	2
IIC1_SCL	AP32	I/O	OV <sub>DD</sub>	2
IIC2_SDA	AN31	I/O	OV <sub>DD</sub>	2
IIC2_SCL	AM31	I/O	OV <sub>DD</sub>	2
	SPI			
SPIMOSI	AN32	I/O	OV <sub>DD</sub>	
SPIMISO	AP33	I/O	OV <sub>DD</sub>	
SPICLK	AK30	I/O	OV <sub>DD</sub>	
SPISEL	AL31	I	OV <sub>DD</sub>	
	Clocks			
PCI_CLK_OUT[0:4]	AN9, AP9, AM10, AN10, AJ11	0	OV <sub>DD</sub>	
PCI_SYNC_IN/PCI_CLOCK	AK12	I	OV <sub>DD</sub>	
PCI_SYNC_OUT	AP11	0	OV <sub>DD</sub>	3
RTC/PIT_CLOCK	AM32	I	OV <sub>DD</sub>	
CLKIN	АМ9	I	OV <sub>DD</sub>	
	JTAG			
ТСК	E20	I	OV <sub>DD</sub>	
TDI	F20	I	OV <sub>DD</sub>	4
TDO	B20	0	OV <sub>DD</sub>	3
TMS	A20	I	OV <sub>DD</sub>	4
TRST	B19	I	OV <sub>DD</sub>	4
	Test			
TEST	D22	I	OV <sub>DD</sub>	6
TEST_SEL	AL13	I	OV <sub>DD</sub>	7
	PMC			
QUIESCE	A18	0	OV <sub>DD</sub>	

Signal	Package Pin Number	Pin Type	Power Supply	Notes				
General Purpose I/O Timers								
GPIO1[0]/GTM1_TIN1/GTM2_TIN2	D27	I/O	OV <sub>DD</sub>					
GPIO1[1]/GTM1_TGATE1/GTM2_TGATE2	E26	I/O	OV <sub>DD</sub>					
GPIO1[2]/GTM1_TOUT1	D28	I/O	OV <sub>DD</sub>					
GPIO1[3]/GTM1_TIN2/GTM2_TIN1	G25	I/O	OV <sub>DD</sub>					
GPIO1[4]/GTM1_TGATE2/GTM2_TGATE1	J24	I/O	OV <sub>DD</sub>					
GPIO1[5]/GTM1_TOUT2/GTM2_TOUT1	F26	I/O	OV <sub>DD</sub>					
GPIO1[6]/GTM1_TIN3/GTM2_TIN4	E27	I/O	OV <sub>DD</sub>					
GPIO1[7]/GTM1_TGATE3/GTM2_TGATE4	E28	I/O	OV <sub>DD</sub>					
GPIO1[8]/GTM1_TOUT3	H25	I/O	OV <sub>DD</sub>					
GPIO1[9]/GTM1_TIN4/GTM2_TIN3	F27	I/O	OV <sub>DD</sub>					
GPIO1[10]/GTM1_TGATE4/GTM2_TGATE3	K24	I/O	OV <sub>DD</sub>					
GPIO1[11]/GTM1_TOUT4/GTM2_TOUT3	G26	I/O	OV <sub>DD</sub>					
	USB Port 1	L		1				
MPH1_D0_ENABLEN/DR_D0_ENABLEN	C28	I/O	OV <sub>DD</sub>					
MPH1_D1_SER_TXD/DR_D1_SER_TXD	F25	I/O	OV <sub>DD</sub>					
MPH1_D2_VMO_SE0/DR_D2_VMO_SE0	B28	I/O	OV <sub>DD</sub>					
MPH1_D3_SPEED/DR_D3_SPEED	C27	I/O	OV <sub>DD</sub>					
MPH1_D4_DP/DR_D4_DP	D26	I/O	OV <sub>DD</sub>					
MPH1_D5_DM/DR_D5_DM	E25	I/O	OV <sub>DD</sub>					
MPH1_D6_SER_RCV/DR_D6_SER_RCV	C26	I/O	OV <sub>DD</sub>					
MPH1_D7_DRVVBUS/DR_D7_DRVVBUS	D25	I/O	OV <sub>DD</sub>					
MPH1_NXT/DR_SESS_VLD_NXT	B26	I	OV <sub>DD</sub>					
MPH1_DIR_DPPULLUP/ DR_XCVR_SEL_DPPULLUP	E24	I/O	OV <sub>DD</sub>					
MPH1_STP_SUSPEND/ DR_STP_SUSPEND	A27	0	OV <sub>DD</sub>					
MPH1_PWRFAULT/ DR_RX_ERROR_PWRFAULT	C25	I	OV <sub>DD</sub>					
MPH1_PCTL0/DR_TX_VALID_PCTL0	A26	0	OV <sub>DD</sub>					
MPH1_PCTL1/DR_TX_VALIDH_PCTL1	B25	0	OV <sub>DD</sub>					
MPH1_CLK/DR_CLK	A25	I	OV <sub>DD</sub>					
	USB Port 0	1	1	1				
MPH0_D0_ENABLEN/DR_D8_CHGVBUS	D24	I/O	OV <sub>DD</sub>					
MPH0_D1_SER_TXD/DR_D9_DCHGVBUS	C24	I/O	OV <sub>DD</sub>					

#### Table 52. MPC8347E (PBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
MPH0_D2_VMO_SE0/DR_D10_DPPD	B24	I/O	OV <sub>DD</sub>	
MPH0_D3_SPEED/DR_D11_DMMD	A24	I/O	OV <sub>DD</sub>	
MPH0_D4_DP/DR_D12_VBUS_VLD	D23	I/O	OV <sub>DD</sub>	
MPH0_D5_DM/DR_D13_SESS_END	C23	I/O	OV <sub>DD</sub>	
MPH0_D6_SER_RCV/DR_D14	B23	I/O	OV <sub>DD</sub>	
MPH0_D7_DRVVBUS/DR_D15_IDPULLUP	A23	I/O	OV <sub>DD</sub>	
MPH0_NXT/DR_RX_ACTIVE_ID	D22	I	OV <sub>DD</sub>	
MPH0_DIR_DPPULLUP/DR_RESET	C22	I/O	OV <sub>DD</sub>	
MPH0_STP_SUSPEND/DR_TX_READY	B22	I/O	OV <sub>DD</sub>	
MPH0_PWRFAULT/DR_RX_VALIDH	A22	I	OV <sub>DD</sub>	
MPH0_PCTL0/DR_LINE_STATE0	E21	I/O	OV <sub>DD</sub>	
MPH0_PCTL1/DR_LINE_STATE1	D21	I/O	OV <sub>DD</sub>	
MPH0_CLK/DR_RX_VALID	C21	I	OV <sub>DD</sub>	
P	rogrammable Interrupt Controller			
MCP_OUT	E8	0	OV <sub>DD</sub>	2
IRQ0/MCP_IN/GPIO2[12]	J28	I/O	OV <sub>DD</sub>	
IRQ[1:5]/GPIO2[13:17]	K25, J25, H26, L24, G27	I/O	OV <sub>DD</sub>	
IRQ[6]/GPIO2[18]/CKSTOP_OUT	G28	I/O	OV <sub>DD</sub>	
IRQ[7]/GPIO2[19]/CKSTOP_IN	J26	I/O	OV <sub>DD</sub>	
	Ethernet Management Interface			
EC_MDC	Y24	0	LV <sub>DD1</sub>	
EC_MDIO	Y25	I/O	LV <sub>DD1</sub>	2
	Gigabit Reference Clock			
EC_GTX_CLK125	Y26	I	LV <sub>DD1</sub>	
Three-Spe	ed Ethernet Controller (Gigabit Ethern	et 1)		
TSEC1_COL/GPIO2[20]	M26	I/O	OV <sub>DD</sub>	
TSEC1_CRS/GPIO2[21]	U25	I/O	LV <sub>DD1</sub>	
TSEC1_GTX_CLK	V24	0	LV <sub>DD1</sub>	3
TSEC1_RX_CLK	U26	I	LV <sub>DD1</sub>	
TSEC1_RX_DV	U24	I	LV <sub>DD1</sub>	
TSEC1_RX_ER/GPIO2[26]	L28	I/O	OV <sub>DD</sub>	
TSEC1_RXD[7:4]/GPIO2[22:25]	M27, M28, N26, N27	I/O	OV <sub>DD</sub>	
TSEC1_RXD[3:0]	W26, W24, Y28, Y27	I	LV <sub>DD1</sub>	
TSEC1_TX_CLK	N25	I	OV <sub>DD</sub>	

#### Table 52. MPC8347E (PBGA) Pinout Listing (continued)

			Input Clock Frequency (MHz) <sup>2</sup>			
CFG_CLKIN_DIV at Reset <sup>1</sup>	SPMF	Input Clock	16.67	25	33.33	66.67
		Natio	C	s <i>b_clk</i> Freq	uency (MH	z)
Low	0010	2 : 1				133
Low	0011	3 : 1			100	200
Low	0100	4 : 1		100	133	266
Low	0101	5 : 1		125	166	333
Low	0110	6 : 1	100	150	200	
Low	0111	7 : 1	116	175	233	
Low	1000	8 : 1	133	200	266	
Low	1001	9:1	150	225	300	
Low	1010	10 : 1	166	250	333	
Low	1011	11 : 1	183	275		1
Low	1100	12 : 1	200	300		
Low	1101	13 : 1	216	325		
Low	1110	14 : 1	233		•	
Low	1111	15 : 1	250			
Low	0000	16 : 1	266			
High	0010	2 : 1				133
High	0011	3 : 1			100	200
High	0100	4 : 1			133	266
High	0101	5 : 1			166	333
High	0110	6 : 1			200	
High	0111	7 : 1			233	
High	1000	8 : 1			L	

Table 57. CSB Frequency Options for Host Mode

<sup>1</sup> CFG\_CLKIN\_DIV selects the ratio between CLKIN and PCI\_SYNC\_OUT.

<sup>2</sup> CLKIN is the input clock in host mode; PCI\_CLK is the input clock in agent mode. DDR2 memory may be used at 133 MHz provided that the memory components are specified for operation at this frequency.

_	•	-		
Characteristic	Symbol	Value	Unit	Notes
Junction-to-case thermal	$R_{ extsf{ heta}JC}$	5	°C/W	5
Junction-to-package natural convection on top	Ψіт	5	°C/W	6

#### Table 62. Package Thermal Characteristics for PBGA (continued)

#### Notes

- 1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
- 2. Per SEMI G38-87 and JEDEC JESD51-2 with the single-layer board horizontal.
- 3. Per JEDEC JESD51-6 with the board horizontal.
- 4. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
- 5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
- 6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

## 20.2 Thermal Management Information

For the following sections,  $P_D = (V_{DD} \times I_{DD}) + P_{I/O}$  where  $P_{I/O}$  is the power dissipation of the I/O drivers. See Table 5 for I/O power dissipation values.

### 20.2.1 Estimation of Junction Temperature with Junction-to-Ambient Thermal Resistance

An estimation of the chip junction temperature, T<sub>J</sub>, can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

 $T_J$  = junction temperature (°C)

 $T_A$  = ambient temperature for the package (°C)

 $R_{\theta IA}$  = junction-to-ambient thermal resistance (°C/W)

 $P_D$  = power dissipation in the package (W)

The junction-to-ambient thermal resistance is an industry-standard value that provides a quick and easy estimation of thermal performance. Generally, the value obtained on a single-layer board is appropriate for a tightly packed printed-circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated. Test cases have demonstrated that errors of a factor of two (in the quantity  $T_J - T_A$ ) are possible.

# 20.2.2 Estimation of Junction Temperature with Junction-to-Board Thermal Resistance

The thermal performance of a device cannot be adequately predicted from the junction-to-ambient thermal resistance. The thermal performance of any component is strongly dependent on the power dissipation of surrounding components. In addition, the ambient temperature varies widely within the application. For