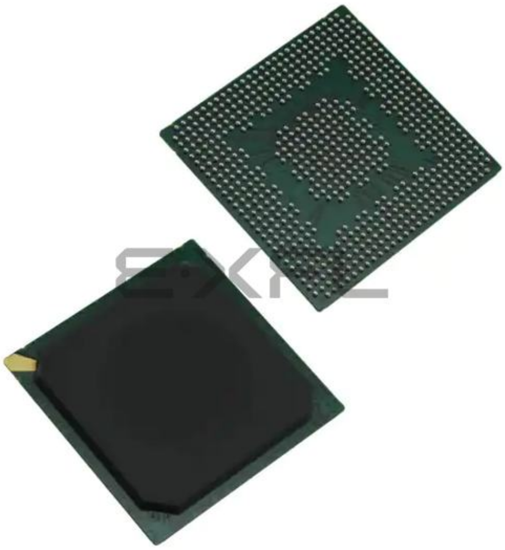
NXP USA Inc. - MPC8347CVRAGD Datasheet



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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e300
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	-
RAM Controllers	DDR
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	-
Package / Case	620-BBGA Exposed Pad
Supplier Device Package	620-HBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8347cvragd

2 Electrical Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC8347E. The MPC8347E is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but are included for a more complete reference. These are not purely I/O buffer design specifications.

2.1 Overall DC Electrical Characteristics

This section covers the ratings, conditions, and other characteristics.

2.1.1 Absolute Maximum Ratings

Table 1 provides the absolute maximum ratings.

Table 1. Absolute Maximum Ratings[1]

Characteristic		Symbol	Max Value	Unit	Notes
Core supply voltage		V_{DD}	–0.3 to 1.32	V	
PLL supply voltage		AV_{DD}	–0.3 to 1.32	V	
DDR DRAM I/O voltage		GV_{DD}	–0.3 to 3.63	V	
Three-speed Ethernet I/O, MII management voltage		LV_{DD}	–0.3 to 3.63	V	
PCI, local bus, DUART, system control and power management, I^2C, and JTAG I/O voltage		OV_{DD}	–0.3 to 3.63	V	
Input voltage	DDR DRAM signals	MV_{IN}	–0.3 to (GV_{DD} + 0.3)	V	2, 5
	DDR DRAM reference	MV_{REF}	–0.3 to (GV_{DD} + 0.3)	V	2, 5
	Three-speed Ethernet signals	LV_{IN}	–0.3 to (LV_{DD} + 0.3)	V	4, 5
	Local bus, DUART, CLKIN, system control and power management, I^2C, and JTAG signals	OV_{IN}	–0.3 to (OV_{DD} + 0.3)	V	3, 5
	PCI	OV_{IN}	–0.3 to (OV_{DD} + 0.3)	V	6
Storage temperature range		T_{STG}	–55 to 150	°C	

Notes:

[1] Functional and tested operating conditions are given in Table 2. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.

[2] **Caution:** MV_{IN} must not exceed GV_{DD} by more than 0.3 V. This limit can be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.

[3] **Caution:** OV_{IN} must not exceed OV_{DD} by more than 0.3 V. This limit can be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.

[4] **Caution:** LV_{IN} must not exceed LV_{DD} by more than 0.3 V. This limit can be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.

[5] (M,L,O)V_{IN} and MV_{REF} may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 2.

[6] OV_{IN} on the PCI interface can overshoot/undershoot according to the PCI Electrical Specification for 3.3-V operation, as shown in Figure 3.

4 Clock Input Timing

This section provides the clock input DC and AC electrical characteristics for the MPC8347E.

4.1 DC Electrical Characteristics

Table 7 provides the clock input (CLKIN/PCI_SYNC_IN) DC timing specifications for the MPC8347E.

Table 6. CLKIN DC Timing Specifications

Parameter	Condition	Symbol	Min	Max	Unit
Input high voltage	—	V_{IH}	2.7	OV_{DD} + 0.3	V
Input low voltage	—	V_{IL}	–0.3	0.4	V
CLKIN input current	$0 V \le V_{IN} \le OV_{DD}$	I_{IN}	—	±10	µA
PCI_SYNC_IN input current	$0 V \le V_{IN} \le 0.5 V$ or $OV_{DD} – 0.5 V \le V_{IN} \le OV_{DD}$	I_{IN}	—	±10	µA
PCI_SYNC_IN input current	$0.5 V \le V_{IN} \le OV_{DD} – 0.5 V$	I_{IN}	—	±50	µA

4.2 AC Electrical Characteristics

The primary clock source for the MPC8347E can be one of two inputs, CLKIN or PCI_CLK, depending on whether the device is configured in PCI host or PCI agent mode. Table 7 provides the clock input (CLKIN/PCI_CLK) AC timing specifications for the MPC8347E.

Table 7. CLKIN AC Timing Specifications

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
CLKIN/PCI_CLK frequency	f_{CLKIN}	—	—	66	MHz	1, 6
CLKIN/PCI_CLK cycle time	t_{CLKIN}	15	—	—	ns	—
CLKIN/PCI_CLK rise and fall time	t_{KH}, t_{KL}	0.6	1.0	2.3	ns	2
CLKIN/PCI_CLK duty cycle	t_{KHK}/t_{CLKIN}	40	—	60	%	3
CLKIN/PCI_CLK jitter	—	—	—	±150	ps	4, 5

Notes:

1. **Caution:** The system, core, USB, security, and TSEC must not exceed their respective maximum or minimum operating frequencies.
2. Rise and fall times for CLKIN/PCI_CLK are measured at 0.4 and 2.7 V.
3. Timing is guaranteed by design and characterization.
4. This represents the total input jitter—short term and long term—and is guaranteed by design.
5. The CLKIN/PCI_CLK driver’s closed loop jitter bandwidth should be <500 kHz at –20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track CLKIN drivers with the specified jitter.
6. The Spread spectrum clocking. Is allowed with 1% input frequency down-spread at maximum 50KHz modulation rate regardless of input frequency.

6 DDR SDRAM

This section describes the DC and AC electrical specifications for the DDR SDRAM interface of the MPC8347E.

NOTE

> The information in this document is accurate for revision 1.1 silicon and earlier. For information on revision 3.0 silicon and earlier versions see the *MPC8347EA PowerQUICC™ II Pro Integrated Host Processor Hardware Specifications*. See Section 23.1, "Part Numbers Fully Addressed by This Document," for silicon revision level determination.

6.1 DDR SDRAM DC Electrical Characteristics

Table 11 provides the recommended operating conditions for the DDR SDRAM component(s) of the MPC8347E.

Table 11. DDR SDRAM DC Electrical Characteristics

Parameter/Condition	Symbol	Min	Max	Unit	Notes
I/O supply voltage	GV_{DD}	2.375	2.625	V	1
I/O reference voltage	MV_{REF}	$0.49 \times GV_{DD}$	$0.51 \times GV_{DD}$	V	2
I/O termination voltage	V_{TT}	$MV_{REF} – 0.04$	$MV_{REF} + 0.04$	V	3
Input high voltage	V_{IH}	$MV_{REF} + 0.18$	$GV_{DD} + 0.3$	V	
Input low voltage	V_{IL}	–0.3	$MV_{REF} – 0.18$	V	
Output leakage current	I_{OZ}	–10	10	μA	4
Output high current (V_{OUT} = 1.95 V)	I_{OH}	–15.2	—	mA	
Output low current (V_{OUT} = 0.35 V)	I_{OL}	15.2	—	mA	
MV_{REF} input leakage current	I_{VREF}	—	5	μA	

Notes:

1. GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.
2. MV_{REF} is expected to be equal to $0.5 \times GV_{DD}$, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF}. This rail should track variations in the DC level of MV_{REF}.
4. Output leakage is measured with all outputs disabled, $0 V \leq V_{OUT} \leq GV_{DD}$.

Table 12 provides the DDR capacitance.

Table 12. DDR SDRAM Capacitance

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input/output capacitance: DQ, DQS	C_{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS	C_{DIO}	—	0.5	pF	1

Note:

1. This parameter is sampled. GV_{DD} = 2.5 V ± 0.125 V, f = 1 MHz, T_A = 25°C, $V_{OUT} = GV_{DD}/2$, V_{OUT} (peak-to-peak) = 0.2 V.

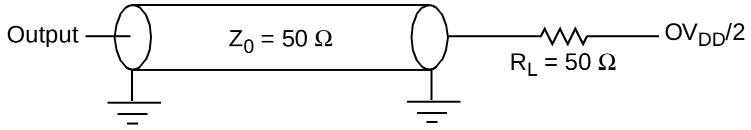


Figure 6. DDR AC Test Load

Table 15 shows the DDR SDRAM measurement conditions.

Table 15. DDR SDRAM Measurement Conditions

Symbol	DDR	Unit	Notes
V_{TH}	MV_{REF} ± 0.31 V	V	1
V_{OUT}	$0.5 \times GV_{DD}$	V	2

Notes:

1. Data input threshold measurement point.
2. Data output measurement point.

Figure 7 shows the DDR SDRAM output timing diagram for source synchronous mode.

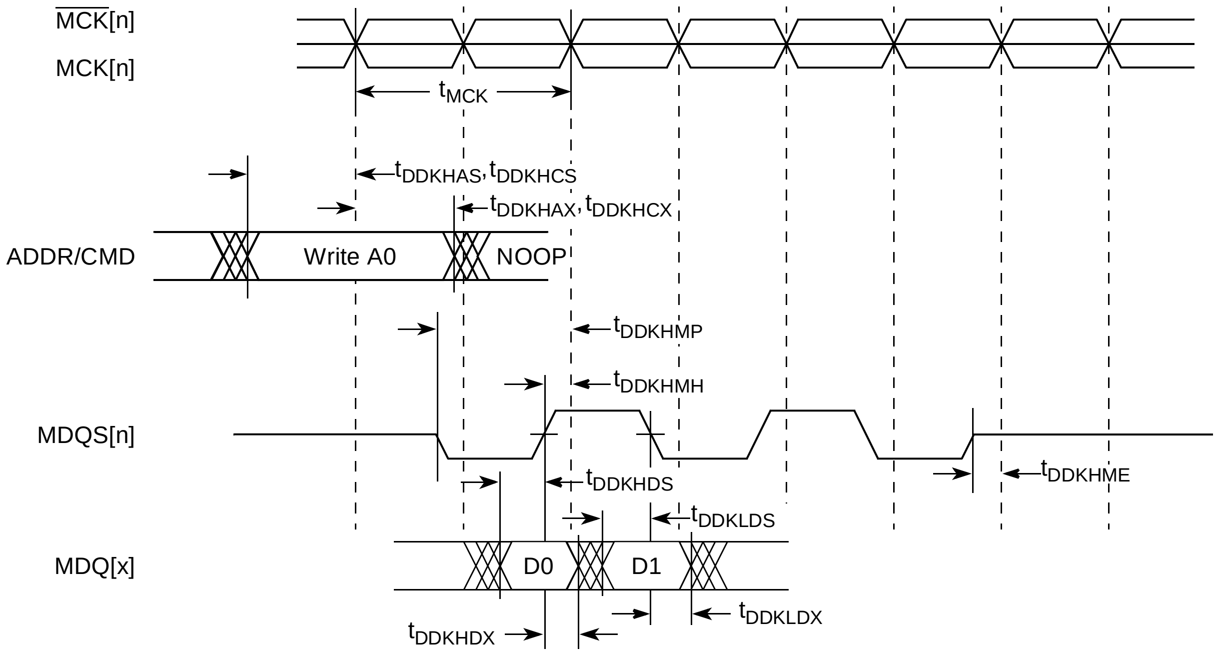


Figure 7. DDR SDRAM Output Timing Diagram for Source Synchronous Mode

Table 16 provides approximate delay information that can be expected for the address and command signals of the DDR controller for various loadings, which can be useful for a system utilizing the DLL. These numbers are the result of simulations for one topology. The delay numbers will strongly depend on the topology used. These delay numbers show the total delay for the address and command to arrive at the DRAM devices. The actual delay could be different than the delays seen in simulation, depending on the system topology. If a heavily loaded system is used, the DLL loop may need to be adjusted to meet setup requirements at the DRAM.

Figure 12 shows the MII receive AC timing diagram.

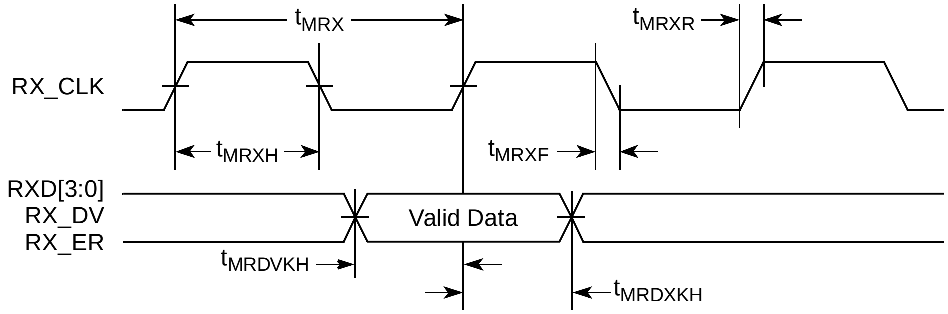


Figure 12. MII Receive AC Timing Diagram

8.2.3 TBI AC Timing Specifications

This section describes the TBI transmit and receive AC timing specifications.

8.2.3.1 TBI Transmit AC Timing Specifications

Table 25 provides the TBI transmit AC timing specifications.

Table 25. TBI Transmit AC Timing Specifications

At recommended operating conditions with LV_{DD}/OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit
GTX_CLK clock period	t_{TTX}	—	8.0	—	ns
GTX_CLK duty cycle	t_{TTXH}/t_{TTX}	40	—	60	%
GTX_CLK to TBI data TXD[7:0], TX_ER, TX_EN delay	t_{TTKHDX}	1.0	—	5.0	ns
GTX_CLK clock rise, V_{IL}(min) to V_{IH}(max)	t_{TTXR}	—	—	1.0	ns
GTX_CLK clock fall time, V_{IH}(max) to V_{IL}(min)	t_{TTXF}	—	—	1.0	ns
GTX_CLK125 reference clock period	t_{G125}[2]	—	8.0	—	ns
GTX_CLK125 reference clock duty cycle	t_{G125H}/t_{G125}	45	—	55	ns

Notes:

1. The symbols for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{TTKHDV} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the valid state (V) or setup time. Also, t_{TTKHDX} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the invalid state (X) or hold time. In general, the clock reference symbol is based on three letters representing the clock of a particular function. For example, the subscript of t_{TTX} represents the TBI (T) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. This symbol represents the external GTX_CLK125 and does not follow the original symbol naming convention

Figure 14 shows the TBI receive AC timing diagram.

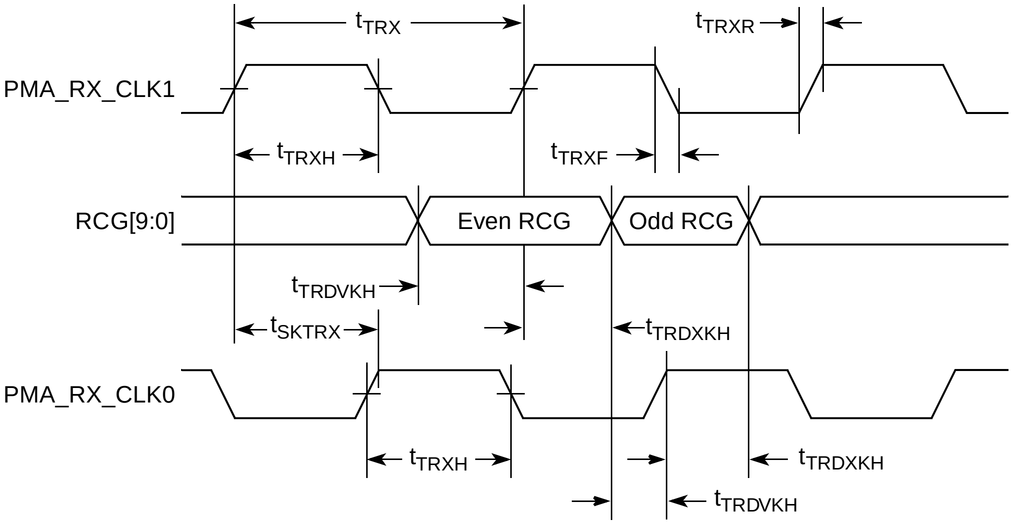


Figure 14. TBI Receive AC Timing Diagram

8.2.4 RGMII and RTBI AC Timing Specifications

Table 27 presents the RGMII and RTBI AC timing specifications.

Table 27. RGMII and RTBI AC Timing Specifications

At recommended operating conditions with LV_{DD} of 2.5 V ± 5%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit
Data to clock output skew (at transmitter)	t_{SKRGT}	–0.5	—	0.5	ns
Data to clock input skew (at receiver)[2]	t_{SKRGT}	1.0	—	2.8	ns
Clock cycle duration[3]	t_{RGT}	7.2	8.0	8.8	ns
Duty cycle for 1000Base-T[4, 5]	t_{RGTH}/t_{RGT}	45	50	55	%
Duty cycle for 10BASE-T and 100BASE-TX[3, 5]	t_{RGTH}/t_{RGT}	40	50	60	%
Rise time (20%–80%)	t_{RGTR}	—	—	0.75	ns
Fall time (20%–80%)	t_{RGTF}	—	—	0.75	ns
GTX_CLK125 reference clock period	t_{G12}[6]	—	8.0	—	ns
GTX_CLK125 reference clock duty cycle	t_{G125H}/t_{G125}	47	—	53	%

Notes:

1. In general, the clock reference symbol for this section is based on the symbols RGT to represent RGMII and RTBI timing. For example, the subscript of t_{RGT} represents the TBI (T) receive (RX) clock. Also, the notation for rise (R) and fall (F) times follows the clock symbol. For symbols representing skews, the subscript is SK followed by the clock being skewed (RGT).
2. This implies that PC board design requires clocks to be routed so that an additional trace delay of greater than 1.5 ns is added to the associated clock signal.
3. For 10 and 100 Mbps, t_{RGT} scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned.
5. Duty cycle reference is $LV_{DD}/2$.
6. This symbol represents the external GTX_CLK125 and does not follow the original symbol naming convention.

Figure 17 and Figure 18 provide the AC test load and signals for the USB, respectively.

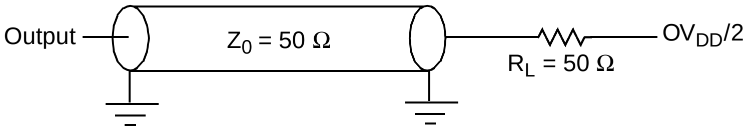


Figure 17. USB AC Test Load

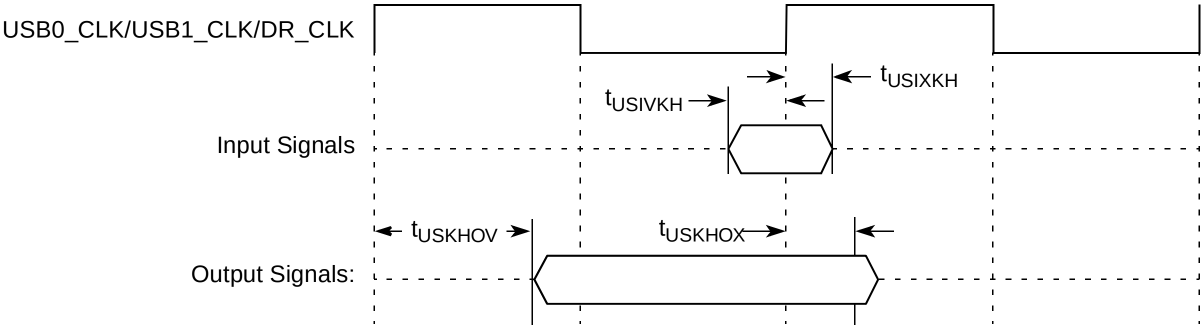


Figure 18. USB Signals

Figure 34 shows the PCI input AC timing diagram.

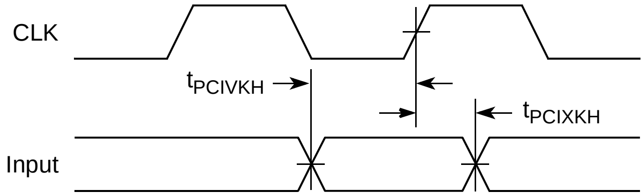


Figure 34. PCI Input AC Timing Diagram

Figure 35 shows the PCI output AC timing diagram.

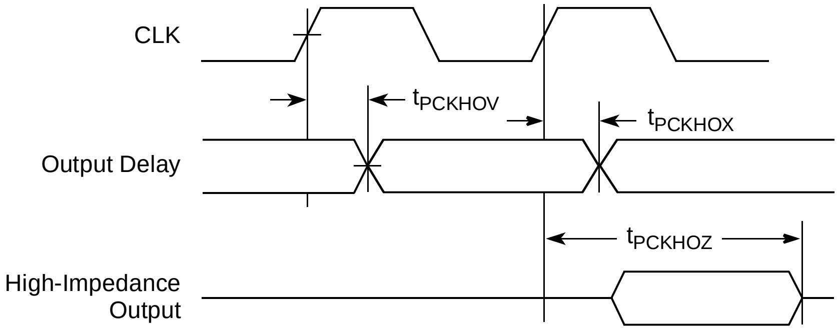


Figure 35. PCI Output AC Timing Diagram

15 GPIO

This section describes the DC and AC electrical specifications for the GPIO.

15.1 GPIO DC Electrical Characteristics

Table 45 provides the DC electrical characteristics for the MPC8347E GPIO.

Table 45. GPIO DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}		2.0	OV_{DD} + 0.3	V
Input low voltage	V_{IL}		–0.3	0.8	V
Input current	I_{IN}			±5	μA
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V

15.2 GPIO AC Timing Specifications

Table 46 provides the GPIO input and output AC timing specifications.

Table 46. GPIO Input AC Timing Specifications[1]

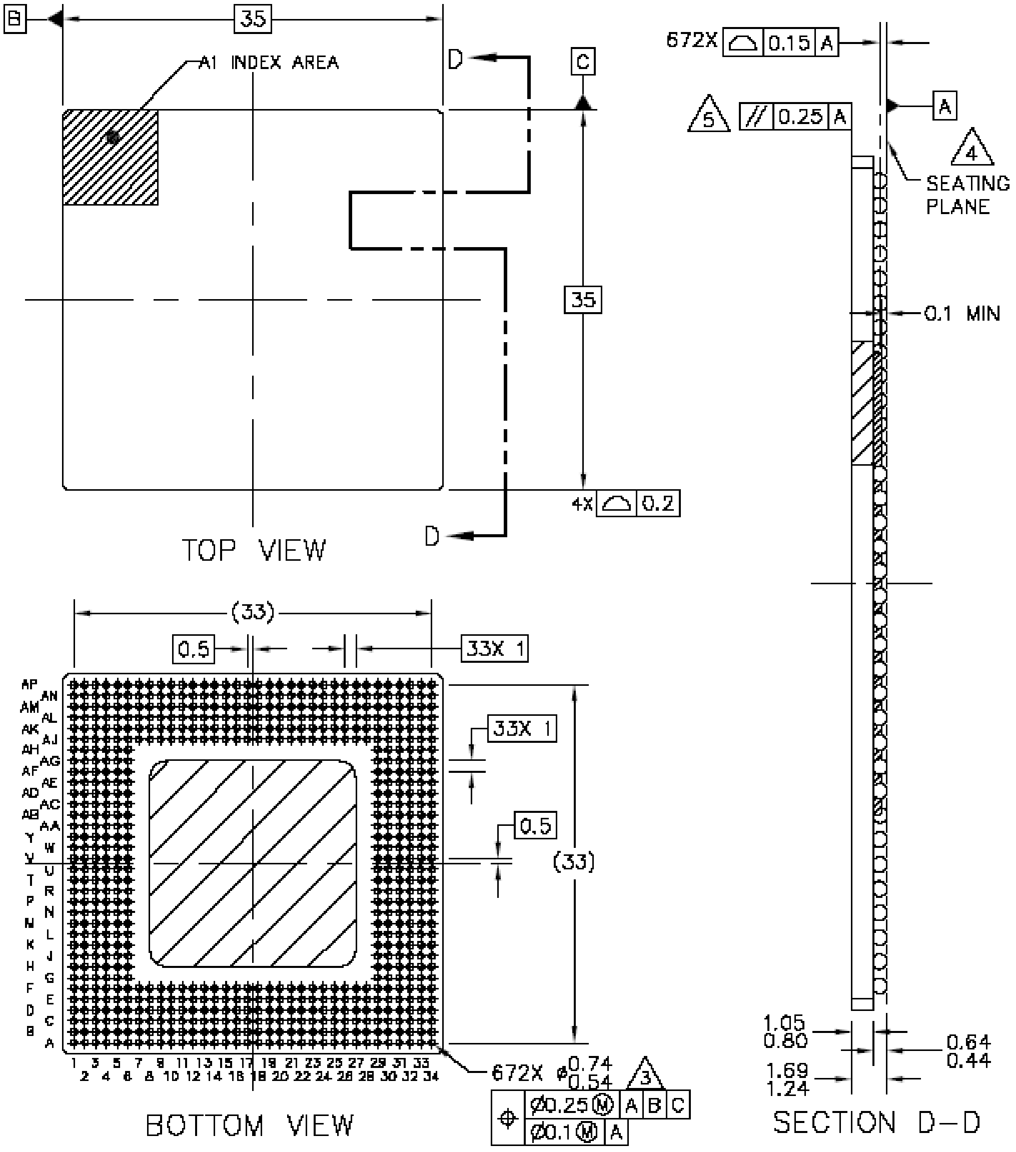
Characteristic	Symbol[2]	Min	Unit
GPIO inputs—minimum pulse width	t_{PIWID}	20	ns

Notes:

1. Input specifications are measured from the 50 percent level of the signal to the 50 percent level of the rising edge of CLKIN. Timings are measured at the pin.
2. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs should be synchronized before use by external synchronous logic. GPIO inputs must be valid for at least t_{PIWID} ns to ensure proper operation.

18.2 Mechanical Dimensions for the MPC8347E TBGA

Figure 39 shows the mechanical dimensions and bottom surface nomenclature for the MPC8347E, 672-TBGA package.



Notes:

1. All dimensions are in millimeters.
2. Dimensions and tolerances per ASME Y14.5M-1994.
3. Maximum solder ball diameter measured parallel to datum A.
4. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.
5. Parallelism measurement must exclude any effect of mark on top surface of package.

Figure 39. Mechanical Dimensions and Bottom Surface Nomenclature for the MPC8347E TBGA

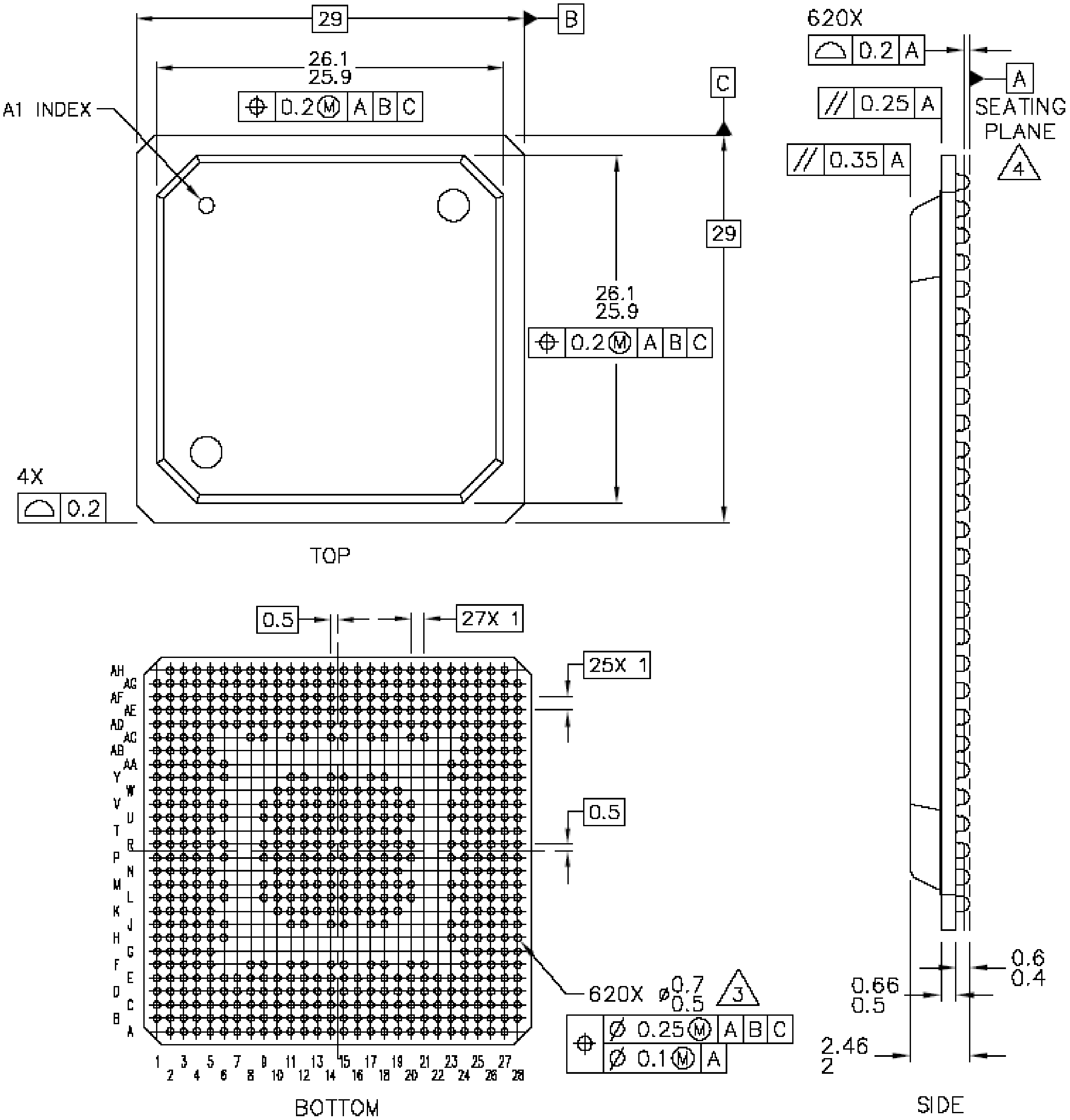
18.3 Package Parameters for the MPC8347E PBGA

The package parameters are as provided in the following list. The package type is 29 mm × 29 mm, 620 plastic ball grid array (PBGA).

Package outline	29 mm × 29 mm
Interconnects	620
Pitch	1.00 mm
Module height (maximum)	2.46 mm
Module height (typical)	2.23 mm
Module height (minimum)	2.00 mm
Solder balls	62 Sn/36 Pb/2 Ag (ZQ package) 95.5 Sn/0.5 Cu/4Ag (VR package)
Ball diameter (typical)	0.60 mm

18.4 Mechanical Dimensions for the MPC8347E PBGA

Figure 40 shows the mechanical dimensions and bottom surface nomenclature for the MPC8347E, 620-PBGA package.



Notes:

1.All dimensions are in millimeters.

2.Dimensioning and tolerancing per ASME Y14. 5M-1994.

3.Maximum solder ball diameter measured parallel to datum A.

4.Datum A, the seating plane, is determined by the spherical crowns of the solder balls.

Figure 40. Mechanical Dimensions and Bottom Surface Nomenclature for the MPC8347E PBGA

Table 51. MPC8347E (TBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
LBCTL	AN26	O	OV_{DD}	
LALE	AK24	O	OV_{DD}	
LGPL0/LSDA10/cfg_reset_source0	AP27	I/O	OV_{DD}	
LGPL1/$\overline{\text{LSDWE}}$/cfg_reset_source1	AL25	I/O	OV_{DD}	
LGPL2/$\overline{\text{LSDRAS}}$/$\overline{\text{LOE}}$	AJ24	O	OV_{DD}	
LGPL3/$\overline{\text{LSDCAS}}$/cfg_reset_source2	AN27	I/O	OV_{DD}	
LGPL4/$\overline{\text{LGTA}}$/LUPWAIT/LPBSE	AP28	I/O	OV_{DD}	
LGPL5/cfg_clkin_div	AL26	I/O	OV_{DD}	
LCKE	AM27	O	OV_{DD}	
LCLK[0:2]	AN28, AK26, AP29	O	OV_{DD}	
LSYNC_OUT	AM12	O	OV_{DD}	
LSYNC_IN	AJ10	I	OV_{DD}	
General Purpose I/O Timers				
GPIO1[0]/GTM1_TIN1/GTM2_TIN2	F24	I/O	OV_{DD}	
GPIO1[1]/$\overline{\text{GTM1\_TGATE1}}$/$\overline{\text{GTM2\_TGATE2}}$	E24	I/O	OV_{DD}	
GPIO1[2]/$\overline{\text{GTM1\_TOUT1}}$	B25	I/O	OV_{DD}	
GPIO1[3]/GTM1_TIN2/GTM2_TIN1	D24	I/O	OV_{DD}	
GPIO1[4]/$\overline{\text{GTM1\_TGATE2}}$/$\overline{\text{GTM2\_TGATE1}}$	A25	I/O	OV_{DD}	
GPIO1[5]/$\overline{\text{GTM1\_TOUT2}}$/$\overline{\text{GTM2\_TOUT1}}$	B24	I/O	OV_{DD}	
GPIO1[6]/GTM1_TIN3/GTM2_TIN4	A24	I/O	OV_{DD}	
GPIO1[7]/$\overline{\text{GTM1\_TGATE3}}$/$\overline{\text{GTM2\_TGATE4}}$	D23	I/O	OV_{DD}	
GPIO1[8]/$\overline{\text{GTM1\_TOUT3}}$	B23	I/O	OV_{DD}	
GPIO1[9]/GTM1_TIN4/GTM2_TIN3	A23	I/O	OV_{DD}	
GPIO1[10]/$\overline{\text{GTM1\_TGATE4}}$/$\overline{\text{GTM2\_TGATE3}}$	F22	I/O	OV_{DD}	
GPIO1[11]/$\overline{\text{GTM1\_TOUT4}}$/$\overline{\text{GTM2\_TOUT3}}$	E22	I/O	OV_{DD}	
USB Port 1				
MPH1_D0_ENABLEN/DR_D0_ENABLEN	A26	I/O	OV_{DD}	
MPH1_D1_SER_TXD/DR_D1_SER_TXD	B26	I/O	OV_{DD}	
MPH1_D2_VMO_SE0/DR_D2_VMO_SE0	D25	I/O	OV_{DD}	
MPH1_D3_SPEED/DR_D3_SPEED	A27	I/O	OV_{DD}	
MPH1_D4_DP/DR_D4_DP	B27	I/O	OV_{DD}	
MPH1_D5_DM/DR_D5_DM	C27	I/O	OV_{DD}	
MPH1_D6_SER_RCV/DR_D6_SER_RCV	D26	I/O	OV_{DD}	
MPH1_D7_DRVVBUS/DR_D7_DRVVBUS	E26	I/O	OV_{DD}	

Table 52. MPC8347E (PBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
$\overline{\text{MCAS}}$	AG6	O	GV$_{DD}$	
$\overline{\text{MCS}}$[0:3]	AE7, AH7, AH4, AF2	O	GV$_{DD}$	
MCKE[0:1]	AG23, AH23	O	GV$_{DD}$	3
MCK[0:5]	AH15, AE24, AE2, AF14, AE23, AD3	O	GV$_{DD}$	
$\overline{\text{MCK}}$[0:5]	AG15, AD23, AE3, AG14, AF24, AD2	O	GV$_{DD}$	
Pins Reserved for Future DDR2 (They should be left unconnected for MPC8347)				
MODT[0:3]	AG5, AD4, AH6, AF4	—	—	
MBA[2]	AD22			
SPARE1	AF12	—	—	7
SPARE2	AG11	—	—	6
Local Bus Controller Interface				
LAD[0:31]	T4, T5, T1, R2, R3, T2, R1, R4, P1, P2, P3, P4, N1, N4, N2, N3, M1, M2, M3, N5, M4, L1, L2, L3, K1, M5, K2, K3, J1, J2, L5, J3	I/O	OV$_{DD}$	
LDP[0]/$\overline{\text{CKSTOP\_OUT}}$	H1	I/O	OV$_{DD}$	
LDP[1]/$\overline{\text{CKSTOP\_IN}}$	K5	I/O	OV$_{DD}$	
LDP[2]	H2	I/O	OV$_{DD}$	
LDP[3]	G1	I/O	OV$_{DD}$	
LA[27:31]	J4, H3, G2, F1, G3	O	OV$_{DD}$	
$\overline{\text{LCS}}$[0:3]	J5, H4, F2, E1	O	OV$_{DD}$	
$\overline{\text{LWE}}$[0:3]/LSDDQM[0:3]/$\overline{\text{LBS}}$[0:3]	F3, G4, D1, E2	O	OV$_{DD}$	
LBCTL	H5	O	OV$_{DD}$	
LALE	E3	O	OV$_{DD}$	
LGPL0/LSDA10/cfg_reset_source0	F4	I/O	OV$_{DD}$	
LGPL1/$\overline{\text{LSDWE}}$/cfg_reset_source1	D2	I/O	OV$_{DD}$	
LGPL2/$\overline{\text{LSDRAS}}$/$\overline{\text{LOE}}$	C1	O	OV$_{DD}$	
LGPL3/$\overline{\text{LSDCAS}}$/cfg_reset_source2	C2	I/O	OV$_{DD}$	
LGPL4/$\overline{\text{LGTA}}$/LUPWAIT/LPBSE	C3	I/O	OV$_{DD}$	
LGPL5/cfg_clkin_div	B3	I/O	OV$_{DD}$	
LCKE	E4	O	OV$_{DD}$	
LCLK[0:2]	D4, A3, C4	O	OV$_{DD}$	
LSYNC_OUT	U3	O	OV$_{DD}$	
LSYNC_IN	Y2	I	OV$_{DD}$	

Table 52. MPC8347E (PBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
MPH0_D2_VMO_SE0/DR_D10_DPPD	B24	I/O	OV$_{DD}$	
MPH0_D3_SPEED/DR_D11_DMMD	A24	I/O	OV$_{DD}$	
MPH0_D4_DP/DR_D12_VBUS_VLD	D23	I/O	OV$_{DD}$	
MPH0_D5_DM/DR_D13_SESS_END	C23	I/O	OV$_{DD}$	
MPH0_D6_SER_RCV/DR_D14	B23	I/O	OV$_{DD}$	
MPH0_D7_DRVVBUS/DR_D15_IDPULLUP	A23	I/O	OV$_{DD}$	
MPH0_NXT/DR_RX_ACTIVE_ID	D22	I	OV$_{DD}$	
MPH0_DIR_DPPULLUP/DR_RESET	C22	I/O	OV$_{DD}$	
MPH0_STP_SUSPEND/DR_TX_READY	B22	I/O	OV$_{DD}$	
MPH0_PWRFAULT/DR_RX_VALIDH	A22	I	OV$_{DD}$	
MPH0_PCTL0/DR_LINE_STATE0	E21	I/O	OV$_{DD}$	
MPH0_PCTL1/DR_LINE_STATE1	D21	I/O	OV$_{DD}$	
MPH0_CLK/DR_RX_VALID	C21	I	OV$_{DD}$	
Programmable Interrupt Controller				
$\overline{\text{MCP\_OUT}}$	E8	O	OV$_{DD}$	2
$\overline{\text{IRQ}}$0/$\overline{\text{MCP_IN}}$/GPIO2[12]	J28	I/O	OV$_{DD}$	
$\overline{\text{IRQ}}$[1:5]/GPIO2[13:17]	K25, J25, H26, L24, G27	I/O	OV$_{DD}$	
$\overline{\text{IRQ}}$[6]/GPIO2[18]/CKSTOP_OUT	G28	I/O	OV$_{DD}$	
$\overline{\text{IRQ}}$[7]/GPIO2[19]/CKSTOP_IN	J26	I/O	OV$_{DD}$	
Ethernet Management Interface				
EC_MDC	Y24	O	LV$_{DD1}$	
EC_MDIO	Y25	I/O	LV$_{DD1}$	2
Gigabit Reference Clock				
EC_GTX_CLK125	Y26	I	LV$_{DD1}$	
Three-Speed Ethernet Controller (Gigabit Ethernet 1)				
TSEC1_COL/GPIO2[20]	M26	I/O	OV$_{DD}$	
TSEC1_CRS/GPIO2[21]	U25	I/O	LV$_{DD1}$	
TSEC1_GTX_CLK	V24	O	LV$_{DD1}$	3
TSEC1_RX_CLK	U26	I	LV$_{DD1}$	
TSEC1_RX_DV	U24	I	LV$_{DD1}$	
TSEC1_RX_ER/GPIO2[26]	L28	I/O	OV$_{DD}$	
TSEC1_RXD[7:4]/GPIO2[22:25]	M27, M28, N26, N27	I/O	OV$_{DD}$	
TSEC1_RXD[3:0]	W26, W24, Y28, Y27	I	LV$_{DD1}$	
TSEC1_TX_CLK	N25	I	OV$_{DD}$	

Table 52. MPC8347E (PBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
SPIMISO	C7	I/O	OV_{DD}	
SPICLK	B7	I/O	OV_{DD}	
SPISEL	A7	I	OV_{DD}	
Clocks				
PCI_CLK_OUT[0:2]	Y1, W3, W2	O	OV_{DD}	
PCI_CLK_OUT[3]/$\overline{\text{LCS}}$[6]	W1	O	OV_{DD}	
PCI_CLK_OUT[4]/$\overline{\text{LCS}}$[7]	V3	O	OV_{DD}	
PCI_SYNC_IN/PCI_CLOCK	U4	I	OV_{DD}	
PCI_SYNC_OUT	U5	O	OV_{DD}	3
RTC/PIT_CLOCK	E9	I	OV_{DD}	
CLKIN	W5	I	OV_{DD}	
JTAG				
TCK	H27	I	OV_{DD}	
TDI	H28	I	OV_{DD}	4
TDO	M24	O	OV_{DD}	3
TMS	J27	I	OV_{DD}	4
$\overline{\text{TRST}}$	K26	I	OV_{DD}	4
Test				
TEST	F28	I	OV_{DD}	6
TEST_SEL	T3	I	OV_{DD}	6
PMC				
$\overline{\text{QUIESCE}}$	K27	O	OV_{DD}	
System Control				
$\overline{\text{PORESET}}$	K28	I	OV_{DD}	
$\overline{\text{HRESET}}$	M25	I/O	OV_{DD}	1
$\overline{\text{SRESET}}$	L27	I/O	OV_{DD}	2
Thermal Management				
THERM0	B15	I	—	8
Power and Ground Signals				
$AV_{DD}1$	C15	Power for e300 PLL (1.2 V)	$AV_{DD}1$	
$AV_{DD}2$	U1	Power for system PLL (1.2 V)	$AV_{DD}2$	

Table 58. CSB Frequency Options for Agent Mode

CFG_CLKIN_DIV at Reset[1]	SPMF	*csb_clk* : Input Clock Ratio[2]	Input Clock Frequency (MHz)[2]			
			16.67	25	33.33	66.67
			csb_clk Frequency (MHz)			
Low	0010	2 : 1				133
Low	0011	3 : 1			100	200
Low	0100	4 : 1		100	133	266
Low	0101	5 : 1		125	166	333
Low	0110	6 : 1	100	150	200	
Low	0111	7 : 1	116	175	233	
Low	1000	8 : 1	133	200	266	
Low	1001	9 : 1	150	225	300	
Low	1010	10 : 1	166	250	333	
Low	1011	11 : 1	183	275		
Low	1100	12 : 1	200	300		
Low	1101	13 : 1	216	325		
Low	1110	14 : 1	233			
Low	1111	15 : 1	250			
Low	0000	16 : 1	266			
High	0010	4 : 1		100	133	266
High	0011	6 : 1	100	150	200	
High	0100	8 : 1	133	200	266	
High	0101	10 : 1	166	250	333	
High	0110	12 : 1	200	300		
High	0111	14 : 1	233			
High	1000	16 : 1	266			

[1] CFG_CLKIN_DIV doubles csb_clk if set high.

[2] CLKIN is the input clock in host mode; PCI_CLK is the input clock in agent mode.

DDR2 memory may be used at 133 MHz provided that the memory components are specified for operation at this frequency.

19.2 Core PLL Configuration

RCWL[COREPLL] selects the ratio between the internal coherent system bus clock (*csb_clk*) and the e300 core clock (*core_clk*). Table 59 shows the encodings for RCWL[COREPLL]. COREPLL values that are not listed in Table 59 should be considered as reserved.

where:

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)
$R_{\theta JC}$ = junction-to-case thermal resistance (°C/W)
$R_{\theta CA}$ = case-to-ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device-related and cannot be influenced by the user. The user controls the thermal environment to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed-circuit board, or change the thermal dissipation on the printed-circuit board surrounding the device.

The thermal performance of devices with heat sinks has been simulated with a few commercially available heat sinks. The heat sink choice is determined by the application environment (temperature, air flow, adjacent component power dissipation) and the physical space available. Because there is not a standard application environment, a standard heat sink is not required.

Table 63 and Table 64 show heat sink thermal resistance for TBGA and PBGA of the MPC8347E.

Table 63. Heat Sink and Thermal Resistance of MPC8347E (TBGA)

Heat Sink Assuming Thermal Grease	Air Flow	35 × 35 mm TBGA
		Thermal Resistance
AAVID 30 × 30 × 9.4 mm pin fin	Natural convection	10
AAVID 30 × 30 × 9.4 mm pin fin	1 m/s	6.5
AAVID 30 × 30 × 9.4 mm pin fin	2 m/s	5.6
AAVID 31 × 35 × 23 mm pin fin	Natural convection	8.4
AAVID 31 × 35 × 23 mm pin fin	1 m/s	4.7
AAVID 31 × 35 × 23 mm pin fin	2 m/s	4
Wakefield, 53 × 53 × 25 mm pin fin	Natural convection	5.7
Wakefield, 53 × 53 × 25 mm pin fin	1 m/s	3.5
Wakefield, 53 × 53 × 25 mm pin fin	2 m/s	2.7
MEI, 75 × 85 × 12 no adjacent board, extrusion	Natural convection	6.7
MEI, 75 × 85 × 12 no adjacent board, extrusion	1 m/s	4.1
MEI, 75 × 85 × 12 no adjacent board, extrusion	2 m/s	2.8
MEI, 75 × 85 × 12 mm, adjacent board, 40 mm side bypass	1 m/s	3.1

Table 64. Heat Sink and Thermal Resistance of MPC8347E (PBGA)

Heat Sink Assuming Thermal Grease	Air Flow	29 × 29 mm PBGA
		Thermal Resistance
AAVID 30 × 30 × 9.4 mm pin fin	Natural convection	13.5
AAVID 30 × 30 × 9.4 mm pin fin	1 m/s	9.6

21.3 Decoupling Recommendations

Due to large address and data buses and high operating frequencies, the MPC8347E can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the MPC8347E system, and the MPC8347E itself requires a clean, tightly regulated source of power. Therefore, the system designer should place at least one decoupling capacitor at each V_{DD}, OV_{DD}, GV_{DD}, and LV_{DD} pin of the MPC8347E. These capacitors should receive their power from separate V_{DD}, OV_{DD}, GV_{DD}, LV_{DD}, and GND power planes in the PCB, with short traces to minimize inductance. Capacitors can be placed directly under the device using a standard escape pattern. Others can surround the part.

These capacitors should have a value of 0.01 or 0.1 µF. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0402 or 0603 sizes.

In addition, distribute several bulk storage capacitors around the PCB, feeding the V_{DD}, OV_{DD}, GV_{DD}, and LV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors are 100–330 µF (AVX TPS tantalum or Sanyo OSCON).

21.4 Connection Recommendations

To ensure reliable operation, connect unused inputs to an appropriate signal level. Unused active low inputs should be tied to OV_{DD}, GV_{DD}, or LV_{DD} as required. Unused active high inputs should be connected to GND. All NC (no-connect) signals must remain unconnected.

Power and ground connections must be made to all external V_{DD}, GV_{DD}, LV_{DD}, OV_{DD}, and GND pins of the MPC8347E.

21.5 Output Buffer DC Impedance

The MPC8347E drivers are characterized over process, voltage, and temperature. For all buses, the driver is a push-pull single-ended driver type (open drain for I^2C).

To measure Z_0 for the single-ended drivers, an external resistor is connected from the chip pad to OV_{DD} or GND. Then the value of each resistor is varied until the pad voltage is $OV_{DD}/2$ (see Figure 43). The output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held high, SW1 is closed (SW2 is open) and R_P is trimmed until the voltage at the pad equals $OV_{DD}/2$. R_P then becomes the resistance of the pull-up devices. R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N)/2$.

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