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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e300
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	-
RAM Controllers	DDR
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	-
Package / Case	672-LBGA
Supplier Device Package	672-LBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8347cvvagdb

2 Electrical Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC8347E. The MPC8347E is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but are included for a more complete reference. These are not purely I/O buffer design specifications.

2.1 Overall DC Electrical Characteristics

This section covers the ratings, conditions, and other characteristics.

2.1.1 Absolute Maximum Ratings

Table 1 provides the absolute maximum ratings.

Table 1. Absolute Maximum Ratings[1]

Characteristic		Symbol	Max Value	Unit	Notes
Core supply voltage		V_{DD}	–0.3 to 1.32	V	
PLL supply voltage		AV_{DD}	–0.3 to 1.32	V	
DDR DRAM I/O voltage		GV_{DD}	–0.3 to 3.63	V	
Three-speed Ethernet I/O, MII management voltage		LV_{DD}	–0.3 to 3.63	V	
PCI, local bus, DUART, system control and power management, I^2C, and JTAG I/O voltage		OV_{DD}	–0.3 to 3.63	V	
Input voltage	DDR DRAM signals	MV_{IN}	–0.3 to (GV_{DD} + 0.3)	V	2, 5
	DDR DRAM reference	MV_{REF}	–0.3 to (GV_{DD} + 0.3)	V	2, 5
	Three-speed Ethernet signals	LV_{IN}	–0.3 to (LV_{DD} + 0.3)	V	4, 5
	Local bus, DUART, CLKIN, system control and power management, I^2C, and JTAG signals	OV_{IN}	–0.3 to (OV_{DD} + 0.3)	V	3, 5
	PCI	OV_{IN}	–0.3 to (OV_{DD} + 0.3)	V	6
Storage temperature range		T_{STG}	–55 to 150	°C	

Notes:

1. Functional and tested operating conditions are given in Table 2. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. **Caution:** MV_{IN} must not exceed GV_{DD} by more than 0.3 V. This limit can be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
3. **Caution:** OV_{IN} must not exceed OV_{DD} by more than 0.3 V. This limit can be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
4. **Caution:** LV_{IN} must not exceed LV_{DD} by more than 0.3 V. This limit can be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
5. (M,L,O)V_{IN} and MV_{REF} may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 2.
6. OV_{IN} on the PCI interface can overshoot/undershoot according to the PCI Electrical Specification for 3.3-V operation, as shown in Figure 3.

Table 5 shows the estimated typical I/O power dissipation for MPC8347E.

Table 5. MPC8347E Typical I/O Power Dissipation

Interface	Parameter	DDR2 GV_{DD} (1.8 V)	DDR1 GV_{DD} (2.5 V)	OV_{DD} (3.3 V)	LV_{DD} (3.3 V)	LV_{DD} (2.5 V)	Unit	Comments
DDR I/O 65% utilization 2.5 V Rs = 20 Ω Rt = 50 Ω 2 pair of clocks	200 MHz, 32 bits	—	0.42	—	—	—	W	—
	200 MHz, 64 bits	—	0.55	—	—	—	W	—
	266 MHz, 32 bits	—	0.5	—	—	—	W	—
	266 MHz, 64 bits	—	0.66	—	—	—	W	—
	300 MHz,[1] 32 bits	—	0.54	—	—	—	W	—
	300 MHz,[1] 64 bits	—	0.7	—	—	—	W	—
	333 MHz,[1] 32 bits	—	0.58	—	—	—	W	—
	333 MHz,[1] 64 bits	—	0.76	—	—	—	W	—
	400 MHz,[1] 32 bits	—	—	—	—	—		—
	400 MHz,[1] 64 bits	—	—	—	—	—		—
PCI I/O load = 30 pF	33 MHz, 32 bits	—	—	0.04	—	—	W	—
	66 MHz, 32 bits	—	—	0.07	—	—	W	—
Local bus I/O load = 25 pF	167 MHz, 32 bits	—	—	0.34	—	—	W	—
	133 MHz, 32 bits	—	—	0.27	—	—	W	—
	83 MHz, 32 bits	—	—	0.17	—	—	W	—
	66 MHz, 32 bits	—	—	0.14	—	—	W	—
	50 MHz, 32 bits	—	—	0.11	—	—	W	—
TSEC I/O load = 25 pF	MII	—	—	—	0.01	—	W	Multiply by number of interfaces used.
	GMII or TBI	—	—	—	0.06	—	W	
	RGMII or RTBI	—	—	—	—	0.04	W	
USB	12 MHz	—	—	0.01	—	—	W	Multiply by 2 if using 2 ports.
	480 MHz	—	—	0.2	—	—	W	
Other I/O		—	—	0.01	—	—	W	—

[1] TBGA package only.

6.2 DDR SDRAM AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR SDRAM interface.

6.2.1 DDR SDRAM Input AC Timing Specifications

Table 13 provides the input AC timing specifications for the DDR SDRAM interface.

Table 13. DDR SDRAM Input AC Timing Specifications

At recommended operating conditions with GV_{DD} of 2.5 V ± 5%.

Parameter	Symbol	Min	Max	Unit	Notes
AC input low voltage	V_{IL}	—	MV_{REF} – 0.31	V	
AC input high voltage	V_{IH}	MV_{REF} + 0.31	GV_{DD} + 0.3	V	
MDQS—MDQ/MECC input skew per byte 333 MHz 266 MHz	t_{DISKEW}	—	 750 1125	ps	1

Note:

1. Maximum possible skew between a data strobe (MDQS[n]) and any corresponding bit of data (MDQ[8n + {0...7}] if 0 <= n <= 7) or ECC (MECC[{0...7}] if n = 8).

Figure 4 illustrates the DDR input timing diagram showing the t_{DISKEW} timing parameter.

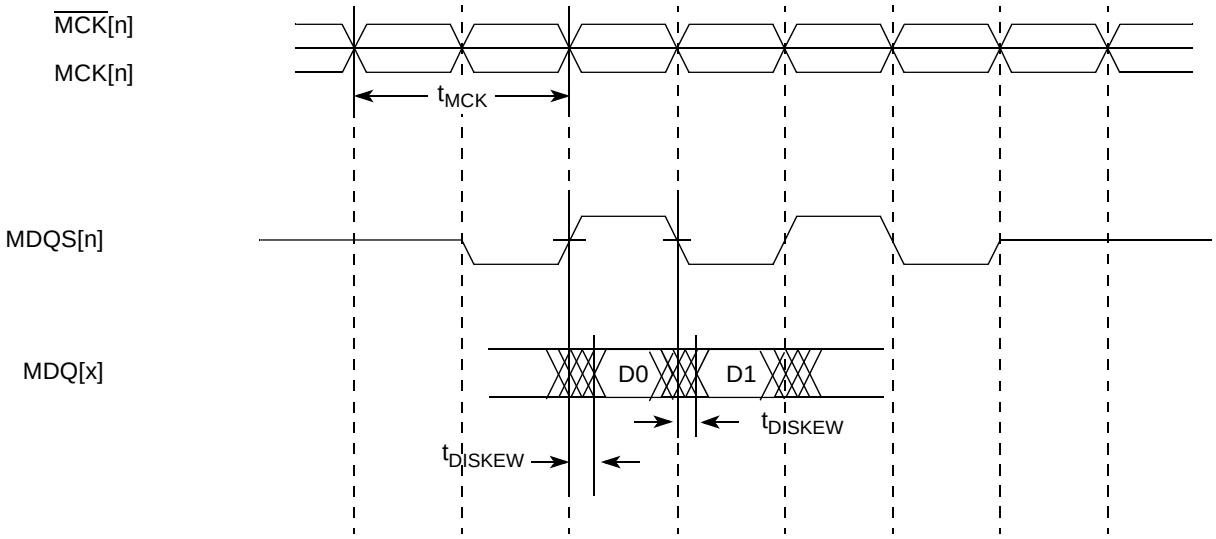


Figure 4. DDR Input Timing Diagram

6.2.2 DDR SDRAM Output AC Timing Specifications

Table 14 and Table 15 provide the output AC timing specifications and measurement conditions for the DDR SDRAM interface.

8 Ethernet: Three-Speed Ethernet, MII Management

This section provides the AC and DC electrical characteristics for three-speeds (10/100/1000 Mbps) and MII management.

8.1 Three-Speed Ethernet Controller (TSEC)— GMII/MII/TBI/RGMII/RTBI Electrical Characteristics

The electrical characteristics specified here apply to the gigabit media independent interface (GMII), the media independent interface (MII), ten-bit interface (TBI), reduced gigabit media independent interface (RGMII), and reduced ten-bit interface (RTBI) signals except management data input/output (MDIO) and management data clock (MDC). The MII, GMII, and TBI interfaces are defined for 3.3 V, and the RGMII and RTBI interfaces are defined for 2.5 V. The RGMII and RTBI interfaces follow the Hewlett-Packard *Reduced Pin-Count Interface for Gigabit Ethernet Physical Layer Device Specification*, Version 1.2a (9/22/2000). The electrical characteristics for MDIO and MDC are specified in Section 8.3, "Ethernet Management Interface Electrical Characteristics."

8.1.1 TSEC DC Electrical Characteristics

GMII, MII, TBI, RGMII, and RTBI drivers and receivers comply with the DC parametric attributes specified in Table 19 and Table 20. The RGMII and RTBI signals in Table 20 are based on a 2.5-V CMOS interface voltage as defined by JEDEC EIA/JESD8-5.

Table 19. GMII/TBI and MII DC Electrical Characteristics

Parameter	Symbol	Conditions		Min	Max	Unit
Supply voltage 3.3 V	LV_{DD}[2]	—		2.97	3.63	V
Output high voltage	V_{OH}	I_{OH} = –4.0 mA	LV_{DD} = Min	2.40	LV_{DD} + 0.3	V
Output low voltage	V_{OL}	I_{OL} = 4.0 mA	LV_{DD} = Min	GND	0.50	V
Input high voltage	V_{IH}	—	—	2.0	LV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	—	–0.3	0.90	V
Input high current	I_{IH}	V_{IN}[1] = LV_{DD}		—	40	µA
Input low current	I_{IL}	V_{IN}[1] = GND		–600	—	µA

Notes:
1. The symbol V_{IN}, in this case, represents the LV_{IN} symbol referenced in Table 1 and Table 2.
2. GMII/MII pins not needed for RGMII or RTBI operation are powered by the OV_{DD} supply.

Figure 9 shows the GMII receive AC timing diagram.

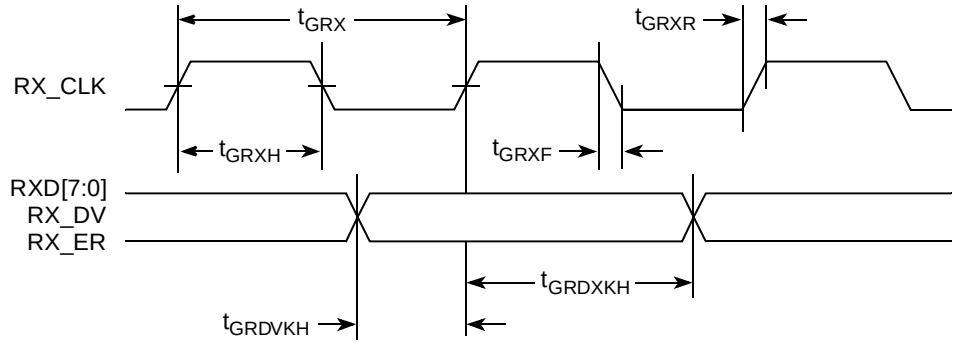


Figure 9. GMII Receive AC Timing Diagram

8.2.2 MII AC Timing Specifications

This section describes the MII transmit and receive AC timing specifications.

8.2.2.1 MII Transmit AC Timing Specifications

Table 23 provides the MII transmit AC timing specifications.

Table 23. MII Transmit AC Timing Specifications

At recommended operating conditions with LV_{DD}/OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit
TX_CLK clock period 10 Mbps	t_{MTX}	—	400	—	ns
TX_CLK clock period 100 Mbps	t_{MTX}	—	40	—	ns
TX_CLK duty cycle	t_{MTXH}/t_{MTX}	35	—	65	%
TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay	t_{MTKHDX}	1	5	15	ns
TX_CLK data clock rise V_{IL}(min) to V_{IH}(max)	t_{MTXR}	1.0	—	4.0	ns
TX_CLK data clock fall V_{IH}(max) to V_{IL}(min)	t_{MTXF}	1.0	—	4.0	ns

Note:

1. The symbols for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). In general, the clock reference symbol is based on two to three letters representing the clock of a particular function. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

17 SPI

This section describes the SPI DC and AC electrical specifications.

17.1 SPI DC Electrical Characteristics

Table 49 provides the SPI DC electrical characteristics.

Table 49. SPI DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}		2.0	OV_{DD} + 0.3	V
Input low voltage	V_{IL}		–0.3	0.8	V
Input current	I_{IN}			±5	μA
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V

17.2 SPI AC Timing Specifications

Table 50 provides the SPI input and output AC timing specifications.

Table 50. SPI AC Timing Specifications[1]

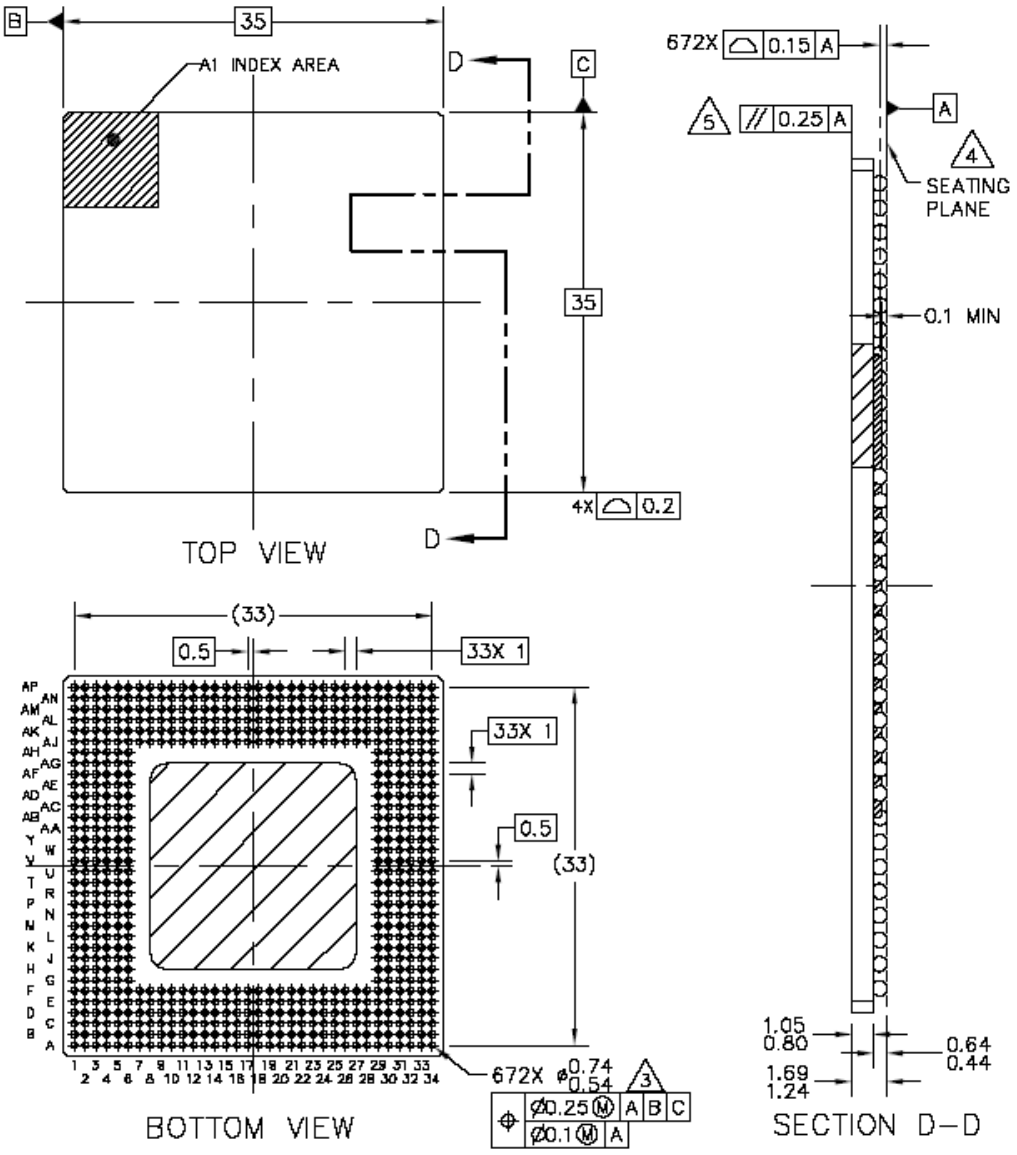
Characteristic	Symbol[2]	Min	Max	Unit
SPI outputs valid—Master mode (internal clock) delay	t_{NIKHOV}		6	ns
SPI outputs hold—Master mode (internal clock) delay	t_{NIKHOX}	0.5		ns
SPI outputs valid—Slave mode (external clock) delay	t_{NEKHOV}		8	ns
SPI outputs hold—Slave mode (external clock) delay	t_{NEKHOX}	2		ns
SPI inputs—Master mode (internal clock input setup time	t_{NIIVKH}	4		ns
SPI inputs—Master mode (internal clock input hold time	t_{NIIXKH}	0		ns
SPI inputs—Slave mode (external clock) input setup time	t_{NEIVKH}	4		ns
SPI inputs—Slave mode (external clock) input hold time	t_{NEIXKH}	2		ns

Notes:

1. Output specifications are measured from the 50 percent level of the rising edge of CLKIN to the 50 percent level of the signal. Timings are measured at the pin.
2. The symbols for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{NIKHOX} symbolizes the internal timing (NI) for the time SPICLK clock reference (K) goes to the high state (H) until outputs (O) are invalid (X).

18.2 Mechanical Dimensions for the MPC8347E TBGA

Figure 39 shows the mechanical dimensions and bottom surface nomenclature for the MPC8347E, 672-TBGA package.



Notes:

1.All dimensions are in millimeters.

2.Dimensions and tolerances per ASME Y14.5M-1994.

3.Maximum solder ball diameter measured parallel to datum A.

4.Datum A, the seating plane, is determined by the spherical crowns of the solder balls.

5.Parallelism measurement must exclude any effect of mark on top surface of package.

Figure 39. Mechanical Dimensions and Bottom Surface Nomenclature for the MPC8347E TBGA

18.3 Package Parameters for the MPC8347E PBGA

The package parameters are as provided in the following list. The package type is 29 mm × 29 mm, 620 plastic ball grid array (PBGA).

Package outline	29 mm × 29 mm
Interconnects	620
Pitch	1.00 mm
Module height (maximum)	2.46 mm
Module height (typical)	2.23 mm
Module height (minimum)	2.00 mm
Solder balls	62 Sn/36 Pb/2 Ag (ZQ package) 95.5 Sn/0.5 Cu/4Ag (VR package)
Ball diameter (typical)	0.60 mm

Table 51. MPC8347E (TBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
DUART				
UART_SOUT[1:2]/MSRCID[0:1]/LSRCID[0:1]	AK27, AN29	O	OV_{DD}	
UART_SIN[1:2]/MSRCID[2:3]/LSRCID[2:3]	AL28, AM29	I/O	OV_{DD}	
$\overline{\text{UART\_CTS}}$[1]/MSRCID4/LSRCID4	AP30	I/O	OV_{DD}	
$\overline{\text{UART\_CTS}}$[2]/MDVAL/ LDVAL	AN30	I/O	OV_{DD}	
$\overline{\text{UART\_RTS}}$[1:2]	AP31, AM30	O	OV_{DD}	
I^2C interface				
IIC1_SDA	AK29	I/O	OV_{DD}	2
IIC1_SCL	AP32	I/O	OV_{DD}	2
IIC2_SDA	AN31	I/O	OV_{DD}	2
IIC2_SCL	AM31	I/O	OV_{DD}	2
SPI				
SPIMOSI	AN32	I/O	OV_{DD}	
SPIMISO	AP33	I/O	OV_{DD}	
SPICLK	AK30	I/O	OV_{DD}	
SPISEL	AL31	I	OV_{DD}	
Clocks				
PCI_CLK_OUT[0:4]	AN9, AP9, AM10, AN10, AJ11	O	OV_{DD}	
PCI_SYNC_IN/PCI_CLOCK	AK12	I	OV_{DD}	
PCI_SYNC_OUT	AP11	O	OV_{DD}	3
RTC/PIT_CLOCK	AM32	I	OV_{DD}	
CLKIN	AM9	I	OV_{DD}	
JTAG				
TCK	E20	I	OV_{DD}	
TDI	F20	I	OV_{DD}	4
TDO	B20	O	OV_{DD}	3
TMS	A20	I	OV_{DD}	4
$\overline{\text{TRST}}$	B19	I	OV_{DD}	4
Test				
TEST	D22	I	OV_{DD}	6
TEST_SEL	AL13	I	OV_{DD}	7
PMC				
$\overline{\text{QUIESCE}}$	A18	O	OV_{DD}	

Table 51. MPC8347E (TBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
$LV_{DD}2$	C6, D9	Power for three-speed Ethernet #2 I/O (2.5 V, 3.3 V)	$LV_{DD}2$	
V_{DD}	E19, E29, F7, F9, F11,F13, F15, F17, F18, F21, F23, F25, F29, H29, J6, K29, M29, N6, P29, T29, U30, V6, V29, W29, AB29, AC5, AD29, AF6, AF29, AH29, AJ8, AJ12, AJ14, AJ16, AJ18, AJ20, AJ21, AJ23, AJ25, AJ26, AJ27, AJ28, AJ29, AK10	Power for core (1.2 V)	V_{DD}	
OV_{DD}	B22, B28, C16, C17, C24, C26, D13, D15, D19, D29, E31, F28, G33, H30, L29, L32, N32, P31, R31, U32, W31, Y29, AA29, AC30, AE31, AF30, AG29, AJ17, AJ30, AK11, AL15, AL19, AL21, AL29, AL30, AM20, AM23, AM24, AM26, AM28, AN11, AN13	PCI, 10/100 Ethernet, and other standard (3.3 V)	OV_{DD}	
MVREF1	M3	I	DDR reference voltage	
MVREF2	AD2	I	DDR reference voltage	

Table 52. MPC8347E (PBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PCI1_IRDY	E13	I/O	OV_{DD}	5
PCI1_STOP	C13	I/O	OV_{DD}	5
PCI1_DEVSEL	B13	I/O	OV_{DD}	5
PCI1_IDSEL	C17	I	OV_{DD}	
PCI1_SERR	C12	I/O	OV_{DD}	5
PCI1_PERR	B12	I/O	OV_{DD}	5
PCI1_REQ[0]	A21	I/O	OV_{DD}	
PCI1_REQ[1]/CPCI1_HS_ES	C19	I	OV_{DD}	
PCI1_REQ[2:4]	C18, A19, E20	I	OV_{DD}	
PCI1_GNT0	B20	I/O	OV_{DD}	
PCI1_GNT1/CPCI1_HS_LED	C20	O	OV_{DD}	
PCI1_GNT2/CPCI1_HS_ENUM	B19	O	OV_{DD}	
PCI1_GNT[3:4]	A20, E18	O	OV_{DD}	
M66EN	L26	I	OV_{DD}	
DDR SDRAM Memory Interface				
MDQ[0:63]	AC25, AD27, AD25, AH27, AE28, AD26, AD24, AF27, AF25, AF28, AH24, AG26, AE25, AG25, AH26, AH25, AG22, AH22, AE21, AD19, AE22, AF23, AE19, AG20, AG19, AD17, AE16, AF16, AF18, AG18, AH17, AH16, AG9, AD12, AG7, AE8, AD11, AH9, AH8, AF6, AF8, AE6, AF1, AE4, AG8, AH3, AG3, AG4, AH2, AD7, AB4, AB3, AG1, AD5, AC2, AC1, AC4, AA3, Y4, AA4, AB1, AB2, Y5, Y3	I/O	GV_{DD}	
MECC[0:4]/MSRCID[0:4]	AG13, AE14, AH12, AH10, AE15	I/O	GV_{DD}	
MECC[5]/MDVAL	AH14	I/O	GV_{DD}	
MECC[6:7]	AE13, AH11	I/O	GV_{DD}	
MDM[0:8]	AG28, AG24, AF20, AG17, AE9, AH5, AD1, AA2, AG12	O	GV_{DD}	
MDQS[0:8]	AE27, AE26, AE20, AH18, AG10, AF5, AC3, AA1, AH13	I/O	GV_{DD}	
MBA[0:1]	AF10, AF11	O	GV_{DD}	
MA[0:14]	AF13, AF15, AG16, AD16, AF17, AH20, AH19, AH21, AD18, AG21, AD13, AF21, AF22, AE1, AA5	O	GV_{DD}	
MWE	AD10	O	GV_{DD}	
MRAS	AF7	O	GV_{DD}	

Table 52. MPC8347E (PBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
$\overline{\text{MCAS}}$	AG6	O	GV_{DD}	
$\overline{\text{MCS}}$[0:3]	AE7, AH7, AH4, AF2	O	GV_{DD}	
MCKE[0:1]	AG23, AH23	O	GV_{DD}	3
MCK[0:5]	AH15, AE24, AE2, AF14, AE23, AD3	O	GV_{DD}	
$\overline{\text{MCK}}$[0:5]	AG15, AD23, AE3, AG14, AF24, AD2	O	GV_{DD}	
Pins Reserved for Future DDR2 (They should be left unconnected for MPC8347)				
MODT[0:3]	AG5, AD4, AH6, AF4	—	—	
MBA[2]	AD22			
SPARE1	AF12	—	—	7
SPARE2	AG11	—	—	6
Local Bus Controller Interface				
LAD[0:31]	T4, T5, T1, R2, R3, T2, R1, R4, P1, P2, P3, P4, N1, N4, N2, N3, M1, M2, M3, N5, M4, L1, L2, L3, K1, M5, K2, K3, J1, J2, L5, J3	I/O	OV_{DD}	
LDP[0]/$\overline{\text{CKSTOP\_OUT}}$	H1	I/O	OV_{DD}	
LDP[1]/$\overline{\text{CKSTOP\_IN}}$	K5	I/O	OV_{DD}	
LDP[2]	H2	I/O	OV_{DD}	
LDP[3]	G1	I/O	OV_{DD}	
LA[27:31]	J4, H3, G2, F1, G3	O	OV_{DD}	
$\overline{\text{LCS}}$[0:3]	J5, H4, F2, E1	O	OV_{DD}	
$\overline{\text{LWE}}$[0:3]/LSDDQM[0:3]/$\overline{\text{LBS}}$[0:3]	F3, G4, D1, E2	O	OV_{DD}	
LBCTL	H5	O	OV_{DD}	
LALE	E3	O	OV_{DD}	
LGPL0/LSDA10/cfg_reset_source0	F4	I/O	OV_{DD}	
LGPL1/$\overline{\text{LSDWE}}$/cfg_reset_source1	D2	I/O	OV_{DD}	
LGPL2/$\overline{\text{LSDRAS}}$/$\overline{\text{LOE}}$	C1	O	OV_{DD}	
LGPL3/$\overline{\text{LSDCAS}}$/cfg_reset_source2	C2	I/O	OV_{DD}	
LGPL4/$\overline{\text{LGTA}}$/LUPWAIT/LPBSE	C3	I/O	OV_{DD}	
LGPL5/cfg_clkin_div	B3	I/O	OV_{DD}	
LCKE	E4	O	OV_{DD}	
LCLK[0:2]	D4, A3, C4	O	OV_{DD}	
LSYNC_OUT	U3	O	OV_{DD}	
LSYNC_IN	Y2	I	OV_{DD}	

Table 52. MPC8347E (PBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
SPIMISO	C7	I/O	OV_{DD}	
SPICLK	B7	I/O	OV_{DD}	
SPISEL	A7	I	OV_{DD}	
Clocks				
PCI_CLK_OUT[0:2]	Y1, W3, W2	O	OV_{DD}	
PCI_CLK_OUT[3]/$\overline{\text{LCS}}$[6]	W1	O	OV_{DD}	
PCI_CLK_OUT[4]/$\overline{\text{LCS}}$[7]	V3	O	OV_{DD}	
PCI_SYNC_IN/PCI_CLOCK	U4	I	OV_{DD}	
PCI_SYNC_OUT	U5	O	OV_{DD}	3
RTC/PIT_CLOCK	E9	I	OV_{DD}	
CLKIN	W5	I	OV_{DD}	
JTAG				
TCK	H27	I	OV_{DD}	
TDI	H28	I	OV_{DD}	4
TDO	M24	O	OV_{DD}	3
TMS	J27	I	OV_{DD}	4
$\overline{\text{TRST}}$	K26	I	OV_{DD}	4
Test				
TEST	F28	I	OV_{DD}	6
TEST_SEL	T3	I	OV_{DD}	6
PMC				
$\overline{\text{QUIESCE}}$	K27	O	OV_{DD}	
System Control				
$\overline{\text{PORESET}}$	K28	I	OV_{DD}	
$\overline{\text{HRESET}}$	M25	I/O	OV_{DD}	1
$\overline{\text{SRESET}}$	L27	I/O	OV_{DD}	2
Thermal Management				
THERM0	B15	I	—	8
Power and Ground Signals				
$AV_{DD}1$	C15	Power for e300 PLL (1.2 V)	$AV_{DD}1$	
$AV_{DD}2$	U1	Power for system PLL (1.2 V)	$AV_{DD}2$	

Table 57. CSB Frequency Options for Host Mode

CFG_CLKIN_DIV at Reset[1]	SPMF	*csb_clk* : Input Clock Ratio[2]	Input Clock Frequency (MHz)[2]			
			16.67	25	33.33	66.67
			csb_clk Frequency (MHz)			
Low	0010	2 : 1				133
Low	0011	3 : 1			100	200
Low	0100	4 : 1		100	133	266
Low	0101	5 : 1		125	166	333
Low	0110	6 : 1	100	150	200	
Low	0111	7 : 1	116	175	233	
Low	1000	8 : 1	133	200	266	
Low	1001	9 : 1	150	225	300	
Low	1010	10 : 1	166	250	333	
Low	1011	11 : 1	183	275		
Low	1100	12 : 1	200	300		
Low	1101	13 : 1	216	325		
Low	1110	14 : 1	233			
Low	1111	15 : 1	250			
Low	0000	16 : 1	266			
High	0010	2 : 1				133
High	0011	3 : 1			100	200
High	0100	4 : 1			133	266
High	0101	5 : 1			166	333
High	0110	6 : 1			200	
High	0111	7 : 1			233	
High	1000	8 : 1				

1 CFG_CLKIN_DIV selects the ratio between CLKIN and PCI_SYNC_OUT.

2 CLKIN is the input clock in host mode; PCI_CLK is the input clock in agent mode.
DDR2 memory may be used at 133 MHz provided that the memory components are specified for operation at this frequency.

Table 58. CSB Frequency Options for Agent Mode

CFG_CLKIN_DIV at Reset[1]	SPMF	*csb_clk* : Input Clock Ratio[2]	Input Clock Frequency (MHz)[2]			
			16.67	25	33.33	66.67
			csb_clk Frequency (MHz)			
Low	0010	2 : 1				133
Low	0011	3 : 1			100	200
Low	0100	4 : 1		100	133	266
Low	0101	5 : 1		125	166	333
Low	0110	6 : 1	100	150	200	
Low	0111	7 : 1	116	175	233	
Low	1000	8 : 1	133	200	266	
Low	1001	9 : 1	150	225	300	
Low	1010	10 : 1	166	250	333	
Low	1011	11 : 1	183	275		
Low	1100	12 : 1	200	300		
Low	1101	13 : 1	216	325		
Low	1110	14 : 1	233			
Low	1111	15 : 1	250			
Low	0000	16 : 1	266			
High	0010	4 : 1		100	133	266
High	0011	6 : 1	100	150	200	
High	0100	8 : 1	133	200	266	
High	0101	10 : 1	166	250	333	
High	0110	12 : 1	200	300		
High	0111	14 : 1	233			
High	1000	16 : 1	266			

1 CFG_CLKIN_DIV doubles csb_clk if set high.

2 CLKIN is the input clock in host mode; PCI_CLK is the input clock in agent mode.
DDR2 memory may be used at 133 MHz provided that the memory components are specified for operation at this frequency.

19.2 Core PLL Configuration

RCWL[COREPLL] selects the ratio between the internal coherent system bus clock (*csb_clk*) and the e300 core clock (*core_clk*). Table 59 shows the encodings for RCWL[COREPLL]. COREPLL values that are not listed in Table 59 should be considered as reserved.

Table 62. Package Thermal Characteristics for PBGA (continued)

Characteristic	Symbol	Value	Unit	Notes
Junction-to-case thermal	$R_{\theta JC}$	5	°C/W	5
Junction-to-package natural convection on top	ψ_{JT}	5	°C/W	6

Notes

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single-layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

20.2 Thermal Management Information

For the following sections, $P_D = (V_{DD} \times I_{DD}) + P_{I/O}$ where $P_{I/O}$ is the power dissipation of the I/O drivers. See Table 5 for I/O power dissipation values.

20.2.1 Estimation of Junction Temperature with Junction-to-Ambient Thermal Resistance

An estimation of the chip junction temperature, T_J, can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

T_J = junction temperature (°C)

T_A = ambient temperature for the package (°C)

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

P_D = power dissipation in the package (W)

The junction-to-ambient thermal resistance is an industry-standard value that provides a quick and easy estimation of thermal performance. Generally, the value obtained on a single-layer board is appropriate for a tightly packed printed-circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated. Test cases have demonstrated that errors of a factor of two (in the quantity $T_J - T_A$) are possible.

20.2.2 Estimation of Junction Temperature with Junction-to-Board Thermal Resistance

The thermal performance of a device cannot be adequately predicted from the junction-to-ambient thermal resistance. The thermal performance of any component is strongly dependent on the power dissipation of surrounding components. In addition, the ambient temperature varies widely within the application. For

Tyco Electronics Chip Coolers™ P.O. Box 3668 Harrisburg, PA 17105-3668 Internet: www.chipcoolers.com	800-522-2800
Wakefield Engineering 33 Bridge St. Pelham, NH 03076 Internet: www.wakefield.com	603-635-5102

Interface material vendors include the following:

Chomerics, Inc. 77 Dragon Ct. Woburn, MA 01801 Internet: www.chomerics.com	781-935-4850
Dow-Corning Corporation Dow-Corning Electronic Materials P.O. Box 994 Midland, MI 48686-0997 Internet: www.dowcorning.com	800-248-2481
Shin-Etsu MicroSi, Inc. 10028 S. 51st St. Phoenix, AZ 85044 Internet: www.microsi.com	888-642-7674
The Bergquist Company 18930 West 78th St. Chanhassen, MN 55317 Internet: www.bergquistcompany.com	800-347-4572

20.3 Heat Sink Attachment

When heat sinks are attached, an interface material is required, preferably thermal grease and a spring clip. The spring clip should connect to the printed-circuit board, either to the board itself, to hooks soldered to the board, or to a plastic stiffener. Avoid attachment forces that can lift the edge of the package or peel the package from the board. Such peeling forces reduce the solder joint lifetime of the package. The recommended maximum force on the top of the package is 10 lb force (4.5 kg force). Any adhesive attachment should attach to painted or plastic surfaces, and its performance should be verified under the application requirements.

20.3.1 Experimental Determination of the Junction Temperature with a Heat Sink

When a heat sink is used, the junction temperature is determined from a thermocouple inserted at the interface between the case of the package and the interface material. A clearance slot or hole is normally

21.3 Decoupling Recommendations

Due to large address and data buses and high operating frequencies, the MPC8347E can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the MPC8347E system, and the MPC8347E itself requires a clean, tightly regulated source of power. Therefore, the system designer should place at least one decoupling capacitor at each V_{DD}, OV_{DD}, GV_{DD}, and LV_{DD} pin of the MPC8347E. These capacitors should receive their power from separate V_{DD}, OV_{DD}, GV_{DD}, LV_{DD}, and GND power planes in the PCB, with short traces to minimize inductance. Capacitors can be placed directly under the device using a standard escape pattern. Others can surround the part.

These capacitors should have a value of 0.01 or 0.1 µF. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0402 or 0603 sizes.

In addition, distribute several bulk storage capacitors around the PCB, feeding the V_{DD}, OV_{DD}, GV_{DD}, and LV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors are 100–330 µF (AVX TPS tantalum or Sanyo OSCON).

21.4 Connection Recommendations

To ensure reliable operation, connect unused inputs to an appropriate signal level. Unused active low inputs should be tied to OV_{DD}, GV_{DD}, or LV_{DD} as required. Unused active high inputs should be connected to GND. All NC (no-connect) signals must remain unconnected.

Power and ground connections must be made to all external V_{DD}, GV_{DD}, LV_{DD}, OV_{DD}, and GND pins of the MPC8347E.

21.5 Output Buffer DC Impedance

The MPC8347E drivers are characterized over process, voltage, and temperature. For all buses, the driver is a push-pull single-ended driver type (open drain for I^2C).

To measure Z_0 for the single-ended drivers, an external resistor is connected from the chip pad to OV_{DD} or GND. Then the value of each resistor is varied until the pad voltage is $OV_{DD}/2$ (see Figure 43). The output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held high, SW1 is closed (SW2 is open) and R_P is trimmed until the voltage at the pad equals $OV_{DD}/2$. R_P then becomes the resistance of the pull-up devices. R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N)/2$.

the large value of the pull-up/pull-down resistor should minimize the disruption of signal quality or speed for the output pins.

21.7 Pull-Up Resistor Requirements

The MPC8347E requires high resistance pull-up resistors (10 kΩ is recommended) on open-drain pins, including I^2C pins, the Ethernet Management MDIO pin, and IPIC interrupt pins.

For more information on required pull-up resistors and the connections required for the JTAG interface, refer to application note AN2931, *PowerQUICC™ Design Checklist*.

22 Document Revision History

Table 66 provides a revision history of this document.

Table 66. Document Revision History

Revision	Date	Substantive Change(s)
11	2/2009	In Section 21.1, "System Clocking," removed "(AVDD1)" and "(AVDD2") from bulleted list. In Section 21.2, "PLL Power Supply Filtering," in the second paragraph, changed "provide five independent filter circuits," and "the five AVDD pins" to provide four independent filter circuits," and "the four AVDD pins." In Table 35, removed row for rise time (t_{I2CR}). Removed minimum value of t_{I2CF}. Added note 5 stating that the device does not follow the I2C-BUS Specifications version 2.1 regarding the t_{I2CF} AC parameter. In Table 54, corrected the max csb_clk to 266 MHz. In Table 60, added PLL configurations 903, 923, A03, A23, and 503 for 533 MHz In Table 35, corrected t_{LBKHOV} parametr to t_{LBKLOV} (output data is driven on falling edge of clock in DLL bypass mode). Similarly, made the same correction to Figure 21, Figure 23, and Figure 24 for output signals. Added Figure 1 and Figure 4. In Table 9.2, clarified that AC table is for ULPI only. Added footnote 4 to Table 67. In Table 67, updated note 1 to say the following: "For temperature range = C, processor frequency is up to 667(TBGA) with a platform frequency of 333 and limited to 400 (PBGA) with a platform frequency of 266." Added footnote 10 and 11 to Table 51 and Table 52. In Table 51, Table 52, updated note 11 to say the following: "SEC1_TXD[3] is required an external pull-up resistor. For proper functionality of the device, this pin must be pulled up or actively driven high during a hard reset. No external pull-down resistors are allowed to be attached to this net." Added footnote 6 to Table 7. In Table 7, updated the note 6 to say the following: "The Spread spectrum clocking. Is allowed with 1% input frequency down-spread at maximum 50KHz modulation rate regardless of input frequency." In 8.1.1, removed the note "The potential applied to the input of a GMII, MII, TBI, RGMII, or RTBI receiver may exceed the potential of the receiver power supply (that is, a RGMII driver powered from a 3.6 V supply driving VOH into a RGMII receiver powered from a 2.5-V supply). Tolerance for dissimilar RGMII driver and receiver supply potentials is implicit in these specifications."
10	4/2007	In Table 3, "Output Drive Capability," changed the values in the Output Impedance column and added USB to the seventh row. In Table 54, "Operating Frequencies for TBGA," added column for 400 MHz. In Section 21.7, "Pull-Up Resistor Requirements," deleted last two paragraphs and after first paragraph, added a new paragraph. Deleted Section 21.8, "JTAG Configuration Signals," and Figure 43, "JTAG Interface Connection."
9	3/2007	In Table 54, "Operating Frequencies for TBGA," in the 'Coherent system bus frequency (*csb_clk*)' row, changed the value in the 533 MHz column to 100–333. In Table 60, "Suggested PLL Configurations," under the subhead, '33 MHz CLKIN/PCI_CLK Options,' added row A03 between Ref. No. 724 and 804. Under the subhead '66 MHz CLKIN/PCI_CLK Options,' added row 503 between Ref. No. 305 and 404. For Ref. No. 306, changed the CORE PLL value to 0000110. In Section 23, "Ordering Information," replaced first paragraph and added a note. In Section 23.1, "Part Numbers Fully Addressed by This Document," replaced first paragraph.