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Understanding [Embedded - Microprocessors](#)

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e300
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	533MHz
Co-Processors/DSP	-
RAM Controllers	DDR
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	-
Package / Case	672-LBGA
Supplier Device Package	672-LBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8347cvvajfb

- On-the-fly power management using CKE
- Registered DIMM support
- 2.5-V SSTL2 compatible I/O
- Dual three-speed (10/100/1000) Ethernet controllers (TSECs)
 - Dual controllers designed to comply with IEEE 802.3®, 802.3u®, 802.3x®, 802.3z®, 802.3ac® standards
 - Ethernet physical interfaces:
 - 1000 Mbps IEEE Std. 802.3 GMII/RGMII, IEEE Std. 802.3z TBI/RTBI, full-duplex
 - 10/100 Mbps IEEE Std. 802.3 MII full- and half-duplex
 - Buffer descriptors are backward-compatible with MPC8260 and MPC860T 10/100 programming models
 - 9.6-Kbyte jumbo frame support
 - RMON statistics support
 - Internal 2-Kbyte transmit and 2-Kbyte receive FIFOs per TSEC module
 - MII management interface for control and status
 - Programmable CRC generation and checking
- PCI interface
 - Designed to comply with *PCI Specification Revision 2.2*
 - Data bus width:
 - 32-bit data PCI interface operating at up to 66 MHz
 - PCI 3.3-V compatible
 - PCI host bridge capabilities
 - PCI agent mode on PCI interface
 - PCI-to-memory and memory-to-PCI streaming
 - Memory prefetching of PCI read accesses and support for delayed read transactions
 - Posting of processor-to-PCI and PCI-to-memory writes
 - On-chip arbitration supporting five masters on PCI
 - Accesses to all PCI address spaces
 - Parity supported
 - Selectable hardware-enforced coherency
 - Address translation units for address mapping between host and peripheral
 - Dual address cycle for target
 - Internal configuration registers accessible from PCI
- Security engine is optimized to handle all the algorithms associated with IPSec, SSL/TLS, SRTP, IEEE Std. 802.11i®, iSCSI, and IKE processing. The security engine contains four crypto-channels, a controller, and a set of crypto execution units (EUs):
 - Public key execution unit (PKEU) :
 - RSA and Diffie-Hellman algorithms

- Programmable field size up to 2048 bits
 - Elliptic curve cryptography
 - F2m and F(p) modes
 - Programmable field size up to 511 bits
- Data encryption standard (DES) execution unit (DEU)
 - DES and 3DES algorithms
 - Two key (K1, K2) or three key (K1, K2, K3) for 3DES
 - ECB and CBC modes for both DES and 3DES
- Advanced encryption standard unit (AESU)
 - Implements the Rijndael symmetric-key cipher
 - Key lengths of 128, 192, and 256 bits
 - ECB, CBC, CCM, and counter (CTR) modes
- ARC four execution unit (AFEU)
 - Stream cipher compatible with the RC4 algorithm
 - 40- to 128-bit programmable key
- Message digest execution unit (MDEU)
 - SHA with 160- or 256-bit message digest
 - MD5 with 128-bit message digest
 - HMAC with either algorithm
- Random number generator (RNG)
- Four crypto-channels, each supporting multi-command descriptor chains
 - Static and/or dynamic assignment of crypto-execution units through an integrated controller
 - Buffer size of 256 bytes for each execution unit, with flow control for large data sizes
- Universal serial bus (USB) dual role controller
 - USB on-the-go mode with both device and host functionality
 - Complies with USB specification Rev. 2.0
 - Can operate as a stand-alone USB device
 - One upstream facing port
 - Six programmable USB endpoints
 - Can operate as a stand-alone USB host controller
 - USB root hub with one downstream-facing port
 - Enhanced host controller interface (EHCI) compatible
 - High-speed (480 Mbps), full-speed (12 Mbps), and low-speed (1.5 Mbps) operations
 - External PHY with UTMI, serial and UTMI+ low-pin interface (ULPI)
- Universal serial bus (USB) multi-port host controller
 - Can operate as a stand-alone USB host controller
 - USB root hub with one or two downstream-facing ports

4 Clock Input Timing

This section provides the clock input DC and AC electrical characteristics for the MPC8347E.

4.1 DC Electrical Characteristics

Table 7 provides the clock input (CLKIN/PCI_SYNC_IN) DC timing specifications for the MPC8347E.

Table 6. CLKIN DC Timing Specifications

Parameter	Condition	Symbol	Min	Max	Unit
Input high voltage	—	V_{IH}	2.7	$OV_{DD} + 0.3$	V
Input low voltage	—	V_{IL}	−0.3	0.4	V
CLKIN input current	$0\text{ V} \leq V_{IN} \leq OV_{DD}$	I_{IN}	—	±10	μA
PCI_SYNC_IN input current	$0\text{ V} \leq V_{IN} \leq 0.5\text{ V}$ or $OV_{DD} - 0.5\text{ V} \leq V_{IN} \leq OV_{DD}$	I_{IN}	—	±10	μA
PCI_SYNC_IN input current	$0.5\text{ V} \leq V_{IN} \leq OV_{DD} - 0.5\text{ V}$	I_{IN}	—	±50	μA

4.2 AC Electrical Characteristics

The primary clock source for the MPC8347E can be one of two inputs, CLKIN or PCI_CLK, depending on whether the device is configured in PCI host or PCI agent mode. Table 7 provides the clock input (CLKIN/PCI_CLK) AC timing specifications for the MPC8347E.

Table 7. CLKIN AC Timing Specifications

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
CLKIN/PCI_CLK frequency	f_{CLKIN}	—	—	66	MHz	1, 6
CLKIN/PCI_CLK cycle time	t_{CLKIN}	15	—	—	ns	—
CLKIN/PCI_CLK rise and fall time	t_{KH}, t_{KL}	0.6	1.0	2.3	ns	2
CLKIN/PCI_CLK duty cycle	t_{KH}/t_{CLKIN}	40	—	60	%	3
CLKIN/PCI_CLK jitter	—	—	—	±150	ps	4, 5

Notes:

- Caution:** The system, core, USB, security, and TSEC must not exceed their respective maximum or minimum operating frequencies.
- Rise and fall times for CLKIN/PCI_CLK are measured at 0.4 and 2.7 V.
- Timing is guaranteed by design and characterization.
- This represents the total input jitter—short term and long term—and is guaranteed by design.
- The CLKIN/PCI_CLK driver's closed loop jitter bandwidth should be <500 kHz at −20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track CLKIN drivers with the specified jitter.
- The Spread spectrum clocking. Is allowed with 1% input frequency down-spread at maximum 50KHz modulation rate regardless of input frequency.

6 DDR SDRAM

This section describes the DC and AC electrical specifications for the DDR SDRAM interface of the MPC8347E.

NOTE

The information in this document is accurate for revision 1.1 silicon and earlier. For information on revision 3.0 silicon and earlier versions see the *MPC8347EA PowerQUICC™ II Pro Integrated Host Processor Hardware Specifications*. See [Section 23.1, “Part Numbers Fully Addressed by This Document,”](#) for silicon revision level determination.

6.1 DDR SDRAM DC Electrical Characteristics

[Table 11](#) provides the recommended operating conditions for the DDR SDRAM component(s) of the MPC8347E.

Table 11. DDR SDRAM DC Electrical Characteristics

Parameter/Condition	Symbol	Min	Max	Unit	Notes
I/O supply voltage	GV_{DD}	2.375	2.625	V	1
I/O reference voltage	MV_{REF}	$0.49 \times GV_{DD}$	$0.51 \times GV_{DD}$	V	2
I/O termination voltage	V_{TT}	$MV_{REF} - 0.04$	$MV_{REF} + 0.04$	V	3
Input high voltage	V_{IH}	$MV_{REF} + 0.18$	$GV_{DD} + 0.3$	V	
Input low voltage	V_{IL}	-0.3	$MV_{REF} - 0.18$	V	
Output leakage current	I_{OZ}	-10	10	μA	4
Output high current ($V_{OUT} = 1.95$ V)	I_{OH}	-15.2	—	mA	
Output low current ($V_{OUT} = 0.35$ V)	I_{OL}	15.2	—	mA	
MV_{REF} input leakage current	I_{VREF}	—	5	μA	

Notes:

- GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.
- MV_{REF} is expected to be equal to $0.5 \times GV_{DD}$, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed $\pm 2\%$ of the DC value.
- V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF} . This rail should track variations in the DC level of MV_{REF} .
- Output leakage is measured with all outputs disabled, $0 \text{ V} \leq V_{OUT} \leq GV_{DD}$.

[Table 12](#) provides the DDR capacitance.

Table 12. DDR SDRAM Capacitance

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input/output capacitance: DQ, DQS	C_{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS	C_{DIO}	—	0.5	pF	1

Note:

- This parameter is sampled. $GV_{DD} = 2.5 \text{ V} \pm 0.125 \text{ V}$, $f = 1 \text{ MHz}$, $T_A = 25^\circ\text{C}$, $V_{OUT} = GV_{DD}/2$, V_{OUT} (peak-to-peak) = 0.2 V.

Table 16. Expected Delays for Address/Command

Load	Delay	Unit
4 devices (12 pF)	3.0	ns
9 devices (27 pF)	3.6	ns
36 devices (108 pF) + 40 pF compensation capacitor	5.0	ns
36 devices (108 pF) + 80 pF compensation capacitor	5.2	ns

Figure 14 shows the TBI receive AC timing diagram.

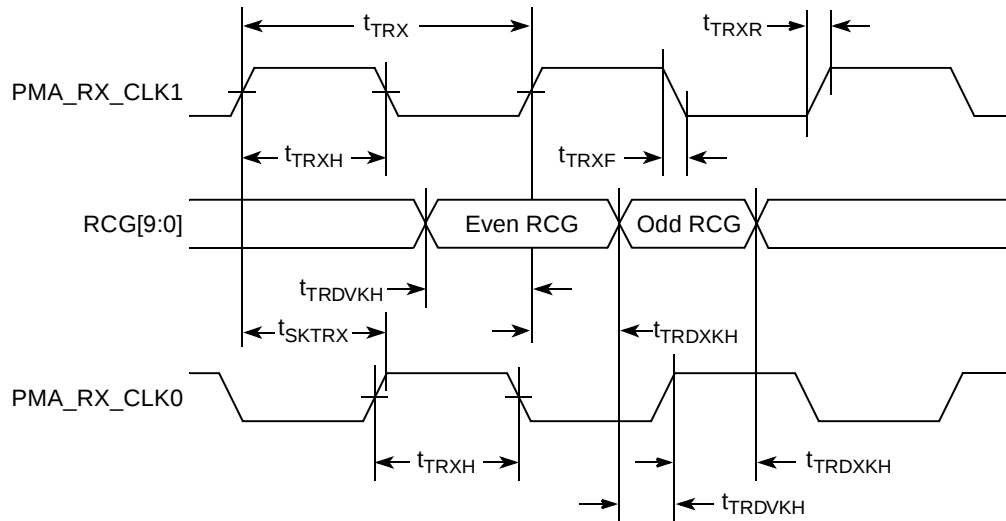


Figure 14. TBI Receive AC Timing Diagram

8.2.4 RGMII and RTBI AC Timing Specifications

Table 27 presents the RGMII and RTBI AC timing specifications.

Table 27. RGMII and RTBI AC Timing Specifications

At recommended operating conditions with V_{DD} of $2.5\text{ V} \pm 5\%$.

Parameter/Condition	Symbol ¹	Min	Typ	Max	Unit
Data to clock output skew (at transmitter)	t_{SKRGT}	-0.5	—	0.5	ns
Data to clock input skew (at receiver) ²	t_{SKRGT}	1.0	—	2.8	ns
Clock cycle duration ³	t_{RGT}	7.2	8.0	8.8	ns
Duty cycle for 1000Base-T ^{4, 5}	t_{RGTH}/t_{RGTF}	45	50	55	%
Duty cycle for 10BASE-T and 100BASE-TX ^{3, 5}	t_{RGTH}/t_{RGT}	40	50	60	%
Rise time (20%–80%)	t_{RGTR}	—	—	0.75	ns
Fall time (20%–80%)	t_{RGTF}	—	—	0.75	ns
GTX_CLK125 reference clock period	t_{G12}^6	—	8.0	—	ns
GTX_CLK125 reference clock duty cycle	t_{G125H}/t_{G125}	47	—	53	%

Notes:

- In general, the clock reference symbol for this section is based on the symbols RGT to represent RGMII and RTBI timing. For example, the subscript of t_{RGT} represents the TBI (T) receive (RX) clock. Also, the notation for rise (R) and fall (F) times follows the clock symbol. For symbols representing skews, the subscript is SK followed by the clock being skewed (RGT).
- This implies that PC board design requires clocks to be routed so that an additional trace delay of greater than 1.5 ns is added to the associated clock signal.
- For 10 and 100 Mbps, t_{RGT} scales to $400\text{ ns} \pm 40\text{ ns}$ and $40\text{ ns} \pm 4\text{ ns}$, respectively.
- Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned.
- Duty cycle reference is $V_{DD}/2$.
- This symbol represents the external GTX_CLK125 and does not follow the original symbol naming convention.

8.3 Ethernet Management Interface Electrical Characteristics

The electrical characteristics specified here apply to the MII management interface signals management data input/output (MDIO) and management data clock (MDC). The electrical characteristics for GMII, RGMII, TBI and RTBI are specified in [Section 8.1, “Three-Speed Ethernet Controller \(TSEC\)—GMII/MII/TBI/RGMII/RTBI Electrical Characteristics.”](#)

8.3.1 MII Management DC Electrical Characteristics

The MDC and MDIO are defined to operate at a supply voltage of 2.5 or 3.3 V. The DC electrical characteristics for MDIO and MDC are provided in [Table 28](#) and [Table 29](#).

Table 28. MII Management DC Electrical Characteristics Powered at 2.5 V

Parameter	Symbol	Conditions		Min	Max	Unit
Supply voltage (2.5 V)	V_{DD}	—		2.37	2.63	V
Output high voltage	V_{OH}	$I_{OH} = -1.0 \text{ mA}$	$V_{DD} = \text{Min}$	2.00	$V_{DD} + 0.3$	V
Output low voltage	V_{OL}	$I_{OL} = 1.0 \text{ mA}$	$V_{DD} = \text{Min}$	$\text{GND} - 0.3$	0.40	V
Input high voltage	V_{IH}	—	$V_{DD} = \text{Min}$	1.7	—	V
Input low voltage	V_{IL}	—	$V_{DD} = \text{Min}$	-0.3	0.70	V
Input high current	I_{IH}	$V_{IN}^1 = V_{DD}$		—	10	μA
Input low current	I_{IL}	$V_{IN} = V_{DD}$		-15	—	μA

Note:

1. The symbol V_{IN} , in this case, represents the V_{IN} symbol referenced in [Table 1](#) and [Table 2](#).

Table 29. MII Management DC Electrical Characteristics Powered at 3.3 V

Parameter	Symbol	Conditions		Min	Max	Unit
Supply voltage (3.3 V)	V_{DD}	—		2.97	3.63	V
Output high voltage	V_{OH}	$I_{OH} = -1.0 \text{ mA}$	$V_{DD} = \text{Min}$	2.10	$V_{DD} + 0.3$	V
Output low voltage	V_{OL}	$I_{OL} = 1.0 \text{ mA}$	$V_{DD} = \text{Min}$	GND	0.50	V
Input high voltage	V_{IH}	—		2.00	—	V
Input low voltage	V_{IL}	—		—	0.80	V
Input high current	I_{IH}	$V_{DD} = \text{Max}$	$V_{IN}^1 = 2.1 \text{ V}$	—	40	μA
Input low current	I_{IL}	$V_{DD} = \text{Max}$	$V_{IN} = 0.5 \text{ V}$	-600	—	μA

Note:

1. The symbol V_{IN} , in this case, represents the V_{IN} symbol referenced in [Table 1](#) and [Table 2](#).

9 USB

This section provides the AC and DC electrical specifications for the USB interface of the MPC8347E.

9.1 USB DC Electrical Characteristics

Table 31 provides the DC electrical characteristics for the USB interface.

Table 31. USB DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	$OV_{DD} + 0.3$	V
Low-level input voltage	V_{IL}	-0.3	0.8	V
Input current	I_{IN}	—	± 5	μA
High-level output voltage, $I_{OH} = -100 \mu A$	V_{OH}	$OV_{DD} - 0.2$	—	V
Low-level output voltage, $I_{OL} = 100 \mu A$	V_{OL}	—	0.2	V

9.2 USB AC Electrical Specifications

Table 32 describes the general timing parameters of the USB interface of the MPC8347E.

Table 32. USB General Timing Parameters (ULPI Mode Only)

Parameter	Symbol ¹	Min	Max	Unit	Notes
USB clock cycle time	t_{USCK}	15	—	ns	2–5
Input setup to USB clock—all inputs	t_{USIVKH}	4	—	ns	2–5
Input hold to USB clock—all inputs	t_{USIXKH}	1	—	ns	2–5
USB clock to output valid—all outputs	t_{USKHOV}	—	7	ns	2–5
Output hold from USB clock—all outputs	t_{USKHGX}	2	—	ns	2–5

Notes:

1. The symbols for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{USIXKH} symbolizes USB timing (US) for the input (I) to go invalid (X) with respect to the time the USB clock reference (K) goes high (H). Also, t_{USKHGX} symbolizes USB timing (US) for the USB clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to USB clock.
3. All signals are measured from $OV_{DD}/2$ of the rising edge of the USB clock to $0.4 \times OV_{DD}$ of the signal in question for 3.3 V signaling levels.
4. Input timings are measured at the pin.
5. For active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to that of the leakage current specification.

Table 39. I²C AC Electrical Specifications (continued)

Parameter	Symbol ¹	Min	Max	Unit
Fall time of both SDA and SCL signals ⁵	t_{I2CF}	—	300	ns
Setup time for STOP condition	t_{I2PVKH}	0.6	—	μ s
Bus free time between a STOP and START condition	t_{I2KHDX}	1.3	—	μ s
Noise margin at the LOW level for each connected device (including hysteresis)	V_{NL}	$0.1 \times OV_{DD}$	—	V
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{NH}	$0.2 \times OV_{DD}$	—	V

Notes:

- The symbols for timing specifications follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)(reference)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, t_{I2DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I²C timing (I2) for the time that the data with respect to the start condition (S) goes invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I²C timing (I2) for the time that the data with respect to the stop condition (P) reaches the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
- MPC8347E provides a hold time of at least 300 ns for the SDA signal (referred to the $V_{IH(min)}$ of the SCL signal) to bridge the undefined region of the falling edge of SCL.
- The maximum t_{I2DVKH} must be met only if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.
- C_B = capacitance of one bus line in pF.
- The MPC8347E does not follow the "I²C-BUS Specifications" version 2.1 regarding the t_{I2CF} AC parameter.

Figure 31 provides the AC test load for the I²C.

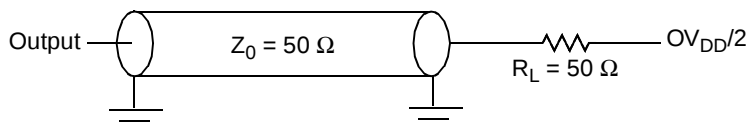
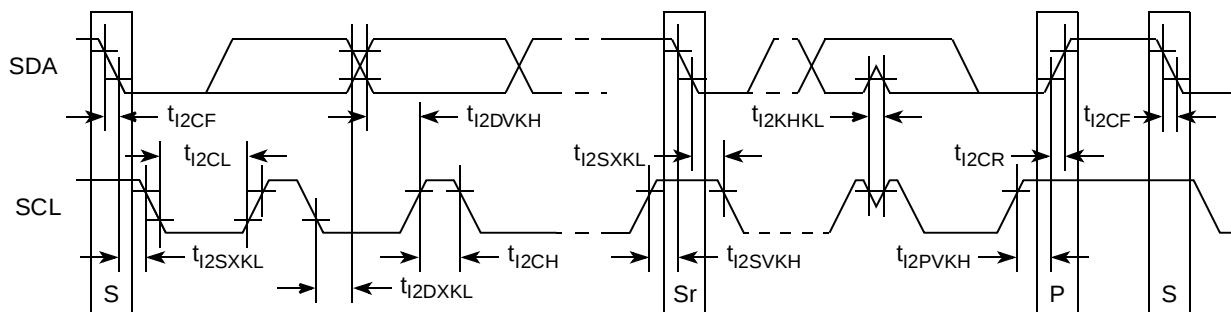
Figure 31. I²C AC Test Load

Figure 32 shows the AC timing diagram for the I²C bus.

Figure 32. I²C Bus AC Timing Diagram

13 PCI

This section describes the DC and AC electrical specifications for the PCI bus of the MPC8347E.

13.1 PCI DC Electrical Characteristics

Table 40 provides the DC electrical characteristics for the PCI interface of the MPC8347E.

Table 40. PCI DC Electrical Characteristics

Parameter	Symbol	Test Condition	Min	Max	Unit
High-level input voltage	V_{IH}	$V_{OUT} \geq V_{OH} \text{ (min) or } V_{OUT} \leq V_{OL} \text{ (max)}$	2	$OV_{DD} + 0.3$	V
Low-level input voltage	V_{IL}		-0.3	0.8	V
Input current	I_{IN}	$V_{IN}^1 = 0 \text{ V or } V_{IN} = OV_{DD}$	—	± 5	μA
High-level output voltage	V_{OH}	$OV_{DD} = \text{min, } I_{OH} = -100 \mu\text{A}$	$OV_{DD} - 0.2$	—	V
Low-level output voltage	V_{OL}	$OV_{DD} = \text{min, } I_{OL} = 100 \mu\text{A}$	—	0.2	V

Note:

1. The symbol V_{IN} , in this case, represents the OV_{IN} symbol referenced in Table 1.

13.2 PCI AC Electrical Specifications

This section describes the general AC timing parameters of the PCI bus of the MPC8347E. Note that the PCI_CLK or PCI_SYNC_IN signal is used as the PCI input clock depending on whether the MPC8347E is configured as a host or agent device. Table 41 provides the PCI AC timing specifications at 66 MHz.

Table 41. PCI AC Timing Specifications at 66 MHz¹

Parameter	Symbol ²	Min	Max	Unit	Notes
Clock to output valid	t_{PCKHOV}	—	6.0	ns	3
Output hold from clock	t_{PCKHOX}	1	—	ns	3
Clock to output high impedance	t_{PCKHOZ}	—	14	ns	3, 4
Input setup to clock	t_{PCIVKH}	3.0	—	ns	3, 5

16 IPIC

This section describes the DC and AC electrical specifications for the external interrupt pins.

16.1 IPIC DC Electrical Characteristics

Table 47 provides the DC electrical characteristics for the external interrupt pins.

Table 47. IPIC DC Electrical Characteristics¹

Characteristic	Symbol	Condition	Min	Max	Unit	Notes
Input high voltage	V_{IH}		2.0	$OV_{DD} + 0.3$	V	
Input low voltage	V_{IL}		-0.3	0.8	V	
Input current	I_{IN}			±5	μA	
Output low voltage	V_{OL}	$I_{OL} = 8.0 \text{ mA}$	—	0.5	V	2
Output low voltage	V_{OL}	$I_{OL} = 3.2 \text{ mA}$	—	0.4	V	2

Notes:

1. This table applies for pins $\overline{IRQ}[0:7]$, $\overline{IRQ_OUT}$, and $\overline{MCP_OUT}$.
2. $\overline{IRQ_OUT}$ and $\overline{MCP_OUT}$ are open-drain pins; thus V_{OH} is not relevant for those pins.

16.2 IPIC AC Timing Specifications

Table 48 provides the IPIC input and output AC timing specifications.

Table 48. IPIC Input AC Timing Specifications¹

Characteristic	Symbol ²	Min	Unit
IPIC inputs—minimum pulse width	t_{PICWID}	20	ns

Notes:

1. Input specifications are measured at the 50 percent level of the IPIC input signals. Timings are measured at the pin.
2. IPIC inputs and outputs are asynchronous to any visible clock. IPIC outputs should be synchronized before use by external synchronous logic. IPIC inputs must be valid for at least t_{PICWID} ns to ensure proper operation in edge triggered mode.

Table 52. MPC8347E (PBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
MPH0_D2_VMO_SE0/DR_D10_DPPD	B24	I/O	OV _{DD}	
MPH0_D3_SPEED/DR_D11_DMMD	A24	I/O	OV _{DD}	
MPH0_D4_DP/DR_D12_VBUS_VLD	D23	I/O	OV _{DD}	
MPH0_D5_DM/DR_D13_SESS_END	C23	I/O	OV _{DD}	
MPH0_D6_SER_RCV/DR_D14	B23	I/O	OV _{DD}	
MPH0_D7_DRVVBUS/DR_D15_IDPULLUP	A23	I/O	OV _{DD}	
MPH0_NXT/DR_RX_ACTIVE_ID	D22	I	OV _{DD}	
MPH0_DIR_DPPULLUP/DR_RESET	C22	I/O	OV _{DD}	
MPH0_STP_SUSPEND/DR_TX_READY	B22	I/O	OV _{DD}	
MPH0_PWRFAULT/DR_RX_VALIDH	A22	I	OV _{DD}	
MPH0_PCTL0/DR_LINE_STATE0	E21	I/O	OV _{DD}	
MPH0_PCTL1/DR_LINE_STATE1	D21	I/O	OV _{DD}	
MPH0_CLK/DR_RX_VALID	C21	I	OV _{DD}	
Programmable Interrupt Controller				
MCP_OUT	E8	O	OV _{DD}	2
IRQ0/MCP_IN/GPIO2[12]	J28	I/O	OV _{DD}	
IRQ[1:5]/GPIO2[13:17]	K25, J25, H26, L24, G27	I/O	OV _{DD}	
IRQ[6]/GPIO2[18]/CKSTOP_OUT	G28	I/O	OV _{DD}	
IRQ[7]/GPIO2[19]/CKSTOP_IN	J26	I/O	OV _{DD}	
Ethernet Management Interface				
EC_MDC	Y24	O	LV _{DD1}	
EC_MDIO	Y25	I/O	LV _{DD1}	2
Gigabit Reference Clock				
EC_GTX_CLK125	Y26	I	LV _{DD1}	
Three-Speed Ethernet Controller (Gigabit Ethernet 1)				
TSEC1_COL/GPIO2[20]	M26	I/O	OV _{DD}	
TSEC1_CRS/GPIO2[21]	U25	I/O	LV _{DD1}	
TSEC1_GTX_CLK	V24	O	LV _{DD1}	3
TSEC1_RX_CLK	U26	I	LV _{DD1}	
TSEC1_RX_DV	U24	I	LV _{DD1}	
TSEC1_RX_ER/GPIO2[26]	L28	I/O	OV _{DD}	
TSEC1_RXD[7:4]/GPIO2[22:25]	M27, M28, N26, N27	I/O	OV _{DD}	
TSEC1_RXD[3:0]	W26, W24, Y28, Y27	I	LV _{DD1}	
TSEC1_TX_CLK	N25	I	OV _{DD}	

Table 52. MPC8347E (PBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
SPIMISO	C7	I/O	OV _{DD}	
SPICLK	B7	I/O	OV _{DD}	
SPISEL	A7	I	OV _{DD}	
Clocks				
PCI_CLK_OUT[0:2]	Y1, W3, W2	O	OV _{DD}	
PCI_CLK_OUT[3]/ $\overline{\text{LCS}}[6]$	W1	O	OV _{DD}	
PCI_CLK_OUT[4]/ $\overline{\text{LCS}}[7]$	V3	O	OV _{DD}	
PCI_SYNC_IN/PCI_CLOCK	U4	I	OV _{DD}	
PCI_SYNC_OUT	U5	O	OV _{DD}	3
RTC/PIT_CLOCK	E9	I	OV _{DD}	
CLKIN	W5	I	OV _{DD}	
JTAG				
TCK	H27	I	OV _{DD}	
TDI	H28	I	OV _{DD}	4
TDO	M24	O	OV _{DD}	3
TMS	J27	I	OV _{DD}	4
$\overline{\text{TRST}}$	K26	I	OV _{DD}	4
Test				
TEST	F28	I	OV _{DD}	6
TEST_SEL	T3	I	OV _{DD}	6
PMC				
$\overline{\text{QUIESCE}}$	K27	O	OV _{DD}	
System Control				
$\overline{\text{PORESET}}$	K28	I	OV _{DD}	
$\overline{\text{HRESET}}$	M25	I/O	OV _{DD}	1
$\overline{\text{SRESET}}$	L27	I/O	OV _{DD}	2
Thermal Management				
THERM0	B15	I	—	8
Power and Ground Signals				
AV _{DD1}	C15	Power for e300 PLL (1.2 V)	AV _{DD1}	
AV _{DD2}	U1	Power for system PLL (1.2 V)	AV _{DD2}	

Table 52. MPC8347E (PBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
MVREF1	AF19	I	DDR reference voltage	
MVREF2	AE10	I	DDR reference voltage	
No Connection				
NC	V1, V2, V5			

Notes:

1. This pin is an open-drain signal. A weak pull-up resistor (1 k Ω) should be placed on this pin to OV_{DD}.
2. This pin is an open-drain signal. A weak pull-up resistor (2–10 k Ω) should be placed on this pin to OV_{DD}.
3. During reset, this output is actively driven rather than three-stated.
4. These JTAG pins have weak internal pull-up P-FETs that are always enabled.
5. This pin should have a weak pull-up if the chip is in PCI host mode. Follow the PCI specifications.
6. This pin must always be tied to GND.
7. This pin must always be left not connected.
8. Thermal sensitive resistor.
9. It is recommended that MDIC0 be tied to GRD using an 18 Ω resistor and MDIC1 be tied to DDR power using an 18 Ω resistor.
10. TSEC1_TXD[3] is required an external pull-up resistor. For proper functionality of the device, this pin must be pulled up or actively driven high during a hard reset. No external pull-down resistors are allowed to be attached to this net.

Table 57. CSB Frequency Options for Host Mode

CFG_CLKIN_DIV at Reset ¹	SPMF	<i>csb_clk</i> : Input Clock Ratio ²	Input Clock Frequency (MHz) ²					
			16.67	25	33.33	66.67		
			<i>csb_clk</i> Frequency (MHz)					
Low	0010	2 : 1				133		
Low	0011	3 : 1				100	200	
Low	0100	4 : 1				100	133	266
Low	0101	5 : 1				125	166	333
Low	0110	6 : 1	100	150	200			
Low	0111	7 : 1	116	175	233			
Low	1000	8 : 1	133	200	266			
Low	1001	9 : 1	150	225	300			
Low	1010	10 : 1	166	250	333			
Low	1011	11 : 1	183	275				
Low	1100	12 : 1	200	300				
Low	1101	13 : 1	216	325				
Low	1110	14 : 1	233					
Low	1111	15 : 1	250					
Low	0000	16 : 1	266					
High	0010	2 : 1					133	
High	0011	3 : 1					100	200
High	0100	4 : 1					133	266
High	0101	5 : 1					166	333
High	0110	6 : 1					200	
High	0111	7 : 1					233	
High	1000	8 : 1						

¹ CFG_CLKIN_DIV selects the ratio between CLKIN and PCI_SYNC_OUT.

² CLKIN is the input clock in host mode; PCI_CLK is the input clock in agent mode.
DDR2 memory may be used at 133 MHz provided that the memory components are specified for operation at this frequency.

Tyco Electronics Chip Coolers™ P.O. Box 3668 Harrisburg, PA 17105-3668 Internet: www.chipcoolers.com	800-522-2800
Wakefield Engineering 33 Bridge St. Pelham, NH 03076 Internet: www.wakefield.com	603-635-5102

Interface material vendors include the following:

Chomerics, Inc. 77 Dragon Ct. Woburn, MA 01801 Internet: www.chomerics.com	781-935-4850
Dow-Corning Corporation Dow-Corning Electronic Materials P.O. Box 994 Midland, MI 48686-0997 Internet: www.dowcorning.com	800-248-2481
Shin-Etsu MicroSi, Inc. 10028 S. 51st St. Phoenix, AZ 85044 Internet: www.microsi.com	888-642-7674
The Bergquist Company 18930 West 78th St. Chanhassen, MN 55317 Internet: www.bergquistcompany.com	800-347-4572

20.3 Heat Sink Attachment

When heat sinks are attached, an interface material is required, preferably thermal grease and a spring clip. The spring clip should connect to the printed-circuit board, either to the board itself, to hooks soldered to the board, or to a plastic stiffener. Avoid attachment forces that can lift the edge of the package or peel the package from the board. Such peeling forces reduce the solder joint lifetime of the package. The recommended maximum force on the top of the package is 10 lb force (4.5 kg force). Any adhesive attachment should attach to painted or plastic surfaces, and its performance should be verified under the application requirements.

20.3.1 Experimental Determination of the Junction Temperature with a Heat Sink

When a heat sink is used, the junction temperature is determined from a thermocouple inserted at the interface between the case of the package and the interface material. A clearance slot or hole is normally

21.3 Decoupling Recommendations

Due to large address and data buses and high operating frequencies, the MPC8347E can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the MPC8347E system, and the MPC8347E itself requires a clean, tightly regulated source of power. Therefore, the system designer should place at least one decoupling capacitor at each V_{DD} , OV_{DD} , GV_{DD} , and LV_{DD} pin of the MPC8347E. These capacitors should receive their power from separate V_{DD} , OV_{DD} , GV_{DD} , LV_{DD} , and GND power planes in the PCB, with short traces to minimize inductance. Capacitors can be placed directly under the device using a standard escape pattern. Others can surround the part.

These capacitors should have a value of 0.01 or 0.1 μF . Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0402 or 0603 sizes.

In addition, distribute several bulk storage capacitors around the PCB, feeding the V_{DD} , OV_{DD} , GV_{DD} , and LV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors are 100–330 μF (AVX TPS tantalum or Sanyo OSCON).

21.4 Connection Recommendations

To ensure reliable operation, connect unused inputs to an appropriate signal level. Unused active low inputs should be tied to OV_{DD} , GV_{DD} , or LV_{DD} as required. Unused active high inputs should be connected to GND. All NC (no-connect) signals must remain unconnected.

Power and ground connections must be made to all external V_{DD} , GV_{DD} , LV_{DD} , OV_{DD} , and GND pins of the MPC8347E.

21.5 Output Buffer DC Impedance

The MPC8347E drivers are characterized over process, voltage, and temperature. For all buses, the driver is a push-pull single-ended driver type (open drain for I^2C).

To measure Z_0 for the single-ended drivers, an external resistor is connected from the chip pad to OV_{DD} or GND. Then the value of each resistor is varied until the pad voltage is $OV_{DD}/2$ (see [Figure 43](#)). The output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held high, SW1 is closed (SW2 is open) and R_P is trimmed until the voltage at the pad equals $OV_{DD}/2$. R_P then becomes the resistance of the pull-up devices. R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N)/2$.

23 Ordering Information

This section presents ordering information for the device discussed in this document, and it shows an example of how the parts are marked.

NOTE

The information in this document is accurate for revision 1.1 silicon and earlier. For information on revision 3.0 silicon and later versions (orderable part numbers ending with A or B), see the *MPC8347EA PowerQUICC™ II Pro Integrated Host Processor Hardware Specifications* (Document Order No. MPC8347EAEC).

23.1 Part Numbers Fully Addressed by This Document

Table 67 shows an analysis of the Freescale part numbering nomenclature for the MPC8347E. The individual part numbers correspond to a maximum processor core frequency. Each part number also contains a revision code that refers to the die mask revision number. For available frequency configuration parts including extended temperatures, refer to the MPC8347E product summary page on our website listed on the back cover of this document or, contact your local Freescale sales office.

Table 67. Part Numbering Nomenclature

MPC	nnnn	e	t	pp	aa	a	r
Product Code	Part Identifier	Encryption Acceleration	Temperature ¹ Range	Package ²	Processor Frequency ³	Platform Frequency	Revision Level
MPC	8347	Blank = Not included E = included	Blank = 0 to 105°C C = -40 to 105°C	ZU = TBGA VV = PB free TBGA ZQ = PBGA VR = PB Free PBGA	e300 core speed AD = 266 AG = 400 AJ = 533 AL = 667	D = 266 F = 333 ⁴	Blank = 1.1 or 1.0

Notes:

- For temperature range = C, processor frequency is limited to 400 (PBGA) with a platform frequency of 266 and up to 667(TBGA)with a platform frequency of 333
- See [Section 18, "Package and Pin Listings,"](#) for more information on available package types.
- Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by Part Number Specifications may support other maximum core frequencies.
- ALF marked parts support DDR1 up to 333 MHz (at 333 MHz CSB as the 'F' marking implies) and DDR2 up to 400 MHz (at 200 MHz CSB). AJF marked parts support DDR1 and DDR2 up to 333 MHz (at a CSB of 333 MHz), but DDR2 at 400 MHz (CSB at 200 MHz) is NOT guaranteed.

Table 68 shows the SVR settings by device and package type.

Table 68. SVR Settings

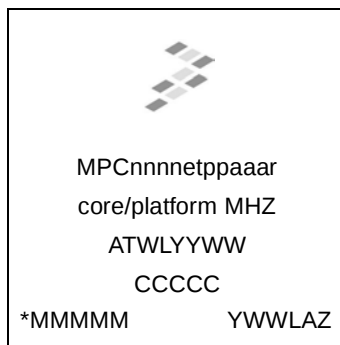
Device	Package	SVR (Rev. 1.0)
MPC8347E	TBGA	8052_0010
MPC8347	TBGA	8053_0010

Table 68. SVR Settings (continued)

MPC8347E	PBGA	8054_0010
MPC8347	PBGA	8055_0010

23.2 Part Marking

Parts are marked as in the example shown in [Figure 44](#).



Notes:

ATWLYYWW is the traceability code.

CCCCC is the country code.

MMMMM is the mask number.

YWWLAZ is the assembly traceability code.

Figure 44. Freescale Part Marking for TBGA or PBGA Devices

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