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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e300
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	266MHz
Co-Processors/DSP	-
RAM Controllers	DDR
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	-
Package / Case	620-BBGA Exposed Pad
Supplier Device Package	620-HBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8347czqaddb

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

2.1.2 Power Supply Voltage Specification

Table 2 provides the recommended operating conditions for the MPC8347E. Note that the values in Table 2 are the recommended and tested operating conditions. Proper device operation outside these conditions is not guaranteed.

Characteristic	Symbol	Recommended Value	Unit	Notes
Core supply voltage	V _{DD}	1.2 V ± 60 mV	V	1
PLL supply voltage	AV _{DD}	1.2 V ± 60 mV	V	1
DDR DRAM I/O supply voltage	GV _{DD}	2.5 V ± 125 mV	V	
Three-speed Ethernet I/O supply voltage	LV _{DD1}	3.3 V ± 330 mV 2.5 V ± 125 mV	V	
Three-speed Ethernet I/O supply voltage	LV _{DD2}	3.3 V ± 330 mV 2.5 V ± 125 mV	V	
PCI, local bus, DUART, system control and power management, I ² C, and JTAG I/O voltage	OV _{DD}	3.3 V ± 330 mV	V	

ating Conditions
,

Note:

¹ GV_{DD}, LV_{DD}, OV_{DD}, AV_{DD}, and V_{DD} must track each other and must vary in the same direction—either in the positive or negative direction.

Figure 2 shows the undershoot and overshoot voltages at the interfaces of the MPC8347E.



3 Power Characteristics

The estimated typical power dissipation for the MPC8347E device is shown in Table 4.

	Core Frequency (MHz)	CSB Frequency (MHz)	Typical at T _J = 65	Typical ^{2,3}	Maximum ⁴	Unit
PBGA	266	266	1.3	1.6	1.8	W
		133	1.1	1.4	1.6	W
	400	266	1.5	1.9	2.1	W
		133	1.4	1.7	1.9	W
	400	200	1.5	1.8	2.0	W
		100	1.3	1.7	1.9	W
TBGA	333	333	2.0	3.0	3.2	W
		166	1.8	2.8	2.9	W
	400	266	2.1	3.0	3.3	W
		133	1.9	2.9	3.1	W
	450	300	2.3	3.2	3.5	W
		150	2.1	3.0	3.2	W
	500	333	2.4	3.3	3.6	W
		166	2.2	3.1	3.4	W
	533	266	2.4	3.3	3.6	W
		133	2.2	3.1	3.4	W

Table 4. MPC8347E Power Dissipation¹

¹ The values do not include I/O supply power (OV_{DD}, LV_{DD}, GV_{DD}) or AV_{DD}. For I/O power values, see Table 5.

² Typical power is based on a voltage of V_{DD} = 1.2 V, a junction temperature of T_J = 105°C, and a Dhrystone benchmark application.

³ Thermal solutions may need to design to a value higher than typical power based on the end application, T_A target, and I/O power.

⁴ Maximum power is based on a voltage of V_{DD} = 1.2 V, worst case process, a junction temperature of T_J = 105°C, and an artificial smoke test.

DDR SDRAM

Table 14. DDR SDRAM Output AC Timing Specifications for Source Synchronous Mode (continued)

At recommended operating conditions with GV_{DD} of 2.5 V ± 5%.

Parameter	Symbol ¹	Min	Мах	Unit	Notes
MDQS epilogue end	t _{DDKLME}	-0.9	0.3	ns	7

Notes:

- The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
 </sub>
- 2. All MCK/MCK referenced measurements are made from the crossing of the two signals ±0.1 V.
- 3. In the source synchronous mode, MCK/MCK can be shifted in 1/4 applied cycle increments through the clock control register. For the skew measurements referenced for t_{AOSKEW} it is assumed that the clock adjustment is set to align the address/command valid with the rising edge of MCK.
- 4. ADDR/CMD includes all DDR SDRAM output signals except MCK/MCK, MCS, and MDQ/MECC/MDM/MDQS. For the ADDR/CMD setup and hold specifications, it is assumed that the clock control register is set to adjust the memory clocks by 1/2 applied cycle.
- 5. Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK(n) clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. In source synchronous mode, this will typically be set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these 2 parameters have been set to the same adjustment value. See the MPC8349E PowerQUICC[™] II Pro Integrated Host Processor Family Reference Manual, for a description and understanding of the timing modifications enabled by use of these bits.
- 6. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the MPC8347E.
- 7. All outputs are referenced to the rising edge of MCK(n) at the pins of the MPC8347E. Note that t_{DDKHMP} follows the symbol conventions described in note 1.

Figure 5 shows the DDR SDRAM output timing for address skew with respect to any MCK.



Figure 5. Timing Diagram for t_{AOSKEW} Measurement

Figure 6 provides the AC test load for the DDR bus.

7 DUART

This section describes the DC and AC electrical specifications for the DUART interface of the MPC8347E.

7.1 DUART DC Electrical Characteristics

Table 17 provides the DC electrical characteristics for the DUART interface of the MPC8347E.

Table 17. DUART DC Electrical Characteristics

Parameter	Symbol	Min	Мах	Unit
High-level input voltage	V _{IH}	2	OV _{DD} + 0.3	V
Low-level input voltage	V _{IL}	-0.3	0.8	V
Input current (0.8 V \leq V _{IN} \leq 2 V)	I _{IN}	—	±5	μA
High-level output voltage, I _{OH} = -100 μA	V _{OH}	OV _{DD} - 0.2	—	V
Low-level output voltage, $I_{OL} = 100 \ \mu A$	V _{OL}	—	0.2	V

7.2 DUART AC Electrical Specifications

Table 18 provides the AC timing parameters for the DUART interface of the MPC8347E.

Table 18. DUART AC Timing Specifications

Parameter	Value	Unit	Notes
Minimum baud rate	256	baud	
Maximum baud rate	>1,000,000	baud	1
Oversample rate	16		2

Notes:

- 1. Actual attainable baud rate will be limited by the latency of interrupt processing.
- 2. The middle of a start bit is detected as the 8th sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16th sample.

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Figure 8 shows the GMII transmit AC timing diagram.



Figure 8. GMII Transmit AC Timing Diagram

8.2.1.2 GMII Receive AC Timing Specifications

Table 22 provides the GMII receive AC timing specifications.

Table 22. GMII Receive AC Timing Specifications

At recommended operating conditions with LV_{DD}/OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol ¹	Min	Тур	Мах	Unit
RX_CLK clock period	t _{GRX}	_	8.0	—	ns
RX_CLK duty cycle	t _{GRXH} /t _{GRX}	40	—	60	%
RXD[7:0], RX_DV, RX_ER setup time to RX_CLK	t _{GRDVKH}	2.0	—	—	ns
RXD[7:0], RX_DV, RX_ER hold time to RX_CLK	t _{GRDXKH}	0.5	—	—	ns
RX_CLK clock rise, V _{IL} (min) to V _{IH} (max)	t _{GRXR}	-	—	1.0	ns
RX_CLK clock fall time, $V_{IH}(max)$ to $V_{IL}(min)$	t _{GRXF}			1.0	ns

Note:

1. The symbols for timing specifications follow the pattern of t_{(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{GRDVKH} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{RX} clock reference (K) going to the high state (H) or setup time. Also, t_{GRDXKL} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{GRX} clock reference (K) going to the low (L) state or hold time. In general, the clock reference symbol is based on three letters representing the clock of a particular function. For example, the subscript of t_{GRX} represents the GMII (G) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).}

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Figure 10 shows the MII transmit AC timing diagram.



Figure 10. MII Transmit AC Timing Diagram

8.2.2.2 MII Receive AC Timing Specifications

Table 24 provides the MII receive AC timing specifications.

Table 24. MII Receive AC Timing Specifications

At recommended operating conditions with LV_{DD}/OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol ¹	Min	Тур	Мах	Unit
RX_CLK clock period 10 Mbps	t _{MRX}	_	400	—	ns
RX_CLK clock period 100 Mbps	t _{MRX}	_	40	—	ns
RX_CLK duty cycle	t _{MRXH} /t _{MRX}	35	—	65	%
RXD[3:0], RX_DV, RX_ER setup time to RX_CLK	t _{MRDVKH}	10.0	—	—	ns
RXD[3:0], RX_DV, RX_ER hold time to RX_CLK	t _{MRDXKH}	10.0	—	—	ns
RX_CLK clock rise V _{IL} (min) to V _{IH} (max)	t _{MRXR}	1.0	—	4.0	ns
RX_CLK clock fall time V _{IH} (max) to V _{IL} (min)	t _{MRXF}	1.0	_	4.0	ns

Note:

The symbols for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t<sub>(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. In general, the clock reference symbol is based on three letters representing the clock of a particular functionI. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
</sub></sub>

Figure 11 provides the AC test load for TSEC.



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Figure 15. RGMII and RTBI AC Timing and Multiplexing Diagrams

8.3 Ethernet Management Interface Electrical Characteristics

The electrical characteristics specified here apply to the MII management interface signals management data input/output (MDIO) and management data clock (MDC). The electrical characteristics for GMII, RGMII, TBI and RTBI are specified in Section 8.1, "Three-Speed Ethernet Controller (TSEC)—GMII/MII/TBI/RGMII/RTBI Electrical Characteristics."

8.3.1 MII Management DC Electrical Characteristics

The MDC and MDIO are defined to operate at a supply voltage of 2.5 or 3.3 V. The DC electrical characteristics for MDIO and MDC are provided in Table 28 and Table 29.

Parameter	Symbol	Conditions		Min	Мах	Unit
Supply voltage (2.5 V)	LV _{DD}	—		2.37	2.63	V
Output high voltage	V _{OH}	$I_{OH} = -1.0 \text{ mA}$	LV _{DD} = Min	2.00	LV _{DD} + 0.3	V
Output low voltage	V _{OL}	I _{OL} = 1.0 mA	LV _{DD} = Min	GND – 0.3	0.40	V
Input high voltage	V _{IH}	—	— LV _{DD} = Min		—	V
Input low voltage	V _{IL}	—	LV _{DD} = Min	-0.3	0.70	V
Input high current	I _{IH}	$V_{IN}^{1} = LV_{DD}$		—	10	μA
Input low current	I _{IL}	V _{IN} =	LV _{DD}	-15	—	μA

Table 28. MII Management DC Electrical Characteristics Powered at 2.5 V

Note:

1. The symbol V_{IN} , in this case, represents the LV_{IN} symbol referenced in Table 1 and Table 2.

Table 29	MII Manad	nement DC	Flectrical	Characteristics	Powered at 3.3 V
10010 23.	min manay	Jennenie DO	LICCUICAI	onaracteristics	

Parameter	Symbol	Conditions		Min	Мах	Unit
Supply voltage (3.3 V)	LV _{DD}	—		2.97	3.63	V
Output high voltage	V _{OH}	I _{OH} = -1.0 mA	$LV_{DD} = Min$	2.10	LV _{DD} + 0.3	V
Output low voltage	V _{OL}	I _{OL} = 1.0 mA	$LV_{DD} = Min$	GND	0.50	V
Input high voltage	V _{IH}	-	—		—	V
Input low voltage	V _{IL}	-	—		0.80	V
Input high current	I _{IH}	LV _{DD} = Max	$V_{IN}^{1} = 2.1 V$	—	40	μA
Input low current	IIL	LV _{DD} = Max	V _{IN} = 0.5 V	-600	—	μA

Note:

1. The symbol V_{IN} , in this case, represents the LV_{IN} symbol referenced in Table 1 and Table 2.

11 JTAG

JTAG

This section describes the DC and AC electrical specifications for the IEEE Std. 1149.1 (JTAG) interface of the MPC8347E

11.1 JTAG DC Electrical Characteristics

Table 36 provides the DC electrical characteristics for the IEEE Std. 1149.1 (JTAG) interface of the MPC8347E.

Characteristic	Symbol	Condition	Min	Мах	Unit
Input high voltage	V _{IH}		OV _{DD} - 0.3	OV _{DD} + 0.3	V
Input low voltage	V _{IL}		-0.3	0.8	V
Input current	I _{IN}			±5	μA
Output high voltage	V _{OH}	I _{OH} = -8.0 mA	2.4	—	V
Output low voltage	V _{OL}	I _{OL} = 8.0 mA	—	0.5	V
Output low voltage	V _{OL}	I _{OL} = 3.2 mA	—	0.4	V

Table 36. JTAG interface DC Electrical Characteristics

11.2 JTAG AC Timing Specifications

This section describes the AC electrical specifications for the IEEE Std. 1149.1 (JTAG) interface of the MPC8347E. Table 37 provides the JTAG AC timing specifications as defined in Figure 27 through Figure 30.

Table 37. JTAG AC Timing Specifications (Independent of CLKIN)¹

At recommended operating conditions (see Table 2).

Parameter	Symbol ²	Min	Мах	Unit	Notes
JTAG external clock frequency of operation	f _{JTG}	0	33.3	MHz	
JTAG external clock cycle time	t _{JTG}	30	_	ns	
JTAG external clock pulse width measured at 1.4 V	t _{JTKHKL}	15	_	ns	
JTAG external clock rise and fall times	t _{JTGR} , t _{JTGF}	0	2	ns	
TRST assert time	t _{TRST}	25	—	ns	3
Input setup times: Boundary-scan data TMS, TDI	t _{JTDVKH} t _{JTIVKH}	4 4		ns	4
Input hold times: Boundary-scan data TMS, TDI	^t jtdxkh ^t jtixkh	10 10		ns	4
Valid times: Boundary-scan data TDO	t _{jtkldv} t _{jtklov}	2 2	11 11	ns	5

JTAG

Figure 28 provides the TRST timing diagram.







Figure 29. Boundary-Scan Timing Diagram

Figure 30 provides the test access port timing diagram.



Figure 30. Test Access Port Timing Diagram

SPI

Figure 36 provides the AC test load for the SPI.



Figure 36. SPI AC Test Load

Figure 37 and Figure 38 represent the AC timings from Table 50. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

Figure 37 shows the SPI timings in slave mode (external clock).



Note: The clock edge is selectable on SPI.



Figure 38 shows the SPI timings in master mode (internal clock).



Figure 38. SPI AC Timing in Master Mode (Internal Clock) Diagram

18.3 Package Parameters for the MPC8347E PBGA

The package parameters are as provided in the following list. The package type is $29 \text{ mm} \times 29 \text{ mm}$, 620 plastic ball grid array (PBGA).

Package outline	$29 \text{ mm} \times 29 \text{ mm}$
Interconnects	620
Pitch	1.00 mm
Module height (maximum)	2.46 mm
Module height (typical)	2.23 mm
Module height (minimum)	2.00 mm
Solder balls	62 Sn/36 Pb/2 Ag (ZQ package)
	95.5 Sn/0.5 Cu/4Ag (VR package)
Ball diameter (typical)	0.60 mm

Signal	Package Pin Number	Pin Type	Power Supply	Notes
MPH1_NXT/DR_SESS_VLD_NXT	D27	I	OV _{DD}	
MPH1_DIR_DPPULLUP/ DR_XCVR_SEL_DPPULLUP	A28	I/O	OV _{DD}	
MPH1_STP_SUSPEND/ DR_STP_SUSPEND	F26	0	OV _{DD}	
MPH1_PWRFAULT/ DR_RX_ERROR_PWRFAULT	E27	I	OV _{DD}	
MPH1_PCTL0/DR_TX_VALID_PCTL0	A29	0	OV _{DD}	
MPH1_PCTL1/DR_TX_VALIDH_PCTL1	D28	0	OV _{DD}	
MPH1_CLK/DR_CLK	B29	I	OV _{DD}	
	USB Port 0			1
MPH0_D0_ENABLEN/DR_D8_CHGVBUS	C29	I/O	OV _{DD}	
MPH0_D1_SER_TXD/DR_D9_DCHGVBUS	A30	I/O	OV _{DD}	
MPH0_D2_VMO_SE0/DR_D10_DPPD	E28	I/O	OV _{DD}	
MPH0_D3_SPEED/DR_D11_DMMD	B30	I/O	OV _{DD}	
MPH0_D4_DP/DR_D12_VBUS_VLD	C30	I/O	OV _{DD}	
MPH0_D5_DM/DR_D13_SESS_END	A31	I/O	OV _{DD}	
MPH0_D6_SER_RCV/DR_D14	B31	I/O	OV _{DD}	
MPH0_D7_DRVVBUS/DR_D15_IDPULLUP	C31	I/O	OV _{DD}	
MPH0_NXT/DR_RX_ACTIVE_ID	B32	I	OV _{DD}	
MPH0_DIR_DPPULLUP/DR_RESET	A32	I/O	OV _{DD}	
MPH0_STP_SUSPEND/DR_TX_READY	A33	I/O	OV _{DD}	
MPH0_PWRFAULT/DR_RX_VALIDH	C32	I	OV _{DD}	
MPH0_PCTL0/DR_LINE_STATE0	D31	I/O	OV _{DD}	
MPH0_PCTL1/DR_LINE_STATE1	E30	I/O	OV _{DD}	
MPH0_CLK/DR_RX_VALID	B33	I	OV _{DD}	
P	rogrammable Interrupt Controller			
MCP_OUT	AN33	0	OV _{DD}	2
IRQ0/MCP_IN/GPIO2[12]	C19	I/O	OV _{DD}	
IRQ[1:5]/GPIO2[13:17]	C22, A22, D21, C21, B21	I/O	OV _{DD}	
IRQ[6]/GPIO2[18]/CKSTOP_OUT	A21	I/O	OV _{DD}	
IRQ[7]/GPIO2[19]/CKSTOP_IN	C20	I/O	OV _{DD}	
	Ethernet Management Interface	1	1	1
EC_MDC	A7	0	LV _{DD1}	
EC_MDIO	E9	I/O	LV _{DD1}	2

Table 51. MPC8347E (TBGA) Pinout Listing (continued)

Table 51. MPC8347	E (TBGA) Pino	ut Listing (continued)
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Signal	Package Pin Number	Pin Type	Power Supply	Notes		
	System Control					
PORESET	C18	ļ	OV _{DD}			
HRESET	B18	I/O	OV _{DD}	1		
SRESET	D18	I/O	OV _{DD}	2		
Thermal Management						
THERM0	K32	l	_	9		
	Power and Ground Signals					
AV _{DD} 1	L31	Power for e300 PLL (1.2 V)	AV _{DD} 1			
AV _{DD} 2	AP12	Power for system PLL (1.2 V)	AV _{DD} 2			
AV _{DD} 3	AE1	Power for DDR DLL (1.2 V)	AV _{DD} 3			
AV _{DD} 4	AJ13	Power for LBIU DLL (1.2 V)	AV _{DD} 4			
GND	A1, A34, C1, C7, C10, C11, C15, C23, C25, C28, D1, D8, D20, D30, E7, E13, E15, E17, E18, E21, E23, E25, E32, F6, F19, F27, F30, F34, G31, H5, J4, J34, K30, L5, M2, M5, M30, M33, N3, N5, P30, R5, R32, T5, T30, U6, U29, U33, V2, V5, V30, W6, W30, Y30, AA2, AA30, AB2, AB6, AB30, AC3, AC6, AD31, AE5, AF2, AF5, AF31, AG30, AG31, AH4, AJ3, AJ19, AJ22, AK7, AK13, AK14, AK16, AK18, AK20, AK25, AK28, AL3, AL5, AL10, AL12, AL22, AL27, AM1, AM6, AM7, AN12, AN17, AN34, AP1, AP8, AP34					
GV _{DD}	A2, E2, G5, G6, J5, K4, K5, L4, N4, P5, R6, T6, U5, V1, W5, Y5, AA4, AB3, AC4, AD5, AF3, AG5, AH2, AH5, AH6, AJ6, AK6, AK8, AK9, AL6	Power for DDR DRAM I/O voltage (2.5 V)	GV _{DD}			
LV _{DD} 1	C9, D11	Power for three-speed Ethernet #1 and for Ethernet management interface I/O (2.5 V, 3.3 V)	LV _{DD} 1			

Signal	Package Pin Number	Pin Type	Power Supply	Notes
	No Connection			
NC	W32, AA31, AA32, AA33, AA34, AB31, AB32, AB33, AB34, AC29, AC31, AC33, AC34, AD30, AD32, AD33, AD34, AE29, AE30, AH32, AH33, AH34, AM33, AJ31, AJ32, AJ33, AJ34, AK32, AK33, AK34, AM34, AL33, AL34, AK31, AH30, AC32, AE32, AH31, AL32, AG34, AE33, AF32, AE34, AF34, AF33, AG33, AG32, AL11, AM11, AP10, Y32, Y34, Y31, Y33	_	_	

Table 51. MPC8347E (TBGA) Pinout Listing (continued)

Notes:

- 1. This pin is an open-drain signal. A weak pull-up resistor (1 k Ω) should be placed on this pin to OV_{DD}.
- 2. This pin is an open-drain signal. A weak pull-up resistor (2–10 kΩ) should be placed on this pin to OV_{DD}.
- 3. During reset, this output is actively driven rather than three-stated.
- 4. These JTAG pins have weak internal pull-up P-FETs that are always enabled.
- 5. This pin should have a weak pull-up if the chip is in PCI host mode. Follow the PCI specifications.
- 6. This pin must always be tied to GND.
- 7. This pin must always be pulled up to OV_{DD} .
- 8. This pin must always be left not connected.
- 9. Thermal sensitive resistor.
- 10.It is recommended that MDIC0 be tied to GRD using an 18 Ω resistor and MDIC1 be tied to DDR power using an 18 Ω resistor.
- 11.TSEC1_TXD[3] is required an external pull-up resistor. For proper functionality of the device, this pin must be pulled up or actively driven high during a hard reset. No external pull-down resistors are allowed to be attached to this net.

Table 52 provides the pinout listing for the MPC8347E, 620 PBGA package.

Table 52. MPC8347E (PBGA) Pinout Listing

Signal	Package Pin Number	Pin Type	Power Supply	Notes
	PCI			
PCI1_INTA/IRQ_OUT	D20	0	OV _{DD}	2
PCI1_RESET_OUT	B21	0	OV _{DD}	
PCI1_AD[31:0]	E19, D17, A16, A18, B17, B16, D16, B18, E17, E16, A15, C16, D15, D14, C14, A12, D12, B11, C11, E12, A10, C10, A9, E11, E10, B9, B8, D9, A8, C9, D8, C8	I/O	OV _{DD}	
PCI1_C/BE[3:0]	A17, A14, A11, B10	I/O	OV _{DD}	
PCI1_PAR	D13	I/O	OV _{DD}	
PCI1_FRAME	B14	I/O	OV _{DD}	5
PCI1_TRDY	A13	I/O	OV _{DD}	5

Signal	Package Pin Number	Pin Type	Power Supply	Notes
	General Purpose I/O Timers			
GPIO1[0]/GTM1_TIN1/GTM2_TIN2	D27	I/O	OV _{DD}	
GPIO1[1]/GTM1_TGATE1/GTM2_TGATE2	E26	I/O	OV _{DD}	
GPIO1[2]/GTM1_TOUT1	D28	I/O	OV _{DD}	
GPIO1[3]/GTM1_TIN2/GTM2_TIN1	G25	I/O	OV _{DD}	
GPIO1[4]/GTM1_TGATE2/GTM2_TGATE1	J24	I/O	OV _{DD}	
GPIO1[5]/GTM1_TOUT2/GTM2_TOUT1	F26	I/O	OV _{DD}	
GPIO1[6]/GTM1_TIN3/GTM2_TIN4	E27	I/O	OV _{DD}	
GPIO1[7]/GTM1_TGATE3/GTM2_TGATE4	E28	I/O	OV _{DD}	
GPIO1[8]/GTM1_TOUT3	H25	I/O	OV _{DD}	
GPIO1[9]/GTM1_TIN4/GTM2_TIN3	F27	I/O	OV _{DD}	
GPIO1[10]/GTM1_TGATE4/GTM2_TGATE3	K24	I/O	OV _{DD}	
GPIO1[11]/GTM1_TOUT4/GTM2_TOUT3	G26	I/O	OV _{DD}	
	USB Port 1	L		1
MPH1_D0_ENABLEN/DR_D0_ENABLEN	C28	I/O	OV _{DD}	
MPH1_D1_SER_TXD/DR_D1_SER_TXD	F25	I/O	OV _{DD}	
MPH1_D2_VMO_SE0/DR_D2_VMO_SE0	B28	I/O	OV _{DD}	
MPH1_D3_SPEED/DR_D3_SPEED	C27	I/O	OV _{DD}	
MPH1_D4_DP/DR_D4_DP	D26	I/O	OV _{DD}	
MPH1_D5_DM/DR_D5_DM	E25	I/O	OV _{DD}	
MPH1_D6_SER_RCV/DR_D6_SER_RCV	C26	I/O	OV _{DD}	
MPH1_D7_DRVVBUS/DR_D7_DRVVBUS	D25	I/O	OV _{DD}	
MPH1_NXT/DR_SESS_VLD_NXT	B26	I	OV _{DD}	
MPH1_DIR_DPPULLUP/ DR_XCVR_SEL_DPPULLUP	E24	I/O	OV _{DD}	
MPH1_STP_SUSPEND/ DR_STP_SUSPEND	A27	0	OV _{DD}	
MPH1_PWRFAULT/ DR_RX_ERROR_PWRFAULT	C25	I	OV _{DD}	
MPH1_PCTL0/DR_TX_VALID_PCTL0	A26	0	OV _{DD}	
MPH1_PCTL1/DR_TX_VALIDH_PCTL1	B25	0	OV _{DD}	
MPH1_CLK/DR_CLK	A25	I	OV _{DD}	
	USB Port 0	1	1	1
MPH0_D0_ENABLEN/DR_D8_CHGVBUS	D24	I/O	OV _{DD}	
MPH0_D1_SER_TXD/DR_D9_DCHGVBUS	C24	I/O	OV _{DD}	

Table 52. MPC8347E (PBGA) Pinout Listing (continued)

As shown in Figure 41, the primary clock input (frequency) is multiplied up by the system phase-locked loop (PLL) and the clock unit to create the coherent system bus clock (csb_clk), the internal clock for the DDR controller (ddr_clk), and the internal clock for the local bus interface unit ($lbiu_clk$).

The *csb_clk* frequency is derived from a complex set of factors that can be simplified into the following equation:

 $csb_clk = \{PCI_SYNC_IN \times (1 + CFG_CLKIN_DIV)\} \times SPMF$

In PCI host mode, PCI_SYNC_IN \times (1 + CFG_CLKIN_DIV) is the CLKIN frequency.

The *csb_clk* serves as the clock input to the e300 core. A second PLL inside the e300 core multiplies the *csb_clk* frequency to create the internal clock for the e300 core (*core_clk*). The system and core PLL multipliers are selected by the SPMF and COREPLL fields in the reset configuration word low (RCWL), which is loaded at power-on reset or by one of the hard-coded reset options. See the chapter on reset, clocking, and initialization in the *MPC8349E Reference Manual* for more information on the clock subsystem.

The internal *ddr_clk* frequency is determined by the following equation:

 $ddr_clk = csb_clk \times (1 + RCWL[DDRCM])$

 ddr_clk is not the external memory bus frequency; ddr_clk passes through the DDR clock divider (÷2) to create the differential DDR memory bus clock outputs (MCK and MCK). However, the data rate is the same frequency as ddr_clk .

The internal *lbiu_clk* frequency is determined by the following equation:

 $lbiu_clk = csb_clk \times (1 + RCWL[LBIUCM])$

lbiu_clk is not the external local bus frequency; *lbiu_clk* passes through the LBIU clock divider to create the external local bus clock outputs (LSYNC_OUT and LCLK[0:2]). The LBIU clock divider ratio is controlled by LCCR[CLKDIV].

In addition, some of the internal units may have to be shut off or operate at lower frequency than the csb_clk frequency. Those units have a default clock ratio that can be configured by a memory-mapped register after the device exits reset. Table 53 specifies which units have a configurable clock frequency.

Unit	Default Frequency	Options
TSEC1	csb_clk/3	Off, csb_clk, csb_clk/2, csb_clk/3
TSEC2, I ² C1	csb_clk/3	Off, csb_clk, csb_clk/2, csb_clk/3
Security core	csb_clk/3	Off, csb_clk, csb_clk/2, csb_clk/3
USB DR, USB MPH	csb_clk/3	Off, csb_clk, csb_clk/2, <i>csb_clk/3</i>
PCI and DMA complex	csb_clk	Off, <i>csb_clk</i>

Table 53. Configurable Clock Units

Clocking

Table 54 provides the operating frequencies for the MPC8347E TBGA under recommended operating conditions (see Table 2).

Characteristic ¹	400 MHz	533 MHz	667 MHz	Unit
e300 core frequency (<i>core_clk</i>)	266–400	266–533	266–667	MHz
Coherent system bus frequency (<i>csb_clk</i>)	100–266	100–266	100–333	MHz
DDR and memory bus frequency (MCLK) ²	100–133	100–133	100–166.67	MHz
Local bus frequency (LCLK <i>n</i>) ³	16.67–133	16.67–133	16.67–133	MHz
PCI input frequency (CLKIN or PCI_CLK)	25–66	25–66	25–66	MHz
Security core maximum internal operating frequency	133	133	166	MHz
USB_DR, USB_MPH maximum internal operating frequency	133	133	166	MHz

Table 54. Operating Frequencies for TBGA

¹ The CLKIN frequency, RCWL[SPMF], and RCWL[COREPLL] settings must be chosen so that the resulting *csb_clk*, MCLK, LCLK[0:2], and *core_clk* frequencies do not exceed their respective maximum or minimum operating frequencies. The value of SCCR[ENCCM], SCCR[USBDRCM], and SCCR[USBMPHCM] must be programmed so that the maximum internal operating frequency of the Security core and USB modules does not exceed the respective values listed in this table.

² The DDR data rate is 2x the DDR memory bus frequency.

³ The local bus frequency is 1/2, 1/4, or 1/8 of the *lbiu_clk* frequency (depending on LCCR[CLKDIV]) which is in turn 1x or 2x the *csb_clk* frequency (depending on RCWL[LBIUCM]).

Table 55 provides the operating frequencies for the MPC8347E PBGA under recommended operating conditions.

Characteristic ¹	266 MHz	333 MHz	400 MHz	Unit
e300 core frequency (<i>core_clk</i>)	200–266	200–333	200–400	MHz
Coherent system bus frequency (<i>csb_clk</i>)	100–266			
Local bus frequency (LCLK <i>n</i>) ²	16.67–133			
PCI input frequency (CLKIN or PCI_CLK)	25–66			
Security core maximum internal operating frequency	133		MHz	
USB_DR, USB_MPH maximum internal operating frequency	133			MHz

Table 55. Operating Frequencies for PBGA

¹ The CLKIN frequency, RCWL[SPMF], and RCWL[COREPLL] settings must be chosen so that the resulting *csb_clk*, MCLK, LCLK[0:2], and *core_clk* frequencies do not exceed their respective maximum or minimum operating frequencies. The value of SCCR[ENCCM], SCCR[USBDRCM], and SCCR[USBMPHCM] must be programmed so that the maximum internal operating frequency of the Security core and USB modules does not exceed the respective values listed in this table.

² The local bus frequency is 1/2, 1/4, or 1/8 of the *lbiu_clk* frequency (depending on LCCR[CLKDIV]) which is in turn 1x or 2x the *csb_clk* frequency (depending on RCWL[LBIUCM]).

19.1 System PLL Configuration

The system PLL is controlled by the RCWL[SPMF] parameter. Table 56 shows the multiplication factor encodings for the system PLL.

RCWL[SPMF]	System PLL Multiplication Factor
0000	× 16
0001	Reserved
0010	× 2
0011	× 3
0100	× 4
0101	× 5
0110	× 6
0111	× 7
1000	× 8
1001	× 9
1010	× 10
1011	× 11
1100	× 12
1101	× 13
1110	× 14
1111	× 15

Table 56. System PLL Multiplication Factors

As described in Section 19, "Clocking," the LBIUCM, DDRCM, and SPMF parameters in the reset configuration word low and the CFG_CLKIN_DIV configuration input signal select the ratio between the primary clock input (CLKIN or PCI_CLK) and the internal coherent system bus clock (*csb_clk*). Table 57 and Table 58 show the expected frequency values for the CSB frequency for select *csb_clk* to CLKIN/PCI_SYNC_IN ratios.

Thermal

Heat Sink Assuming Thermal Crosse	Air Flow	29 × 29 mm PBGA
neat Sink Assuming merinal Grease		Thermal Resistance
AAVID $30 \times 30 \times 9.4$ mm pin fin	2 m/s	8.8
AAVID 31 \times 35 \times 23 mm pin fin	Natural convection	11.3
AAVID 31 \times 35 \times 23 mm pin fin	1 m/s	8.1
AAVID 31 \times 35 \times 23 mm pin fin	2 m/s	7.5
Wakefield, $53 \times 53 \times 25$ mm pin fin	Natural convection	9.1
Wakefield, $53 \times 53 \times 25$ mm pin fin	1 m/s	7.1
Wakefield, $53 \times 53 \times 25$ mm pin fin	2 m/s	6.5
MEI, $75 \times 85 \times 12$ no adjacent board, extrusion	Natural convection	10.1
MEI, $75 \times 85 \times 12$ no adjacent board, extrusion	1 m/s	7.7
MEI, $75 \times 85 \times 12$ no adjacent board, extrusion	2 m/s	6.6
MEI, $75 \times 85 \times 12$ mm, adjacent board, 40 mm side bypass	1 m/s	6.9

Table 64. Heat Sink and Thermal Resistance of MPC8347E (PBGA) (continued)

Accurate thermal design requires thermal modeling of the application environment using computational fluid dynamics software which can model both the conduction cooling and the convection cooling of the air moving through the application. Simplified thermal models of the packages can be assembled using the junction-to-case and junction-to-board thermal resistances listed in the thermal resistance table. More detailed thermal models can be made available on request.

Heat sink vendors include the following list:

Aavid Thermalloy 80 Commercial St. Concord, NH 03301	603-224-9988
Alpha Novatech 473 Sapena Ct. #12 Santa Clara, CA 95054 Internet: www.alphanovatech.com	408-567-8082
International Electronic Research Corporation (IERC) 413 North Moss St. Burbank, CA 91502 Internet: www.ctscorp.com	818-842-7277
Millennium Electronics (MEI) Loroco Sites 671 East Brokaw Road San Jose, CA 95112 Internet: www.mei-thermal.com	408-436-8770