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NXP USA Inc. - MPC8347CZQAGD Datasheet



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Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e300
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	-
RAM Controllers	DDR
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	-
Package / Case	620-BBGA Exposed Pad
Supplier Device Package	620-HBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8347czqagd

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Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Parameter/Condition	Min	Мах	Unit	Notes
Input hold time for POR configuration signals with respect to negation of HRESET	0	_	ns	
Time for the MPC8347E to turn off POR configuration signals with respect to the assertion of $\overline{\text{HRESET}}$	—	4	ns	3
Time for the MPC8347E to turn on POR configuration signals with respect to the negation of HRESET	1	_	^t PCI_SYNC_IN	1, 3

Table 9. RESET Initialization Timing Specifications (continued)

Notes:

1. t_{PCI_SYNC_IN} is the clock period of the input clock applied to PCI_SYNC_IN. In PCI host mode, the primary clock is applied to the CLKIN input, and PCI_SYNC_IN period depends on the value of CFG_CLKIN_DIV. See the *MPC8349E PowerQUICC™ II Pro Integrated Host Processor Family Reference Manual*.

- 2. t_{CLKIN} is the clock period of the input clock applied to CLKIN. It is valid only in PCI host mode. See the MPC8349E PowerQUICC™ II Pro Integrated Host Processor Family Reference Manual.
- 3. POR configuration signals consist of CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV.

Table 10 lists the PLL and DLL lock times.

Table 10. PLL and DLL Lock Times

Parameter/Condition	Min Max Unit N		Notes	
PLL lock times	—	100	μs	
DLL lock times	7680	122,880	csb_clk cycles	1, 2

Notes:

1. DLL lock times are a function of the ratio between the output clock and the coherency system bus clock (csb_clk). A 2:1 ratio results in the minimum and an 8:1 ratio results in the maximum.

2. The csb_clk is determined by the CLKIN and system PLL ratio. See Section 19, "Clocking."

DDR SDRAM

Table 14. DDR SDRAM Output AC Timing Specifications for Source Synchronous Mode (continued)

At recommended operating conditions with GV_{DD} of 2.5 V ± 5%.

Parameter	Symbol ¹	Min	Мах	Unit	Notes
MDQS epilogue end	t _{DDKLME}	-0.9	0.3	ns	7

Notes:

- The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
 </sub>
- 2. All MCK/MCK referenced measurements are made from the crossing of the two signals ±0.1 V.
- 3. In the source synchronous mode, MCK/MCK can be shifted in 1/4 applied cycle increments through the clock control register. For the skew measurements referenced for t_{AOSKEW} it is assumed that the clock adjustment is set to align the address/command valid with the rising edge of MCK.
- 4. ADDR/CMD includes all DDR SDRAM output signals except MCK/MCK, MCS, and MDQ/MECC/MDM/MDQS. For the ADDR/CMD setup and hold specifications, it is assumed that the clock control register is set to adjust the memory clocks by 1/2 applied cycle.
- 5. Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK(n) clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. In source synchronous mode, this will typically be set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these 2 parameters have been set to the same adjustment value. See the MPC8349E PowerQUICC[™] II Pro Integrated Host Processor Family Reference Manual, for a description and understanding of the timing modifications enabled by use of these bits.
- 6. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the MPC8347E.
- 7. All outputs are referenced to the rising edge of MCK(n) at the pins of the MPC8347E. Note that t_{DDKHMP} follows the symbol conventions described in note 1.

Figure 5 shows the DDR SDRAM output timing for address skew with respect to any MCK.



Figure 5. Timing Diagram for t_{AOSKEW} Measurement

Figure 6 provides the AC test load for the DDR bus.

DDR SDRAM

Load	Delay	Unit
4 devices (12 pF)	3.0	ns
9 devices (27 pF)	3.6	ns
36 devices (108 pF) + 40 pF compensation capacitor	5.0	ns
36 devices (108 pF) + 80 pF compensation capacitor	5.2	ns

Table 16. Expected Delays for Address/Command

7 DUART

This section describes the DC and AC electrical specifications for the DUART interface of the MPC8347E.

7.1 DUART DC Electrical Characteristics

Table 17 provides the DC electrical characteristics for the DUART interface of the MPC8347E.

Table 17. DUART DC Electrical Characteristics

Parameter	Parameter Symbol Min		Мах	Unit
High-level input voltage	V _{IH}	2	OV _{DD} + 0.3	V
Low-level input voltage	V _{IL}	-0.3	0.8	V
Input current (0.8 V \leq V _{IN} \leq 2 V)	I _{IN}	—	±5	μA
High-level output voltage, I _{OH} = -100 μA	V _{OH}	OV _{DD} - 0.2	—	V
Low-level output voltage, $I_{OL} = 100 \ \mu A$	V _{OL}	—	0.2	V

7.2 DUART AC Electrical Specifications

Table 18 provides the AC timing parameters for the DUART interface of the MPC8347E.

Table 18. DUART AC Timing Specifications

Parameter	Value	Unit	Notes
Minimum baud rate	256	baud	
Maximum baud rate	>1,000,000	baud	1
Oversample rate	16		2

Notes:

- 1. Actual attainable baud rate will be limited by the latency of interrupt processing.
- 2. The middle of a start bit is detected as the 8th sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16th sample.

Ethernet: Three-Speed Ethernet, MII Management





Figure 15. RGMII and RTBI AC Timing and Multiplexing Diagrams

Table 35. Local Bus Gener	al Timing Parameters—D	LL Bypass ⁹ (continued)

Parameter	Symbol ¹	Min	Мах	Unit	Notes
Local bus clock to output valid	t _{LBKLOV}	_	3	ns	3
Local bus clock to output high impedance for LAD/LDP	t _{LBKHOZ}	—	4	ns	8

Notes:

- The symbols for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{LBIXKH1} symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one (1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
 </sub>
- 2. All timings are in reference to the falling edge of LCLK0 (for all outputs and for LGTA and LUPWAIT inputs) or the rising edge of LCLK0 (for all other inputs).
- 3. All signals are measured from $OV_{DD}/2$ of the rising/falling edge of LCLK0 to $0.4 \times OV_{DD}$ of the signal in question for 3.3 V signaling levels.
- 4. Input timings are measured at the pin.
- 5. t_{LBOTOT1} should be used when RCWH[LALE] is not set and when the load on the LALE output pin is at least 10 pF less than the load on the LAD output pins.
- 6. t_{LBOTOT2} should be used when RCWH[LALE] is set and when the load on the LALE output pin is at least 10 pF less than the load on the LAD output pins.the
- 7. t_{LBOTOT3} should be used when RCWH[LALE] is set and when the load on the LALE output pin equals to the load on the LAD output pins.
- 8. For purposes of active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
- 9. DLL bypass mode is not recommended for use at frequencies above 66 MHz.

Figure 19 provides the AC test load for the local bus.



Figure 19. Local Bus C Test Load

Local Bus

Figure 20 through Figure 25 show the local bus signals.



Figure 20. Local Bus Signals, Nonspecial Signals Only (DLL Enabled)



Figure 21. Local Bus Signals, Nonspecial Signals Only (DLL Bypass Mode)





Figure 22. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 2 (DLL Enabled)



Figure 23. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 2 (DLL Bypass Mode)

Table 37. JTAG AC Timing Specifications (Independent of CLKIN)¹ (continued)

At recommended operating conditions (see Table 2).

Parameter	Symbol ²	Min	Max	Unit	Notes
Output hold times: Boundary-scan data TDO	^t jtkldx ^t jtklox	2 2		ns	5
JTAG external clock to output high impedance: Boundary-scan data TDO	^t jtkldz ^t jtkloz	2 2	19 9	ns	5, 6

Notes:

- 1. All outputs are measured from the midpoint voltage of the falling/rising edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50 Ω load (see Figure 26). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
- 2. The symbols for timing specifications follow the pattern of t_{(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. In general, the clock reference symbol is based on three letters representing the clock of a particular function. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).}}
- 3. TRST is an asynchronous level sensitive signal. The setup time is for test purposes only.
- 4. Non-JTAG signal input timing with respect to t_{TCLK}.
- 5. Non-JTAG signal output timing with respect to t_{TCLK} .
- 6. Guaranteed by design and characterization.

Figure 26 provides the AC test load for TDO and the boundary-scan outputs of the MPC8347E.



Figure 26. AC Test Load for the JTAG Interface

Figure 27 provides the JTAG clock input timing diagram.



Figure 27. JTAG Clock Input Timing Diagram

15 GPIO

This section describes the DC and AC electrical specifications for the GPIO.

15.1 GPIO DC Electrical Characteristics

Table 45 provides the DC electrical characteristics for the MPC8347E GPIO.

Table 45. GPIO DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Мах	Unit
Input high voltage	V _{IH}		2.0	OV _{DD} + 0.3	V
Input low voltage	V _{IL}		-0.3	0.8	V
Input current	I _{IN}			±5	μA
Output high voltage	V _{OH}	I _{OH} = -8.0 mA	2.4	—	V
Output low voltage	V _{OL}	I _{OL} = 8.0 mA	_	0.5	V
Output low voltage	V _{OL}	I _{OL} = 3.2 mA	—	0.4	V

15.2 GPIO AC Timing Specifications

Table 46 provides the GPIO input and output AC timing specifications.

Table 46. GPIO Input AC Timing Specifications¹

Characteristic	Symbol ²	Min	Unit
GPIO inputs—minimum pulse width	t _{PIWID}	20	ns

Notes:

1. Input specifications are measured from the 50 percent level of the signal to the 50 percent level of the rising edge of CLKIN. Timings are measured at the pin.

 GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs should be synchronized before use by external synchronous logic. GPIO inputs must be valid for at least t_{PIWID} ns to ensure proper operation. 17 SPI

This section describes the SPI DC and AC electrical specifications.

17.1 SPI DC Electrical Characteristics

Table 49 provides the SPI DC electrical characteristics.

Table 49. SPI DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Мах	Unit
Input high voltage	V _{IH}		2.0	OV _{DD} + 0.3	V
Input low voltage	V _{IL}		-0.3	0.8	V
Input current	I _{IN}			±5	μA
Output high voltage	V _{OH}	I _{OH} = -8.0 mA	2.4	—	V
Output low voltage	V _{OL}	I _{OL} = 8.0 mA	—	0.5	V
Output low voltage	V _{OL}	I _{OL} = 3.2 mA	—	0.4	V

17.2 SPI AC Timing Specifications

Table 50 provides the SPI input and output AC timing specifications.

Table 50. SPI AC Timing Specifications¹

Characteristic	Symbol ²	Min	Мах	Unit
SPI outputs valid—Master mode (internal clock) delay	t _{NIKHOV}		6	ns
SPI outputs hold—Master mode (internal clock) delay	t _{NIKHOX}	0.5		ns
SPI outputs valid—Slave mode (external clock) delay	t _{NEKHOV}		8	ns
SPI outputs hold—Slave mode (external clock) delay	t _{NEKHOX}	2		ns
SPI inputs—Master mode (internal clock input setup time	t _{NIIVKH}	4		ns
SPI inputs—Master mode (internal clock input hold time	t _{NIIXKH}	0		ns
SPI inputs—Slave mode (external clock) input setup time	t _{NEIVKH}	4		ns
SPI inputs—Slave mode (external clock) input hold time	t _{NEIXKH}	2		ns

Notes:

1. Output specifications are measured from the 50 percent level of the rising edge of CLKIN to the 50 percent level of the signal. Timings are measured at the pin.

The symbols for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{NIKHOX} symbolizes the internal timing (NI) for the time SPICLK clock reference (K) goes to the high state (H) until outputs (O) are invalid (X).
</sub>

Signal	Package Pin Number	Pin Type	Power Supply	Notes
MECC[0:4]/MSRCID[0:4]	W4, W3, Y3, AA6, T1	I/O	GV _{DD}	
MECC[5]/MDVAL	U1	I/O	GV _{DD}	
MECC[6:7]	Y1, Y6	I/O	GV _{DD}	
MDM[0:8]	B1, F1, K1, R4, AD4, AJ1, AP3, AP7, Y4	0	GV _{DD}	
MDQS[0:8]	B2, F5, J1, P2, AC1, AJ2, AN4, AL8, W2	I/O	GV _{DD}	
MBA[0:1]	AD1, AA5	0	GV _{DD}	
MA[0:14]	W1, U4, T3, R3, P1, M1, N1, L3, L1, K2, Y2, K3, J3, AP2, AN6	0	GV _{DD}	
MWE	AF1	0	GV _{DD}	
MRAS	AF4	0	GV _{DD}	
MCAS	AG3	0	GV _{DD}	
MCS[0:3]	AG2, AG1, AK1, AL4	0	GV _{DD}	
MCKE[0:1]	H3, G1	0	GV _{DD}	3
MCK[0:5]	U2, F4, AM3, V3, F2, AN3	0	GV _{DD}	
MCK[0:5]	U3, E3, AN2, V4, E1, AM4	0	GV _{DD}	
(They sh	Pins Reserved for Future DDR2 hould be left unconnected for MPC834	7)		
MODT[0:3]	AH3, AJ5, AH1, AJ4	_	_	
MBA[2]	H4		_	
SPARE1	AA1		_	8
SPARE2	AB1		_	6
	Local Bus Controller Interface		1	1
LAD[0:31]	AM13, AP13, AL14, AM14, AN14, AP14, AK15, AJ15, AM15, AN15, AP15, AM16, AL16, AN16, AP16, AL17, AM17, AP17, AK17, AP18, AL18, AM18, AN18, AP19, AN19, AM19, AP20, AK19, AN20, AL20, AP21, AN21	I/O	OV _{DD}	
LDP[0]/CKSTOP_OUT	AM21	I/O	OV _{DD}	
LDP[1]/CKSTOP_IN	AP22	I/O	OV _{DD}	
LDP[2]	AN22	I/O	OV _{DD}	
LDP[3]	AM22	I/O	OV _{DD}	
LA[27:31]	AK21, AP23, AN23, AP24, AK22	0	OV _{DD}	
LCS[0:3]	AN24, AL23, AP25, AN25	0	OV _{DD}	
LWE[0:3]/LSDDQM[0:3]/LBS[0:3]	AK23, AP26, AL24, AM25	0	OV _{DD}	

Table 51. MPC8347E (TBGA) Pinout Listing (continued)

Table 51	. MPC8347E	(TBGA)	Pinout	Listing	(continued)
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Signal	Package Pin Number	Pin Type	Power Supply	Notes	
	DUART				
UART_SOUT[1:2]/MSRCID[0:1]/LSRCID[0:1]	AK27, AN29	0	OV _{DD}		
UART_SIN[1:2]/MSRCID[2:3]/LSRCID[2:3]	AL28, AM29	I/O	OV _{DD}		
UART_CTS[1]/MSRCID4/LSRCID4	AP30	I/O	OV _{DD}		
UART_CTS[2]/MDVAL/ LDVAL	AN30	I/O	OV _{DD}		
UART_RTS[1:2]	AP31, AM30	0	OV _{DD}		
	I ² C interface				
IIC1_SDA	AK29	I/O	OV _{DD}	2	
IIC1_SCL	AP32	I/O	OV _{DD}	2	
IIC2_SDA	AN31	I/O	OV _{DD}	2	
IIC2_SCL	AM31	I/O	OV _{DD}	2	
	SPI				
SPIMOSI	AN32	I/O	OV _{DD}		
SPIMISO	AP33	I/O	OV _{DD}		
SPICLK	AK30	I/O	OV _{DD}		
SPISEL	AL31	I	OV _{DD}		
	Clocks				
PCI_CLK_OUT[0:4]	AN9, AP9, AM10, AN10, AJ11	0	OV _{DD}		
PCI_SYNC_IN/PCI_CLOCK	AK12	I	OV _{DD}		
PCI_SYNC_OUT	AP11	0	OV _{DD}	3	
RTC/PIT_CLOCK	AM32	I	OV _{DD}		
CLKIN	АМ9	I	OV _{DD}		
	JTAG				
ТСК	E20	I	OV _{DD}		
TDI	F20	I	OV _{DD}	4	
TDO	B20	0	OV _{DD}	3	
TMS	A20	I	OV _{DD}	4	
TRST	B19	I	OV _{DD}	4	
Test					
TEST	D22	I	OV _{DD}	6	
TEST_SEL	AL13	I	OV _{DD}	7	
РМС					
QUIESCE	A18	0	OV _{DD}		

Signal	Package Pin Number	Pin Type	Power Supply	Notes
	No Connection			
NC	W32, AA31, AA32, AA33, AA34, AB31, AB32, AB33, AB34, AC29, AC31, AC33, AC34, AD30, AD32, AD33, AD34, AE29, AE30, AH32, AH33, AH34, AM33, AJ31, AJ32, AJ33, AJ34, AK32, AK33, AK34, AM34, AL33, AL34, AK31, AH30, AC32, AE32, AH31, AL32, AG34, AE33, AF32, AE34, AF34, AF33, AG33, AG32, AL11, AM11, AP10, Y32, Y34, Y31, Y33	_	_	

Table 51. MPC8347E (TBGA) Pinout Listing (continued)

Notes:

- 1. This pin is an open-drain signal. A weak pull-up resistor (1 k Ω) should be placed on this pin to OV_{DD}.
- 2. This pin is an open-drain signal. A weak pull-up resistor (2–10 kΩ) should be placed on this pin to OV_{DD}.
- 3. During reset, this output is actively driven rather than three-stated.
- 4. These JTAG pins have weak internal pull-up P-FETs that are always enabled.
- 5. This pin should have a weak pull-up if the chip is in PCI host mode. Follow the PCI specifications.
- 6. This pin must always be tied to GND.
- 7. This pin must always be pulled up to OV_{DD} .
- 8. This pin must always be left not connected.
- 9. Thermal sensitive resistor.
- 10.It is recommended that MDIC0 be tied to GRD using an 18 Ω resistor and MDIC1 be tied to DDR power using an 18 Ω resistor.
- 11.TSEC1_TXD[3] is required an external pull-up resistor. For proper functionality of the device, this pin must be pulled up or actively driven high during a hard reset. No external pull-down resistors are allowed to be attached to this net.

Table 52 provides the pinout listing for the MPC8347E, 620 PBGA package.

Table 52. MPC8347E (PBGA) Pinout Listing

Signal	Package Pin Number	Pin Type	Power Supply	Notes
	PCI			
PCI1_INTA/IRQ_OUT	D20	0	OV _{DD}	2
PCI1_RESET_OUT	B21	0	OV _{DD}	
PCI1_AD[31:0]	E19, D17, A16, A18, B17, B16, D16, B18, E17, E16, A15, C16, D15, D14, C14, A12, D12, B11, C11, E12, A10, C10, A9, E11, E10, B9, B8, D9, A8, C9, D8, C8	I/O	OV _{DD}	
PCI1_C/BE[3:0]	A17, A14, A11, B10	I/O	OV _{DD}	
PCI1_PAR	D13	I/O	OV _{DD}	
PCI1_FRAME	B14	I/O	OV _{DD}	5
PCI1_TRDY	A13	I/O	OV _{DD}	5

Table 52. MPC8347E (PBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
SPIMISO	C7	I/O	OV _{DD}	
SPICLK	B7	I/O	OV _{DD}	
SPISEL	A7	I	OV _{DD}	
	Clocks			
PCI_CLK_OUT[0:2]	Y1, W3, W2	0	OV _{DD}	
PCI_CLK_OUT[3]/LCS[6]	W1	0	OV _{DD}	
PCI_CLK_OUT[4]/LCS[7]	V3	0	OV _{DD}	
PCI_SYNC_IN/PCI_CLOCK	U4	I	OV _{DD}	
PCI_SYNC_OUT	U5	0	OV _{DD}	3
RTC/PIT_CLOCK	E9	I	OV _{DD}	
CLKIN	W5	I	OV _{DD}	
	JTAG			
тск	H27	I	OV _{DD}	
TDI	H28	I	OV _{DD}	4
TDO	M24	0	OV _{DD}	3
TMS	J27	I	OV _{DD}	4
TRST	K26	I	OV _{DD}	4
	Test			
TEST	F28	I	OV _{DD}	6
TEST_SEL	ТЗ	I	OV _{DD}	6
	РМС			
QUIESCE	K27	0	OV _{DD}	
	System Control			
PORESET	K28	I	OV _{DD}	
HRESET	M25	I/O	OV _{DD}	1
SRESET	L27	I/O	OV _{DD}	2
	Thermal Management			
THERM0	B15	I	—	8
	Power and Ground Signals			
AV _{DD} 1	C15	Power for e300 PLL (1.2 V)	AV _{DD} 1	
AV _{DD} 2	U1	Power for system PLL (1.2 V)	AV _{DD} 2	

			Inpu	it Clock Fre	quency (M	Hz) ²
CFG_CLKIN_DIV at Reset ¹	SPMF	Input Clock	16.67	25	33.33	66.67
		Natio	C	s <i>b_clk</i> Freq	uency (MH	z)
Low	0010	2 : 1				133
Low	0011	3 : 1			100	200
Low	0100	4 : 1		100	133	266
Low	0101	5 : 1		125	166	333
Low	0110	6 : 1	100	150	200	
Low	0111	7 : 1	116	175	233	
Low	1000	8 : 1	133	200	266	
Low	1001	9 : 1	150	225	300	
Low	1010	10 : 1	166	250	333	
Low	1011	11 : 1	183	275		
Low	1100	12 : 1	200	300		
Low	1101	13 : 1	216	325		
Low	1110	14 : 1	233		<u>.</u>	
Low	1111	15 : 1	250			
Low	0000	16 : 1	266			
High	0010	4 : 1		100	133	266
High	0011	6 : 1	100	150	200	
High	0100	8 : 1	133	200	266	
High	0101	10 : 1	166	250	333	
High	0110	12 : 1	200	300		
High	0111	14 : 1	233			
High	1000	16 : 1	266			

Table 58. CSB Frequency Options for Agent Mode

¹ CFG_CLKIN_DIV doubles csb_clk if set high.

² CLKIN is the input clock in host mode; PCI_CLK is the input clock in agent mode. DDR2 memory may be used at 133 MHz provided that the memory components are specified for operation at this frequency.

19.2 Core PLL Configuration

RCWL[COREPLL] selects the ratio between the internal coherent system bus clock (*csb_clk*) and the e300 core clock (*core_clk*). Table 59 shows the encodings for RCWL[COREPLL]. COREPLL values that are not listed in Table 59 should be considered as reserved.

Tyco Electronics Chip Coolers [™] P.O. Box 3668 Harrisburg, PA 17105-3668 Internet: www.chipcoolers.com	800-522-2800
Wakefield Engineering 33 Bridge St. Pelham, NH 03076 Internet: www.wakefield.com	603-635-5102
Interface material vendors include the following:	
Chomerics, Inc. 77 Dragon Ct. Woburn, MA 01801 Internet: www.chomerics.com	781-935-4850
Dow-Corning Corporation Dow-Corning Electronic Materials P.O. Box 994 Midland, MI 48686-0997 Internet: www.dowcorning.com	800-248-2481
Shin-Etsu MicroSi, Inc. 10028 S. 51st St. Phoenix, AZ 85044 Internet: www.microsi.com	888-642-7674
The Bergquist Company 18930 West 78th St. Chanhassen, MN 55317 Internet: www.bergquistcompany.com	800-347-4572

20.3 Heat Sink Attachment

When heat sinks are attached, an interface material is required, preferably thermal grease and a spring clip. The spring clip should connect to the printed-circuit board, either to the board itself, to hooks soldered to the board, or to a plastic stiffener. Avoid attachment forces that can lift the edge of the package or peel the package from the board. Such peeling forces reduce the solder joint lifetime of the package. The recommended maximum force on the top of the package is 10 lb force (4.5 kg force). Any adhesive attachment should attach to painted or plastic surfaces, and its performance should be verified under the application requirements.

20.3.1 Experimental Determination of the Junction Temperature with a Heat Sink

When a heat sink is used, the junction temperature is determined from a thermocouple inserted at the interface between the case of the package and the interface material. A clearance slot or hole is normally

Thermal

required in the heat sink. Minimize the size of the clearance to minimize the change in thermal performance caused by removing part of the thermal interface to the heat sink. Because of the experimental difficulties with this technique, many engineers measure the heat sink temperature and then back calculate the case temperature using a separate measurement of the thermal resistance of the interface. From this case temperature, the junction temperature is determined from the junction-to-case thermal resistance.

$$T_J = T_C + (R_{\theta JC} \times P_D)$$

where:

 T_J = junction temperature (°C) T_C = case temperature of the package (°C) $R_{\theta JC}$ = junction-to-case thermal resistance (°C/W) P_D = power dissipation (W)

System Design Information

21 System Design Information

This section provides electrical and thermal design recommendations for successful application of the MPC8347E.

21.1 System Clocking

The MPC8347E includes two PLLs:

- 1. The platform PLL generates the platform clock from the externally supplied CLKIN input. The frequency ratio between the platform and CLKIN is selected using the platform PLL ratio configuration bits as described in Section 19.1, "System PLL Configuration."
- 2. The e300 core PLL generates the core clock as a slave to the platform clock. The frequency ratio between the e300 core clock and the platform clock is selected using the e300 PLL ratio configuration bits as described in Section 19.2, "Core PLL Configuration."

21.2 PLL Power Supply Filtering

Each PLL gets power through independent power supply pins (AV_{DD}1, AV_{DD}2, respectively). The AV_{DD} level should always equal to V_{DD} , and preferably these voltages are derived directly from V_{DD} through a low frequency filter scheme.

There are a number of ways to provide power reliably to the PLLs, but the recommended solution is to provide four independent filter circuits as illustrated in Figure 42, one to each of the four AV_{DD} pins. Independent filters to each PLL reduce the opportunity to cause noise injection from one PLL to the other.

The circuit filters noise in the PLL resonant frequency range from 500 kHz to 10 MHz. It should be built with surface mount capacitors with minimum effective series inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

To minimize noise coupled from nearby circuits, each circuit should be placed as closely as possible to the specific AV_{DD} pin being supplied. It should be possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of package, without the inductance of vias.

Figure 42 shows the PLL power supply filter circuit.



Figure 42. PLL Power Supply Filter Circuit

System Design Information

the large value of the pull-up/pull-down resistor should minimize the disruption of signal quality or speed for the output pins.

21.7 Pull-Up Resistor Requirements

The MPC8347E requires high resistance pull-up resistors (10 k Ω is recommended) on open-drain pins, including I²C pins, the Ethernet Management MDIO pin, and IPIC interrupt pins.

For more information on required pull-up resistors and the connections required for the JTAG interface, refer to application note AN2931, *PowerQUICCTM Design Checklist*.